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# Investigation of Indium Oxide Effect on Indium Particles Properties Used as Silicon Nanowires Catalyst

*Rabia Benabderrahmane Zaghoulani*

## Abstract

In this chapter, we investigate on indium particles elaboration by different annealing processes: rapid thermal annealing (RTA) and conventional processes. The elaborated particles are dedicated to be used as catalyst for silicon nanowires' (SiNWs) growth by vapor–liquid–solid (VLS) process. The annealing parameters effect on indium particles properties is studied. After conventional annealing, the indium layer is cracked into elongated and inhomogeneous islands of micrometric sizes. XRD analysis depicts, in addition to pure indium planes, the presence of new peaks attributed to indium oxide ( $\text{In}_2\text{O}_3$ ) planes formed during annealing. After hydrogen treatment with a flow rate of 60 sccm during 10 min, some  $\text{In}_2\text{O}_3$  peaks are eliminated and replaced by new indium peaks, explaining the amelioration of indium particles morphology. These formed particles have been used as catalyst for SiNWs' growth. A low density of SiNWs is obtained, attributed to  $\text{In}_2\text{O}_3$  persistence, decreasing the indium catalytic effect. Quasi-spherical and homogeneously distributed indium particles with an average size of 422 nm are successfully grown in one step by the RTA process during short time (5 min) at lower temperature (450°C). XRD analysis shows the absence of indium oxide in the contrary to those formed by the conventional furnace. SiNWs with higher density are obtained, highlighting the harmful role of indium oxide.

**Keywords:** indium catalyst, annealing, indium oxide, silicon nanowires, vapor–liquid–solid process

## 1. Introduction

The advancement of nanotechnologies has made possible the development of new applications in all fields. In particular, the nanostructuring of materials has paved the way toward new concepts. Important efforts have been dedicated to metallic nanoparticles, thanks to their interesting properties in comparison to bulk materials. Specially, they are widely studied to be used for many purposes in various applications: passivation of silicon for photovoltaics [1], plasmonics [2, 3], and bionanotechnology [4]. Metallic nanoparticles are also used as catalyst for silicon nanowires' (SiNWs) growth by top-down [5, 6] or bottom-up approaches [7].

Silicon nanowires' properties, especially their diameter, could be tuned by controlling the metallic particles properties. In the literature, many metallic nanoparticles are reported as catalysts, such as Au [8], Ti [9], Al [10], Cu [11], Ga [12], and Pt [13]. During last years, indium is considered a very interesting catalyst because it forms a low temperature eutectic with silicon (157°C) and it induces shallow defects as it acts as a p-type dopant encouraging its use as catalyst. An important issue in SiNWs' synthesis is the indium catalyst elaboration.

Indium nanoparticles could be elaborated by different techniques such as vapor deposition technique [14], electrochemical reduction [15], chemical reduction of salts [16], laser ablation [17], and reduction of indium-tin oxide or indium layers by hydrogen or helium plasma [18–20]. Iacopi et al. have obtained indium particles with diameter range of 40–80 nm by electrodeposition on silicon substrate from an aqueous solution ( $\text{InCl}_3$ , KCl, and HCl) [21]. Kumar et al. have reported on the growth of indium droplets obtained with an average diameter of 90 nm by indium evaporation followed by annealing at 300°C during 5 min [22]. The obtained particles' properties are closely related to experimental parameters such as the precursor's concentration, the plasma flow rate, the exposition duration and the substrate temperature, or the annealing parameters.

In this chapter, we report on an ex situ formation of indium particles to be used as catalyst for SiNWs' growth using two annealing processes: a rapid thermal annealing (RTA) and a conventional process. A comparative study is carried out to investigate the annealing process effect on SiNWs' properties. In particular, the effect of indium oxide is presented.

## 2. VLS process

The bottom-up approach is presented as an interesting alternative for low-cost nanowires growth. Indeed, it requires few technological steps with the possibility of SiNWs' growth on any substrate. Several techniques have been reported, mainly chemical vapor deposition (CVD), plasma-assisted chemical vapor deposition (PECVD), laser ablation, and molecular beam epitaxy (MBE). PECVD is the technique adopted in this work. It has the same principle as the conventional CVD except that the chemical reactions will take place after the formation of plasma from the reactor gases, offering the possibility to work at low temperatures. The deposited layers' properties strongly depend on the substrate temperature, the pressure, the growth time, the reactive gases, and the gas flow rates. The principle of SiNWs' growth by PECVD can be resumed in four main steps:

1. The deposition of catalytic particles (in situ or ex situ).
2. The formation of a metal-silicon eutectic by supplying the particles with a precursor gas [the silane ( $\text{SiH}_4$ ) in the case of silicon nanowires].
3. Saturation of metal particle with silicon (Si), nucleation and precipitation of silicon at the substrate–metal particle interface.
4. The growth of SiNWs.

The SiNWs' growth is generally explained by the vapor–liquid–solid (VLS) mode proposed by R. S. Wagner and W. C. Ellis. In this mode, the growth depends on three main elements: the precursor in its gaseous state, and the metal-silicon

alloy in the liquid state, the nanowire in the solid state, and hence the nomination vapor–liquid–solid mode.

The SiNWs' growth in a PECVD reactor is carried out by following the next steps:

- At  $T_{\text{work}} > T_{\text{eutectic of metal-Si}}$ : the metallic particle is in its liquid state.
- Introducing the precursor gas ( $\text{SiH}_4$ ): The silane molecules in the vapor state are adsorbed on the particle surface according to the following equation:



- Incorporation of Si atoms in the droplet, formation of the metal-Si alloy, and the silicon diffusion toward the alloy-substrate interface. The silicon concentration in the droplet will exceed the equilibrium concentration at the working temperature, leading to the droplet saturation and the silicon nucleation.

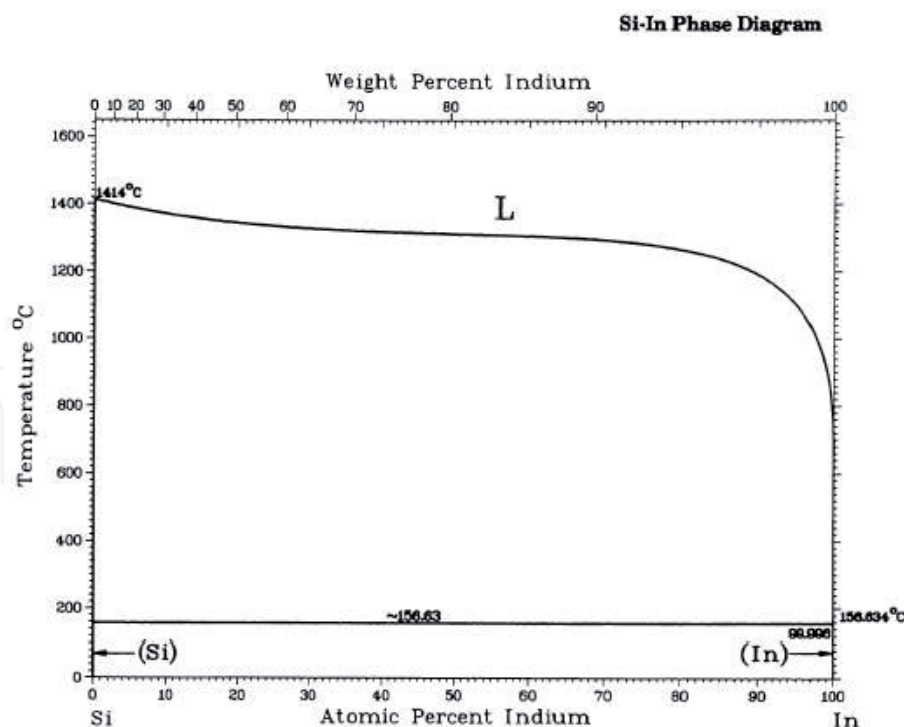
### 3. Indium as catalyst for silicon nanowires' growth

In the VLS mode, the catalyst surface's properties play an important role in the SiNWs' growth. In order to adsorb the maximum of gaseous species, the surface should be rough. For example, silane dissociation and adsorption are better on the gold-silicon (Au-Si) system's surface than that of silicon. Indeed, the high adsorption and dissociation efficiency of silane at the Au-Si droplet permits the nanowires' growth with a constant radius. Other parameters influence SiNWs' growth, such as the surface tension of the catalyst droplet and the solid–liquid interface tension. The choice of the catalyst metal is very important, matching some criteria:

- The eutectic temperature of the metal-silicon alloy
- Vapor pressure
- Silicon solubility in the metal
- Technological compatibility with the current semiconductor industry
- Metal diffusion in SiNWs and formation of recombination centers
- Oxidation, etc.

Gold is the most commonly used metal despite silicon contamination with defects, introducing deep energy levels in the silicon bandgap. Gold, with a simple diagram phase, permits the solubility and nucleation of silicon easily at a relatively low eutectic temperature ( $363^\circ\text{C}$ ). Moreover, gold does not oxidize, increasing its catalytic activity. Gold-catalyzed SiNWs are well controlled and already integrated into prototypes such as transistors [23], biosensors [24], and photo-anodes [25].

Since 2001, post-transition metals like aluminum, indium, and bismuth have been studied. All these metals introduce shallow defects (dopants for silicon). Aluminum, for example, has an eutectic temperature ( $577^\circ\text{C}$ ) higher than that of gold and is very chemically reactive, especially with oxygen.



**Figure 1.**  
Phase diagram of indium-silicon system [26].

Bismuth (Bi) is a promising catalyst. The energy level of the impurity introduced by bismuth into the silicon gap is close to the conduction band, so bismuth is an N-type dopant for silicon. Bismuth exhibits a low silicon eutectic temperature (271°C), which allows working at low growth temperatures and using flexible substrates. Despite these advantages, it is difficult to use it as SiNWs catalyst because it has a high vapor pressure, so it can evaporate easily during growth. It has a low surface tension (0.37 N/m), while gold has a higher surface tension (1.14 N/m). Unidirectional growth has been shown to be difficult with low surface tension catalysts.

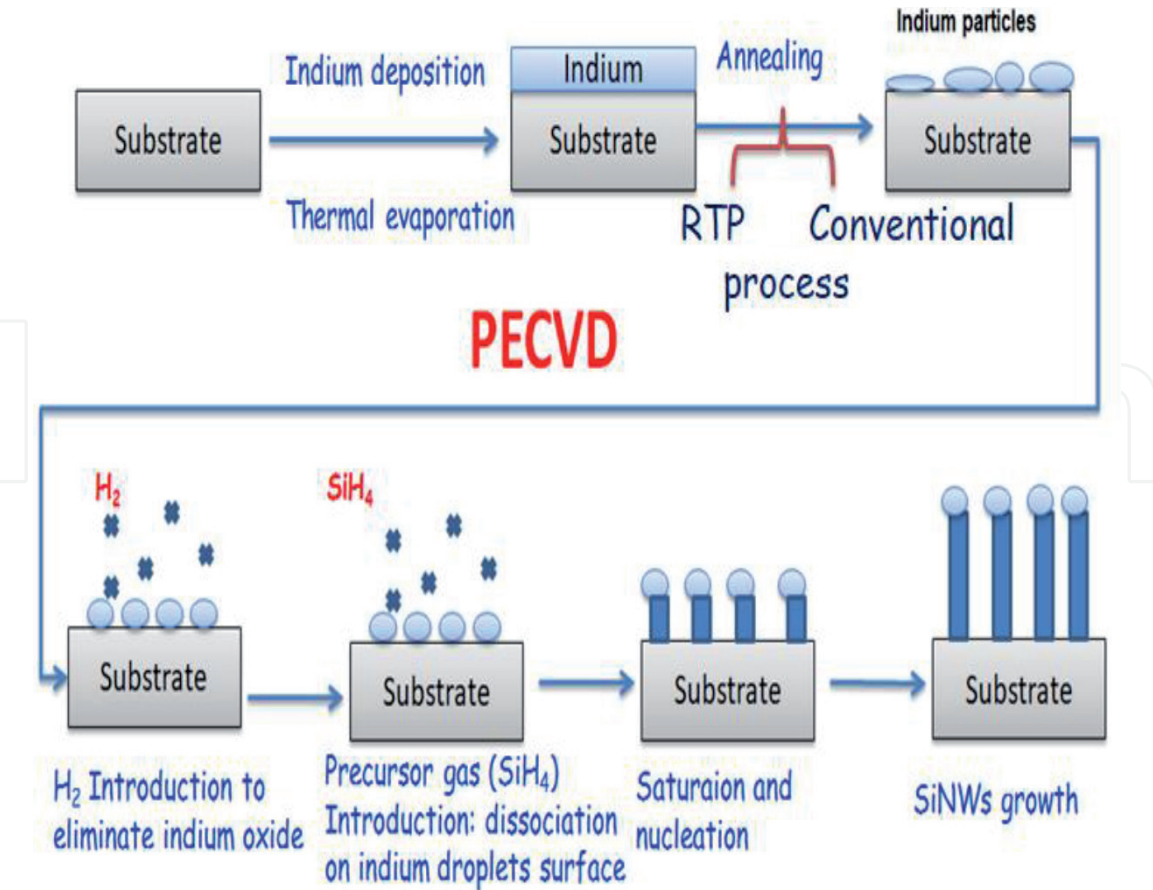
Indium is an interesting metal to be used as catalyst. It presents a simple phase diagram with silicon (**Figure 1**), forming an eutectic system at 157°C, permitting low growth temperatures and flexible substrates' use. Indium has a surface tension (0.55 N/m) higher than that of bismuth but lower than gold. However, in the presence of oxygen, indium could be oxidized, reducing thereby its catalytic behavior.

#### 4. Experimental details

**Figure 2** describes the silicon nanowires growth process [27]. Indium particles (In-Nps) were grown ex situ by annealing indium-coated silicon p-type (100) substrates. Indium layers of 100 nm thickness were deposited on silicon substrates by thermal evaporation. The used annealing procedures are: (1) conventional annealing with a vacuum pressure of  $10^{-2}$  mbar at 600°C during 45 min, (2) RTA annealing using a home-built RTA furnace with a vacuum pressure of  $10^{-6}$  mbar at different temperatures (300, 350, 400, and 450°C) during 5 min.

To synthesize SiNWs, the samples are introduced to the PECVD reactor with substrate temperature set to 400°C. Prior to precursor ( $\text{SiH}_4$ ) introduction, the samples are treated by hydrogen plasma during 10 min with a flow rate of 60 sccm. Then,  $\text{SiH}_4$  is introduced during 15 min with a flow rate of 10 sccm.

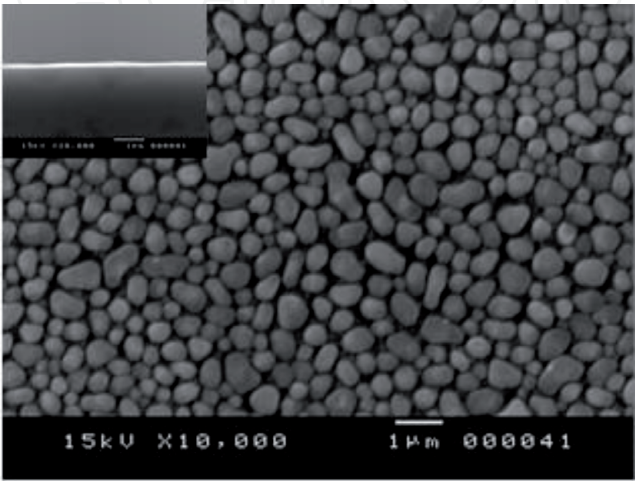




**Figure 2.**  
*SiNWs' growth process adopted in this work.*

**5. Annealing process effect on indium particles' catalyst**

The indium-coated silicon substrate annealed in the conventional furnace during 45 min at 600°C shows elongated and inhomogeneous islands of micrometric sizes (**Figure 3**). The chosen work temperature is well above the indium melting temperature (157°C), offering sufficient kinetic energy to metallic atoms to form regular particles. The observed morphology could be attributed to the presence of indium oxide. X-ray diffraction (XRD) analysis was performed to confirm these observations.

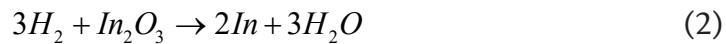


**Figure 3.**  
*(a) SEM image of indium-coated silicon substrate annealed under conventional process. Inset: Cross-sectional SEM view of the as-deposited indium-coated silicon substrate.*

In **Figure 4**, we compare the XRD spectra of the as-deposited indium layer and the annealed sample. The XRD patterns of the as-deposited sample show only the presence of the planes of the tetragonal crystal structure of indium. However, after annealing, the XRD spectrum shows the disappearance of indium peaks except two peaks. These peaks are replaced by peaks attributed to indium oxide planes with the presence of very intense (222) indium oxide peak. Indium oxide can explain the obtained indium particles morphology. This phenomenon is attributed to the high melting temperature (1900°C) of indium oxide compared to the chosen annealing temperature.

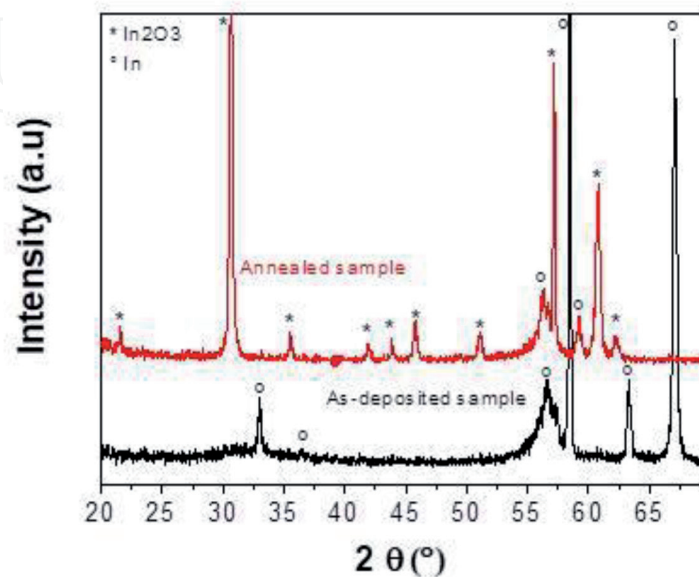
So, in order to ameliorate the indium particles properties, a hydrogen plasma treatment was performed in a PECVD reactor at a substrate temperature of 400°C during 10 min, with two different flow rates of 60 and 100 sccm. XRD analysis shows the persistence of indium oxide presence after 60 sccm H<sub>2</sub> treatment, indicating that this flow rate is not sufficient to eliminate all In<sub>2</sub>O<sub>3</sub>. When increasing hydrogen flow, In<sub>2</sub>O<sub>3</sub> peaks have been disappeared and replaced by indium peaks (**Figure 5**). This result is confirmed by the SEM image of the obtained structures (**Figure 6**). It is noticed that the indium particles become more homogeneous and regular in size and form. Quasi-spherical particles with average size of 440 nm (**Figure 6(c)**) are obtained.

H<sub>2</sub> plasma treatment leads to the indium oxide elimination as depicted by Eq. (2) and the indium loss through evaporation leading to particles properties enhancement (density, size, and shape). Moreover, XRD results highlight the fact that the H<sub>2</sub> plasma flow rate (100 sccm) was sufficient to eliminate all indium oxide.

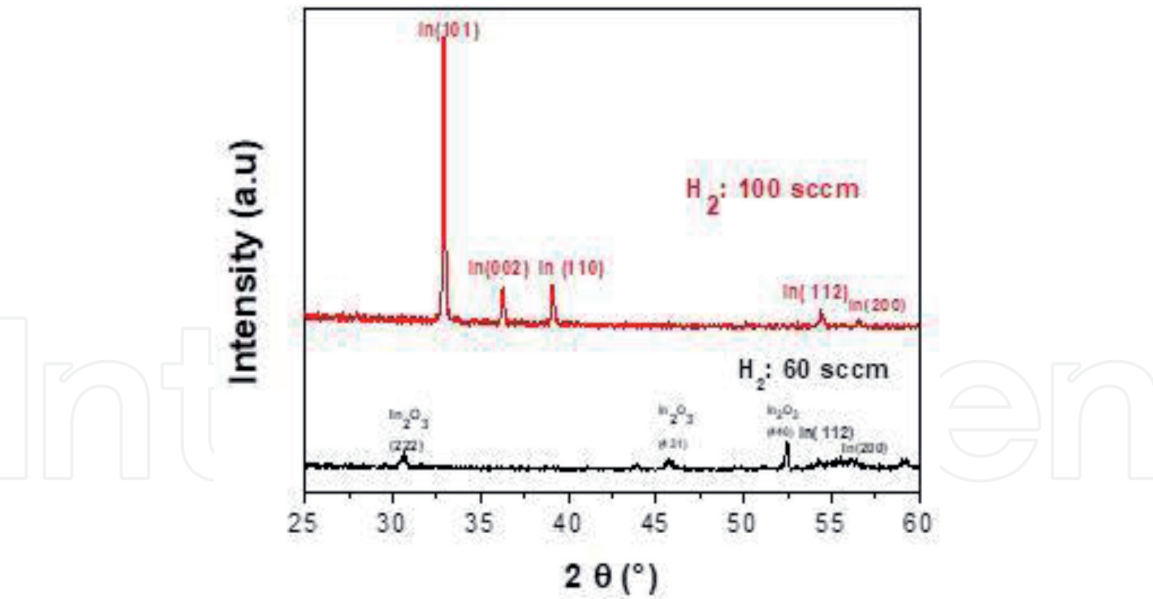


## 5.1 Discussion

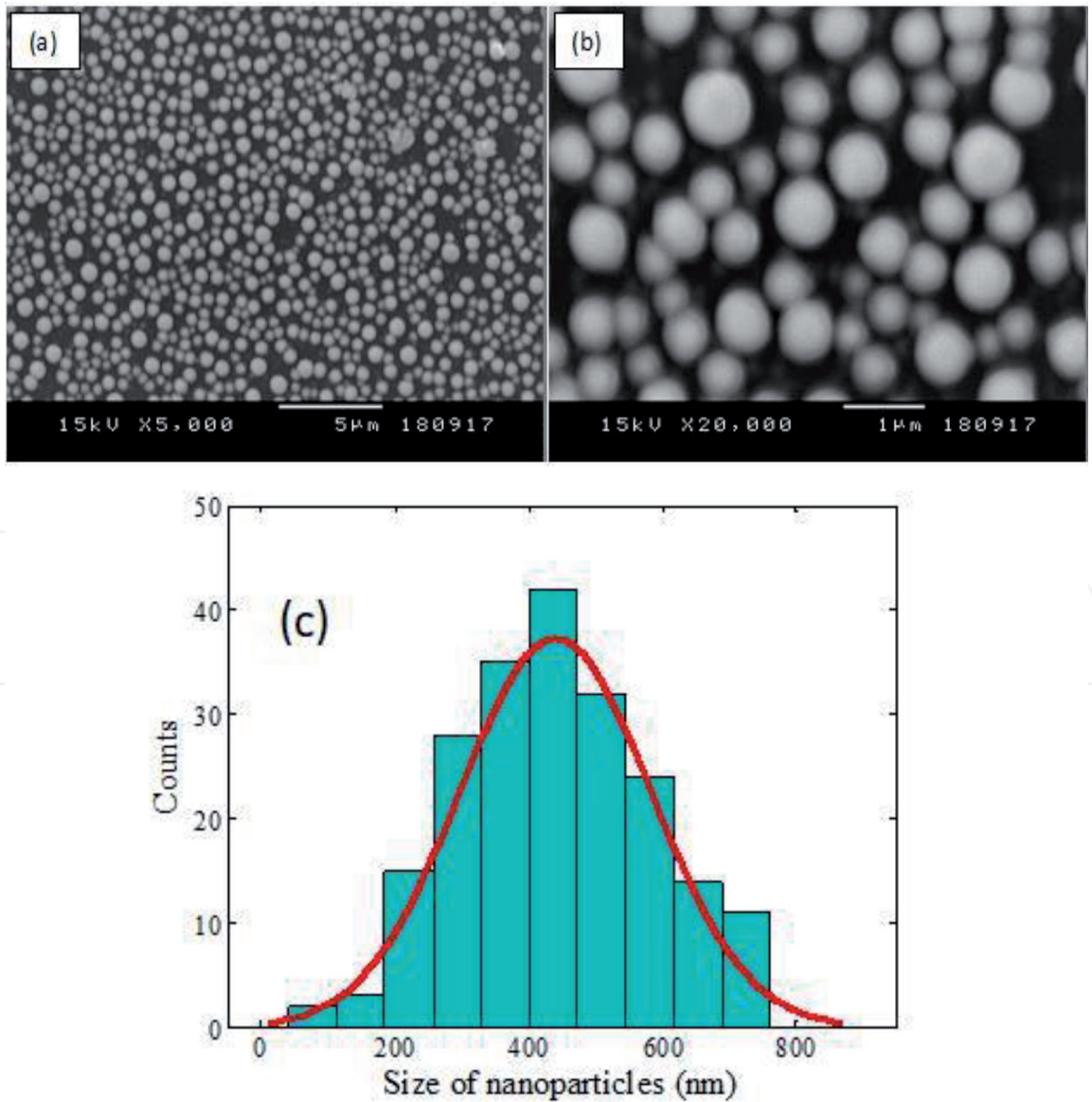
In this section, we have noted the indium oxide formation during the conventional annealing that is attributed to the oxygen presence. This observation is explained by the low vacuum pressure in the furnace (10<sup>-2</sup> mbar) where the heating is mainly provided by thermal conduction. In order to eliminate the oxygen and



**Figure 4.**  
XRD spectra of as-deposited indium layer and annealed sample.



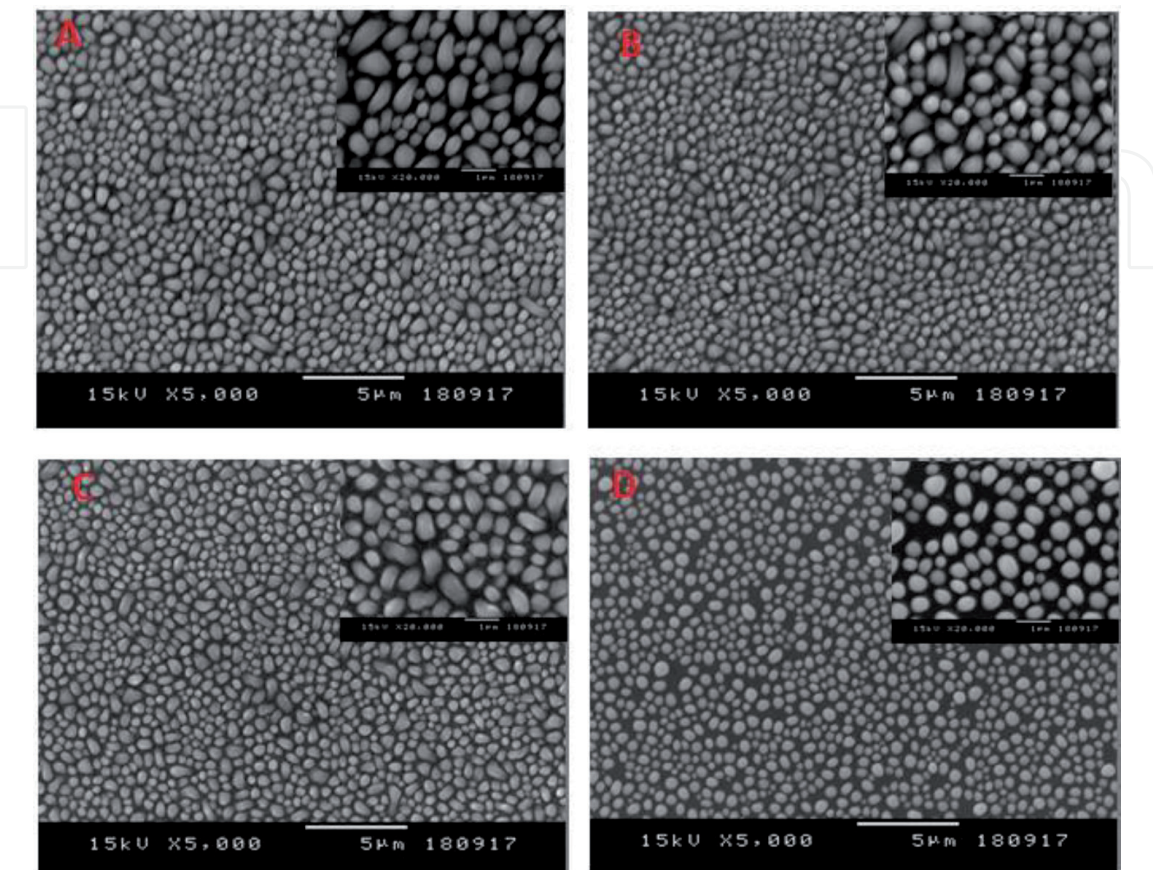
**Figure 5.**  
XRD spectra of annealed layers and treated by  $H_2$  treatment with flow rates of 60 and 100 sccm.



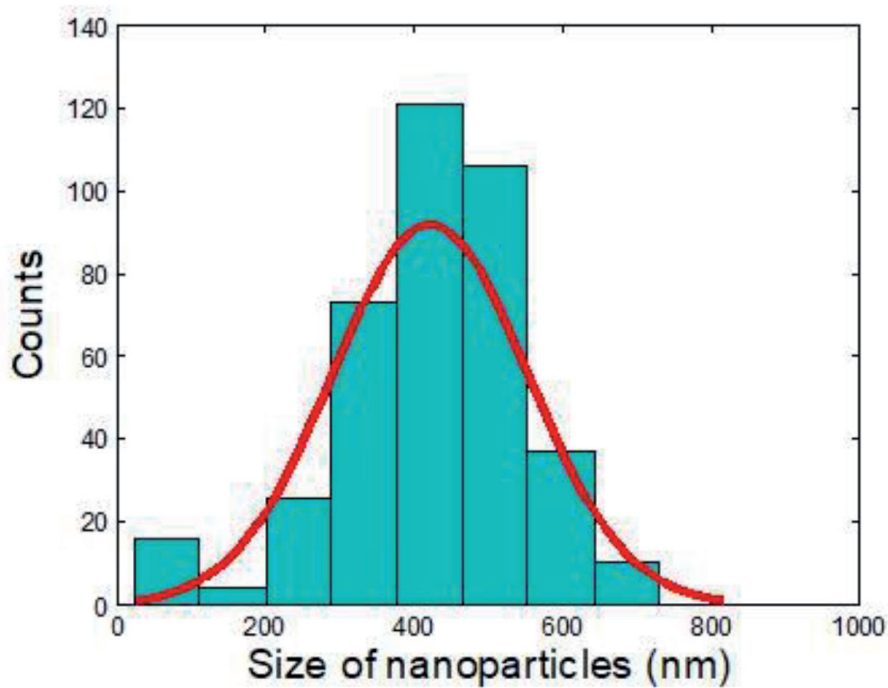
**Figure 6.**  
(a-b) SEM images of indium particles obtained after conventional annealing followed by  $H_2$  treatment with flow rate of 100 sccm (c) the corresponding histogram indicating the size distribution.



form pure indium particles, samples must be annealed in ultra-vacuum atmosphere; however, the thermal conduction will be very slow. In this case, the annealing will occur for long durations consuming thereby much energy.

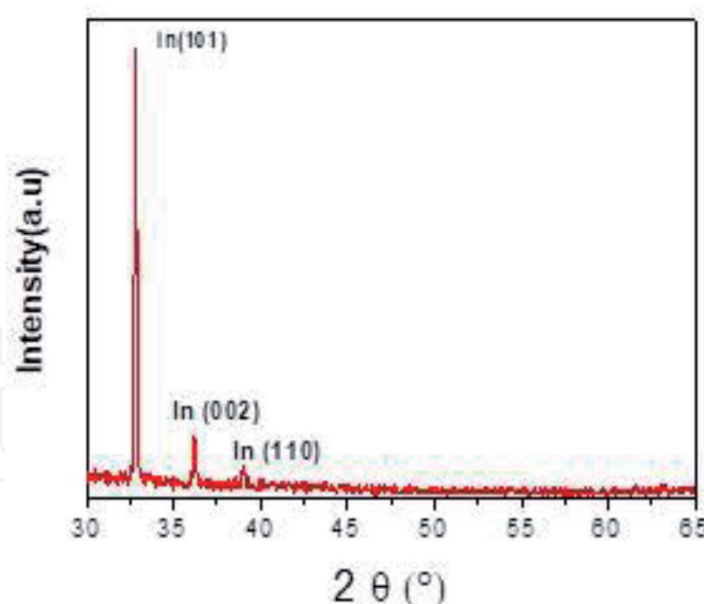


(a)



(b)

**Figure 7.**  
(a) SEM image of indium particles obtained after RTA annealing; A: 300°C, B: 350°C, C: 400°C, and D: 450°C and (b) the corresponding histogram indicating the size distribution.



**Figure 8.**  
*XRD patterns of the sample annealed at 450°C.*

In order to overcome this problem, RTA annealing based on radiation heating by infrared short waves (400–1400 nm) is used. The heating duration could be decreased, thanks to high silicon absorption in this wavelength range.

Indium-coated substrates were annealed at different temperatures (300, 350, 400, and 450°C) during 5 min. It is noticed in **Figure 7(a)** that for the temperatures 300 and 350°C, the surface morphologies are quite similar. The substrates are covered with inhomogeneous particles in size and shape, with a high surface density. An improvement in the particles shape is obtained at 400°C. At the temperature of 450°C, quasi-spherical and homogeneous particles are obtained. The structures elaborated at 450°C show an average size of 422 nm (**Figure 7(b)**). This amelioration is attributed to the indium oxide absence as confirmed by XRD (**Figure 8**).

## 6. Indium-catalyzed SiNWs grown by VLS mode

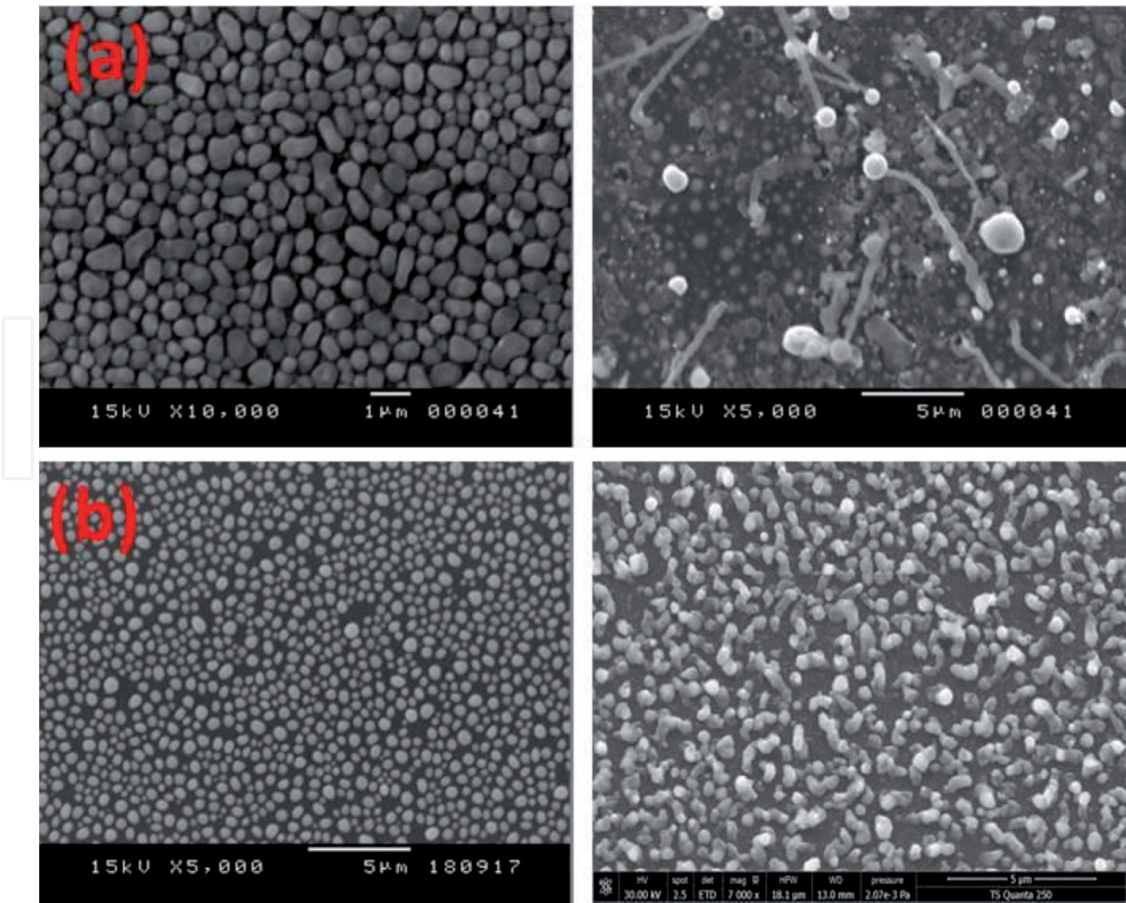
### 6.1 Influence of indium oxide

To study the indium oxide influence on the grown silicon nanowires, a comparative study is carried on. Silicon nanowires are grown using indium nanoparticles elaborated by the two different annealing processes: the conventional and the RTA annealing. **Figure 9(a)** and **(b)** shows the SEM images of the obtained nanowires. The elaborated indium particles have been treated by hydrogen gas with a flow rate of 60 sccm for 10 min before the silane introduction during 15 min.

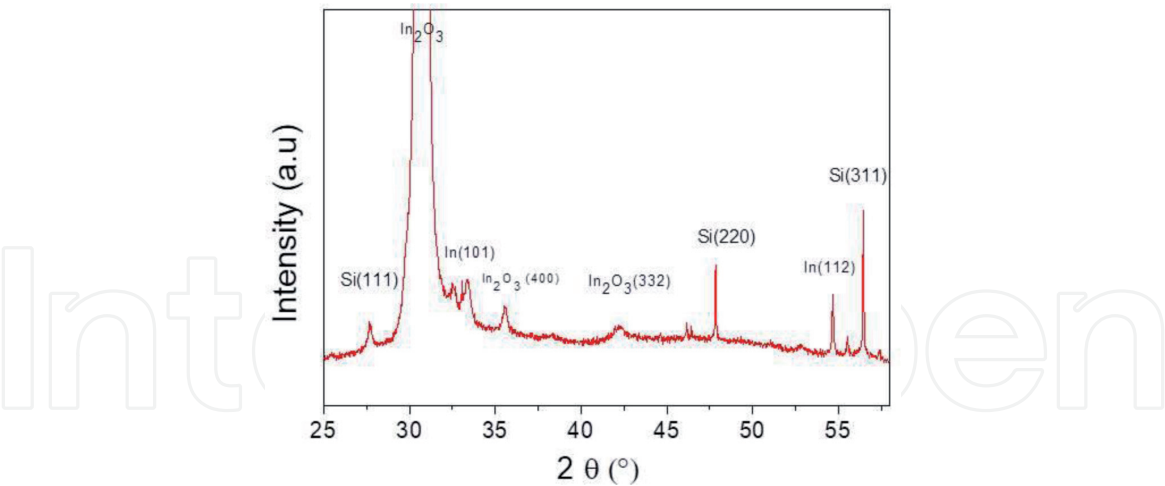
As observed, the indium particles elaborated by conventional annealing morphology are enhanced and quasi-spherical particles are obtained. Despite this improvement, the SiNWs' density is very low due to the persistence of indium oxide after the hydrogen treatment as explained in Section 3. The indium oxide forming a shell around indium is decreasing its catalytic effect. To confirm the persistence of indium oxide, XRD of the obtained SiNWs is performed (**Figure 10**). In addition to silicon and indium peaks, we notice the presence of  $\text{In}_2\text{O}_3$  peaks explaining the obtained low density.

Using indium particles elaborated at 450°C by the RTA process, the SiNWs' density is ameliorated, which is attributed to indium oxide's absence. The quasi-totality of indium particles is active to catalyze the SiNWs' growth.





**Figure 9.** SEM images of (a) indium particles obtained by conventional annealing and the obtained SiNWs and (b) indium particles obtained by RTA annealing and the obtained SiNWs.



**Figure 10.** XRD spectrum of SiNWs catalyzed by indium particles elaborated by conventional annealing.

Indium particles catalyzing the growth are located on the top of the silicon nanowires confirming the VLS mode. Moreover, we notice that the SiNWs' morphology does not seem to depend on the annealing process. The obtained SiNWs in both cases are bent and kinked.

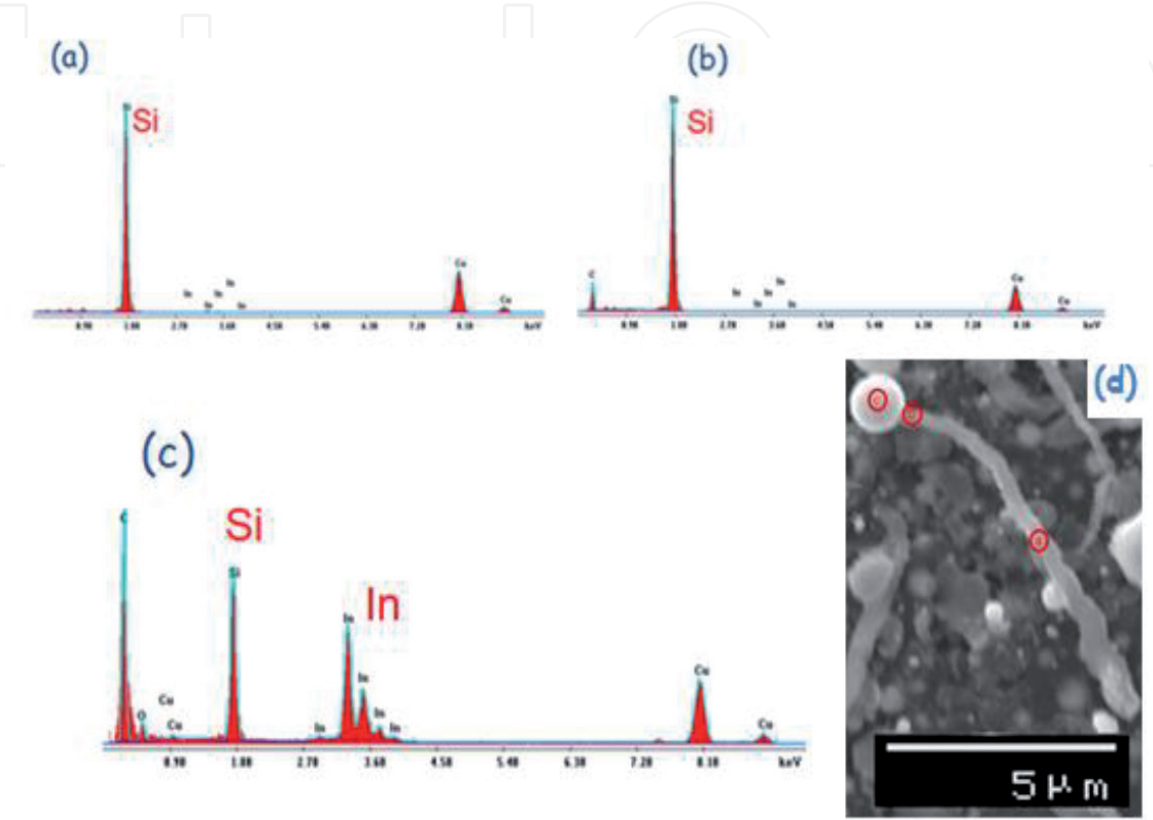
### 6.2 Indium diffusion in SiNWs

In order to study the indium diffusion in the obtained SiNWs, energy dispersive spectroscopy (EDS) is performed on the top and in the middle of a silicon nanowire. **Figure 11** shows that the wire is consisting of silicon only indicating that indium

does not diffuse in the contrary of other catalysts like gold. In addition to that, EDS performed on the catalyst particle shows that the particle is consisting of a indium-silicon alloy as explained by the VLS mode (**Table 1**).

6.3 Indium catalyst removal

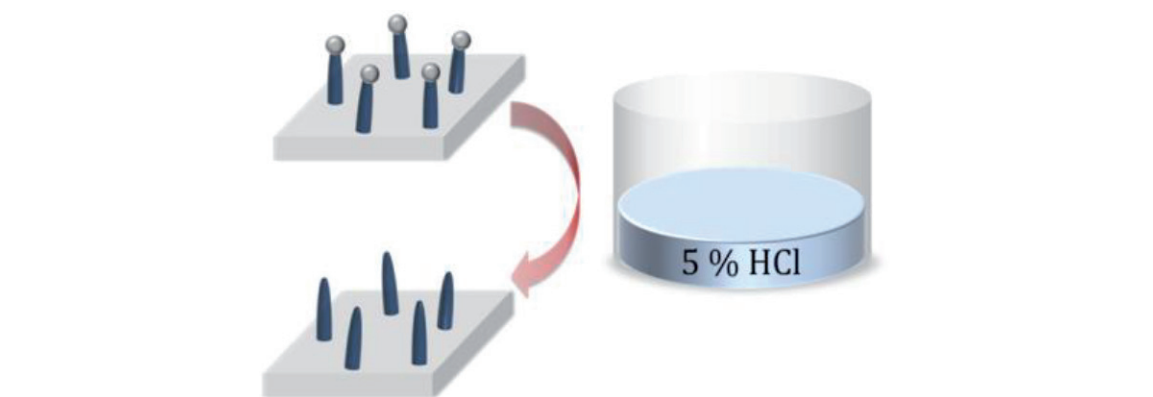
Residual indium could be removed by a simple chemical method consisting of soaking samples in 5% hydrochloric acid (HCl) solution (**Figure 12**). The reaction



**Figure 11.**  
EDS spectra of a wire performed (a) in the middle, (b) on the top, and (c) on the particle catalyst as shown in (d).

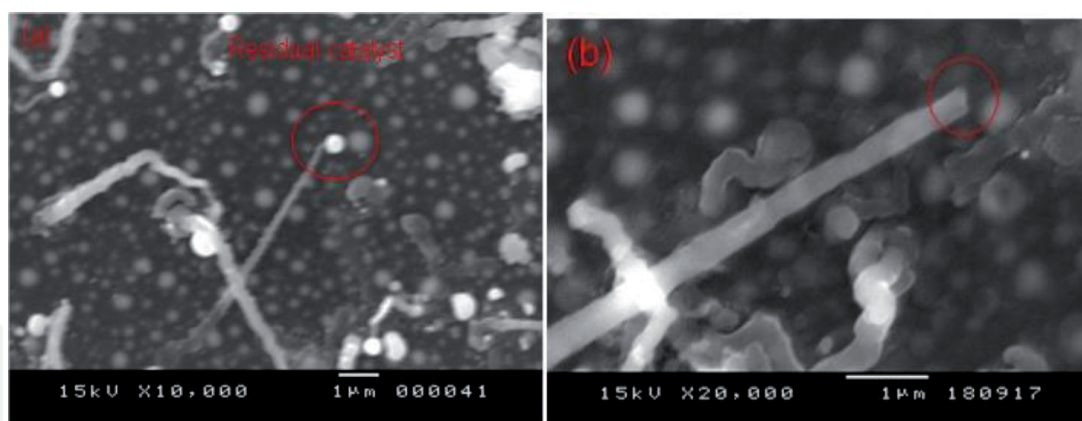
Element (atomic %)	Particle	Top of SiNW	Middle of SiNW
Si	51.1	98.8	99.4
In	48.9	1.2	0.6

**Table 1.**  
Atomic percentage of silicon and indium in a grown silicon wire.



**Figure 12.**  
Illustration of the experimental protocol used.





**Figure 13.** SEM images of SiNWs (a) before and (b) after catalyst elimination.

between In and HCl could potentially produce two types of indium chloride:  $\text{InCl}_2$  or  $\text{InCl}_3$ . **Figure 13** shows the grown silicon nanowires before and after indium catalyst elimination.

## 7. Conclusions

In this work, indium is used as catalyst for silicon nanowires' growth by VLS mode using PECVD. Indium is considered as a promising metal to replace gold as it forms a low-eutectic alloy with silicon and it introduces shallow defects.

Indium catalyst is elaborated by annealing indium-coated silicon substrates using two different annealing processes: conventional and RTA annealing. The annealing conditions influence the catalyst morphology and as a consequence the grown SiNWs. In this work, we have shown that the indium oxide presence is affecting the growth, in particular the density.

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