Chapter

CMOS Integrated Circuits for Various Optical Applications

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Abstract

This chapter presents several CMOS integrated circuits (ICs) realized for various optical applications such as high-definition multimedia interface (HDMI), light detection and ranging (LiDAR), and Gigabit Ethernet (GbE). First, 4-channel 10-Gb/s per channel optical transmitter and receiver array chipset implemented in a 0.13-μm CMOS process are introduced to realize a 10-m active optical cable for HDMI 2.1 specifications. Second, a 16-channel optical receiver array chip is realized in a 0.18-μm CMOS technology for LiDAR applications. Third, a 40-GHz voltage-mode mirrored-cascode transimpedance amplifier (MC-TIA) is implemented in a 65-nm CMOS for a feasible 100-GbE application. Even with advanced nano-CMOS technologies, we have suggested novel circuit techniques for optimum performance, such as input data detection (IDD) for low power, feedforward and asymmetric preemphasis for high speed, double-gain feedforward for high gain, selectable equalizer (SEQ) for specific bandwidth, mirrored-cascode for fully differential topology, etc. We believe that these novel circuit techniques help to achieve low-cost, low-power solutions for various optical applications.

Keywords: active optical cables, CMOS, GbE, HDMI, integrated circuits, LiDAR, TIA, VCSEL driver

1. Introduction

Optical fibers provide a number of advantages over copper-based electrical cables, which include wide bandwidth, low attenuation, low weight, low electromagnetic interference, low crosstalk between channels, etc. Particularly for high-speed digital interconnects, optical fibers may be the ultimate solution to achieve the desired performance. In this chapter, a few CMOS integrated circuits (ICs) are introduced for various optical applications such as high-definition multimedia interface (HDMI), light detection and ranging (LiDAR), and Gigabit Ethernet (GbE).

Section 2.1 presents 4-channel CMOS transmitter (Tx) and receiver (Rx) chipsets for the applications of 10-Gb/s per channel HDMI active optical cables (AOC). Section 2.2 describes a feedforward voltage-mode CMOS Rx IC for LiDAR applications. Section 2.3 introduces a 40-GHz CMOS Rx IC. Then, conclusion is followed.

2. Circuit description

2.1 CMOS chipsets for HDMI active optical cables

High-performance networking and computing systems mandate high-speed optical interconnects to satisfy the extreme bandwidth requirements [1, 2]. Previously, parallel optical interconnects could provide terabit-per-second data bus in board scale [1] and also multi-gigabit-per-second data transport for mega-cloud systems, reaching a 100-m distance [2]. We have recently demonstrated active optical cables specified by HDMI 2.0 standard for true 4K video at 60-Hz resolution for 10-m distance, where 4-channel CMOS Tx and Rx chipsets were integrated on a printed circuit board (PCB) with pluggable connectors at its both ends to transport data via plastic optical fibers (POF) [3]. POF is well known for its benefits over costly glass optical fibers such as low cost, lightweight, resilient to bending, etc. [4]. In this section, we demonstrate a 10-m AOC utilizing graded-index POF with −60-dB/km loss characteristics that equips 4-channel CMOS transmitter and receiver chipsets to support HDMI 2.1 specification, i.e., true 8 Mpixel/60 fps display with no data encoding or compression. For this purpose, it is necessary to align optical devices, optical subassembly, and POF precisely within the tolerance range of ±10 μm.

Figure 1 shows the block diagram of the 4-channel optical ICs, where a 4-channel Tx and Rx chipsets are separately integrated with optical devices. Here, we have employed a number of circuit techniques to optimize the performance, which include feedforward preemphasis at Tx for high-speed operations; input data detection (IDD) for automatic turning off each vertical-cavity surface-emitting laser (VCSEL) diode during its idle time to lower current consumption; double-gain feedforward transimpedance amplifier (TIA) for high gain; selective equalizer for either 6 or 10 Gb/s, depending upon desired HDMI specification; and photodiode

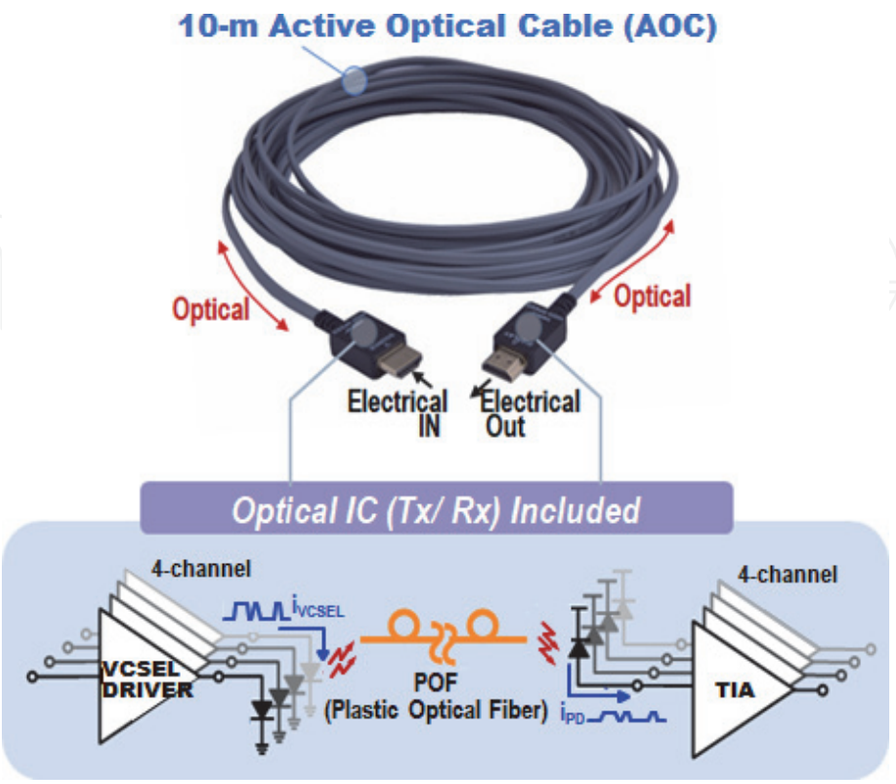

Figure 1.
Block diagram of the 4-channel optical ICs.

monitor for checking if each photodiode emits appropriate photocurrents to the 4-channel Rx array chip.

2.1.1 Optical power budget

There are various sources of coupling loss occurred in its optical alignment. For example, 3-dB coupling loss occurs at the interface of a VCSEL diode to prism due to 50% coupling efficiency, whereas 1-dB coupling loss occurs at the interface of a photodiode to prism [5]. The optimal pitch between VCSEL diodes and photodiodes was carefully selected to be 400 μm to prevent extra coupling loss from misalignment.

Meanwhile, the low-cost POF shows −60-dB/km attenuation, resulting in 1-dB loss. Also, the thermal loss of a VCSEL diode is typically 2 dB at 70°C. Hence, the optical power budget is set to 10 dB including 3-dB additional margin, which leads to the feasible assumption of 0-dBm Tx power and −10-dBm Rx sensitivity.

2.1.2 VCSEL driver

Figure 2 shows the schematic diagram of a 10-Gb/s VCSEL driver that consists of a main driver, a pre-driver, an EQ, and an input buffer. The main driver operates with two current sources, i.e., the bias current (I_{BIAS}) and the modulation current (I_{MOD}). When M_{5N} in the main driver is turned off, the current sum (I_{BIAS}+I_{MOD}) flows through the VCSEL diode. When M_{5N} is on, only I_{BIAS} is supplied to the VCSEL diode. The feedforward preemphasis is conducted by using a capacitor (C_{FF}) to alleviate the distortion effects of the output waveforms from the bond-wire inductance and the parasitic capacitance of a VCSEL diode. Simulations confirm 19.2% faster rising time in the output waveforms.

Considering the device reliability of VCSEL diodes, it is not clever to keep I_{BIAS} to flow continuously through the array chip because it will rise the device

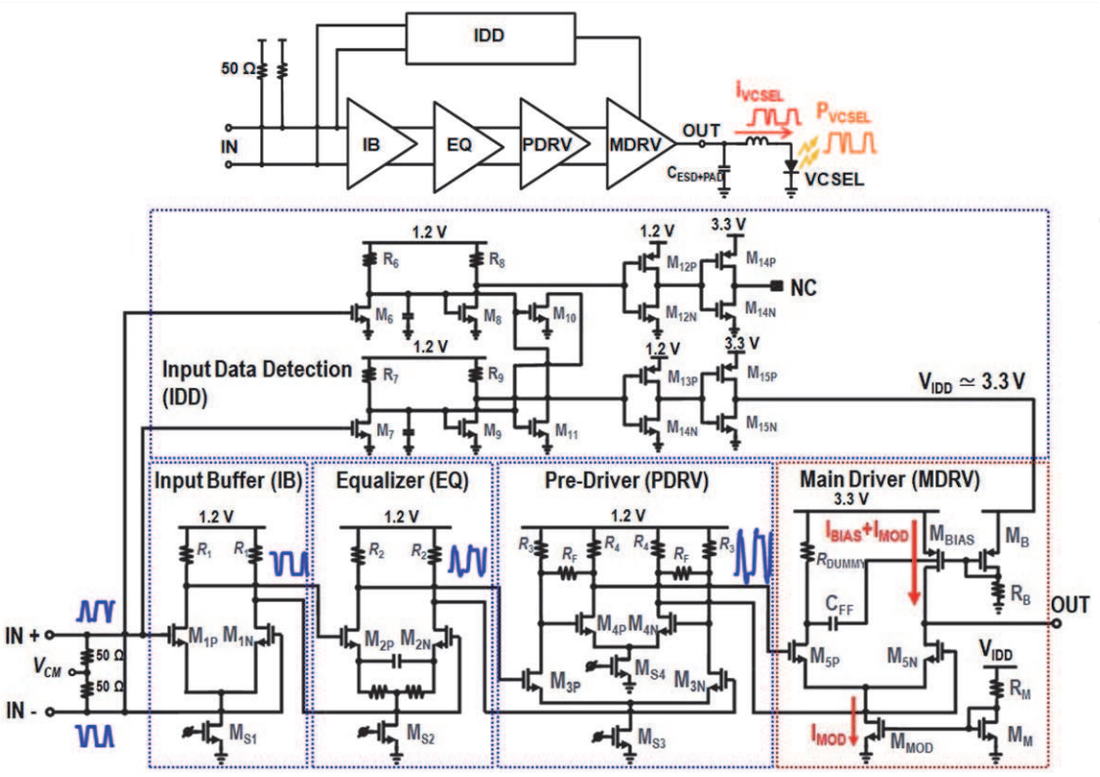

Figure 2.
Schematic diagram of the VCSEL driver.

temperature and thus the slope efficiency and expectant life period of VCSEL diodes will be severely deteriorated. Hence, input data detection circuit can be employed to avoid the superfluous current flow by turning off VCSEL diodes when no input signal transitions occur. Only with the emergence of input data, IDD detects the data transition and generates an average DC voltage, i.e., 3.3 V in this work through an active low-pass filter (LPF).

Then, this DC voltage turns on the two current sources in the main driver. Certainly, the turn-on delay of the current sources should be shorter than the signal delay from the main driver input.

Figure 3 shows the chip microphotograph of the 4-channel VCSEL driver array realized in a 0.13-μm CMOS process, where the chip core of each channel occupies the area of 350 × 250 μm^2. Each channel dissipates 21.25 mA (max.), in which the main driver consumes 11.6 mA.

Figure 4 demonstrates the optically measured output eye diagrams at 10 Gb/s with a 10-m POF connected to a digital communication analyzer (DCA Agilent 861150D), where it is clearly seen that there is no overlap area of 0.6-UI optical mask condition.

Table 1 compares the performance of the 4-channel Tx array chip with prior arts, in which only this work provides the measured optical magnitude amplitude (OMA) with a 10-m attached.

2.1.3 Voltage-mode CMOS feedforward TIA

Typically, the front end of an optical Rx comprises a photodiode and a TIA that converts the incoming current signals from the photodiode into output voltages. For optimum performance, TIA is usually required to achieve high transimpedance gain, wide bandwidth, low noise, and low power consumption.

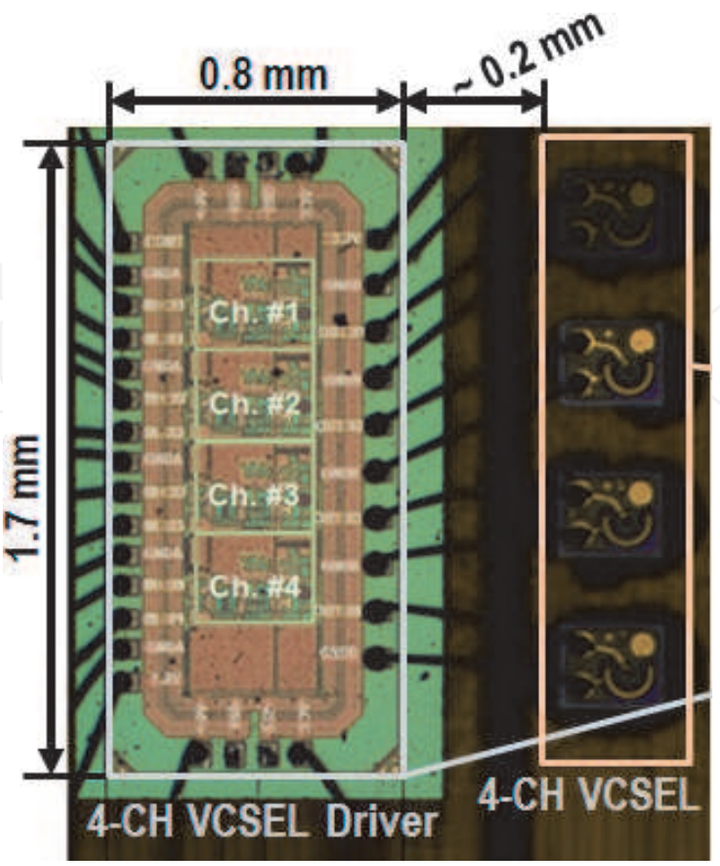

Figure 3.
Chip microphotograph of the 4-channel VCSEL driver array.

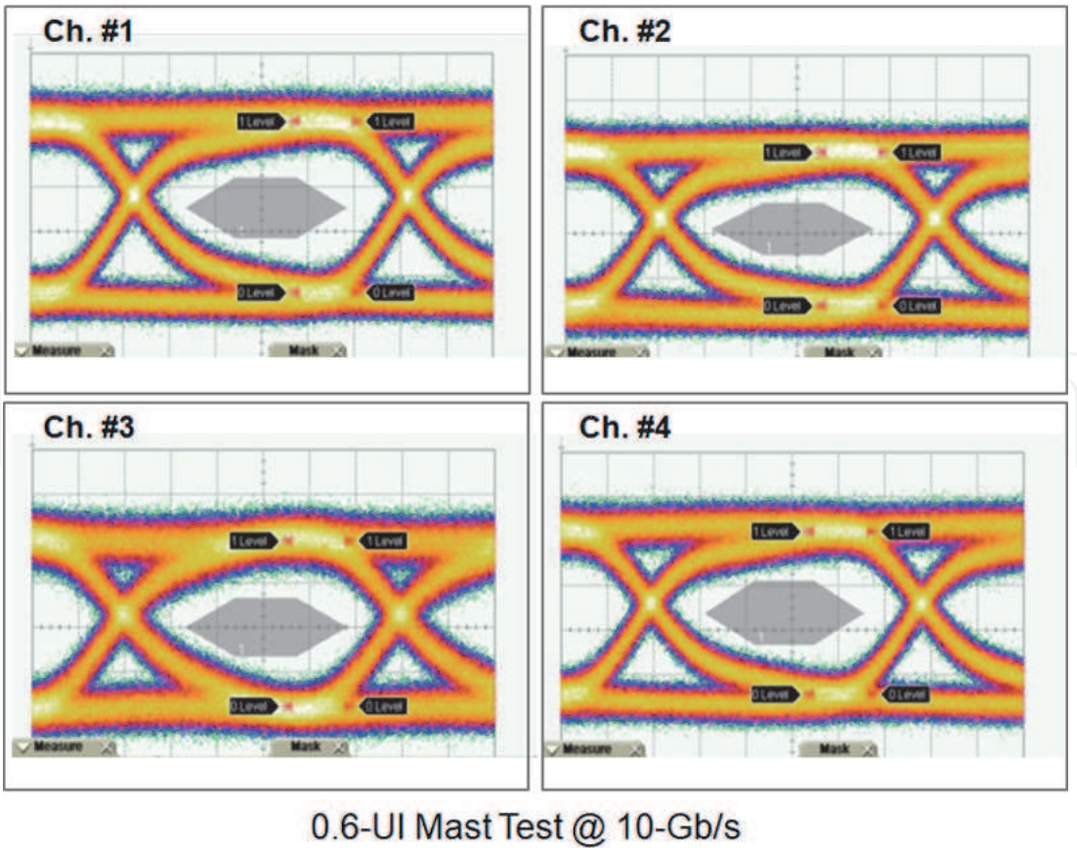

Figure 4.
4-channel eye mask at 10 Gb/s.

Parameters	[6]	[7]	[8]	[9]	[10]	This work
CMOS [nm]	65	65	90	28	65	**130**
Dara rate [Gb/s]	10	25	25	28	15	**10**
Channels	4	4	1	1	1	**4**
V_{DD} [V]	1.2/2.5	1.0/3.3	1.2/2.65	2.9	1.0/2.5	**1.2/3.3**
C_{VCSEL} [pF]	–	0.15	0.3	–	0.5	**0.85**
I_{MOD} [mA_{pp}]	4.0	6.7	–	5.5	6.0	**6.0**
I_{BIAS} [mA]	6.0	4–12	–	2.5	2.0	**5.6**
RMS jitter [% UI]	1.01	3.5	–	–	7.35	**4.8***
OMA [dBm]	–	−1	1.23	0.032	2.3	**>−6.77***
Current dissip. [mA]	16.3	67.6	38.6	17.6	23.8	**21.25**
Core area [mm^2]	0.125	0.353	0.006	0.001	0.04	**0.074**

**Measured with a 10-m POF attached.*

Table 1.
Performance summary of the 4-channel Tx array chip with prior arts.

To this end, we have developed a double-gain feedforward TIA, also known as the voltage-mode CMOS feedforward (VCF) TIA. **Figure 5** shows the schematic diagram that consists of the VCF input stage with DC offset current cancelation scheme, a single-to-differential converter, a selectable equalizer (EQ), an output buffer (OB), and a photodiode monitor. The double-gain feedforward input stage merges an inverter with a feedback resistor and a common-source amplifier

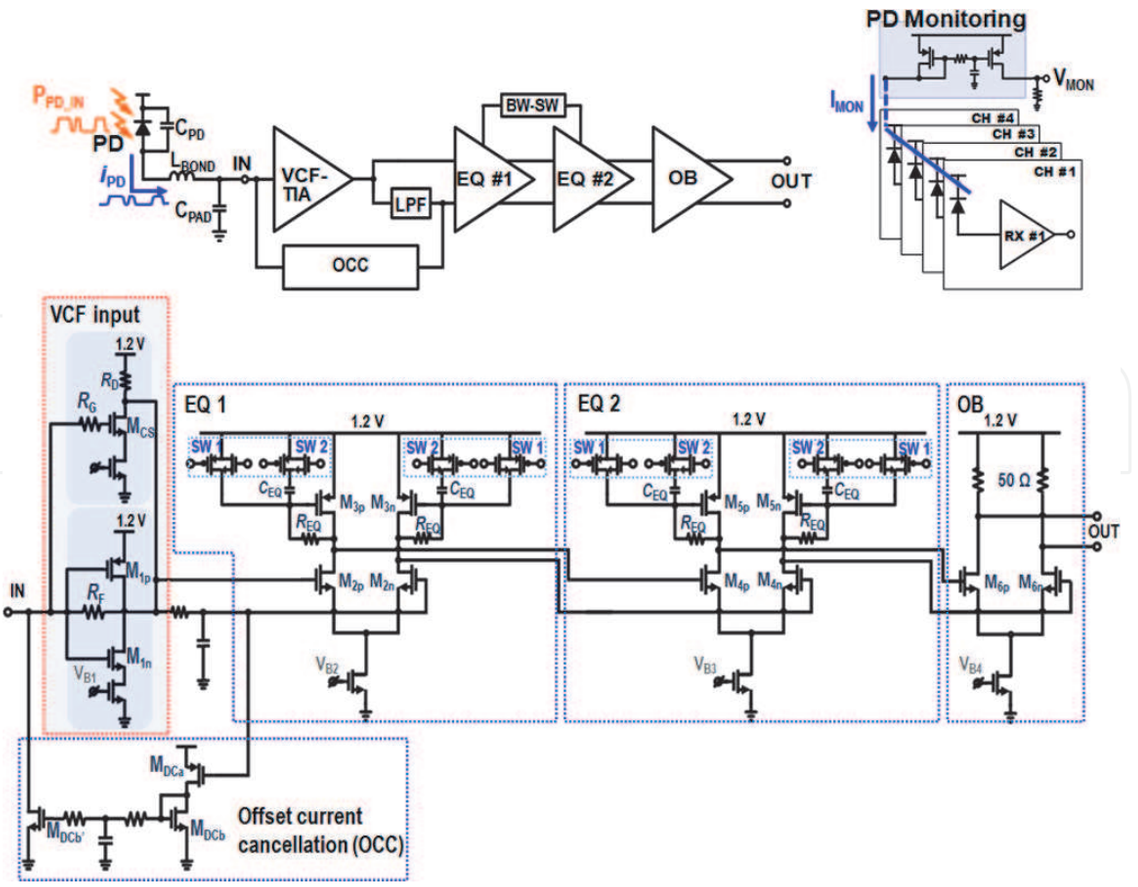

Figure 5.
Schematic diagram of the VCF-TIA.

together so that the transimpedance gain can be twice higher than a conventional inverter input stage. A two-stage EQ is followed not only to extend the bandwidth but also to select the operation speed to be either 6 Gb/s or 10 Gb/s with respect to the HDMI specification. With the switch 1 (SW1) turned on, the bandwidth is extended to 6 GHz for 10-Gb/s operations with a slight gain peaking. With the switch 2 (SW2) turned on, the bandwidth shrinks to 4 GHz for 6-Gb/s operations.

As for monitoring the input signal strength, the received signal strength indicator (RSSI) is utilized with an external resistor. However, a multichannel Rx array chip mandates the same number of external resistors for RSSI, which complicates the PCB assembly. Therefore, we suggest a simple PMOS current mirror circuit that generates an average DC voltage via only one fixed external resistor, thereby detecting the photodiode failure easily.

Figure 6 shows the chip microphotograph of the 4-channel Rx array chip realized in a 0.13-μm CMOS process, where the core of each channel occupies an area of $400 \times 150\ \mu m^2$. Each channel consumes 21.2 mA, in which the OB dissipates 8.2 mA. For optical measurements, we have utilized a 4-channel GaAs p-i-n photodiode array that provides 0.6-A/W responsivity.

Figure 7 demonstrates the optically measured output eye diagrams of the 4-channel Rx array chip at the digital oscilloscope (Agilent DSA-X 92004A) via a 10-m POF, which was driven by a pulse pattern generator (Agilent ParBERT 81250) with 2^{31}-1 PRBS differential input swings of 800 mV_{pp} at different data rates of 5 Gb/s, 6.25 Gb/s, 8 Gb/s, and 10 Gb/s, respectively. When the SW1 was turned on, it obtained wide and clean eyes up to 10 Gb/s. Otherwise, the highest achievable data rate was 6.25 Gb/s, where the total jitter was measured to be 34.5 ps_{pp}. Also, the bit error rate (BER) of the 4-channel Rx array chip was measured by utilizing an error detector (Agilent ParBERT 81250-N4873A). With a 10-m POF attached, the

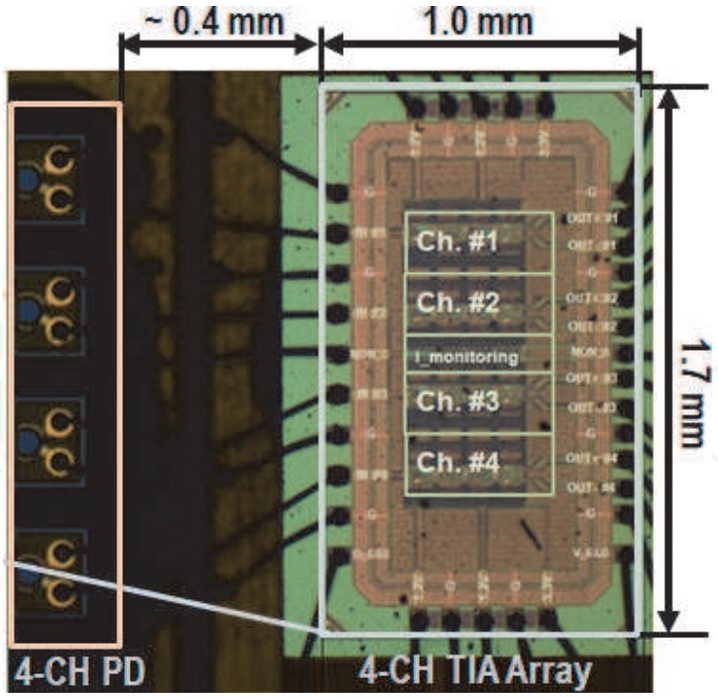

Figure 6.
Chip microphotograph of the 4-channel VCF-TIA array.

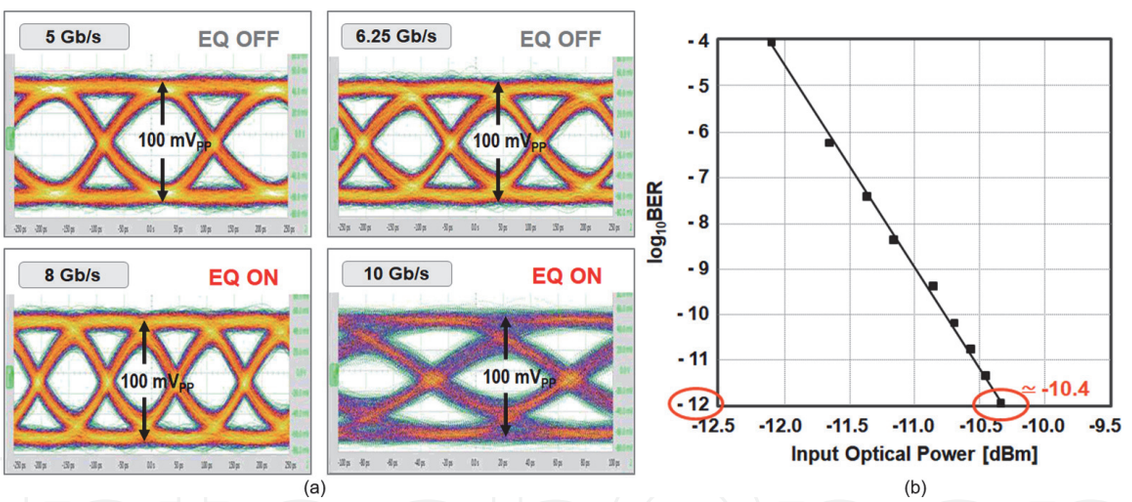

Figure 7.
Measured eye diagrams.

sensitivity of the 4-channel Rx array chip was measured to be -10.4 dBm for 10^{-12} BER at 10-Gb/s data rates.

Table 2 compares the performance of the 4-channel Rx array chip with prior arts, in which it should be noted that this work provides the measured optical sensitivity with a 10-m attached.

2.2 CMOS Rx IC for LiDAR

Light detection and ranging systems utilize laser pulses to detect surrounding targets efficiently and thus to characterize the scene in three-dimensional images [15, 16]. Therefore, LiDARs can be exploited to various applications such as unmanned vehicles to recognize pedestrians, driving lanes, natural objects, other vehicles, etc. For obtaining high-resolution images, a linear-mode LiDAR sensor with a multichannel optical Rx array can be an effective solution because the Rx

Parameters	[11]	[12]	[13]	[14]	This work
CMOS [nm]	130	180	65	65	**130**
Dara rate [Gb/s]	10	10	12	18	**10**
Channels	1	1	1	1	**4**
V_{DD} [V]	1.5	1.8	1.2	1.2	**1.2**
C_{PD} [pF]	0.25	0.2	0.05	Integrated	**0.25**
TZ gain [dBΩ]	50	68.3	–	102	**56.7**
BW [GHz]	7.0	7.0	3.5	12.5	**6.0**
Sensitivity for 10^{-12} BER [dBm]	−12.4**	−19	−16.8	−4.9	**−10.4***
Power dissip. [mW]	7.5$^{\Delta}$	81	23	48	**25.4**
Energy efficiency [pJ/b]	0.75$^{\Delta}$	8.1	1.92	2.7	**2.54**
Core area [mm^2]	0.016$^{\Delta}$	0.78	0.12	0.23	**0.06**

**Measured with a 10-m POF attached.*

***Electrically estimated.*

$^{\Delta}$Single-ended TIA input stage only.

Table 2.
Performance summary of the 4-channel Rx array chip with prior arts.

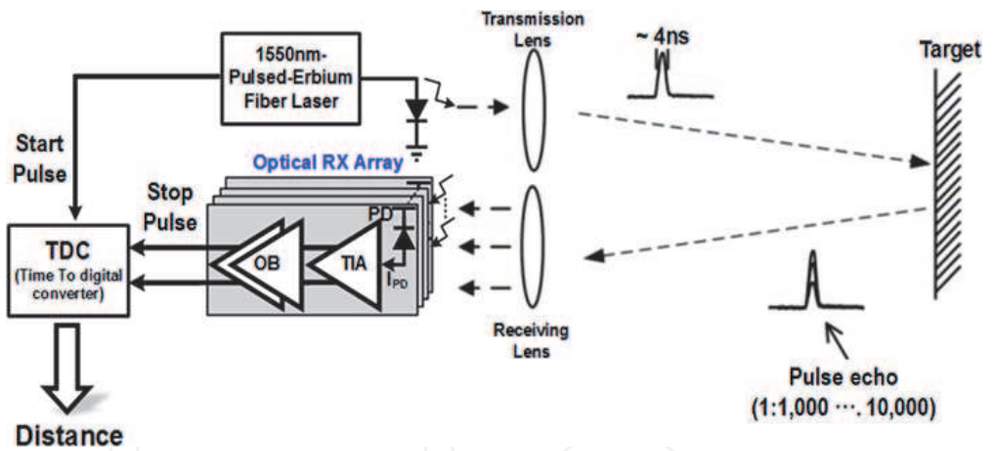

Figure 8.
Simplified block diagram of a typical LiDAR system.

array not only improves the object detection rate but also reduces the confusion matrix of point classification [17].

Figure 8 shows the simplified block diagram of the front-end circuitry in a typical linear-mode LiDAR sensor, which consists of a multichannel TIA array and a time-to-digital converter (TDC). As a photodetector, avalanche photodiodes (APDs) are exploited to acquire the detection range up to several tens of meters [18–21].

However, APDs need very high bias voltages of 50–200 V, thereby requiring overcurrent protection circuitry to avoid device saturation or damage. In this work, we have utilized an InGaAs p-i-n photodiode with 0.9-A/W responsivity biased with a low supply voltage of 5 V.

As a TIA, the most popular configuration has been a voltage-mode inverter with a feedback resistor. But, this inverter TIA has an inherent design trade-off between transimpedance gain and bandwidth, which may lead to considerable noise increase and sensitivity degradation [22]. Therefore, we have employed the

VCF-TIA in this work, hence clearly detecting the targets of 5% reflection rate within the range of 0.5–25 m.

2.2.1 Overview of linear-mode LiDAR sensor

The linear-mode LiDAR sensor emits optical laser pulses with 4-ns pulse width from a 1550-nm pulsed erbium fiber laser with the average power of 0.34–1.4 W and at the rate of 25 kHz. Also, a beam spread with the fan angle of 15o and the line intensity uniformity of less than 10% is utilized to transform laser beams into straight lines in far field. As a target, a 1×1 m^2 black panel of which reflection rate is only 5% is utilized. In the Rx module, a 16-channel VCF-TIA array chip is wire bonded to a 16-channel InGaAs p-i-n photodiode array (Hamamatsu G7150-16) on an FR4 PC board.

2.2.2 VCF-TIA

TIA design for LiDAR sensors mandates wide-range transimpedance gain, i.e., high gain to detect the minimum input pulses for long-range detection versus low gain for short-range detection, wide bandwidth to recover the reflected narrow pulses, low noise for weak signal detection, and low power dissipation per channel to guarantee the reliability of multichannel Rx chips.

Figure 9 depicts the schematic diagram of the VCF-TIA, which comprises the VCF input stage for current-to-voltage conversion, a low-pass filter for single-to-differential conversion, a differential gain stage for gain boosting, and an OB for 50-Ω impedance matching. First, the small-signal analysis shows that the input resistance and the mid-band transimpedance gain (Z_T) of the VCF input stage are given by

$$R = \frac{v}{i} = \frac{\left(1 + \frac{R}{r_{o1}\|r_{o2}\|\|r_{o3}\|R_L}\right)}{\left(g_{m1} + g_{m2} + g_{m3} + \frac{1}{r_{o1}\|r_{o2}\|\|r_{o3}\|R_L}\right)} \cong \frac{1 + (3R_f/r_o)}{g_{m1} + g_{m2} + g_{m3}} \cong \frac{1}{g_{m1} + g_{m2} + g_{m3}} \tag{1}$$

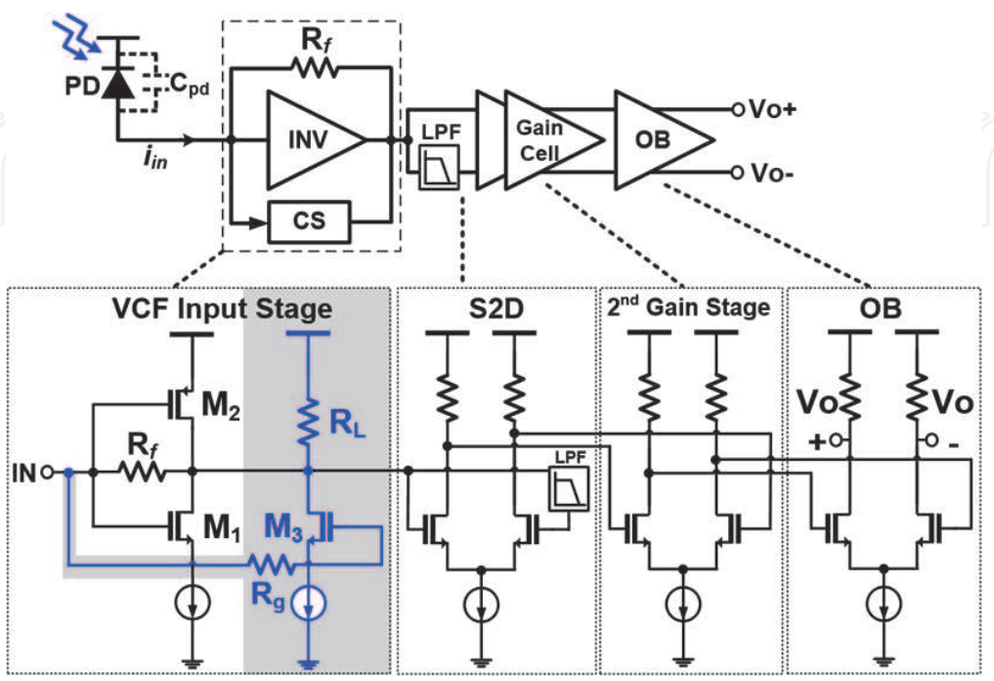

Figure 9.
Schematic diagram of the VCF-TIA.

$$Z_T = \frac{v_{out}}{i_{in}} = \frac{1 - R_f\left(g_{m1} + g_{m2} + g_{m3}\right)}{\frac{1}{R_L} + \left(g_{m1} + g_{m2} + g_{m3}\right)} \cong -R_f \tag{2}$$

where R_f is the feedback resistance, the load resistance (R_L) is assumed to be very large, and $g_{mi(i=1\sim3)}$ and $r_{oi(=1\sim3)}$ represent the transconductance and the output resistance of a transistor $M_{i(i=1\sim3)}$, respectively.

It is clearly seen that the input resistance (R_{in}) can be lowered by increasing g_m and thus R_f can be enlarged twice higher than in a conventional inverter TIA, so that the transimpedance gain can be doubled.

Second, the bandwidth (f_{-3dB}) of the VCF input stage is largely determined by the time constant (τ_3) at the gate of M_3 because the input time constant (τ_{in}) can be non-dominant by the boosted g_m and the output time constant (τ_{out}) can be negligible due to the small drain-bulk capacitances. Therefore, the bandwidth is given by

$$f_{-3dB} = \frac{1}{2\pi(\tau + \tau_3 + \tau_{out})} \cong \frac{1}{2\pi\tau_3} \frac{1}{2\pi R_g\left\{C_{gs3} + C_{gd3}\left[1 + \left(g_{m1} + g_{m2} + g_{m3}\right)R_f\right]\right\}} \tag{3}$$

where R_g is the series resistance at the gate of M_3 and C_{gs3} and C_{gd3} represent the capacitances of the feedforward transistor (M_3).

Third, the input-referred equivalent noise current spectral density of the VCF input stage is given by

$$\begin{aligned} i_{eq}^{2} &\cong i_{Rf}^{2} + \left(\frac{1}{R_f} + sC_T\right) \times \left[\frac{i_{d1}^{2}}{g_{m1}^{2}} + \frac{i_{d2}^{2}}{g_{m2}^{2}} + \frac{\left(i_{d3}^{2} + i_{RL}^{2}\right)}{g_{m3}^{2}} + v_{Rg}^{2}\right] \\ &\cong \frac{4kT}{R_f} + 4kT\left[\Gamma\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + \frac{1}{g_{m3}}\right) + R_g\right] \times \left(\omega C_T\right)^2 \end{aligned} \tag{4}$$

where k is the Boltzmann's constant, T is the absolute temperature, Γ is the noise factor of a MOSFET, and $i_{Rf}^{'}$, $i_{RL}^{'}$, and $i_{di(i=1\ 3)}^{'}$ represent the thermal noise current spectral densities of R_f, R_L, and $M_{i(i=1\sim3)}$, respectively. $v_{Rg}^{'}$ is the thermal noise voltage spectral density of R_g, and C_T (=C_{pd} + C_{in}) is the total input capacitance of the VCF input stage that consists of the photodiode capacitance (C_{pd}) and the input parasitic capacitance (C_{in}) of the VCF input stage. It is clearly seen that the critical factors to determine the high-frequency noise are R_f, g_m, and R_g. Increasing R_f boosts the transimpedance gain and lowers the low-frequency noise, while decreasing R_g not only reduces the high-frequency noise but also extends the bandwidth. The values of g_m should be judiciously selected to optimize the design trade-off between input resistance, bandwidth, and high-frequency noise.

Meanwhile, the VCF-TIA equips the function of overcurrent signal detection because the unexpected situations of overcurrent signals may often occur on real roads such as collisions with pedestrians and other cars. Therefore, all the 16 channels of the VCF-TIA array chip exploit automatic gain control (AGC) scheme to avoid the potential danger that consists of 4 NMOS switches with series resistors. This four-level gain control is satisfactory to accommodate the input photocurrents from 1 μA_{pp} to 1.1 mA_{pp}. All the switches are closed simultaneously with a control voltage (V_{cont}) larger than 0.65 V which corresponds to 800 μA_{pp} input currents. For a larger current, the VCF-TIA output would be saturated.

Test chips of the 16-channel VCF-TIA array were realized in a 0.18-μm CMOS process. **Figure 10** shows the test setup for the linear-mode LiDAR sensor, where an infrared camera was also used to capture black and white images for the target distance of 2, 5, 15, and 25 m, respectively.

The distance (R) between a target and the pulsed erbium fiber laser is estimated by

$$R = \frac{c \times t_{ns}}{2} = 0.15 \times t_{ns} \tag{5}$$

where c is the speed of light and t_{ns} is the round-trip time [15].

Figure 11 demonstrates the recovered output pulses with 340-mW average laser power, revealing that the Rx module can detect the target vividly within the range of 25 m.

Figure 12 shows the measured constant output pulses even with the variation of average optical powers from 0.65 W to 1.4 W, where the target is located at 0.5 m away from the laser source.

Figure 13 depicts the measured transimpedance gain, where the maximum value of 76 dBΩ is maintained for small input currents from the minimum detectable current of 1.14 μA_{pp} to the maximum current of 327 μA_{pp} with the photodiode responsivity of 0.9 A/W. Also, the minimum transimpedance gain becomes 41 times lower, i.e., 44 dBΩ. Hence, the input dynamic range (DR) defined by the ratio of the maximum and minimum detectable input currents times the gain variation, as described in [22], is given by

$$DR \equiv DR(highgainmode) \times max\ gain\ ratio = \left(\frac{327}{1.14}\right) \times (41) = 11,760 \tag{6}$$

2.3 High-speed CMOS receiver ICs

Recently, 100-Gigabit Ethernet (100 GbE) systems have received a great deal of attention [23]. Although quad 25-Gb/s per channel circuits can be a feasible solution in practice, there is still a need to increase the per channel bandwidth further so that a single-channel 100-Gb/s operation can be ultimately realized.

Previously, a number of high-speed TIAs have been introduced, in which the single-ended shunt-feedback topology was mostly preferred to achieve high sensitivity and low power consumption [24]. However, the single-ended circuit is vulnerable to common-mode noises occurred from power supply rails and silicon substrate, which might be detrimental in a 4-channel 25-Gb/s/ch optical Rx array chip for the applications of 100-GbE systems. Therefore, differential architecture is strongly desired even at the TIA input stage in order to reduce common-mode

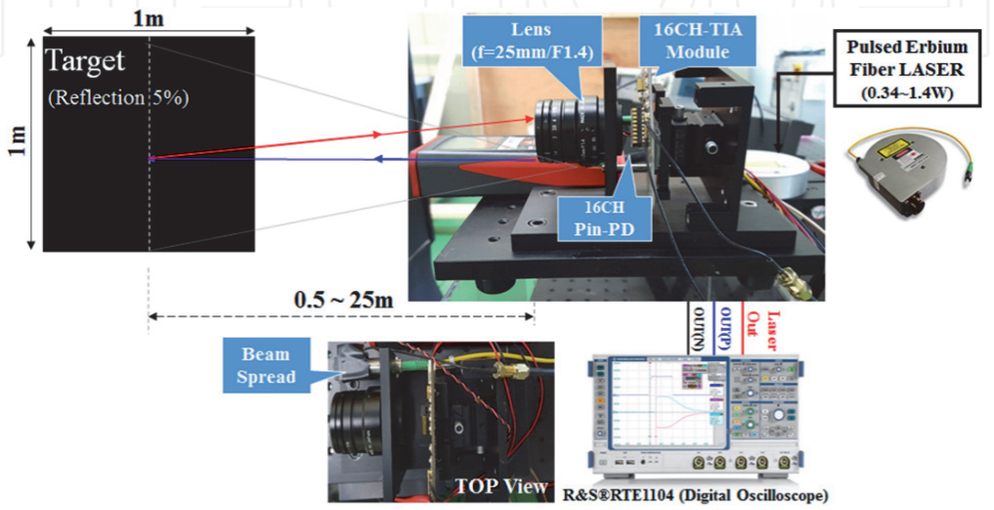

Figure 10.
Test setup of the 16-channel VCF-TIA array.

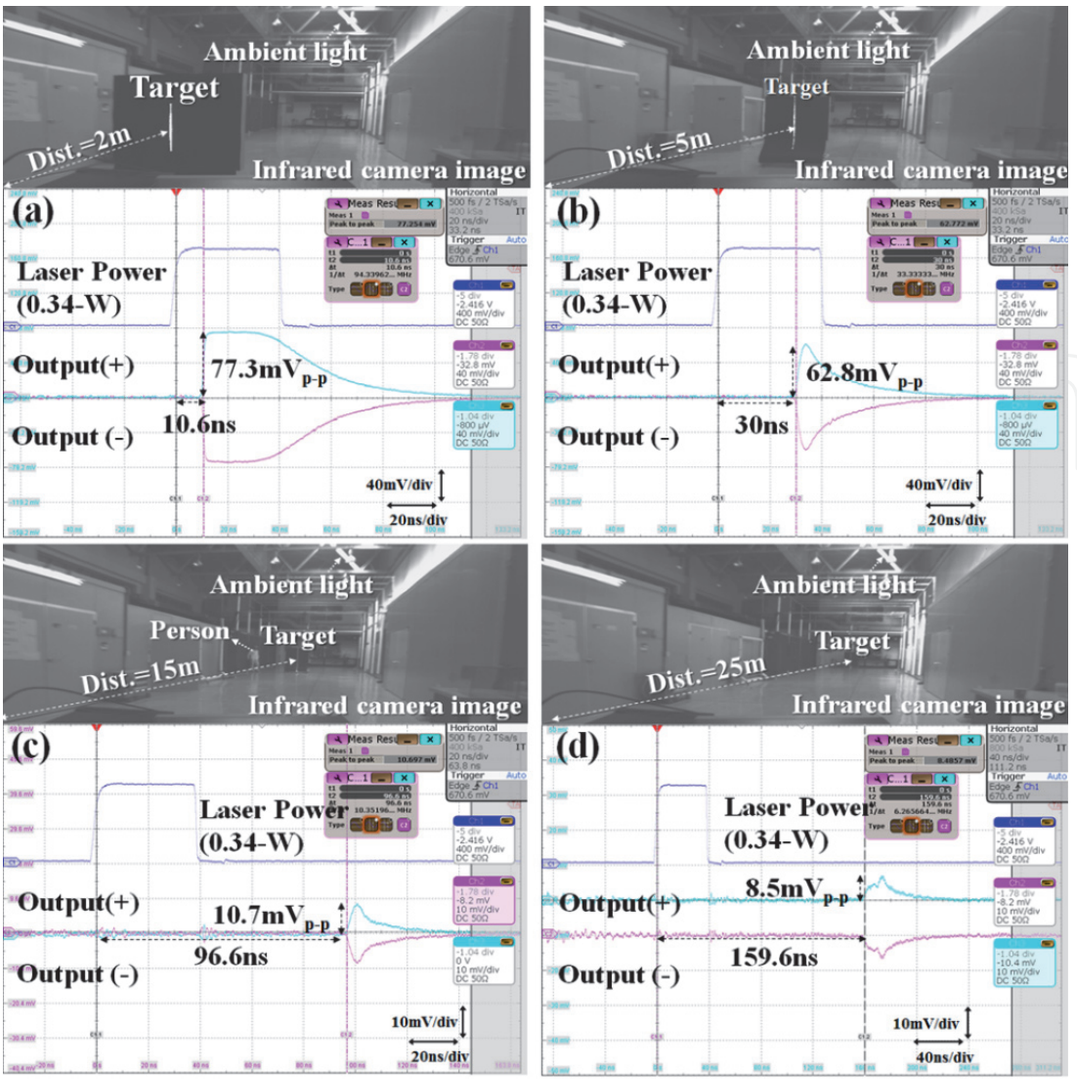

Figure 11.
Recovered output pulses from 2 to 25 m.

noises. In [25], two photodiodes were utilized to construct a fully differential TIA, which successfully alleviated the effects of the coupled common-mode noises. Yet, it was costly and rendered the PC board design complicated especially in the case of multichannel parallel interconnects. Alternatively, pseudo-differential structure was suggested, which however mandates either a passive low-pass filter (LPF) or a dummy TIA as a replica circuit [26]. The former cannot provide fully differential signaling without the following differential amplifier stages after the LPF, which certainly increases chip area and power consumption. The latter can hardly remove the DC offset between the TIA core and the dummy, let alone the increase of power consumption. Recently, we have presented a fully differential modified regulated cascode TIA in [27]. Yet, it suffered inherent noise degradation because of the current-mode common-gate input configuration.

In this chapter, a novel mirrored-cascode (MC) input configuration is introduced to overcome all these shortcomings, in which the NMOS cascode amplifier with a resistive feedback generates negative output voltages while its mirrored-cascode circuit via an AC-coupling capacitor yields positive counterparts. Since the MC input configuration shares the basic topology of a typical cascode TIA, it can provide an inherent advantage of noise performance over current-mode configurations such as a common-gate TIA [28], a regulated cascode TIA [29], and a current mirror TIA [30].

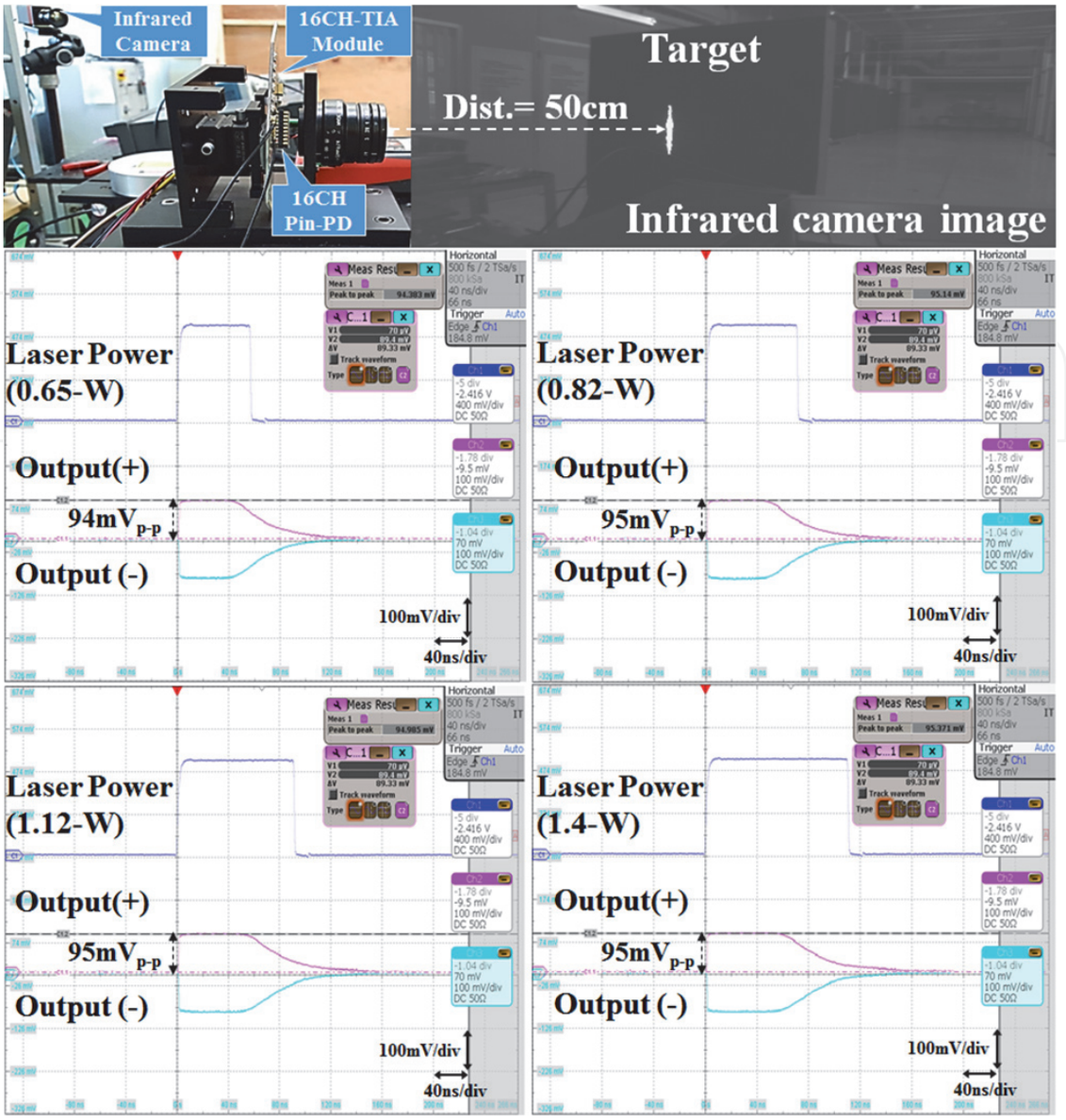

Figure 12.
Recovered output pulses within 0.5 m.

Meanwhile, a standard 65-nm CMOS process was utilized to implement the high-speed fully differential mirrored-cascode transimpedance amplifier (MC-TIA) with extensive exploitation of inductive peaking techniques to achieve 40-GHz bandwidth. In particular, asymmetric T-coil transformers were employed owing to their broadband characteristics, thereby reducing silicon area and lowering chip cost [31]. **Figure 14** shows the schematic diagram of the proposed MC-TIA.

2.3.1 Mirrored-cascode input configuration

Figure 15 depicts the simplified schematic diagram of the MC input stage, where the single-ended input current (i_{pd}) from a p-i-n photodiode flows into an NMOS cascode stage (M_1, M_3, R_1, and R_{F1}), giving rise to a negative output voltage (v_{o1}). It is noted that the drain voltage of M_1 is almost equal to the inverted gate voltage of M_1. Then, this negative voltage passes through an AC-coupling capacitor (C_c), appears at the gate of M_2 as an input signal of the mirrored-cascode stage (M_2, M_4, R_2, and R_{F2}), and hence generates a positive output voltage (v_{o2}) at the drain of M_4.

The input resistance of the MC input stage is given by

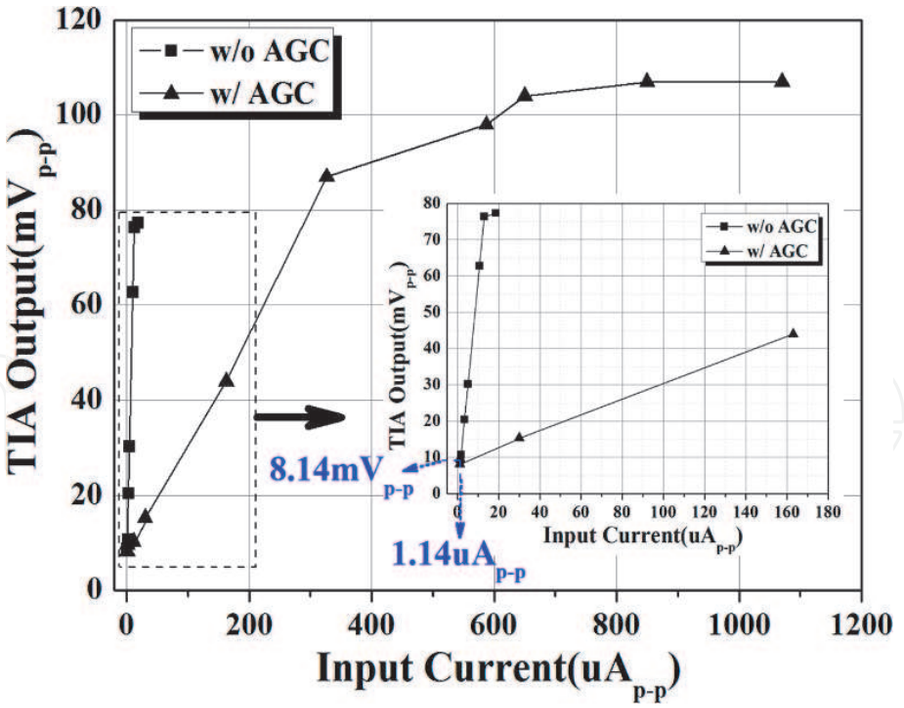

Figure 13.
Measured transimpedance gain with AGC.

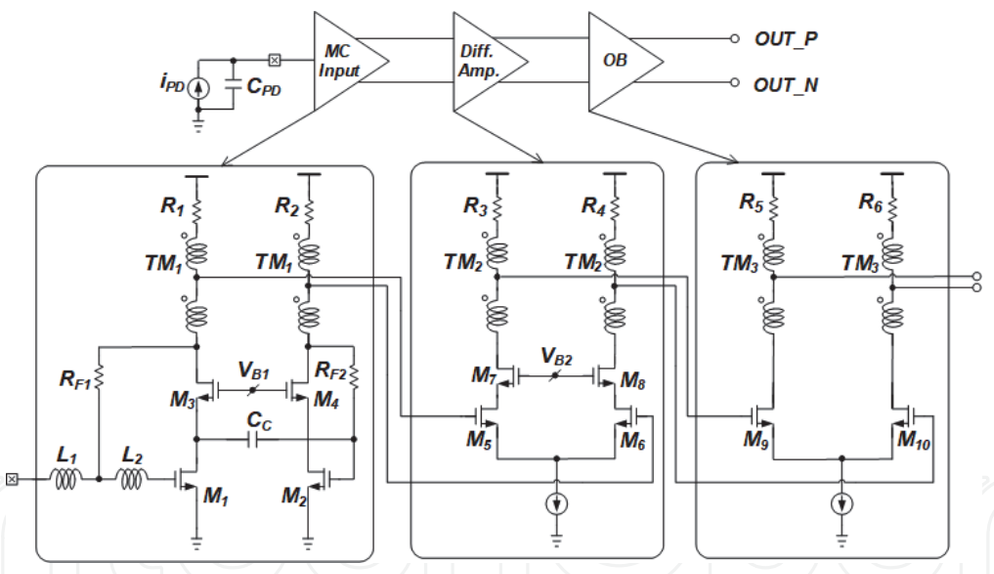

Figure 14.
Schematic diagram of the MC-TIA.

$$Z(0) = \frac{v}{i} = \frac{R_{F1}}{1 + g_{m1}R_1} \tag{7}$$

where g_{m1} is the transconductance of M_1.
The mid-band small-signal transimpedance gain at each drain node is given by

$$\begin{aligned} \frac{v_{o1}}{i_{pd}}(0) &= -\left(\frac{g_{m1}R_1R_{F1}}{1 + g_{m1}R_1}\right) \cong -R_{F1} \\ \frac{v_{o2}}{i_{pd}}(0) &= \frac{g_{m1}(g_{m2}R_2)R_{F1}}{(1 + g_{m1}R_1)g_{m3}} \cong R_{F1} \end{aligned} \tag{8}$$

where $g_{mi(i=1\sim3)}$ is the transconductance of $M_{i(i=1\sim3)}$.

The intrinsic output resistance (r_o) and the bulk transconductance (g_{mb}) of MOSFETs are omitted for simplicity. Provided that $g_{m2} = g_{m3}$, the transimpedance gain of both outputs would be the same as R_{F1}.

The equivalent noise current spectral density is given by

$$\begin{aligned} i_{eq}^{2} &\cong i_{RF1}^{2'} + \frac{1}{g_{m1}^{2}}\left[\begin{array}{l} i_{d1}^{2} + i_{R1}^{2} + i_{RF2}^{2'} \\ \quad + \left(i_{d2}^{2} + i_{R2}^{2}\right) \\ \hline g_{m2}^{2}R_{F2}^{2} \end{array}\right]\omega^{2}(C_{PD}+C_{1})^{2} \\ &\frac{4kT}{R_{F1}} + \left[\begin{array}{l} \frac{4kT\Gamma}{g_{m1}} + \frac{4kT}{g_{m1}^{2}R_{1}} + \frac{4kT}{g_{m1}^{2}R_{F2}} \\ \quad + \frac{4kT\Gamma}{g_{m1}^{2}g_{m2}R_{F2}^{2}} + \frac{4kT}{g_{m1}^{2}g_{m2}R_{F2}^{2}R_{2}} \end{array}\right]\omega^{2}(C_{PD}+C_{1})^{2} \\ &\cong \frac{4kT}{R_{F1}} + \frac{4kT\Gamma}{g_{m1}}\omega^{2}(C_{PD}+C_{1})^{2} \end{aligned} \tag{9}$$

where C_{in1} represents the parasitic capacitance of M_1, i.e., $C_{in1} = C_{gs1} + 2C_{gd1}$. Hence, it is clearly seen that the noise current spectral density of the MC input stage would be almost the same as that of an NMOS cascode input stage and certainly reduced by increasing g_{m2} ($=g_{m1}$).

2.3.2 Measured results

Test chips of the MC-TIA were fabricated in a standard 65-nm CMOS technology. **Figure 16** shows the chip microphotograph where the chip core occupies the

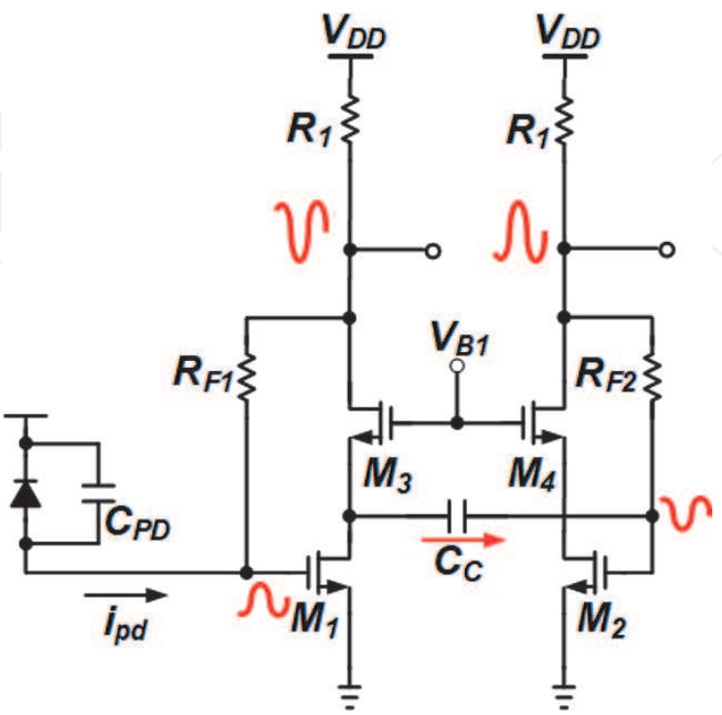

Figure 15.
Simplified schematic diagram of the VCF input stage.

area of 0.9 × 0.67 mm^2 including I/O pads. DC measurements reveal that the MC-TIA dissipates 55.2 mW (including the OB) from a single 1.2-V supply.

Figure 17 demonstrates the measured frequency response of the MC-TIA, where the differential transimpedance gain of 54 dBΩ and the −3-dB bandwidth of 40 GHz were measured with the gain flatness of ±1 dB. Also, the input impedance of the MC-TIA was measured to be in the range of 30–80 Ω within the bandwidth. The group delay variations of the MC-TIA were measured to be within ±10 ps. The single-ended integrated output noise voltage (1.42 mV_{rms}) of the MC-TIA was measured by using Agilent DCA 86100D oscilloscope in the absence of input signals [27, 29, 32].

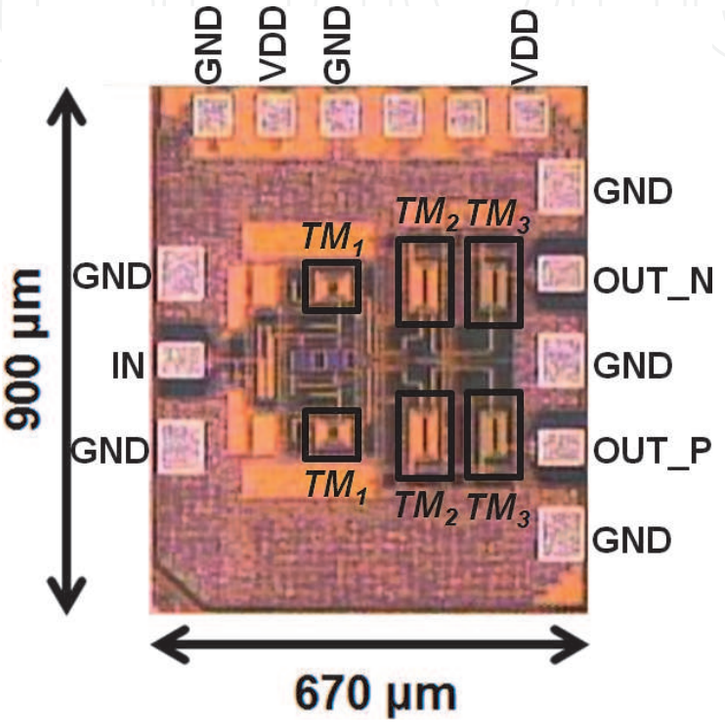

Figure 16.
Chip microphotograph of the MC-TIA.

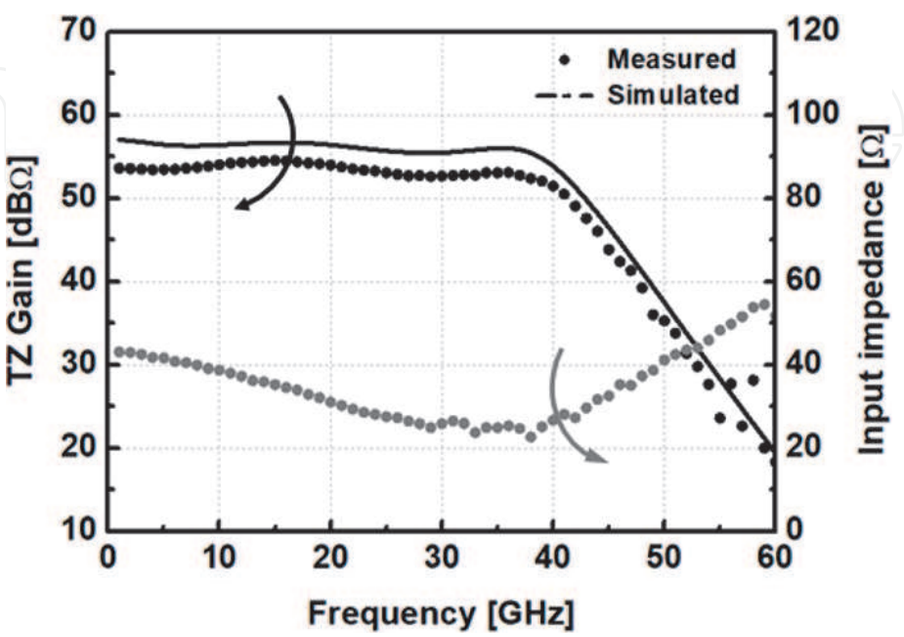

Figure 17.
Measured frequency response of the MC-TIA.

Considering the inherent oscilloscope noise of 1.01 mV_{rms}, the integrated input-referred noise current of the MC-TIA is given by

$$I_{n,in} = \frac{2\sqrt{(1.42\text{ mV})^2 - (1.01\text{ mV})^2}}{54\text{ dB}\Omega} = 3.984\ \mu A_{rms} \tag{10}$$

Then, the average input-referred noise current spectral density is given by

$$I_{n,in,avg} = \frac{I_{n,in}}{\sqrt{BW}} = 19.9\text{ pA}/\sqrt{\text{Hz}}, \tag{11}$$

which corresponds to the optical sensitivity of –13 dBm for 10^{-12} bit error rate with 0.6-A/W photodiode responsivity.

The eye diagrams of the MC-TIA were measured by utilizing RF probes and Anritsu MP1800A signal analyzer, of which operation speeds were limited to 32 Gb/s. It should be noted that the output voltage levels were measured with 50-Ω termination that caused 6-dB loss during the measurements.

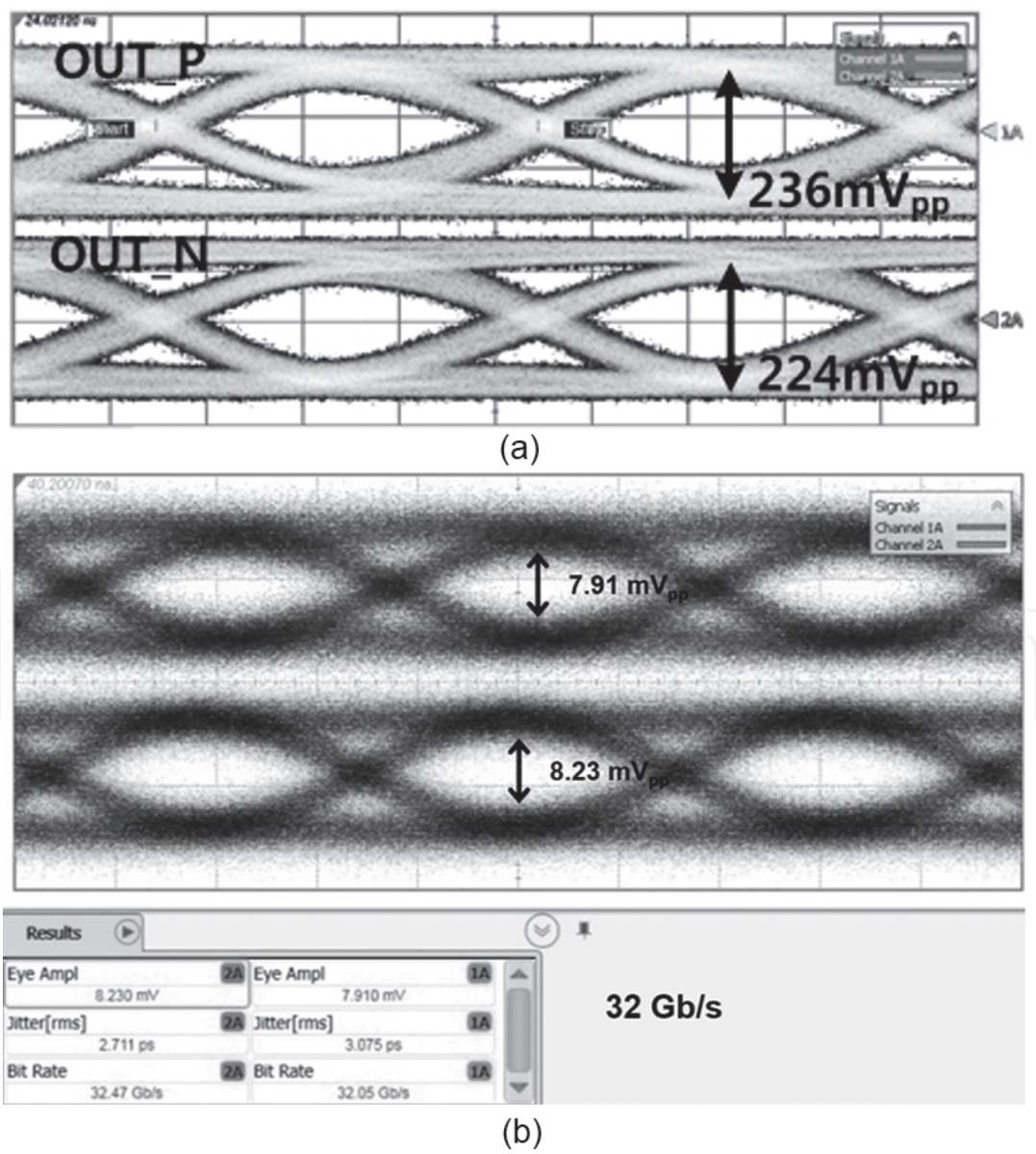

Figure 18.
Measured eye diagrams of the MC-TIA (a) with 1.5 mA_{pp} and (b) 100 μA_{pp} input currents, respectively.

Parameters	[24]	[34]	[33]	[32]	[30]	This work
CMOS [nm]	45 SOI	65	65	65	65	**65**
Architecture	INV (single)	SF (single)	RGC (single)	RGC+PA (single)	DMF (diff.)	**MC (diff.)**
V_{DD} [V]	1.0	1.6/2.2	1.2	1.0/3.3	1.2	**1.2**
BW [GHz]	30	40	21.6	21.4	50	**40**
PD cap. [fF]	60	40	200	N/A	50	**50**
TZ gain [dBΩ]	55	55	46.7	76.8	52	**54**
Noise current spectral density [pA/$\sqrt{}$Hz]	20.47	12.5	30	17.77	22.42	**19.8**
GD variation [ps]	±3.9	±32	N/A	N/A	N/A	±**10**
Power dissip. [mW]	9	122	39.9	137.5	49.2	**55.2**
Chip size [mm^2]	0.29	0.54	0.56	0.32	0.96	**0.6**

**INV, inverter; SF, source follower; RGC, regulated cascode; PA, post amplifier; DMF, dual-mode feedforward; single, single-ended; diff., differential; PD cap., photodiode capacitance.*
Bold: **Table 3** *summarizes the performance of the MC-TIA with the previously reported CMOS TIAs, showing a low-noise low-power fully differential solution for 100-GbE applications.*

Table 3.
Performance comparison with previously reported CMOS TIAs.

Figure 18(a) demonstrates the measured eye diagrams with 1.5 mA_{pp} 2^{15}-1 PRBS inputs at different data rates of 25 Gb/s and 32 Gb/s, respectively. It is clearly seen that the output voltage levels of larger than 210 mV_{pp} were measured with 50-Ω loads with the input currents of 1.5 mA_{pp}. The differential voltage swings of the MC-TIA were measured to be 236 mV_{pp} and 224 mV_{pp} (with less than 5.1% mismatch) at 25-Gb/s operations and 211 mV_{pp} and 198 mV_{pp} (with less than 6.2% mismatch) for 32-Gb/s operations. For both cases, delay mismatch at the differential outputs were measured to be less than 2 ps. **Figure 18(b)** demonstrates the measured eye diagrams with 100 μA_{pp} 2^{15}-1 PRBS inputs, where the voltage swings of 7.91 mV_{pp} and 8.23 mV_{pp} (with less than 4% mismatch) were achieved for differential outputs at 32-Gb/s operations. Even in this case, delay mismatch at the differential outputs was measured to be less than 2 ps.

Table 3 summarizes the performance of the MC-TIA with the previously reported CMOS TIAs.

3. Conclusions

We have demonstrated a number of CMOS integrated circuits for various optical applications, which included 4-channel 10-Gb/s/ch Tx and Rx array chipsets for HDMI active optical cables, 16-channel TIA array chip for 0.5–25 m range detection LiDAR, and 40-GHz TIA chip for 100 GbE. Even with advanced nano-CMOS technologies, we have proposed and exploited several novel circuit techniques for their optimum performance, such as input data detection for low power, feedforward and asymmetric preemphasis for high speed, double-gain feedforward for high gain, selectable equalizer for specific bandwidth, mirrored-cascode for fully differential topology, etc. We believe that the continuous introduction of novel circuit techniques is very crucial and necessary to develop low-cost CMOS ICs for various optical applications.

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