Chapter

High Capacitance Dielectrics for Low Voltage Operated OFETs

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Abstract

Low-voltage, organic field-effect transistors (OFETs) have a high potential to be key components of low-cost, flexible, and large-area electronics. However, to be able to employ OFETs in the next generation of the electronic devices, the reduction of their operational voltage is urgently needed. Ideally, to be power efficient, OFETs are operated with gate voltages as low as possible. To fulfill this requirement, low values of transistor threshold voltage (V_t) and subthreshold swing (SS) are essential. Ideally, V_t should be around 0 V and SS close to 60 mV/dec, which is the theoretical limit of subthreshold swing at 300 K. This is a very challenging task as it requires the gate dielectric thickness to be reduced below 10 nm. Here, the most promising strategies toward high capacitance dielectrics for low voltage operated OFETs are covered and discussed.

Keywords: thin-film transistor (TFT), organic field-effect transistor (OFET), low voltage transistor operation, high gate capacitance, ultra-thin dielectric, high-k dielectric, high-k/low-k hybrid dielectric, self-assembled monolayer (SAM), anodization

1. Introduction

In this chapter, the most important approaches toward reducing the operating voltage of organic field-effect transistors (OFETs) are described. First, the operation principle of OFETs is covered. This includes the description of the most common organic FET structures and the discussion of the device physics, which has mostly been derived from the theory of the metal-oxide-semiconductor field-effect transistor (MOSFET). Next, the key parameters of organic field-effect transistors that determine the operational voltage of these devices are discussed. Then, compatible electronic materials and device fabrication methods for low voltage operated OFETs are introduced. Finally, the chapter ends by presenting the state-of-the-art low voltage organic transistors and describing the latest key developments relating to manufacturing of such devices.

This chapter is organized in the following order: first, a brief overview of thin-film transistor (TFT) history, applications, device architectures, as well as the basics of TFT operation and differences among TFTs, OFETs, and MOSFETs are presented in Section 2; then, different methods of decreasing the operating voltage of TFTs and OFETs are considered, and various electronic materials and fabrication techniques, which are used to realize low voltage transistor operation, are discussed in Section 3. Lastly, the key findings of this chapter are summarized in conclusions.

2. Thin-film transistors (TFTs)

Thin-film transistors (TFTs) were first introduced by Weimer in 1962 and are a class of field-effect transistors (FETs), which rely on the application of an electric field to the gate electrode to modulate the density of charge carriers in the channel, which is formed at the dielectric/semiconductor interface. A typical FET is made by stacking thin films of a semiconductor layer, a dielectric layer, and metal contacts. Therefore, it behaves in a similar way to the metal-oxide-semiconductor field-effect transistor (MOSFET). Even though TFTs and MOSFETs have been developed simultaneously, MOSFETs have dominated the majority of microelectronic research interests and industrial production due to their much better performance. However, the high MOSFET performance usually comes with high cost and high temperature processing, which is not compatible with the growing demand for low cost, low temperature processing of flexible, stretchable, and large-area electronics. Other dissimilarities between TFTs and MOSFETs, as shown in **Figure 1**, include structural and material differences. Usually, TFTs are made on insulating substrates [e.g. glass or flexible films such as polyethylene terephthalate (PEN) or poly(ethylene terephthalate) (PET)], while MOSFETs are fabricated on semiconducting silicon wafers that simultaneously act as substrates and device active layers. Importantly, both types of transistors operate in a fundamentally different way: MOSFETs operate in the inversion mode, and TFTs operate in the accumulation (enhancement) mode [1, 2].

The demand for low cost, large-area applications in flat panel displays (FPDs) fuelled research on finding a viable substitution for crystalline and polycrystalline silicon. In 1979, significantly cheaper amorphous hydrogenated silicon (a-Si:H) was developed, and subsequently, it was introduced to thin-film transistors as the active layer that resulted in an increased interest in TFTs [3]. Since then, the use of a-Si:H TFTs has gradually grown, and eventually, they have started to dominate the whole liquid crystal display (LCD) industry. Nowadays, a-Si:H TFTs are the backbone of both active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode (AMOLED) display technologies.

In 1987, Koezuka et al. reported a special type of TFTs that used organic semiconductors as the active layer, so-called organic field-effect transistors (OFETs). The demonstrated devices used electrochemically polymerized polythiophene, which belongs to the family of conducting (i.e. conjugated) polymers (CPs) as the active layer [4]. Accordingly, it has been shown that the thin-film transistor design is the structure of choice for low conductivity materials such as organic semiconductors. As a result, the TFT design was utilized to realize a wide range of field-effect transistors using organic semiconductors (OSCs) [5]. Since then, the performance of organic semiconductors has continuously improved, and

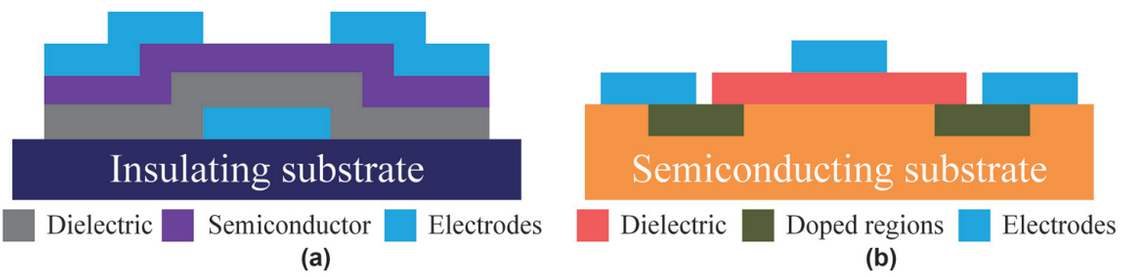

Figure 1.
Typical structures of (a) a bottom-gate top-contact TFT and (b) a MOSFET. Doped regions refer to the MOSFET source and drain regions.

nowadays, OFETs can compete with or even surpass a-Si:H TFTs in a broad range of electronic applications [6].

Although Si is the most common material used in electronics due to its advantages such as abundancy, low cost manufacturing, ease of doping, and high charge carrier mobility, novel applications in electronics such as flexible, stretchable, and large-area circuits and displays have directed the attention of scientists to alternative materials. Frequently, electronic devices such as discrete sensors, simple displays, as well as basic RFID tags and smart cards are realized in various shapes and sizes, and thus, unconventional electronic materials and device processing techniques have had to be researched to appropriately respond to these upward demands. From the most recent trends in material research, it appears that organic and metal oxide semiconductors are the two most promising alternatives to silicon for low cost electronic applications.

In addition, it is believed that many next generation electronic devices will be portable and thus will require considerably reduced power consumption. As a result, the rapid development of low voltage TFTs and OFETs is highly desirable. However, before such low power devices can be realized, a significant reduction in transistor operational voltage is required. Unfortunately, it is still extremely challenging for both organic and metal oxide semiconductor transistors to achieve high performance and low operating voltages at the same time [7–9]. In this chapter, the most promising approaches toward high capacitance dielectrics for high performance, low voltage TFTs, and OFETs are discussed and evaluated.

2.1 OFET architectures

Organic field-effect transistors can be fabricated on a variety of rigid and flexible substrates, namely, silicon/silicon oxide wafers, glass, PEN, PET, and other types of flexible films. Depending on the position of the gate electrode and where each layer is deposited, OFETs are categorized into four different structures, namely, coplanar bottom-gate, staggered bottom-gate, coplanar top-gate, and staggered top-gate, as shown in **Figure 2**. Staggered (also called bottom-contact) or coplanar (also called top-contact) configurations refer to whether the drain/source and gate electrodes are on the opposite or on the same side regarding the semiconductor layer. Although all of the abovementioned structures are used in the fabrication of OFETs, each of them shows a better performance in a particular application, and/or due to the fabrication limitations, one is more desirable than the other [3, 10]. For example, the coplanar top-gate structure is routinely used in flat

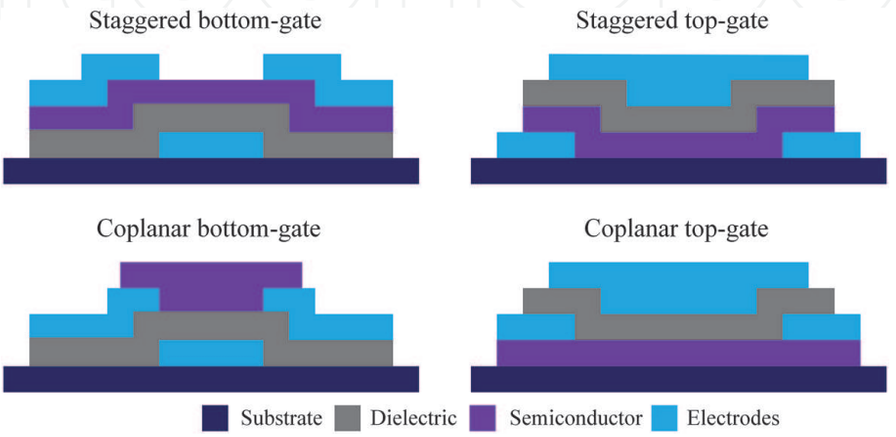

Figure 2.
The most common structures of OFETs.

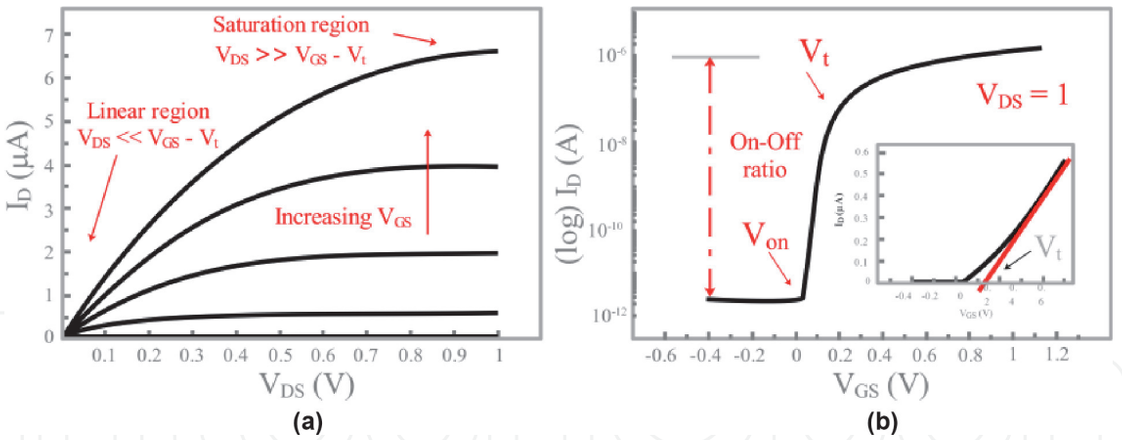

Figure 3.
Typical output (a) and transfer (b) characteristics of a low voltage OFET operating at 1 V.

panel displays. In this structure, the drain/source electrodes are self-aligned with the channel region, which result in the minimization of the parasitic capacitance that reduces image flicker and sticking [10]. Also, top-gate structures usually have higher mobility than their bottom-gate counterparts [11]. The coplanar bottom-gate structure is usually used in electronic nose applications (i.e. e-sensing) due to a larger sensing area [12]. As the device structure directly affects the device performance in terms of contact resistance, parasitic capacitance, charge carrier mobility, sensing capability, and so on, it is crucial to meticulously determine the device architecture regarding the intended use of the device.

2.2 Fundamentals of OFET operation

In an n-channel OFET operating in the accumulation (enhancement) mode, when a positive voltage bias is applied to the gate terminal, electrons start to accumulate at the dielectric/semiconductor interface, which forms a current path (channel) between the source and the drain contacts. Once the source-drain voltage bias is applied, the current starts to flow from the source to the drain electrode. As illustrated in **Figure 3**, depending on the condition of the channel, there are three different operation modes of OFETs, namely, cut-off region, as well as linear and saturation regimes. If the applied gate voltage (V_{GS}) is below a certain value, i.e., smaller than the threshold voltage (V_t), then it is not possible to accumulate enough charges (i.e. electrons) to open the channel. Therefore, no current can flow in the channel, which is called a cut-off region. On the other hand, if $V_{GS} > V_t$, one can have two scenarios: first, when the drain-source voltage (V_{DS}) is equal or larger than V_{GS}-V_t, the amount of the source-drain current (I_{DS}) flowing in the channel is constant and the OFET works in the saturation regime; second, if V_{DS} is lower than V_{GS}-V_t, I_{DS} follows the Ohm's law and the resistance of the channel (R_C) is proportional to V_{DS} and inversely proportional to I_{DS}. This region is called the linear regime, and I_{DS} is described by:

$$I_{DS} = C_G \mu_{lin} \frac{W}{L} [(V_{GS} - V_t) V_{DS}], \tag{1}$$

where C_G is the gate capacitance per unit area, μ_{lin} is the charge carrier mobility in the linear regime, W is the channel width, and L is the channel length of the device.

In the saturation regime, V_{DS} is equal or larger than V_{GS}-V_t, and I_{DS} is independent of V_{DS}. Therefore, the equation is simplified to:

$$I_{DS} = \frac{W}{2L} C_G \mu_{sat} (V_{GS} - V_t)^2, \tag{2}$$

where μ_{sat} is the charge carrier mobility in the saturation regime.

Typical output and transfer characteristics of an OFET operating at 1 V are illustrated in **Figure 3a**, **b**, respectively. In general, the most essential OFET parameters are as follows (cf. **Figure 3a**, **b**):

- Turn-on voltage (V_{ON}) is the value of V_{GS} at which I_{DS} starts to increase.
- Threshold voltage (V_t) is the minimum V_{GS} at which the number of the accumulated charge carriers at the dielectric/semiconductor interface is sufficient to create a conduction path (channel) between the source and the drain electrodes. The lower V_t, the lower the operational voltage of an OFET.
- Subthreshold swing (SS) is the parameter, which describes the necessary V_{GS} to increase I_{DS} by one order of magnitude (decade) in the subthreshold region, i.e., $V_{ON} < V_{GS} < V_t$. As small value of SS as possible is highly desirable because it leads to lower device power consumption and higher device switching speed. It is usually determined by the following expression:

$$SS = \ln 10 \frac{k_b T}{q} \left(1 + \frac{C_{ch}}{C_i}\right), \tag{3}$$

where k_b is the Boltzmann constant, T is the temperature in Kelvin, q is the electron charge, C_i is the gate dielectric capacitance, and C_{ch} is the effective channel capacitance.

- On-off current ratio defines a ratio of the measured maximum to minimum source-drain current. High "on" and low "off" currents in an OFET are highly desirable.
- The field-effect mobility of charge carriers in the linear (μ_{lin}) and saturation regimes (μ_{sat}) is usually determined by calculating the transconductance (i.e., $g_m = \frac{dI_{DS}}{dV_{GS}}$) in both regions, respectively. In the linear regime,

$$\mu_{lin} = \frac{g_m}{C_i \frac{W}{L} V_{DS}}, \tag{4}$$

and in the saturation regime,

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)}{\frac{1}{2} C_i \frac{W}{L}} \tag{5}$$

- The total interfacial trap density N_{it} of an OFET can be calculated by Eq. (6) [9]:

$$N_{it} = \left(\frac{SS \log(e)}{kT/q} - 1\right) \frac{C_i}{q^2} \tag{6}$$

where C_i is the gate capacitance density, q is the electron charge, k is the Boltzmann constant, T is the temperature in Kelvin, and SS is the subthreshold swing.

3. Low voltage OFETs

As mentioned in the previous section, I_{DS} is described in the linear and saturation regimes by Eqs. (2) and (3), respectively. In the ideal case, the source-drain current should be maximum, while the gate bias voltage is as low as possible. However, this only can be achieved when both the threshold voltage (V_t) and the subthreshold swing (SS) are sufficiently low enabling an OFET to be operated at a low voltage and maximum performance [13]. Referring back to Eq. (2), the only parameters that can be changed to compensate the reduction in I_{DS} are the gate dielectric capacitance (C_G) and the channel width (W) and length (L). However, W and L depend on the device geometry. Therefore, in order to accumulate the same number of charges within the channel of an OFET and maintain high I_{DS}, it is essential to increase the gate dielectric capacitance (C_G). One may argue that increasing the gate capacitance may deteriorate the transistor's switching speed. Indeed, the maximum switching speed of an OFET is usually defined by its cut-off frequency f_c as shown in Eq. (7) [14]:

$$f_c = \frac{g_m}{2\pi C_G} = \frac{\mu(V_G - V_t)}{2\pi L^2}, \tag{7}$$

where μ_{sat} is the charge carrier mobility in the saturation regime, L is the channel length, V_G is the gate voltage, V_t is the threshold voltage, and f_c is quantified by the g_m/C_G ratio.

As can be seen, increasing the gate capacitance directly decreases the cut-off frequency. However, low operation voltage OFETs are designed for completely different purposes and are typically not used in high switching speed applications because they are not meant to be a substitution for silicon-based transistors. For example, in OFET-based sensors, which generally sense analog quantities such as analyte concentration or pressure, the high operating frequency is not needed as analog quantities do not change rapidly [15]. Therefore, delivering the highest possible source-drain current at the lowest possible gate voltage is more critical than the high operation frequency. However, like in the design of any other electronic systems, some applications require high switching speed. It has been shown that thinning of the channel layer thickness [16] and engineering of the semiconductor/dielectric interface in transistors may result in reduced trap density (N_{it}) within the channel [17], and in consequence, OFETs with improved f_c. However, depending on the intended applications a trade-off situation should always be considered. To better understand the operation physics of organic FETs, the next part of this chapter discusses the background of dielectrics and the theory of parallel plate capacitors, as well as the influence of the gate insulator properties on the performance of OFETs.

3.1 Dielectrics: background

By definition, an insulator is a material, which has an extremely high resistivity to electric current. In other words, a lack of charge transport in insulator materials leads to insulating behavior. In general, insulators can be polar or nonpolar. The main difference between polar and nonpolar dielectrics is that the atoms or molecules of polar dielectrics have an asymmetric shape, whereas the atoms or molecules of nonpolar dielectrics have a symmetric shape. Polar atoms or molecules have a permanent dipole moment, and thus, they behave like tiny electric dipoles. In the absence of an external electric field, the tiny dipoles are randomly arranged, and the

net electric dipole moment of polar dielectrics is zero. Applying an external electric field forces the atoms or molecules within the polar dielectric medium to change their orientation and alignment to the electric field. The alignment of dipoles can be increased by increasing the external electric field and decreasing the temperature. On the contrary, nonpolar atoms and molecules do not have permanent dipole moment. When nonpolar atoms or molecules are subjected to an external electric field, the positive and negative charges are displaced in the opposite direction. This displacement continues until the external force is balanced by the restoring force due to the internal electric field. The internal electric field created due to the polarization of the dielectric is always opposite to the direction of the external electric field. Hence, the net electric field is reduced because of the polarization of the dielectric medium. However, when the external electric field is removed, the dipole moments of each nonpolar atom and molecule of the dielectric medium become zero.

In the case of a parallel plate capacitor, which consists of two parallel plates separated by a distance d, the electric field (E) is described by $E = V/d$, where V is a bias voltage applied to the capacitor. In vacuum, the charge (Q) on the plates is linearly proportional to the applied electric field and determined by Eq. (8):

$$Q = \varepsilon_0 E = \frac{\varepsilon_0 V}{d} \tag{8}$$

The ability of the capacitor to store charges is measured by its capacitance (C) and is defined by:

$$C = \frac{Q}{V} = \frac{\varepsilon_0}{d} \tag{9}$$

where ε_0 is the vacuum permittivity (8.86×10^{-12} C^2N^{-1} m^{-2}), d is the distance between the plates, Q is the accumulated charge, and V is the potential difference between the plates. The polarization of a dielectric in a capacitor increases the capacitance by a factor equal to the relative permittivity ε_r of the material (also referred to as the dielectric constant k). Accordingly,

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{10}$$

where ε_0 is the vacuum permittivity (8.86×10^{-12} C^2N^{-1} m^{-2}), ε_r is the dielectric permittivity, A is the plate overlap area, and d is the distance between the two plates.

As shown in Eq. (10), the capacitance varies directly with ε_r (k) and inversely with d. Consequently, in order to increase the capacitance of a parallel plate capacitor, two approaches are usually considered: the increase of C can be accomplished, first, by decreasing the dielectric thickness (d) and, second, by increasing the dielectric constant (k). However, conventional dielectric materials such as silicon dioxide or silicon nitride, which have been used abundantly in diverse applications throughout electronic devices, have reached their fundamental material limits, and decreasing their thickness below 2 nm is extremely challenging because it results in significantly increased leakage currents, which strongly affects the transistor operation reliability and its performance [18]. As a result, increasing C by employing high dielectric constant (high-k) materials using existing or novel high-k materials appears to be much more viable option. However, the development of new

dielectric materials that possess high k and simultaneously show low leakage currents and high dielectric breakdown strength is not easy. Despite the obvious advantages of these materials in capacitor and OFET applications, they also possess serious drawbacks such as highly polar surfaces, which result in high charge trap densities particularly at the semiconductor/dielectric interface and polarization effects in the bulk, which lead to instability of the transistor threshold voltage and appearance of the source-drain current hysteresis [19]. In this light, many attempts to develop new high-k materials that can be inexpensively processed using novel, low cost deposition techniques have recently been carried out. Lately, a wide range of novel high dielectric constant materials ranging from high-k organic/inorganic nanocomposites, through multilayer high-k/low-k dielectric stacks to ultra-thin anodized oxides has been reported as promising alternatives to the conventional high-k insulators [20, 21]. In general, the dielectric materials used in OFETs are usually divided into four main categories, namely, inorganic [22, 23], organic [24, 25], electrolyte [26, 27], and hybrid dielectrics [28, 29].

3.2 Dielectrics in electronic devices

Dielectrics in electronic devices are usually utilized as insulators between conduction layers. A very important physical property of each dielectric is its energy gap (E_g). A large E_g is favorable because it requires electrons to acquire tremendous energy for excitation and transfer from the valence band to the conduction band. Usually, high-k dielectric materials have smaller E_g than SiO_2. In regard to the gate leakage current, small energy gaps may display a higher probability of direct tunneling across the dielectric by Schottky emission and/or Poole-Frenkel effect [30]. The relation between the energy gap and the dielectric constant of the most common inorganic high-k materials is illustrated in **Figure 4**. **Table 1** summarizes their most important electrical and structural properties. The major applications of high-k dielectrics are in capacitors [31], transistors [32], and memory devices such as dynamic random-access memory (DRAM) [33] and resistive memories (memristors) [34].

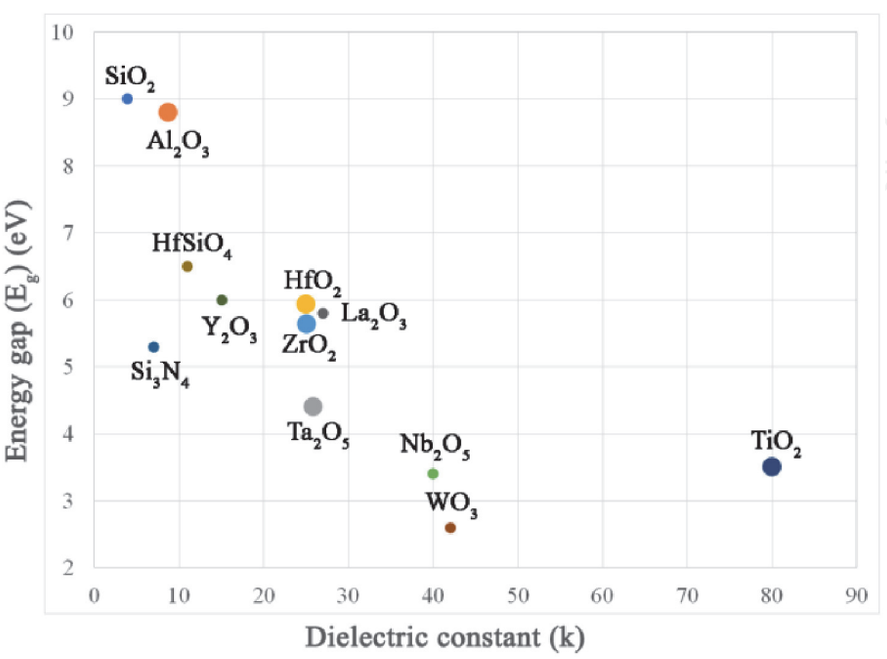

Figure 4.
Dielectric constant (k) *vs. energy gap* (E_g) *for the most common inorganic dielectric materials [35].*

Material	Dielectric constant (k)	Energy gap (eV)	Crystal structure
SiO_2	3.9	9	Amorphous
Al_2O_3	9	8.8	Amorphous
Ta_2O_5	26	4.4	Amorphous
HfO_2	25	5.8	Monoclinic, tetragonal, cubic
ZrO_2	25	5.8	Monoclinic, tetragonal, cubic
Nb_2O_5	40	3.4	Amorphous
TiO_2	80	3.5	Tetragonal (rutile, anatase, brookite)
WO_3	42	2.6	Monoclinic, tetragonal, rhombic
La_2O_3	27	5.8	Hexagonal
$HfSiO_4$	11	6.5	Tetragonal
Si_3N_4	5–7.5	5.3	Hexagonal, tetragonal
Y_2O_3	15	6	Cubic

Table 1.
The most important electrical, physical, and structural properties of some high-k inorganic materials [35].

3.3 Dielectrics in low voltage OFETs

3.3.1 Organic dielectrics

Organic dielectrics applied in OFETs are typically thicker than 200 nm because they are routinely deposited from solution by spin-coating, drop casting, or ink-jet printing, which result in low dielectric capacitance and subsequently in high operating voltage OFETs ($V_{GS} > \pm 20$ V) [36, 37]. Therefore, different methods have been used to overcome this problem including decreasing the gate dielectric thickness by depositing ultra-thin insulator films ($d < 10$ nm) [38, 39], utilizing high-k organic insulator materials [40], or doing both at the same time [41]. In case of using high-k materials [36], several groups have successfully employed high dielectric constant organic insulators and significantly lowered the operation voltage of OFETs. **Table 2** shows few examples of recently reported low voltage OFETs using organic dielectrics.

Among them, Li et al. used a high-k relaxor ferroelectric polymer as the gate dielectric ($k \approx 60$) and reduced the transistor operating voltage to 3 V [42]. Although V_G was reduced to 3 V, it has been found that highly polar dielectric materials possess high surface energy, which leads to increased trapping and, as a consequence, significantly lower field-effect mobility. Also, it turned out that the fluorinated surfaces of such materials are often incompatible with solution-processed

Ref.	Dielectric	Method	V_G (V)	C_i (nF/cm^2)	Semiconductor	μ (cm^2/Vs)	I_{ON}/I_{OFF}	Year
[39]	PVP	Spin coating	−3	250	Pentacene	0.5	$\sim 10^5$	2006
[17]	Cross-linked PVA	Spin coating	−2	12.2	TIPS-pentacene	1	$\sim 10^4$	2012
[42]	P(VDF-TrFE-CFE)	Spin coating	−3	330	pBTTTC16	0.4 ± 0.2	$\sim 10^4$	2012
[43]	PVA	Spin coating	−3	27	rr-P3HT	0.1	$\sim 10^3$	2012

Table 2.
Examples of low voltage OFETs using organic dielectrics.

organic semiconductors (OSCs) [43]. Machado and Hümmelgen have shown that using high-k cross-linked poly(vinyl alcohol) (crPVA, $k \sim 6.2$) as the gate dielectric might result in well-performing poly(3-hexyltiophene) (P3HT) OFETs [43]. However, their devices operated with $V_{GS} > 5$ V, and they suffered from relatively high leakage currents ($I_{Leak} > 20$ nA at $V_{GS} = 5$ V) [44]. Apart from using high-k insulator materials, a lot of efforts have been devoted to develop ultra-thin dielectric films ($d < 10$ nm), which can be processed from solution. Both cross-linked polymers of minimum thickness (<50 nm) [44] and self-assembled monolayers (SAMs) (e.g. octadecylphosphonic acid, ODPA) have been explored as the potential gate dielectric candidates for OFETs [45, 46]. However, cross-linked polymers and SAMs have usually been used in the bottom-gate OFETs, as they are difficult to be deposited on top of organic semiconductors (cf. **Figure 2**). Also, the possibility of contamination of the active layer by cross-linking agents, which may contribute to increased leakage currents and electrical instability of the transistors, limits the use of ultra-thin cross-linked polymer insulators to bottom-gate OFETs. In addition, it turns out that ultra-thin dielectrics are not fully compatible with low cost, high throughput printing techniques, and it is very challenging to process them reliably over large-area flexible substrates [47].

A promising way forward to address this problem and realize low voltage OFETs with low capacitance dielectrics is to use a material blend consisting of a small molecule organic semiconductor and an insulating polymer as the active layer. Using this approach, Feng et al. reported low voltage ($V_{GS} < 2$ V), solution-processed organic FETs with gate capacitance as small as 12.2 nF/cm^2 (cf. **Table 2**). This was achieved by employing a bottom-gate bottom-contact OFET architecture and using 6,13-bis(triisopropylsilylethynyl)-pentacene blended with polystyrene and UV cross-linked polyvinyl alcohol (PVA) as the active and the gate dielectric layers, respectively. It has been claimed that the low subthreshold swing value ($SS \sim 100$ mV/dec) was achieved due to a significant decrease in the effective channel capacitance described by Eq. (3) and very smooth PVA surface with a root-mean-square (RMS) roughness 0.3 nm, which contributed to the exceptionally low interface trap density.

In summary, to realize low voltage operated OFETs, low values of threshold voltage and subthreshold swing are required. Alternatively, one can achieve low voltage operated OFETs reducing the number of traps optimizing the dielectric/semiconductor interface. However, both approaches are not trivial, and more materials and device research are needed to find the optimal solutions for the intended applications.

3.3.2 Inorganic dielectrics

Today silicon is the most used material in the electronic industry. Si can be reacted with oxygen to form excellent dielectrics [1]. However, SiO_2 has relatively low dielectric constant ($k = 3.9$), and therefore, it is rather problematic to realize low voltage ($1 \leq V_G \leq 3$) and ultra-low voltage ($V_G \leq 1$) OFETs. Decreasing the thickness of SiO_2 to achieve the required capacitances is extremely difficult because of the charge tunneling effect that significantly increases the gate leakage current when SiO_2 is thinner than 2 nm. In this case, several alternative metal oxide dielectrics (e.g. Al_2O_3, HfO_2, Ta_2O_5, ZrO_2, TiO_2, Y_2O_3, CeO_2, etc.) have been investigated to be used as a gate insulator in OFETs [48]. Herein, we focus on the two most promising metal oxide dielectrics for OFETs, namely, Al_2O_3 and Ta_2O_5.

3.3.2.1 Aluminum oxide (Al_2O_3)

Aluminum oxide is an inert, water insoluble metal oxide, which due to large energy gap ($E_g \sim 8.8$ eV), high dielectric constant ($k \sim 9$), and the low cost is

abundantly used in the electronic industry as an insulator [13]. The competent insulating behavior makes Al_2O_3 particularly suitable for low voltage OFETs. Thanks to its amorphous crystal structure, it can be deposited using a wide range of deposition techniques including r.f. magnetron sputtering, plasma-assisted oxidation, sol-gel, anodization, and so on. Also, the availability of aluminum in the form of plastic aluminized foils makes it a potential material of choice for the next generation of smart electronic goods. Al_2O_3 can be very thin ($d \leq 3$ nm) and still maintain excellent insulating properties. As such, it has received a lot of attention from different research groups working on low voltage inorganic TFTs and OFETs in recent years. For example, in 2011, Avis et al. proposed a 70-nm thick sol-gel AlO_x as the gate dielectric for 5 V zinc-tin-oxide (ZTO) thin-film transistors [49]. In the same year, Lan et al. proposed a 140 nm anodic Al_xO_y for using in indium oxide (In_2O_3) and indium-gallium-zinc-oxide (IGZO) TFTs [50]. Although the reported transistors operated at 6 V, their application may be somewhat limited due to the high temperature processing ($T \sim 300$°C). Even though the abovementioned TFTs are incompatible with most of flexible plastic substrates, they can still be used in printed electronics but on high temperature plastic films or rigid substrates (e.g. glass). In parallel research, Chen et al. proposed high performance, low voltage ZnO TFTs employing 100 nm Al_2O_3 deposited by DC magnetron sputtering as the gate dielectric [51]. The minimum operating voltage of the proposed devices was 4 V, but due to the thick Al_2O_3, the transistors could not be operated with lower V_{GS}. In 2017, Cai et al. reported 1 V IGZO TFTs that employed a 3 nm thick solution processed anodic Al_2O_3 [52]. The demonstrated devices operated at 1 V, had on/off current ratios larger than 10^5, displayed field-effect mobilities of around 5.4 $cm^2/V{\cdot}s$, and possessed subthreshold swing of 68 mV/dec, which is close to the theoretical limit of *SS* at 300 K. In 2018, Ma et al. proposed low voltage IGZO TFTs using a 5 nm Al_2O_3 dielectric that resulted in transistors operating at 0.6 V [53].

In addition, there were few attempts to use pristine aluminum oxide as the gate insulator in OFETs. For example, Shang et al. proposed low threshold voltage pentacene OFETs and circuits [54]. The demonstrated devices possessed field-effect mobility 0.16 cm^2/Vs, I_{ON}/I_{OFF} current ratio about 10^5, threshold voltage 0.3 V, and subthreshold swing 0.6 V/decade. The low voltage device was achieved by growing the oxide layer using atomic layer deposition (ALD) technique. ALD provides high quality, pinhole free oxide layers and is typically used for high performance TFTs and FETs. However, this material deposition method requires very expensive equipment, and the materials have to be synthesized in high vacuum, which may not meet the demands of low cost, room temperature, large-area manufacturing of electronics. Sun et al. reported 3 V pentacene OFETs using 50 nm thick solution deposited Al_2O_3 [55]. The demonstrated devices possessed field-effect mobility near 3 cm^2/Vs, I_{ON}/I_{OFF} current ratio about 10^6, threshold voltage −0.9 V, and subthreshold swing 107 mV/decade. However, it appears that the best performing OFETs have been obtained with SAM-modified Al_2O_3 where self-assembled monolayers are used as a buffer between the organic semiconductor and the aluminum oxide [56, 57].

3.3.2.2 Tantalum pentoxide (Ta_2O_5)

Tantalum pentoxide (Ta_2O_5) is a highly promising dielectric material because it has high transparency, high melting point (1785°C), high dielectric constant and shows good thermal and chemical stabilities. As such, it has been used in a wide range of electronic applications such as in dynamic random-access memory (DRAM), metal-insulator-metal (MIM) capacitors, memory resistors (memristors), and recently in organic and inorganic TFTs [58]. The dielectric constant of Ta_2O_5

Ref.	Dielectric	Method	d (nm)	V_G (V)	C_i (nF/cm^2)	Semi-conductor	μ (cm^2/Vs)	I_{ON}/I_{OFF}	Year
[49]	Al_2O_3	Sol–gel	70	3	80	ZTO	33	~10^8	2011
[50]	Al_2O_3	Anodization	140	4	54	IGZO	21.6	~10^8	2011
[51]	Al_2O_3	D.C. sputtering	100	4	117	ZnO	27	~10^6	2012
[52]	Al_2O_3	Anodization	3	1	1000	IGZO	5.4	~10^5	2017
[53]	Al_2O_3	ALD	5	0.6	720	IGZO	3.8	~10^6	2018
[54]	Al_2O_3	ALD	30	−3	165	Pentacene	0.16	~10^5	2011
[55]	Al_2O_3	Spin coating	50	−3	125	Pentacene	2.7	~10^6	2016
[60]	Ta_2O_5	R.f. sputtering	130	−3	163	Pentacene	0.8	66	2004
[61]	Ta_2O_5	e-beam	200	3	89	a-IGZO	61.5	~10^5	2010
[62]	Ta_2O_5	e-beam	100	−2	185	P3HT	0.02	~10^5	2002

Table 3.
Examples of low voltage TFTs and OFETs using inorganic dielectrics.

depends on its thickness and deposition technique and varies from ~35 in the bulk to ~25 in a thin film [59]. This is at least two to six times larger than the dielectric constant of Al_2O_3 (k = 9) and SiO_2 (k = 3.9), respectively. As a result, Ta_2O_5 appears to be a good candidate as the gate dielectric in OFETs. Ta_2O_5 can be grown using different methods, namely, thermal oxidation, plasma-assisted oxidation, r.f. sputtering, atomic layer deposition, and anodization [60]. However, its dielectric properties can significantly differ depending on which of the growth methods is used. Recently, Chiu et al. have used a 200 nm e-beam deposited Ta_2O_5 for amorphous indium-gallium-zinc oxide (a-IGZO) TFTs, which operated at 3 V [61]. Lately, Bartic et al. have proposed 3 V bottom-gate bottom-contact and top-gate bottom-contact P3HT OFETs employing a 100 nm film of Ta_2O_5 deposited by e-beam evaporation as the gate dielectric [62]. Although both inorganic and organic transistors have yielded high performance, e-beam evaporation is a relatively expensive deposition technique, and it is not compatible with the idea of low cost, large-area electronics. In addition, thick Ta_2O_5 films employed in the aforementioned TFTs made it impossible to operate the transistors at or below 1 V, which hinders their use in special applications such as portable, ultra-low power electronics, or aqueous sensors. **Table 3** summarizes all device parameters of the above-discussed TFTs and OFETs.

3.3.3 Organic-inorganic bilayer dielectrics

3.3.3.1 Self-assembled monolayers (SAMs)

Self-assembled monolayers (SAMs) are ordered, two-dimensional organic molecular assemblies formed spontaneously by chemical absorption of an amphiphilic surfactant on a variety of substrates. In particular, silane SAMs are long-chain hydrocarbon molecules, which form an ordered supramolecular structure on solid surfaces after absorption. As such, they have been vastly used for surface modification and capping. One highly promising way to suppress the insulator surface charge traps in OFETs is to treat the transistor dielectric surface with hydrophobic SAMs, such as hexamethyldisilane (HMDS) [63], octyltrichlorosilane (OTS),

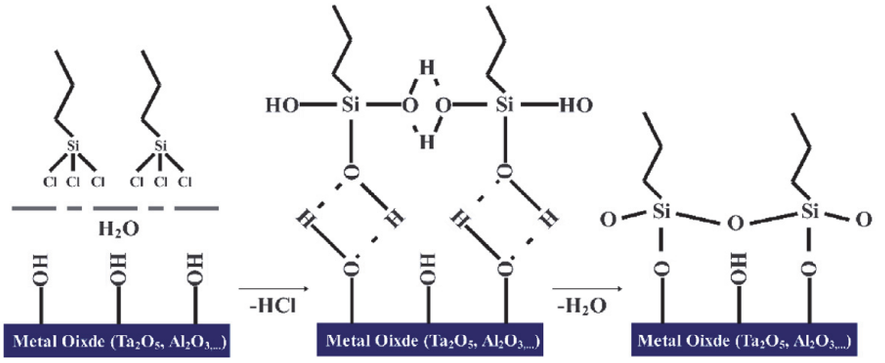

Figure 5.
Schematic representation of the silanization reaction.

or *n*-octadecyltrichlorosilane (ODTS). As reported in [64, 65], carrier mobility is significantly improved with increasing the SAM alkyl chain length, i.e., HMDS < OTS < ODTS, in comparison with the untreated surface [66]. Also, having a longer alkyl chain SAM improves adhesion and hydrophobicity of the modified surface [67].

n-octadecyltrichlorosilane (ODTS) is a self-assembled monolayer that has previously been shown to have good compatibility with SiO_2 and metal oxide dielectrics. Nowadays, it is typically used as a passivation layer for metal oxides providing capping of polar surfaces or as a hydrophobic coating layer preventing electrical instability of organic semiconductors and OFETs [3]. Essentially, ODTS appears to be one of the most used SAMs in organic FETs. It has been reported that ODTS significantly improves dielectric/semiconductor interface by passivating the metal oxide dielectric surface that leads to the reduction of charge carrier traps and, in consequence, to higher charge carrier mobility [66]. During silanization, ODTS molecules are attached to the dielectric surface through the chemical reaction of –SiCl with –OH groups on the metal oxide surface. This results in –Si–O–M structures. The other two –SiCl bonds of the ODTS molecule react with proximate OTS molecules, which form a cross-linked monolayer (**Figure 5**).

3.3.3.2 Organic-inorganic hybrid dielectrics

To achieve the best of both worlds, several research groups have been researching the organic-inorganic bilayer and multilayer dielectrics (also known as hybrid and high-k/low-k dielectric) for low voltage OFETs. Liu et al. reported polymer field-effect transistors utilizing two diketopyrrolopyrrole (DPP)-based copolymers (i.e. PDQT and PDVT-10) as the semiconductor and OTS-modified poly(vinyl alcohol) (PVA) as the gate dielectric [68]. Their devices operated at around 3 V, and it was claimed that the OTS modification of PVA enhanced carrier mobility, lowered the leakage current, resulted in less hysteresis, and generally led to better performing devices than OFETs with untreated PVA. Urasinska-Wojcik et al. fabricated 1 V organic FETs using a mixed SAM/Al_2O_3 bilayer as the gate dielectric and poly(3,6-di (2-thien-5-yl)-2,5-di (2-octyldodecyl)-pyrrolo([3,4-c]pyrrole-1,4-dione) thieno [3,2-b] thiophene) (DPPDTT) as the organic semiconducting layer [57]. As reported, the self-assembled monolayer surface modification made Al_2O_3 surface smoother, and it was concluded that the SAM passivation helped tuning the threshold voltage and improved field-effect mobility of the proposed OFETs when compared with untreated devices. Mohammadian et al. proposed 1 V OFETs gated by ODTS-treated Ta_2O_5 and DPPDTT as the organic semiconductor [69]. The proposed transistors operated with the field-effect carrier mobility around 0.2 cm^2V^{-1} s^{-1}, threshold

Ref.	Dielectric	Method	d (nm)	V_G (V)	C_i (nF/cm^2)	OSC	μ (cm^2/Vs)	I_{ON}/I_{OFF}	Year
[68]	PVA/OTS	Spin-coating	230 + OTS thickness	3	28	PDVT-10	11	$\sim 10^4$	2014
[57]	Al_2O_3/OTS	Anodization	4 + ODTS thickness	1	340	PDPP2TTT	0.1	$\sim 10^3$	2015
[69]	Ta_2O_5/ODTS	Anodization	4 + ODTS thickness	1	670	DPPDTT	0.2	5×10^3	2019

Table 4.
Parameters of the previously demonstrated low voltage OFETs using organic/inorganic bilayer dielectrics.

voltage −0.55 V, subthreshold swing 120 mV/dec, and current on/off ratio in excess of 5×10^3. The ODTS surface treatment used in the reported OFETs did not only make the surface smoother and improve the charge carrier mobility but also was used as a support of the main Ta_2O_5 dielectric. It was found that adding the extra insulator layer to the high-k dielectric increased its overall thickness and therefore decreased the gate capacitance, but because of low threshold voltage ($V_T = -0.55$ V), 1 V OFET operation was still possible. The same approach toward the gate dielectric engineering for low voltage OFETs was reported in [70, 71]. **Table 4** summarizes the key parameters of all above-discussed OFETs.

3.4 High-k metal oxide deposition techniques

3.4.1 Radio frequency (r.f.) magnetron sputtering

Radio frequency (r.f.) magnetron sputtering is a thin-film vapor deposition (PVD) technique. The process begins when a voltage is applied to a target material in the presence of argon gas. In such an instance, plasma is created in the surrounding of the target and ionized argon gas molecules start to bombard the target atoms. This bombardment leads the atoms to be sputtered off into the plasma. Then, these vaporized atoms are deposited when they condense as a thin film on the substrate. In order to properly deposit the sputtered materials, several process parameters should carefully be considered. First, the distance between the samples and the target should be optimized. Second, the chamber pressure should carefully be controlled to get the best quality of the deposited films. Last but not least the applied sputtering power should not exceed the maximum value for a given material because higher applied power could result in the target damage and poor quality of the deposited films. Usually, for Ta deposition r.f. magnetron sputtering is performed in the optimum pressure $P = 5 \times 10^{-3}$ mBar, samples are 10 cm apart from the target and power does not exceed 70 W. **Figure 6** demonstrates the schematic of the r.f. magnetron sputtering deposition process.

3.4.2 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a popular material deposition method, which is a subclass of chemical vapor deposition (CVD) technique. ALD is a high yield process delivering a highly conformal, pinhole free oxide layers at a relatively low temperature. In this process, two chemicals react with each other, and the oxide is achieved by repeating sequential, self-limiting surface reactions where precursors are separately deposited onto the substrate [59]. One ALD advantage in comparison with other vacuum deposition methods is that the oxide layer grows per cycle (GPC) allowing to have a sub-nanometer control over the deposited layer. ALD has two main drawbacks. First, the temperature of the oxidation process is relatively

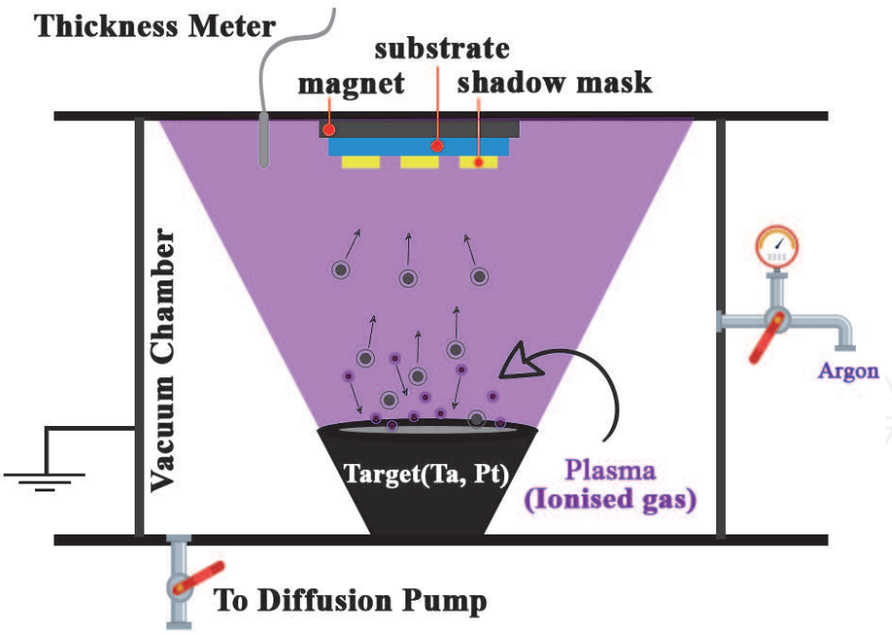

Figure 6.
Schematic of the r.f. magnetron sputtering process.

high ($T \sim 300°C$), and thus it cannot be used for majority of plastic substrates. Second, a number of research groups reported several percentages of carbon contamination in the deposited oxide layers [72].

3.4.3 Plasma-assisted oxidation

Plasma-assisted oxidation is a widespread oxidation technique, which relies on oxidation of materials using highly reactive oxygen species. In general, oxidation of metals up to 2 nm is a straightforward process, but deeper oxidations are difficult to produce because the initial layer shields further oxidation. The description of the complete plasma oxidation process is complex and consists of several parts: volume processes in chemically active plasma of oxygen or its mixtures with inert gases, transport of particles through the transient region between undisturbed plasma and metal sample immersed into plasma, processes on the surface of the sample, and the transport of both oxygen and metal ions through the growing oxide layer. Importantly, oxygen plasma is also widely used for cleaning, etching, and removing unwanted organic residues from surfaces [73]. Hsiao et al. have shown that high quality Al_2O_3 and Ta_2O_5 can be successfully grown by plasma-assisted oxidation in a controlled environment [72].

3.4.4 Solution-based techniques: spin-coating

Spin coating is a common method to produce thin, uniform polymer films on flat substrates. In the spin-coating process (**Figure 7**), the solution is first deposited on the substrate, and then it is accelerated rapidly to a desirable spin speed. This method is normally used for deposition of polymer films with thicknesses, which range from few nanometers to several micrometers. Depending on the spin speed, spin acceleration, and viscosity (concentration) of the solution, the thickness of the deposited layers can be precisely controlled [74].

3.4.5 Other solution-based techniques: anodization

The material discussed in this section is tantalum oxide (Ta_2O_5), which is generally used as an insulator in electronic devices such as capacitors, memristors,

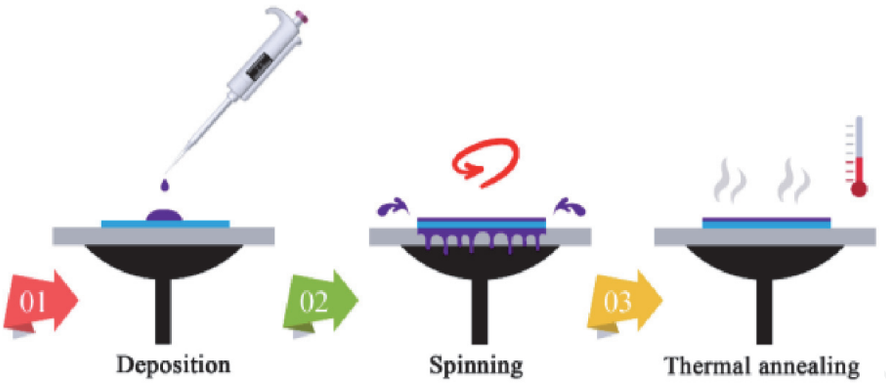

Figure 7.
Schematic of the spin-coating process.

TFTs, and OFETs. One of the most reliable and straightforward ways to form tantalum oxide is electrochemical oxidation (so-called anodization). Several metals such as Al, Ti, and Ta have very high chemical affinity with oxygen. Therefore, under ambient conditions, they will rapidly react with this gas forming a "native oxide" on their surfaces. The "air-formed" oxide film protects the metals from further oxidation (i.e. oxidation of the metal bulk) but is extremely thin—its thickness varies from a few angstroms to circa 2 nm, and it is very often not homogenous in thickness and can contain numerous defects and flaws. For example, the native oxide layer of tantalum has been reported to be usually around 3–4 nm [75]. As a result, the native oxide cannot be used as a protective film for preventing corrosion or as an insulator in capacitors and transistors.

Anodization is an electrochemical process, which allows improving this natural oxide film and produces stable oxide films with negligible reactivity. **Figure 8** shows a typical anodization bath to perform the oxidation. During the process, the metal to be oxidized is made the anode. An electrolytic cell is filled with an electrolyte. It has been shown previously that the nature of the electrolyte determines the type of anodic oxide film. The electric circuit is completed with a counter electrode which is made of a chemically inert metal (e.g. Au, Pt) or alloy (e.g. stainless steel). In **Figure 8**, an Au plate is shown as the cathode.

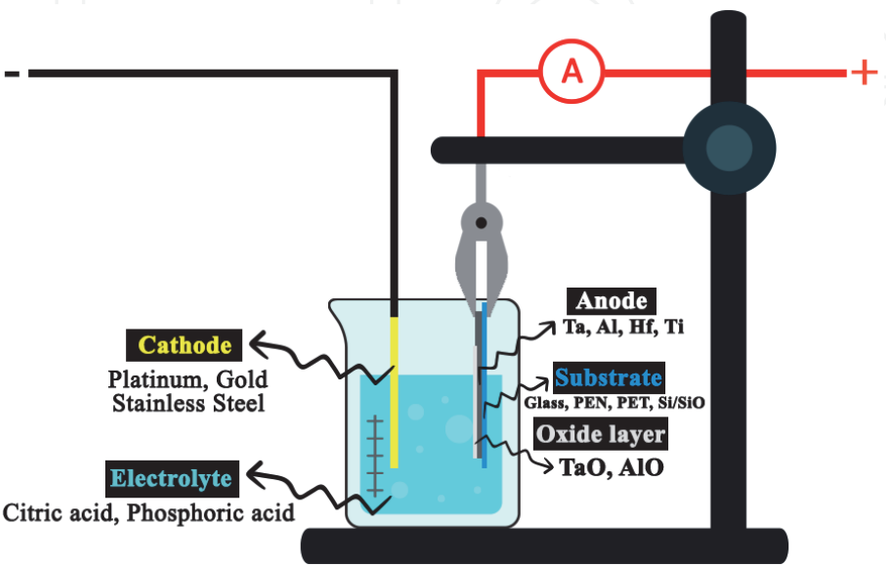

Figure 8.
Schematic of the anodization process.

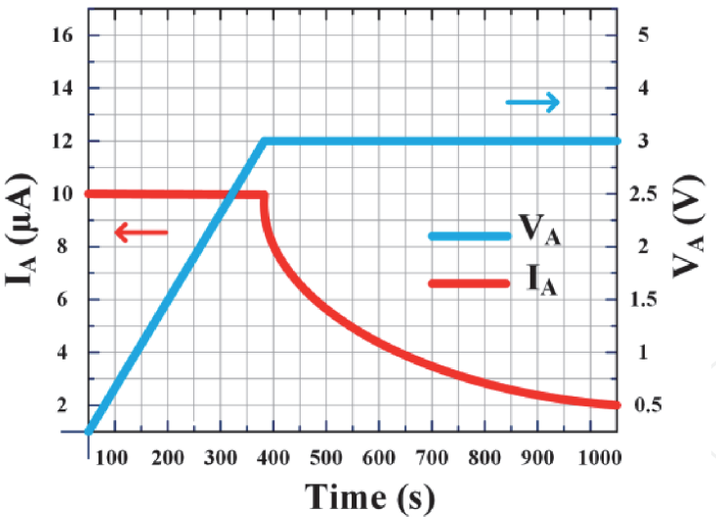

Figure 9.
Anodization voltage (V_A) and anodization current (I_A) vs. anodization time (t).

Figure 9 illustrates the electric drive conditions for anodization in constant current mode (I_A = const.). In the constant current mode, the thickness of an oxide depends only on the cell voltage, which is allowed to rise to the required value, i.e. the thickness d of the resulting films can be very precisely controlled via anodization voltage V_A because $d = c \cdot V_A$, where c is the anodization ratio describing the thickness of the formed film per applied volt (Å/V). Importantly, c is related to the electric breakdown field E_B via $E_B \approx c^{-1}$.

The anodization current I_A is kept constant via the anodization voltage V_A compensation until the desired voltage is achieved and then decreases to very low values. The "leakage current" flowing under constant voltage conditions is electronic, but if the voltage is increased, then ionic current begins to flow again with further film formation until a new equilibrium is established. However, it is not possible to increase the voltage to a very high value. The upper limit on voltage lies between 500 and 700 V due to breakdown and arcing in the barrier layer. The most interesting fact is that the thickness of the barrier type film is not affected by electrolyzing time, surface roughness, and temperature of the electrolyte. In fact, the formed oxide film will exactly follow or slightly smooth out the initial surface topography of the anodized metal.

The anodization ratio of tantalum anodized in 1 mM citric acid (CA) has been reported in the literature [74–76] and usually is between 1.8 and 2.2 nm/V. **Table 5** compares the information relating to the anodization of metals and in particular anodization of tantalum in the recent works [68, 78–80].

Ref.	Metal oxide	Anodization ratio (nm/V)	Forming electrolyte
[74]	Ta_2O_5	1.8	0.1 M H_3PO_4
[75]	Ta_2O_5	2.2	0.01 M CA
[76]	Ta_2O_5	2.0	0.01 M CA
[77]	TiO_2	1.5	0.001 M CA
[66]	Al_2O_3	1.3	0.001 M CA

CA—citric acid.

Table 5.
A summary of anodization ratios and forming electrolytes relating to the anodization of Al_2O_3, TiO_2 and Ta_2O_5.

4. Conclusions

In this chapter, the most promising strategies toward lowering the operational voltage of organic FETs have been reviewed and discussed. This includes reducing the transistor threshold voltage and subthreshold swing. Apart from the semiconductor/insulator interface engineering that is not always straightforward, one either can employ high-k dielectric materials, reduce their thickness, or do both at the same time. The best performing dielectric materials in OFETs appear to be metal oxides. They intrinsically possess high dielectric constants and display low leakage currents. Also, they can be made ultra-thin ($d \leq 3$ nm), and when deposited on plastic films, they are flexible and robust. However, depending on the intended applications, one can also use pristine organic, organic-inorganic hybrid, or high-k/low-k multilayer dielectrics. Anodic oxidation is a very promising technique, which can considerably lower manufacturing costs of high-k materials and realize inexpensive low voltage OFETs and OFET-based circuits. It is a cheap, solution-based deposition process that can be performed under ambient conditions. Since the anodization is a self-limiting and self-healing process, it can give pinhole-free, homogenous oxide layers that can be grown in ambient atmosphere at room temperature. As such, anodization has a high potential to be used in manufacturing of future OFET-based electronic devices and circuits.

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