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Design and Fabrication of Nanowire-Based Conductance Biosensor using Spacer Patterning Technique

U. Hashim, S. Fatimah Abd Rahman and M. E. A. Shohini
Nano Biochip Research Group
Institute of Nano Electronics Engineering (INEE)
Universiti Malaysia Perlis,01000 Kangar, Perlis,
Malaysia

1. Introduction

A biosensor can be generally defined as a device that consists of a biological recognition system, often called a bioreceptor, and a transducer [1]. The combination of nanotechnology and biosensor has leaded a new discovery called Nano-biosensor [2]. Advances in this field potentially created useful approaches to new detection methods and revolutionize the way in of biosensing. Nano-biosensor, although still an emerging technology, promise fast, accurate, and inexpensive ways to measure an extremely wide variety of analytes produced or consumed in biological and biochemical processes, as well as ways to measure more directly the activity of biological systems or their components [3].

One feature of DNA sensors that could make both goals attainable is the utilization of a transduction mechanism that is nano-scale and can be easily integrated with CMOS technology. The ultimate goal of researchers is to develop a suitable base requires a base that can interact individually, requiring a detector of a similar size [2]. Molecular electronic properties have usually been examined using electrodes with nanoscale wires (nanowires) as small as the molecular sizes, fabricated by electron-beam lithography (EBL), photolithography or electromigration methods [3-6]. However, these techniques are very expensive due to its low throughput. In this study we present parallel processes for nanometer pattern generation on a wafer scale with resolution comparable to the best electron beam lithography.

The focus of this work is the fabrication of nanowire based on spacer patterning lithography (SPL); a type of size reduction technique. The design and fabrication of nanowire using SPL require the proper selection and integration of material and methodology. Up to this point, we describe the design of specifying the process flow and material that is appropriate to fabricate the device using conventional CMOS process. The process flow involves every step in SPL including the deposition of a sacrificial layer, the definition of vertical step by means of lithography and etch-back process, the deposition of a conformal layer, final anisotropic etching and formation of gold pad by Physical Vapor Deposition (PVD).

Source: Biosensors, Book edited by: Pier Andrea Serra,
ISBN 978-953-7619-99-2, pp. 302, February 2010, INTECH, Croatia, downloaded from SCIYO.COM

Fig. 1. Step Requirement for fabricating Nanowire using SPL

1.1 Operation principle

The operation principle of the sensor is as follows. Any tiny size sample like DNA should be bound ligand with an absorbed receptor on the Si nanowires. When molecules are fixed between them, it can change the charge carrier density of the wires. This change of charge carrier density results in an effective change of conductance by time that can be monitored electronically. The sensor structure allows for direct conversion of molecular recognition and binding events to electronic signals. [3]

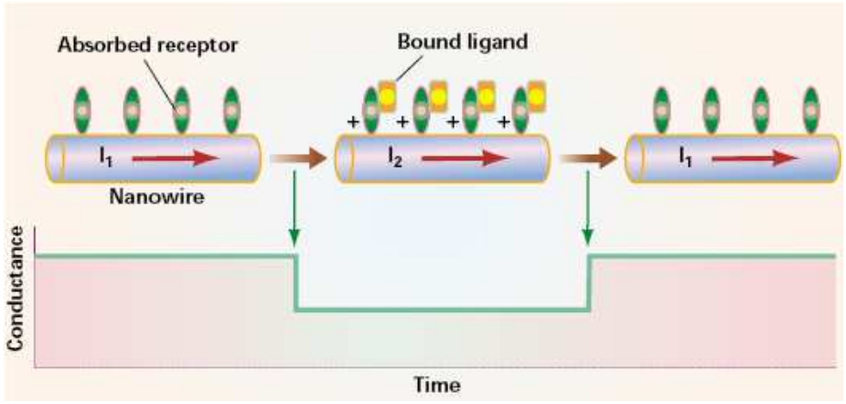

Fig. 2. Operation principle of nanowire filled with DNA [7].

2. Experimental details

In this research, the following flow is used to conduct the research starting from material used until the detection of DNA hybridization.

2.1 Starting material

The 4 inch silicon-on-insulator (SOI) wafers is used as starting material with a BOX thickness of 160 nm, a top Si layer of 160 nm thickness and boron doped 9–23 Ωcm. Reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing include:

- Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.
- Resistance to latchup due to complete isolation of the n- and p- well structures.

Silicon on insulator (SOI) wafer is used to reduce parasitic device capacitance and thus improve the final device performance. Prior to fabrication process, the first step is to check the wafer type from its specification, measure wafer thickness (Si thickness), measure the sheet resistance and check the dopant type. After doing this, lightly scribe the backside of each wafer, protect the top surface, using the sribe tool provided. Mark gently but make it

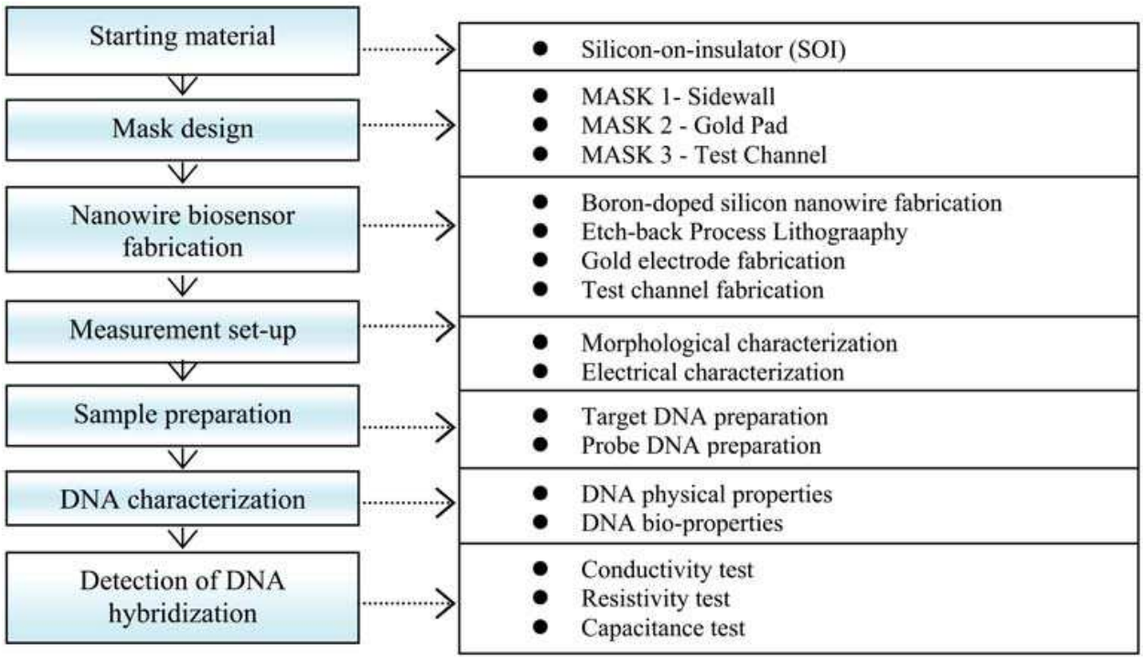

Fig. 3. Research methodology flow

visible and place scribed wafer in container. Wafer is cleaned before each process. Then, the SOI wafer is doped with boron on the silicon layer using spin on dopant technique. Concentration and sheet resistance is checked again to make sure the doping process gives effect to the structure.

2.2 Mask specification and layout design

As for the lithography process, three photomask are employed to fabricate the nanowire using conventional photolithography technique. Commercial Chrome mask is expected to be used in this research for better photomasking process. Mask 1 is used to develop the sidewall, Mask 2 is used for the gold pad and Mask 3 is for the test channel. The photomask is designed using AutoCAD and then printed onto a chrome glass surface.

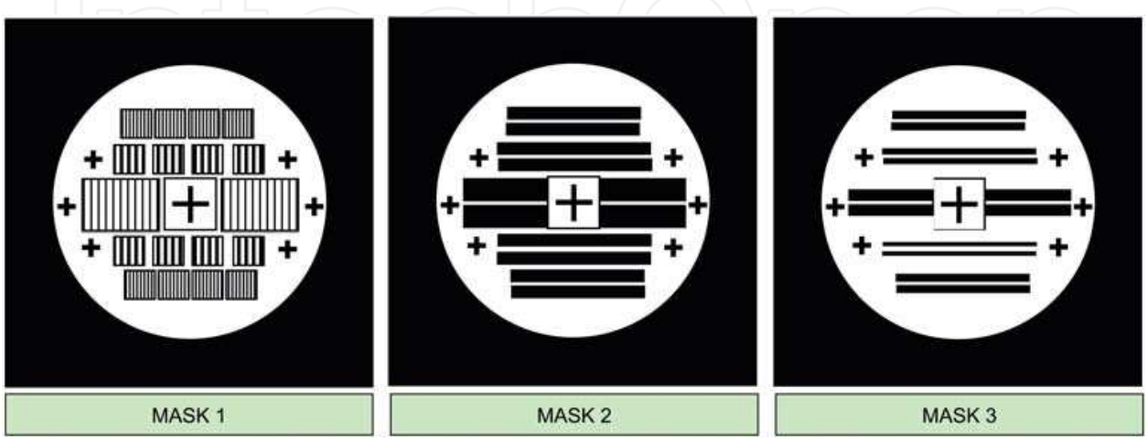

Fig. 4. Mask design for Nanowire fabrication

3. Process fabrication development

The fabrication of nanowire in this research uses the Spacer Patterning Lithography (SPL) method which is low-cost and compatible to standard CMOS fabrication process. Spacer patterning lithography coupled with anisotropic etching using ICP-RIE is the two main processes used in this experiment to fabricate this silicon nanowire. Electrical properties of silicon nanowire are then controlled by choosing a silicon substrate with an intended dopant type and concentration.

3.1 Spacer patterning lithography

The process begins with the deposition of the 200-500 nm layer layer of silicon oxide (SiO_2) as the sacrificial layer on a clean highly doped SOI wafer following by the first mask pattern on top of it. This SiO_2 and Si_3N_4 are deposited by Plasmalab 80 plus Compact Plasma System by Oxford Instruments, plasma enhance will deposit the SiO_2 layer before making the proper mask alignment on top of it. The conditions are 700 sccm N_2O, 150 sccm Ar, 1000 mT pressure, 30 Watt power and 150^oC temperature for SiO_2. After deposition, photo resist (PR) solution will be loaded onto the SiO_2 layer before making the proper mask alignment on top of the PR. By using MIDAS exposure system (by applying UV light through a mask), pattern from the first mask is transferred on the PR. Buffered Oxide Etch (BOE) can be used to remove the silicon oxide layer but in this case, vertical profile is needed, so dry etch is the choice to etch the silicon oxide layer. Prior to this, development and etching process using SAMCO ICP-RIE inductive coupled plasma – reactive ion etching at 2.5nm s^{-1}, the pattern layer is finally moved onto the SiO_2 layers. The conditions are 50 sccm CF_4, 30 sccm Ar, 250V bias, 800Watt ICP power and 5 Pa pressure. This recipe etched produced vertical sidewall profile with an angle 82^o-88^o. The residue PR is then removed using the Plasma-PreenII-862 system by Plasmatic Systems Inc. Then, a thin layer about 100nm-200nm of Silicon Nitride (Si_3N_4) is deposited on top of it. The conditions are 60 sccm Ar, 285 sccm N2, 600mT pressure, 25 Watt power and 150^oC temperature.

This thin layer of Silicon Nitride (Si_3N_4) is deposited uniformly onto the SOI to create the layer for spacer formation (the main process of the SPL technique). The spacer is then defined using ICP-RIE etching by removing the silicon oxide. The spacer formed will be the next mask for the highly doped crystalline silicon substrate. The nanowire is then defined using ICP-RIE etching by removing the silicon. This process is the critical step on fabrication process, since it determines the nanowire size and dimension as can see in Figure 5.

3.2 Gold pad contact formation

Prior characterization and electrical testing, contact point is formed by deposition of aurum (gold) material prior to the fabricated nanowire. Gold is used to have a good reliability via contact and it has a very good conductivity. This is to ensure the device has a good electron flow and no bias effect to the sensing nanowire.

A layer of 500nm thick of Aurum is deposited using E-beam Evaporator onto the surface of the fabricated nanowire. The layer is then coated and patterned using photolithography process to form the contact point. Aqua Regia is used for etching. Finally, the photoresist layer is removed to expose the gold pad for contact.

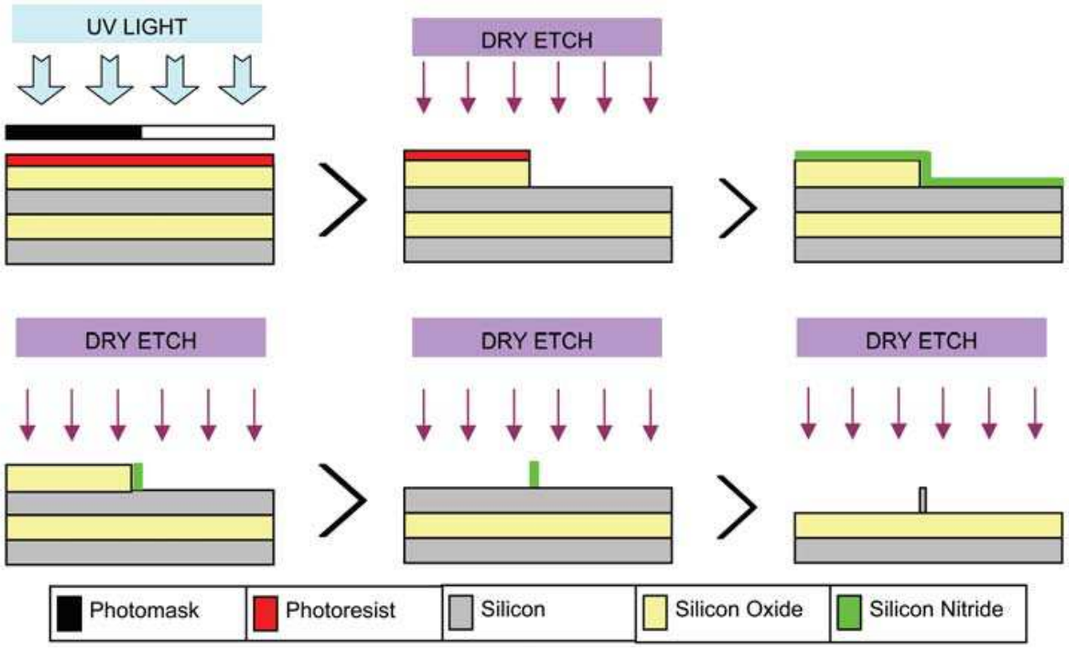

Fig. 5. Layer by layer alignment and patterning method.

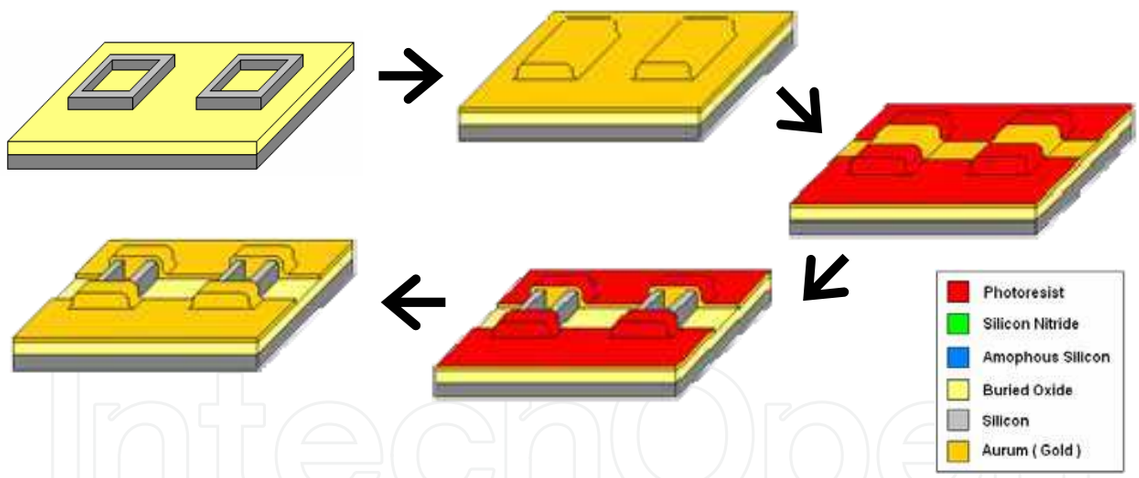

Fig. 6. Process flow of gold pad.

3.3 Test channel formation

Figure 7 shows the fabrication of the Si_3N_4 passivation layer which uses the Si_3N_4 to isolate the testing area and the electrical contact point. Starting with the deposition of the Si_3N_4 using Plasma Enhanced Chemical Vapor Deposition (PECVD), a layer of Si_3N_4 is deposited on the surface of the nanowire and the gold pad. Then, a photoresist is coated and patterned using photolithography process. Inductively Coupled Plasma Reactive-Ion-Etching (ICP-RIE) is used to etch the Si_3N_4 between the patterns and exposed the nanowire area for DNA sample drop and contact point. Finally, the photoresist layer is removed to form the Si_3N_4 passivation layer.

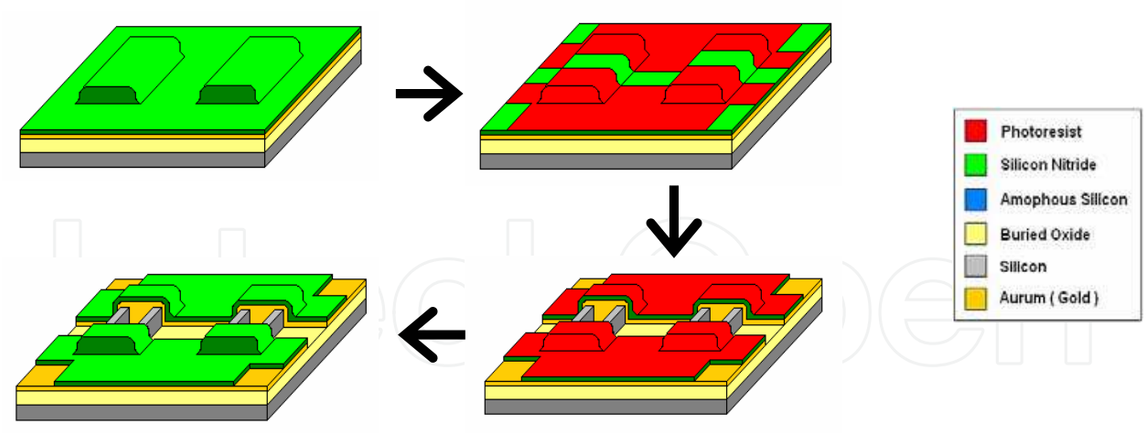

Fig. 7. Si_3N_4 passivation layer process flow

4. Detection of DNA hybridization

There are two types of sample needs to be prepared and tested in this experiment.

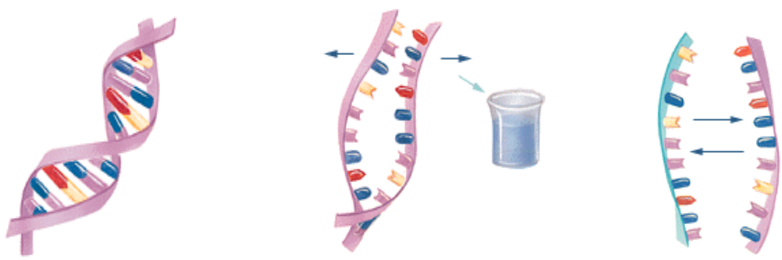

Fig. 8. DNA sample

Preparation of 2 sample known as separate ds-DNA (Probe DNA) and various unknown ss-DNA (Target DNA). The Probe DNA is a known reference sample DNA for testing the unidentified Target DNA. The mixture of these 2 DNA will hybridize or not is known earlier for testing purpose.

The process of identification starts with the Probe DNA is denatured by heat or chemical denaturant and placed in solution or on a solid substrate, forming a reference segment. Then, a various unknown ss-DNA (Target DNA) is prepared. Unknown DNA sample is introduced to the reference segment. The complement of the reference segment will hybridize to it. This concentration must be suitable to the size of nanowire area. Identification of electrical form is counter measured to test the sample and conclude the result. The semiconductor parameter analyzer (SPA) system is used to characterize the conductivity of the nanowire. Spectrum analyzer (SA) is used to manipulate the output signal and easier identification process.

A DNA molecule is positioned on the nanowires by electrostatic trapping from a dilute aqueous buffer. This technique was developed for the trapping of single molecules, and has been shown to be successful for a variety of nanoparticles.

In this procedure, the reference plane of the first-tier calibration was placed in the first pad, as described above. The reference plane of the second-tier calibration was located at the second contact pads fabricated on the silicon substrate. The signal line of this nanowire

fabricated in the second level of metal (metal 2), and its ground plane was fabricated in the first level of metal (metal 1). This allowed us to directly measure the scattering parameters of the contact pads we had fabricated on the silicon wafer.

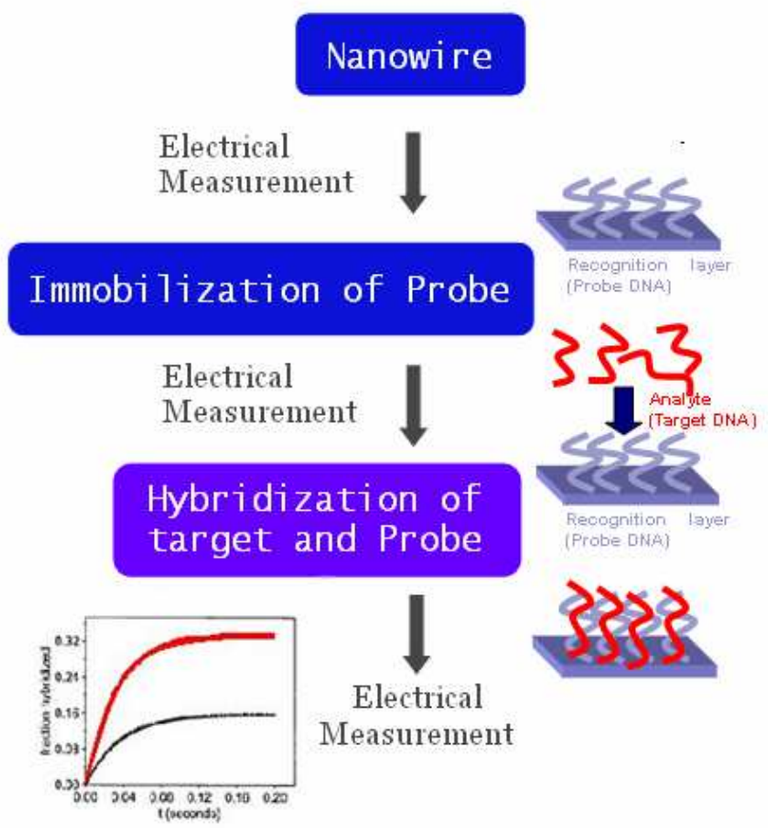

Fig. 9. Signal identification

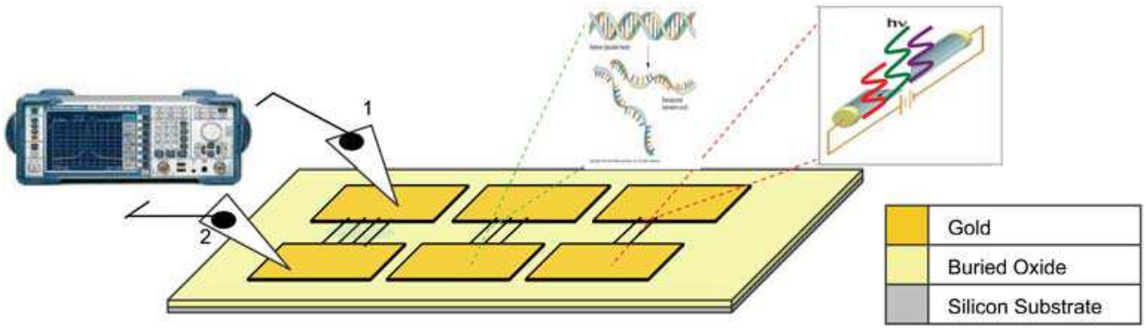

Fig. 10. Pad to pad measurement of different nanowire pattern using spectrum analyzer / semiconductor parameter analyzer

5. Results and discussions

A 1µm thick hard mask oxide is depositedon a SOI wafer and followed by 100nm thickness of Si_3N_4 conformal layer is deposited on the hard mask oxide by LPCVD. This Si_3N_4 layer

serves as a sacrificial support for the sidewall spacers patterning. The pattern transfer is carried out using MIDAS MDA400M UV with light source of 350 Watt intensity system through the photomask glass with chrome pattern to the 1 μm positive photoresist layer. After resist development, etching process is conducted by plasma reactive ion etching (RIE). The Si_3N_4 is removed by CHF_3/Ar based plasma etch, which provide high etch selectivity of Si_3N_4 to oxide layer. Based on Figure 11, after removing the oxide layer, the sidewall Si_3N_4 spacer is left and it serves as a hard mask to etch the underlying silicon layer to form as silicon nanowire. The resulting pattern sidewall profile was observed by scanning electron microscope. The pattern is not ideally vertical, showing some broadening feature from top to bottom layer but this condition is still acceptable for forming spacer using SPL technique. The SiO_2 etched produced vertical sidewall profile with an angle 82^o-88^o as can see in Figure 7. The length of nanowire totally depends on width of spacer. This certain restriction of nanowire length as long as the uniformity of anisotropic etching could cover up the whole wafer size.

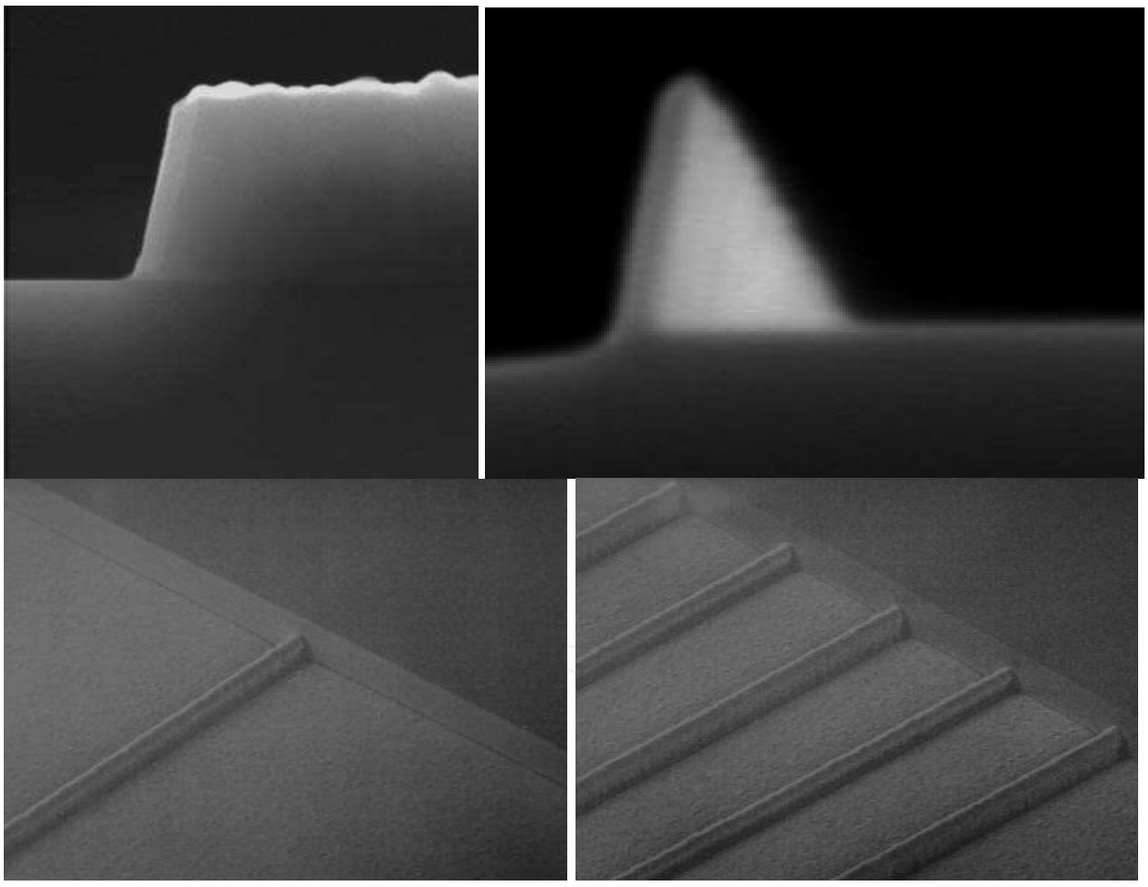

Fig. 11. Image of sidewall and spacer formation under SEM

The height of the spacer were not perfectly the same because of the Si layer is over etched during etch back process and it is not easy to confirm the height of two separating layer while etching.

Subsequently, the silicon layer is then anisotropically etched by CF_4/O_2 based plasma ion etch. This nanowire is formed on a top of 90 nm silicon layer with underlying of 150 nm

oxide layer and boron-doped of 9-23 ohm-cm. The hard mask oxide is removed by the same recipe from before. Figure 12 shows SEM photographs of the nanowire.

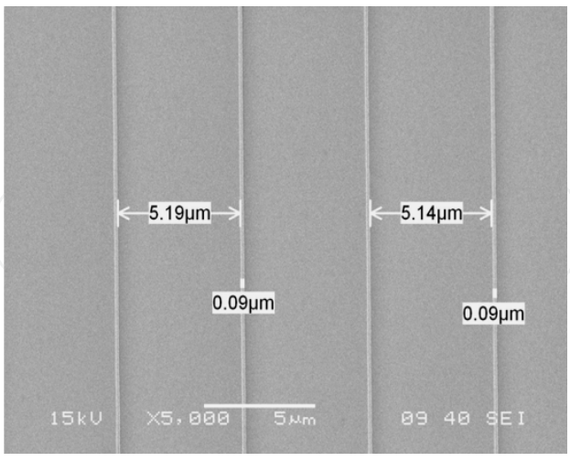

Fig. 12. The SEM image of the silicon nanowires.

Then, the two metal electrodes which are designated as source (S) and drain (D) are fabricated on top of individual nanowire using photolithography process. A 10 nm of Ti and followed by 50 nm of Au layer is evaporated on the silicon nanowire surface. Aqua regia was used to etch the Au layer and Ti layer in room temperature. Au is used as probing point because of good conductivity and low interconnection resistance.

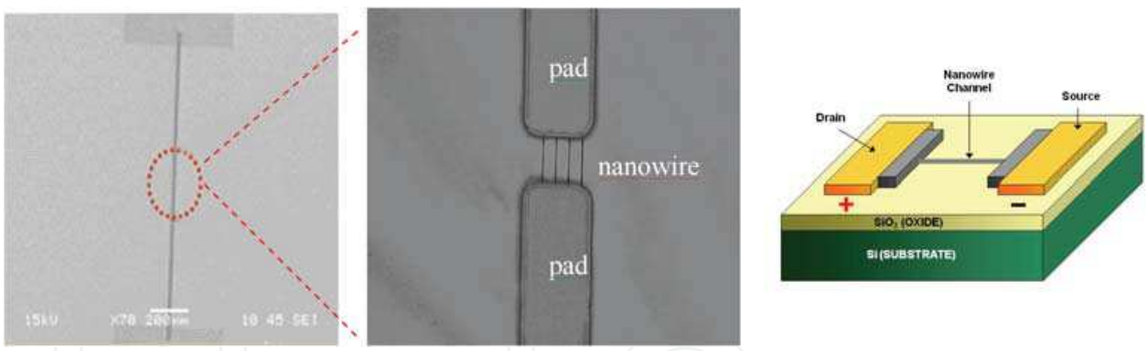

Fig. 13. HPM image observed the connected nanowire between the two electrode pads and the 3-D model of overall pattern fabricated on the sample.

Characterization and optimization of the fabricated nanowire is the crucial steps in the development of this biosensor. It's extremely important to produce the perfect nanowire at the nano-scale resolution [9].

6. Summary

The sublithographic nanowire was fabricated by the spacer lithography. We have shown an example application of these techniques. Experiments show the nanowire conductive conductor can be fabricated by spacer lithography and used for the detection of DNA hybridization without labeling. DNA hybridization was detected by conductance measurements, and the conductance was found to decrease as input frequency decreases when hybridization occurs. Due to the full compatibility with silicon microfabrication

technology, DNA chips without any requirement of labeling process are thus practical which can be capable of cost reduction and dramatically speed up evaluation of DNA hybridization.

7. Acknowledgement

The authors wish to thank Universiti Malaysia Perlis (UniMAP), Ministry of Science, Technology & Innovation (MOSTI) and Ministry of Higher Education for giving the opportunities to do this research in the Micro & Nano Fabrication Cleanroom. The appreciation also goes to all the team members in the Institute of Nanoelectronics Engineering especially in the Nano Biochip Research Group.

Biographical notes:

Uda Hashim received his PhD in Microelectronic from Universiti Kebangsaan Malaysia (UKM) in 2000. He is a Professor and Director of the Institute of Nano Electronic Engineering in Universiti Malaysia Perlis (UniMAP), Malaysia. He is the core researcher of microelectronics & nanotechnology cluster and also the team leader in the UniMAP Nano-Biochip Research Group. His current research interest includes Research Managements, Nanoelectronics, Biochips, E-Beam Lithography, Photolithography, Nano-structure formation, Semiconductor processing, CMOS process and devices. He has produced more than 100 academic papers in journals as well as conference proceedings worldwide in nanotechnology especially in nanoelectronics related field of research.

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Biosensors

Edited by Pier Andrea Serra

ISBN 978-953-7619-99-2
Hard cover, 302 pages
Publisher InTech
Published online 01, February, 2010
Published in print edition February, 2010

A biosensor is defined as a detecting device that combines a transducer with a biologically sensitive and selective component. When a specific target molecule interacts with the biological component, a signal is produced, at transducer level, proportional to the concentration of the substance. Therefore biosensors can measure compounds present in the environment, chemical processes, food and human body at low cost if compared with traditional analytical techniques. Bringing together researchers from 11 different countries, this book covers a wide range of aspects and issues related to biosensor technology, such as biosensor applications in the fields of drug discovery, diagnostics and bacteria detection, optical biosensors, biotelemetry and algorithms applied to biosensing.

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