Chapter

Industrial Silicon Solar Cells

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Abstract

The chapter will introduce industrial silicon solar cell manufacturing technologies with its current status. Commercial p-type and high efficiency n-type solar cell structures will be discussed and compared so that the reader can get a head-start in industrial solar cells. A brief over-view of various process steps from texturing to screen-printed metallization is presented. Texturing processes for mono-crystalline and multi-crystalline silicon wafers have been reviewed with the latest processes. An over-view of the thermal processes of diffusion and anti-reflective coating deposition has been presented. The well-established screen-printing process for solar cell metallization is introduced with the fast-firing step for sintering of the contacts. I-V testing of solar cells with various parameters for solar cell characterization is introduced. Latest developments in various processes and equipment manufacturing are also discussed along with the expected future trends.

Keywords: silicon, solar cells, manufacturing, multi-crystalline, mono-crystalline, texturing

1. Introduction

Photovoltaics are an important renewable energy source which has grown rapidly from 8 GW in 2007 to 400 GW in 2017 [1]. Along with the increasing demand, the PV system costing has also dropped significantly from 35.7 $/W$_p$ in 1980 to 0.34 $/W$_p$ in 2017 accelerating its adoption [2]. Silicon (Si) which is an important material of the microelectronics industry has also been the widely used bulk material of solar cells since the 1950s with a market share of >90% [2]. The chapter will introduce the typical steps for manufacturing commercial silicon solar cells. A brief history of solar cells and over-view of the type of silicon substrates along with the different solar cell architecture will be introduced in Sections 2 and 3. Subsequently, the wet-chemistry and high temperature steps used in fabrication will be described in Sections 4 and 5. Section 6 will discuss about the metallization process along with typical characterization parameters for commercial solar cells. Finally, future roadmap and expected trends will be discussed in the concluding section.

2. Evolution of solar cells

The 'photovoltaic effect' literally means generation of a voltage upon exposure to light. The phenomenon was first observed by the French physicist Edmund Becquerel on an electrochemical cell in 1839, while it was observed by British scientists W.G. Adams and R.E. Day on a solid-state device made of selenium in 1876 [3]. From the 1950s onwards, there was rapid progress in the performance of commercial

solar cells from <1% to >23% [2] and silicon has been the 'work-horse' of the photovoltaic industry since then. The evolution of silicon solar cells is shown in **Figure 1**.

The first silicon solar cells demonstrated by Russell Ohl of Bell Laboratories during 1940s were based on natural junctions formed from impurity segregation during the recrystallization process [3]. The cells had an efficiency of <1% due to lack of control over the junction location and the quality of the silicon material. The nomenclature for naming the regions (p-type: side which is illumination and n-type: other side) given by Ohl are since then being used for the solar cell naming conventions.

During the 1950s, there was rapid development in the high-temperature diffusion process for dopants in silicon. Person, Fuller and Chaplin of Bell Laboratories demonstrated a 4.5% efficient solar cell with lithium-based doping, which improved to 6% with boron diffusion. The solar cell had a 'wrap-up' around structure (**Figure 1(b)**) with both contacts on back side to avoid shading losses, but led to higher resistive losses due to the wrap-around structure. By 1960, the cell structure evolved to as shown in **Figure 1(c)**. Since the application was for space explorations, high resistivity substrate of 10 Ω cm was used to have maximum radiation resistance. Vacuum evaporated contacts were used on both sides, while a silicon monoxide coating was used as an anti-reflective coating (ARC) on the front-side (FS) [3].

In early 1970s it was found that having sintered aluminum on the rear-side improved the cell performance by forming a heavily doped interface known as the 'back-surface field (Al-BSF)' and gettering of the impurities [3]. The Al-BSF reduces recombination of the carriers on the rear-side and hence improves the voltage and the long-wavelength spectral response. Implementation of finer and closely

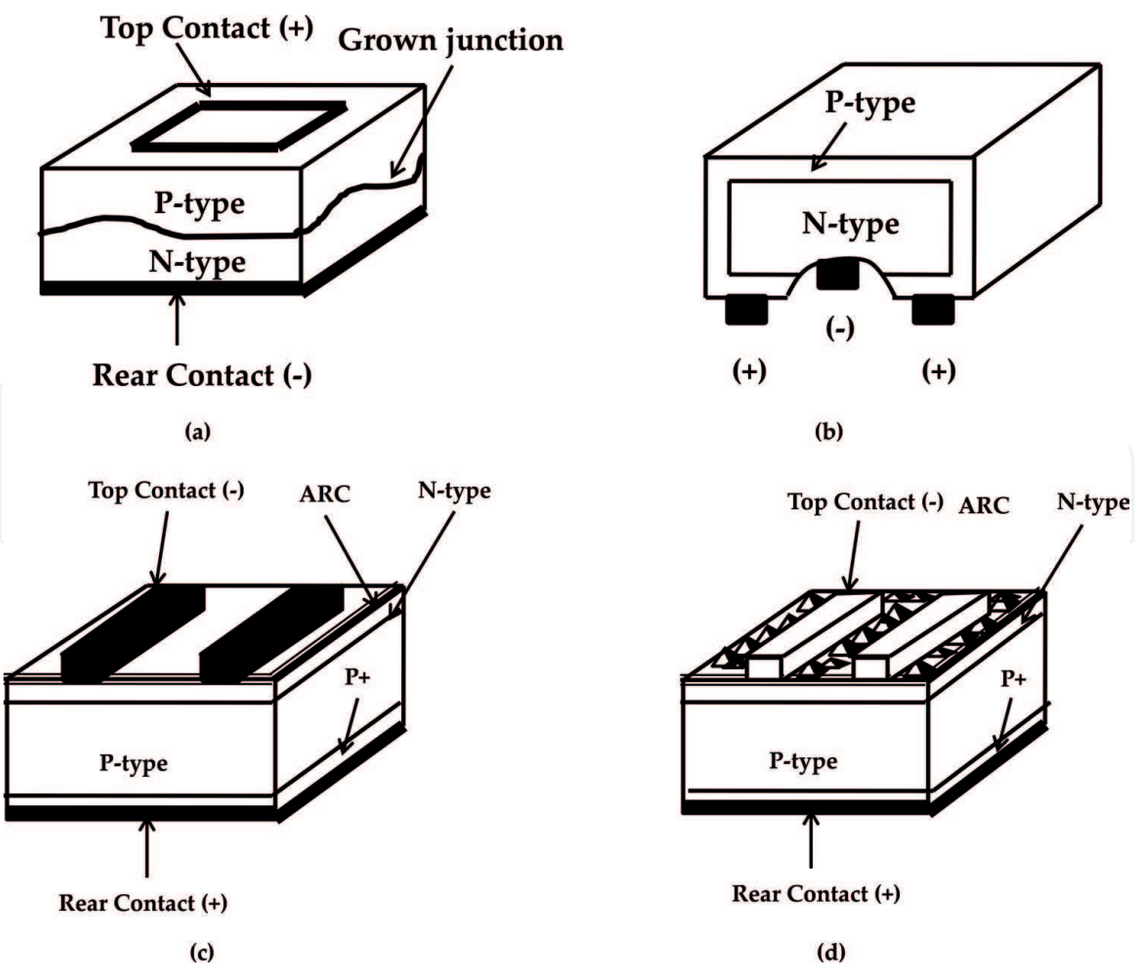

Figure 1.
Evolution of silicon solar cells. (a) 1941: Solar cell reported with grown-in junction, (b) 1954: Solar cell p-n junction formed with dopant diffusion, (c) 1970: Violet cell with Aluminum back-surface field, (d) 1974: Black cell with chemically textured surface [3].

spaced fingers reduced the requirement on the junction doping and eliminated the dead layer. An ARC of titanium dioxide (TiO_x) was used and its thickness was selected to reduce the reflection for shorter wavelengths and gave a violet appearance to the solar cells. Further improvement was made by texturing the wafers using anisotropic etching of (100) wafers to expose the (111) surfaces. The texturing led to improved light-trapping and gave the cells a dark velvet appearance. The improved cell architecture is shown in **Figure 1(d)**. In 1976, Rittner and Arndt demonstrated terrestrial solar cells with efficiencies approaching 17% [3].

The passivated emitter solar cell (PESC) achieved a milestone of 20% efficiency in 1984–1986. The metal/silicon contact area was only 0.3% in PESC cells, while a double layer ARC of ZnS/MgF_2 was used in both cell structures. In 1994, passivated emitter rear locally diffused (PERL) cell with an efficiency of 24% were demonstrated [3]. As compared to the PESC cell, the PERL cell had inverted pyramids on FS for better light-trapping and oxide-based passivation on both sides. Oxide passivation layer on the rear-side also improved the internal reflectance of the long wavelength and hence the spectrum response.

In addition to the evolving solar cell architectures, there has also been continuous development in the manufacturing domain in terms of increased throughput, improved process-steps and reduced costs. A brief over-view of the manufacturing of Si substrates and various types of solar cells is given in the next section.

3. Commercial silicon solar cell technologies

Si is the second most abundant material on earth after oxygen and has been widely used in the semiconductor industry. Metallurgical grade silicon (Mg-Si) of 98% purity is obtained by heating quartz (SiO_2) with carbon at high temperatures of 1,500-2,000 [4]. Mg-Si is further purified to obtain solar grade silicon chunks of 99.99% purity. The refined solar grade Si chunks are then processed further to obtain mono-crystalline and multi-crystalline forms of Si ingots, which are a large mass of silicon. In mono-crystalline Si, the atoms are arranged in the same crystal orientation throughout the material. For solar cells, (100) orientation is preferred as it can be easily textured to reduce the surface reflection [5]. Multi-crystalline Si, as the name suggest has multiple grains of Si material with different orientations, unlike the mono-crystalline substrates. Mono-crystalline material have higher minority carrier lifetime compared to multi-crystalline Si and hence higher solar cell efficiencies for a given solar cell technology.

The Czochralski (Cz) method for making mono-crystalline Si ingots is illustrated in **Figure 2(a)**. High purity molten silicon with dopant is maintained above the melting point and then a seed crystal is pulled at a very slow rate to obtain an ingot of as large as 300 mm in diameter and 2 m in length [6]. The molten silicon can be doped with either p-type or n-type dopants to obtain the specific type of mono-crystalline Si ingot of up to 200 kg [2]. Wafers sawn from the ingots have circular edges and hence the shape is called a 'psuedo square'. Multi-crystalline silicon ingots are made by melting high purity Si and crystallizing them in a large crucible by directional solidification process [7] as demonstrated in **Figure 2(b)**. The process does not have a reference crystal orientation like the Cz process and hence forms silicon material of different orientations. Currently the multi-crystalline Si ingots weigh >800 kg [2] which are then cut into bricks and wafers are sawn further. Current size of mono-crystalline and multi-crystalline wafers for solar cell fabrication is 6 inch × 6 inch. The area of the mono-crystalline wafers will be little less due to the pseudo-square shape. The most widely used base material for making solar cells is boron doped p-type Si substrates. N-type Si substrates for also used

for making high efficiency solar cells, but have additional technical challenges like obtaining uniform doping along the ingot compared to p-type substrates.

A broad classification of different types of solar cells along with efficiency ranges is shown in **Figure 3**. The standard aluminum back-surface field (Al-BSF) technology is one of the most common solar cell technology given its relatively simple manufacturing process. It is based on full rear-side (RS) Al deposition by screen-printing process and formation of a p^+ BSF which helps repel the electrons from the rear-side of p-type substrate and improve the cell performance. The manufacturing flow for Al-BSF solar cells is shown in **Figure 4**. The standard design of commercial solar cells is with grid-pattern FS and full area RS contacts.

The passivated emitter rear contact (PERC) solar cell improves on the Al-BSF architecture by addition of rear-side passivation layer to improve rear-side passivation and internal reflection. Aluminum-oxide is a suitable material for RS passivation with average solar cell efficiencies nearing 21% obtained in production [8]. An existing

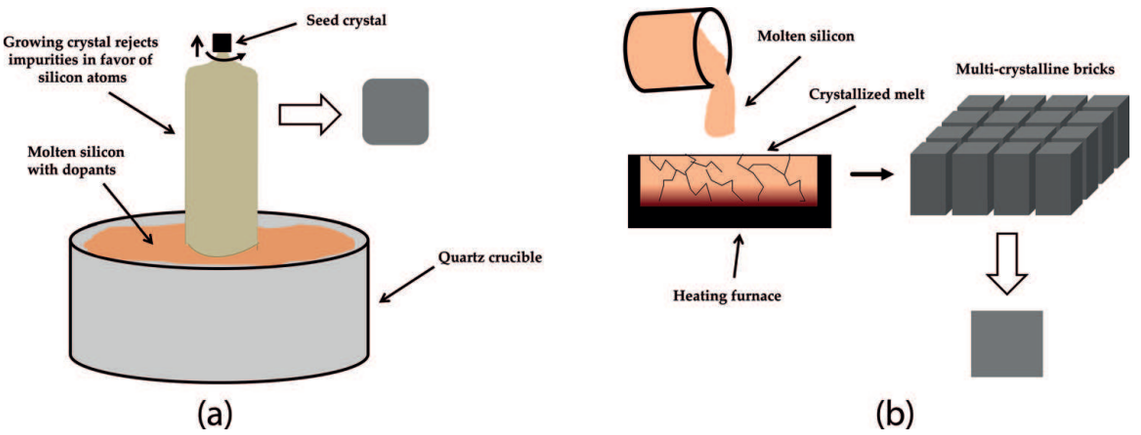

Figure 2.
Illustration of (a) Cz process for mono-crystalline ingots and (b) directional solidification process for multi-crystalline ingots.

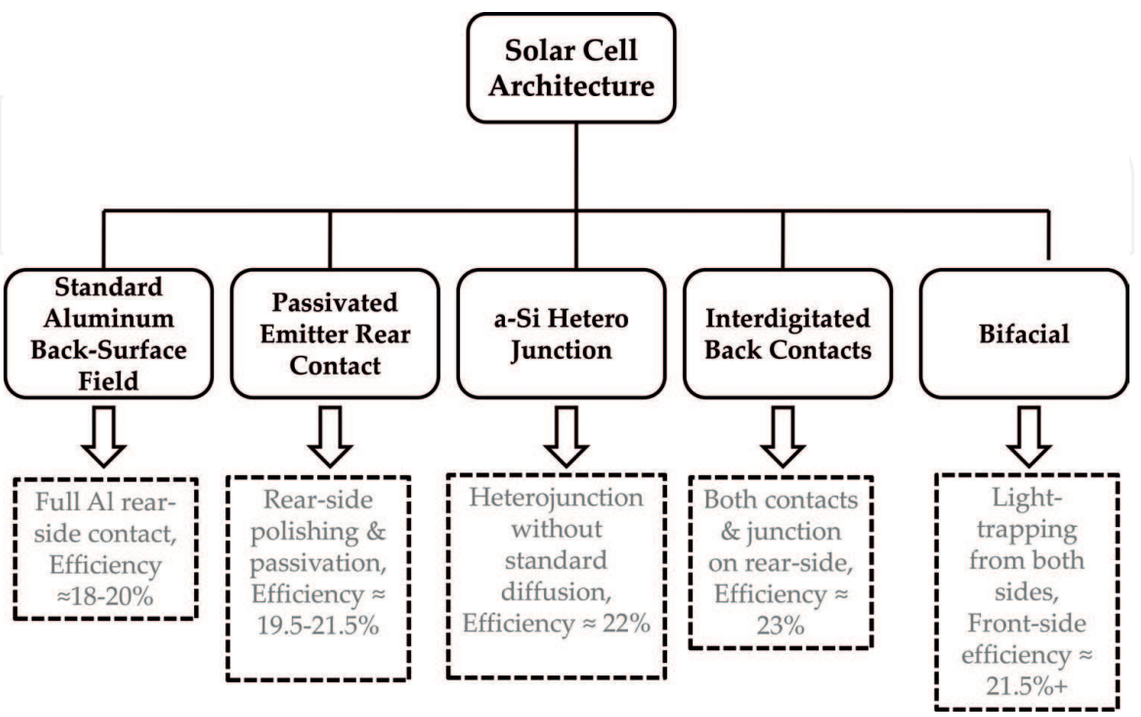

Figure 3.
Broad classification of different types of solar cell.

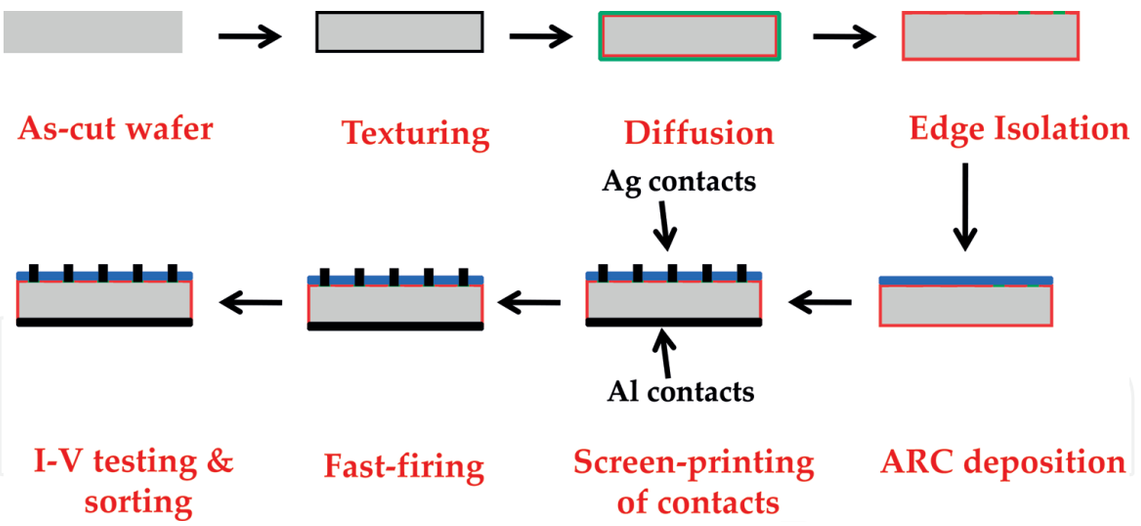

Figure 4.
Manufacturing flow of Al-BSF solar cells.

Al-BSF solar cell line can be upgraded to PERC process by two additional tools (RS passivation layer deposition and laser for localized contact opening on the RS).

The remaining three cell architectures are mainly higher efficiency technologies based on n-type Si substrates. The a-Si heterojunction solar cell has a-Si layers on the FS and RS of n-type Si substrate to form 'heterojunctions' unlike the conventional high temperature diffusion-based p-n junction. Such technology allows processing at lower temperatures, but is very sensitive to the quality of the surface interfaces. a-Si-based heterojunction solar cell was commercially manufactured by Sanyo Electric, which is now taken over by Panasonic [9]. In the interdigitated back contact (IBC) solar cell design, both contacts are present on the rear-side eliminating the FS contact shading losses. Typically for IBC solar cells, the junction will also be located on the rear-side. One of the early manufacturers of the high efficiency n-type IBC solar cell is SunPower Corporation [10]. Bifacial cells, as the name suggests can capture light from both sides of the solar cells. This entails that the rear-side also has a grid-pattern contacts to enable light collection. An example of the bifacial technology is the BiSON solar cell developed and commercialized by ISC, Konstanz [11]. It should be noted that the indicated classification is not an exhaustive list of various other types of solar cell architectures which are in R&D phase, close to commercialization or already being manufactured. The subsequent sections will give an over-view of the process steps for manufacturing of Al-BSF solar cells.

4. Wet-chemistry processes for solar cell fabrication

Wet-chemistry-based treatment is an important step in solar cell processing for saw damage removal (SDR) for the as-cut wafers, texturing of the surface to increase the absorption of incoming solar radiation and edge isolation after the diffusion process. As discussed in the previous section, there are mainly mono-crystalline and multi-crystalline silicon wafers used for fabrication of solar cells. The wet-chemistry-based processing for the respective types of wafers will be discussed ahead.

4.1 Texturing of mono-crystalline silicon wafers

As indicated in Section 2, the development of solar cells started primarily with mono-crystalline wafers and hence employed well-established methods from the domain of microelectronics. Alkaline anisotropic etching based on KOH/NaOH

is used for pyramidal texturing of mono-crystalline wafers. An as-cut mono-crystalline wafer has a weighted average reflectance of >30% (over wavelength of 300–1,200 nm) which reduces to 11–12% after the texturing process. Typical morphology of an alkaline textured surface is shown in **Figure 5**. The anisotropic etching solution etches the (100) surface of the wafers to expose the (111) faces which have a higher density of silicon atoms and hence a slower etch rate compared to the (100) faces. This results in formation of random pyramid structures which form an angle of 54.7° with respect to the wafer surface.

Typical parameters for the alkaline texturing process are shown in **Table 1**. It should be noted that the values of various parameters are indicative and are not to be taken as absolute as there are a variety of additive manufacturers in the market. Isopropyl alcohol (IPA) was initially used as an additive in the texturing solution, which is not involved in the etching reaction, but acts as a wetting agent to improve the homogeneity of texturing process by preventing the H_2 bubbles (generated during the reaction) adhering to the silicon surface [12]. However by 2010, IPA was gradually replaced with alternative additives due to drawbacks like unstable concentration as the bath temperature is close to the boiling point of IPA (82.4°C), high costs, high consumption, health hazards and explosiveness [12]. Many groups have published development work to replace IPA with alternate additives to overcome the disadvantages of IPA, increase the process window and reduce the surface reflectance [12–16]. Additives also reduce the processing time to <10 minutes and increases the bath life to >100 runs.

The texturing process of the mono-crystalline wafers is typically performed in a 'batch' which implies that the wafers are loaded in a carrier with slots to hold the wafers (100 slots in a carrier) and then the batch is processed sequentially in baths for texturing, cleaning, treatment steps to remove the organic residue and metal contamination and drying the processed wafers. The carriers are typically coated with PVDF which has very good resistance to various chemicals, abrasion and mechanical wear and tear. Typical carrier for mono-crystalline wafers handling is shown in **Figure 6**. The batch texturing tool has dedicated baths for each step with dosing tanks for chemicals used in the bath. The tool processes many carriers simultaneously and can reach a throughput of >6,000 wafers/h with processing of four carriers at the same time.

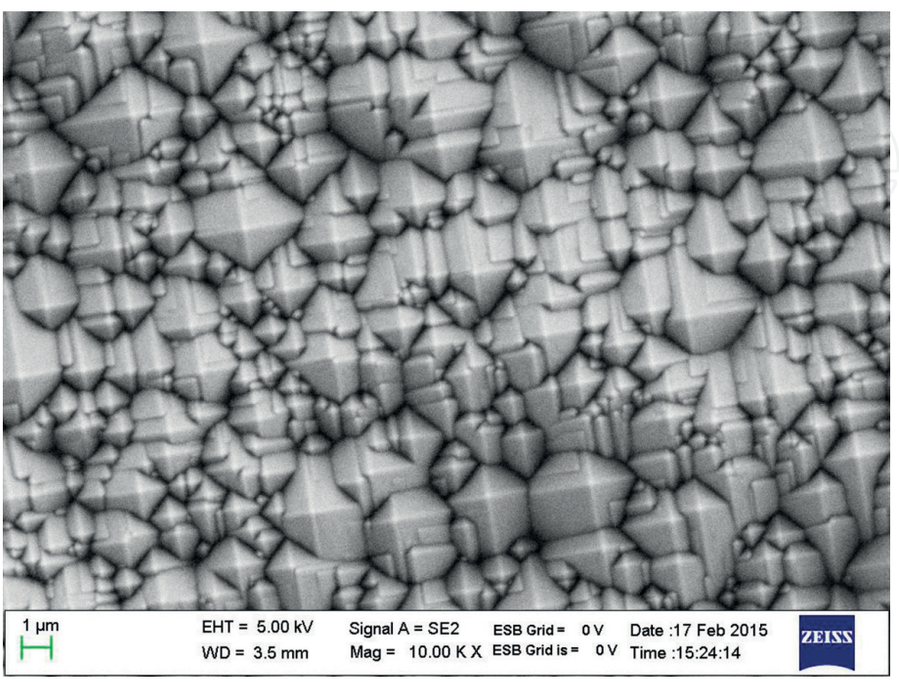

Figure 5.
Typical surface morphology of an alkaline textured mono-crystalline wafer.

Process	KOH/IPA	KOH/additive
KOH (%)	3	<3
IPA (%)	6	—
Additive (%)	—	<2
Process temperature [°C]	>80	70–100
Pyramid size [μm]	5–12	2–7
Process time [min]	30–40	5–10
Organic content [wt%]	4–10	<1.0
Boiling point [°C]	83	>100
Bath lifetimes	<15	>100

Table 1.
Process parameters for IPA-based and additive-based alkaline texturing of mono-crystalline wafers.

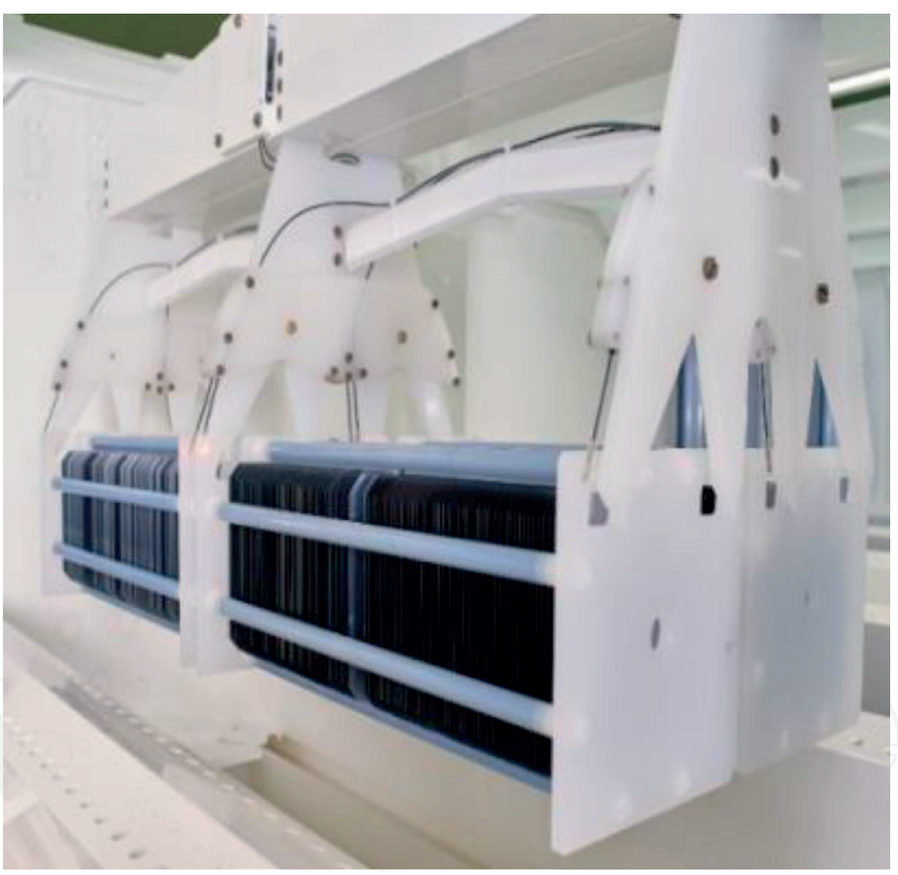

Figure 6.
Carriers for loading wafers in the batch tool. Source: RCT solutions GmbH.

4.2 Texturing of multi-crystalline silicon wafers

Multi-crystalline wafers offer a cost advantage compared to the mono-crystalline wafers and hence have been more widely adopted. However, the alkaline chemistry used for texturing mono-crystalline wafers does not work well for multi-crystalline wafers due to the presence of different grain orientations. An alternative acidic chemistry based on HF and HNO_3 was developed to remove the saw damage and texture the multi-crystalline wafers simultaneously [17, 18]. The acidic solution-based texturing operates at temperatures below room temperature and hence leads to

reduced reaction gas emission, little heat generation, higher stability of the etching solution and better control of the etch rate [18]. A comparison of alkaline texturing and acidic texturing process for multi-crystalline wafers is shown in **Figure 7**.

The acidic texturing process of multi-crystalline wafer can be done in significantly reduced time compared to the alkaline texturing process and hence can be implemented in an 'inline' configuration where the wafers are passed through rollers immersed in the etching bath. A representative image of an inline process along with the typical acidic texturing process is shown in **Figure 8**. For a five lane configuration, the inline tool can have a throughput of up to 4,000 wafers/h. It is important to note that the wafer surface facing down in the etching solution is textured better than the top-side and is the 'sunny-side' for further processing. The acidic texturing process leads to formation of porous silicon on the textured surface which absorbs light and also increases the surface recombination [18]. Hence the porous silicon is removed using a dilute alkaline solution. Subsequently, an acidic clean (HF + HCl) is performed to remove oxides and metal contamination from the wafer surfaces.

It is important to note that the acidic texturing process discussed above is suitable for the slurry-wire sawn (SWS) multi-crystalline wafers. In the past few years, diamond-wire sawing (DWS) process has replaced the slurry-wire-based cutting due to process and economic advantages [19]. The saw damage of the SWS multi-crystalline wafers is more than the DWS wafers, which have deep straight grooves and a much more smoother surface than the slurry-wire sawn wafers [19]. The saw damage for the SWS wafers plays an important role for initiating the texturing process, which does not occur for the DWS wafers.

Various methods have been proposed to texture DWS multi-crystalline wafers and are summarized in **Table 2** [20]. By tuning the various methods, reflectance of close to 0% can be obtained and hence the term 'black silicon' has been used for the texturing process of DWS multi-crystalline wafers. RIE was the first method for making black silicon and uses sulfur hexaflouride (SF_6) to react with Si and gases like Cl_2 and O_2 for passivating and limiting the reaction [20]. Recently, commercial multi PERC solar cells with average efficiency of 21.3% have been demonstrated with RIE-based

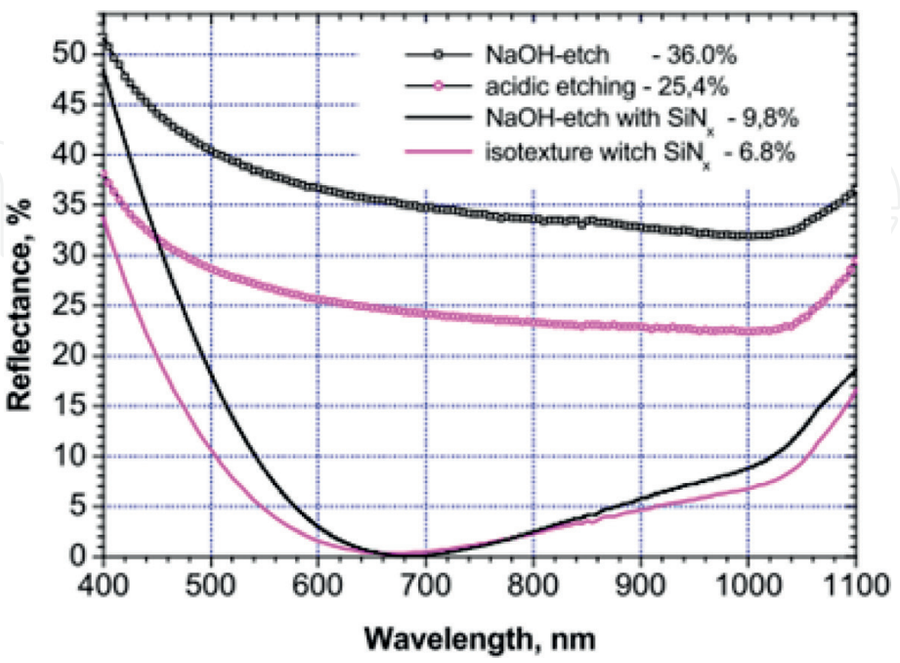

Figure 7.
Comparison of alkaline and acidic texturing for multi-crystalline wafers. Reflectance curves after deposition of SiN_x:H are also showed for comparison [17].

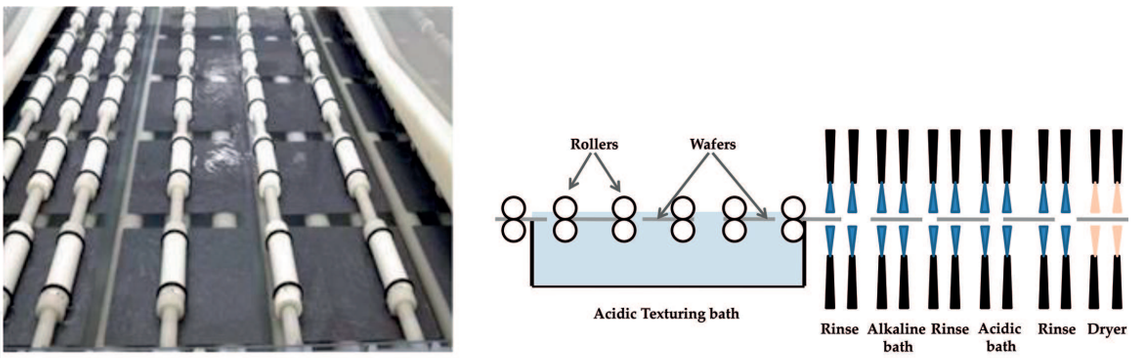

Figure 8.
(a) Representative inline process with five lanes and (b) acidic texturing process flow for multi-crystalline wafers.

Method	Reagents	Mask	Catalyst	Minimum reflectance (%)
Reactive ion etching (RIE)	SF_6/O_2, $SF_6/Cl_2/O_2$, $SF_6/O_2/CH_4$	None	None	4.0
Plasma immersion ion implantation (PIII)	SF_6/O_2	None	None	1.8
Laser irradiation	CCl_4, $C_2Cl_3F_3$, SF_6, Cl_2, N_2, air	None	None	2.5
Plasma etching	SF_6	Ag nano particles	None	4.2
Metal-assisted chemical etching (MACE)	$AgNO_3/HF/HNO_3$	None	Ag, Au	0.3
Electrochemical etching	HF, EtOH,H_2O	None	None	<5.0

Table 2.
Various methods for texturing diamond-wire sawn multi-crystalline wafers [20].

texturing process [21]. However, since RIE is a vacuum-based process the throughput is low as compared to a typical inline process and also additional pre-processing and post-processing is required to remove the saw damage and damage due to ion-bombardment, respectively. A variant of the RIE method which does not require vacuum or plasma has been implemented in a commercial tool [22].

One of the approaches for texturing DWS multi-crystalline wafers is to upgrade the existing acidic texturing-based chemistry with additives [23–25]. Such an approach can potentially have a lower CoO compared to the MACE-based approach [23]. Reflectance of such an additive-based approach has been demonstrated to be similar to the conventional isotexturing solution with solar cell efficiency of 18.7% for the Al-BSF-based structure [24].

MACE-based texturing is similar to the conventional acidic etching method with an additional step of catalytic metal deposition. The process flow consists of SDR, catalyst metal deposition, chemical etching and post-treatment. Efficiencies of 19.2% have been obtained for commercial multi Al-BSF cells using batch-type MACE texturing process [26]. Inline-type MACE-based commercial tool has been demonstrated with the possibility to tune the reflectance in the range of 12–23% and obtain average efficiency for Al-BSF and PERC structure of 18.8 and 20.2%, respectively [27]. Representative images of textured surface based on MACE process are shown in **Figure 9**. The cost of ownership (CoO) of the inline MACE process is potentially lower compared to the batch-based MACE process with scope to reduce it further by recycling Ag from the texturing bath [27].

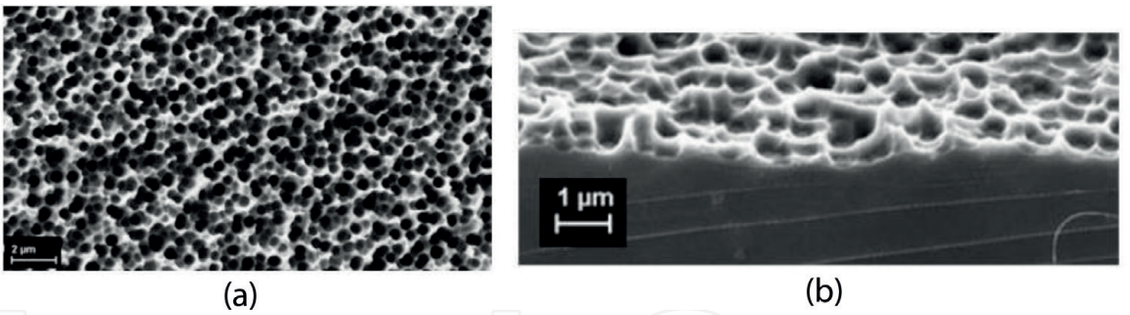

Figure 9.
MACE textured DWS multi wafers, (a) surface with R_{avg} = 12% and (b) surface with R_{avg} = 22% [27].

4.3 Wet-chemistry-based edge isolation

The emitter region in a solar cell is fabricated by a high temperature diffusion process (to be discussed in sections ahead). During the diffusion process, phosphor silicate glass (PSG) is deposited on the wafer which should be removed before deposition of the ARC layer. As depicted in **Figure 10**, after the diffusion step, the n-type region is also present on the edges and the rear-side of the wafer. The n-type layer on edges and the rear-side will short-circuit the emitter with the base substrate and hence it is important to etch these regions and isolate the emitter on the FS from the base substrate as depicted in **Figure 10(c)**.

The edge isolation process can be performed in an inline manner similar to the texturing process discussed in the previous section. The exception in this case is that the chemical should etch only the rear-side and edges without interacting with the FS. A representative image of the edge isolation process is shown in **Figure 11**. It is important to note that the rollers are present only on the bottom-side to avoid any contact of the etching solution with the front-side. The subsequent steps after the RS etching are similar to those in the inline texturing machine.

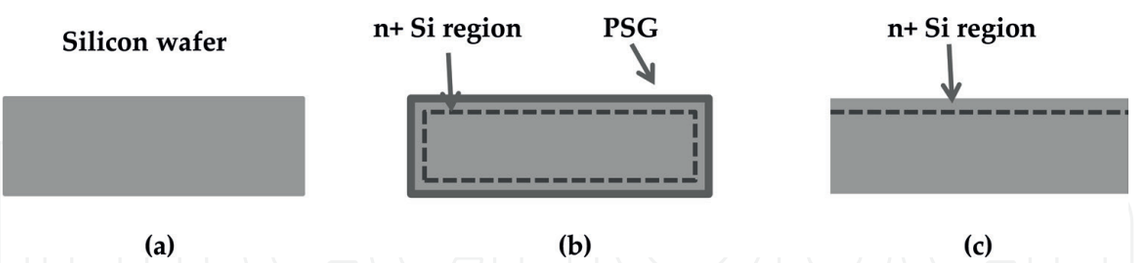

Figure 10.
Processing of silicon wafer after diffusion and edge isolation (a) Textured silicon wafer, (b) Diffused silicon wafer, (c) Diffused silicon wafer after edge-isolation.

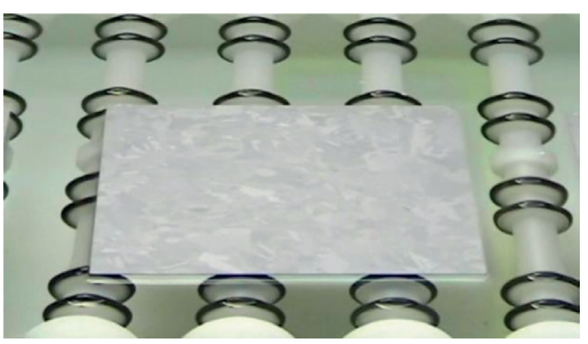

Figure 11.
Representative image of solar cell in an inline edge-isolation bath.

5. Thermal processes for solar cell fabrication

High temperature processes form a vital part of solar cell fabrication. Examples of such processes are forming the p-n junction by diffusion, firing of screen-printed contacts, activating surface passivation layers or annealing process induced defects. The section glimpses the basic physics of emitter diffusion process and plasma enhanced chemical vapor deposition (PECVD).

5.1 Emitter diffusion

Emitter diffusion is one of the crucial thermal steps in the industrial solar cell fabrication. The n-type emitter of the crystalline p-type silicon solar cells is formed by phosphorus (P) diffusion. In the diffusion process, the Si wafers are sent in a furnace and exposed at 800–900°C to phosphoryl chloride ($POCl_3$) and O_2 which results in PSG deposition on the Si wafer surfaces. This step is called as pre-deposition, where the PSG [28] acts as a source of phosphorus (P) dopants to diffuse into the Si wafer. The next step is drive-in, where the supply of dopant gases is disconnected and P from the PSG layer diffuses further into the Si wafer. Hannes et al. [29] illustrates for the optimum process feasibility for photovoltaic applications, three different effects have to be considered. Firstly, the in-diffusion of P from the PSG and its presence in electrically active and inactive states in the Si wafer, which increases Shockley-Read-Hall (SRH) recombination. Secondly, the gettering of impurities into the Si layer towards the PSG layer. Finally, the metal contact formation with the P-doped Si emitter draws out the generated power.

The diffusion process is quantified by sheet resistance which depends on the depth of p-n junction and P concentration profile. The sheet resistance has units of Ω/cm (commonly measured as Ω/□) and is measured using a four-point probe system. The definition of sheet resistance is illustrated in Eq. (1).

$$R = \frac{\rho l}{A} = \frac{\rho l}{W * D} = \frac{\rho}{D} = \rho_{sheet} \tag{1}$$

where R = resistance of a rectangular section (Ω); ρ = resistivity (Ω cm); l = length of the rectangular section (cm); A = area of the rectangular section (cm^2); W = width of the rectangular section (cm); D = depth of the rectangular section (cm) and ρ_{sheet} = resistance for given depth (D) when l = W (Ω/□).

The earlier values of emitter sheet resistance were 30–60 Ω/□ with p-n junction depths of >400 nm and high P surface concentration. With improvements in the front-side silver (Ag) contacting paste, the emitter sheet resistance is now in the range of 90–110 Ω/□ with junction depth of around 300 nm and lower P surface concentration. Shifting to larger sheet-resistance allows to capture more light in the UV and blue spectrum, while also reducing the surface recombination to improve the V_{oc}. It should be noted that the diffusion process occurs on the FS (directly exposed to the gases) and also on the edges and RS. If the edge isolation process is not carried out (as discussed in Section 4.3), the emitter will be short-circuited with the substrate.

Figure 12 shows the $POCl_3$ diffusion process in a closed quartz-tube system. $POCl_3$ is a liquid source supplied to the process tube by bubbling it with a carrier gas N_2. By mixing O_2 with the $POCl_3$, there will be an epitaxial growth of PSG layer as indicated in Eq. (2) [30].

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5(PSG) + 6Cl_2 \tag{2}$$

At the Si surface, $2P_2O_5$ is reduced to elemental phosphorus during the drive-in step as shown in Eq. (3) [30].

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \quad (3)$$

Chlorine which is a by-product during the pre-deposition cleans the wafers and quartz-tube by forming complexes with metals. PSG is used as source for driving in the P atoms into Si surface. During the drive-in process, $POCl_3$ is switched off and only O_2 is added to build up a thin oxide layer beneath the PSG to enhance the diffusion of P atoms into Si surface.

Inside the diffusion tube there are five heating zones as illustrated in **Figure 13**. The zones are:

- Loading zone (LZ)—area from where the wafers are loaded into the tube.
- Center loading zone (CLZ)—area between the loading zone and centre zone.
- Center zone (CZ)—center area of the tube.
- Center gas zone (CGZ)—area between the centre zone and gas zone.
- Gas zone (GZ)—area from where the gases move out through the exhaust.

Typically the temperatures of each heating zone are adjusted to obtain equal emitter sheet resistance for all wafers across the boat.

Environment of diffusion process should be very clean and hence quartz material is used for the tubes. Cleanliness of the tubes and loading-area maintenance also affects the process results. Since in gas-phase diffusion there is no residue in the tube, it results in a cleaner process. By half pitch loading in the low pressure (LP) conditions [31], the throughput can be increased. Commonly 1,000 wafers are loaded in a single tube and with five diffusion tubes in a batch-type diffusion system, a throughput of up to 3,800 wafers/h can be achieved for solar cell manufacturing.

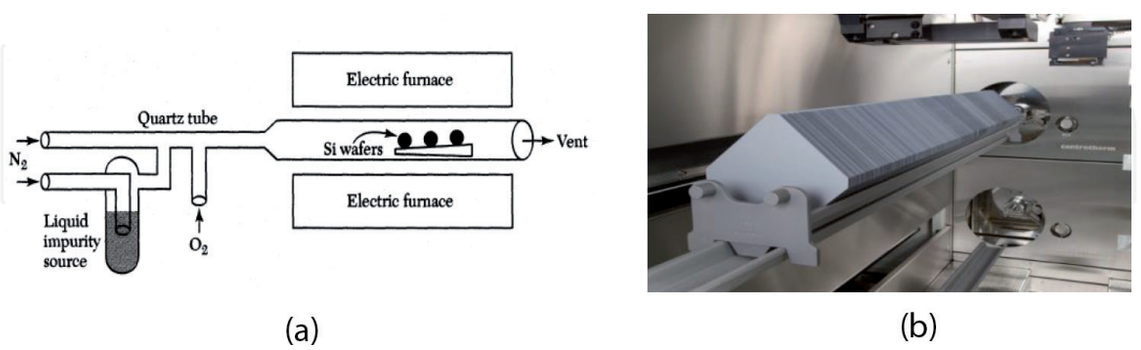

Figure 12.
(a) Schematic representation of the batch-type diffusion process and (b) representative image of a batch-type diffusion equipment. Source: centrotherm GmbH.

Figure 13.
Heating zones inside the diffusion tube.

An inline diffusion system where the wafers are transported on a belt with phosphoric acid as the source of P dopants was also used in commercial production [32]. However, compared to the inline process, the batch process is more clean, effective and efficient. For n-type solar cells or advanced solar cells concepts like PERT, the p-type batch diffusion is based on boron (B) dopant sources like boron tribromide (BBr_3) [33, 34].

5.2 Anti-reflective coating (ARC) deposition

A bare Si surface reflects >30% of the light incident. As discussed in Section 4, the texturing process improves the light-capturing. It is desirable to reduce the reflectance further which is obtained by depositing an ARC layer. TiO_x was one of the earliest material to be used as an ARC layer for solar cells, however since it could not provide adequate surface passivation it was eventually replaces by SiN_x:H [37]. Thermally grown silicon oxide (SiO_2) was also employed as the passivating material in the record breaking passivated emitter rear locally diffused (PERL) cells [37]. High thermal budget and long process time made SiO_2-based passivation unsuitable for mass-production of solar cells [37]. A comprehensive review of various ARC and passivating material for solar cell applications is discussed in [37].

The plasma enhanced chemical vapour deposition (PECVD) process is suitable for depositing an ARC layer of SiN_x:H which not only reduces the reflection but also passivates the front-side n-type emitter and the bulk thus improving the solar cell efficiency [36, 37]. A schematic of a batch-type PECVD system is shown in **Figure 14**. The wafers are loaded in a graphite boat with the front-sides facing each other. An RF plasma based on process gases ammonia (NH_3) and silane (SiH_4) operating at a temperature of 400–450°C deposit the hydrogenated SiN_x:H layer as per Eq. (4) [35]. The hydrogen incorporated in the SiN_x:H film diffuses into the bulk during the firing step (discussed in next section) and passivates the dangling bonds to improve the solar cell performance [36, 37].

$$3SiH_4 + 2NH_3 + N_2 \rightarrow Si_3N_4 + 9H_2 \tag{4}$$

The refractive index (RI) of the SiN_x:H film is controlled by the ratio of SiH_4/NH_3 gas, while the thickness depends on the deposition duration. The SiN_x:H-based ARC can minimize the reflection for a single wavelength and the wavelength-thickness is given by [38],

$$t = \frac{\lambda_0}{4n_1} \tag{5}$$

where t = thickness of the SiN_x:H ARC layer, λ_0 = wavelength of incoming light and n_1 = refractive index of the SiN_x:H layer.

Based on the relationship, the ARC is also called as a 'quarter wavelength ARC'. For solar cells, the RI and thickness are selected to minimize the reflection at a wavelength of 600 nm as it is the peak of the solar spectrum. The thickness and RI of the ARC is selected to be the geometric mean of materials on either side, i.e., glass/air and Si. The typical thickness of the SiN_x:H ARC is 80–85 nm with RI of 2.0–2.1 giving the solar cell a color of blue to violet blue. A representative image of textured multi-crystalline solar cell deposited with SiN_x:H is shown in **Figure 15(a)**, while the variation of SiN_x:H color based on its thickness is shown in **Figure 15(b)**. It is important to note that there is a dependence on the surface texture and ARC color for given deposition parameters. There is a variety of solar modules where the color of the solar cells is darker unlike the typical blue color. A typical ARC

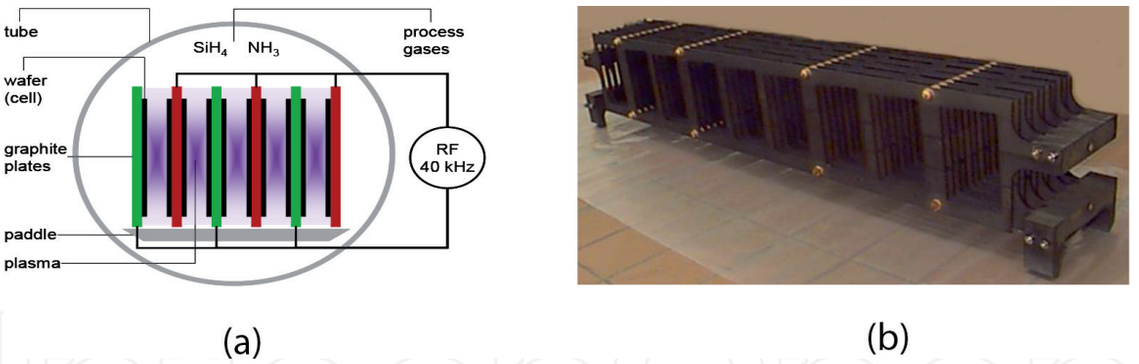

Figure 14.
(a) Schematic diagram of batch-type PECVD process for SiN_x:H deposition and (b) graphite boat for loading Si wafers in the PECVD furnace.

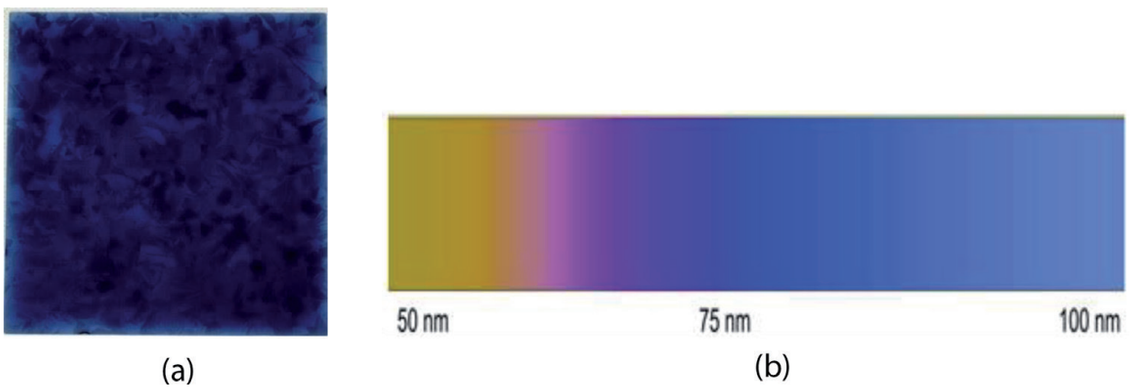

Figure 15.
(a) Representative image of SiN_x:H coated multi-crystalline solar cell, (b) variation of SiN_x:H layer based on its thickness.

deposition stage in a solar cell manufacturing line consists of two PECVD systems, each with four tubes and a throughput of up to 3,500 wafers/h.

SiN_x:H is not suitable for passivating p-type Si and hence dielectrics like Al_2O_3 are used for RS passivation for cell architecture like PERC cells [8] or for p-type emitters in n-type solar cells. For PERC solar cells, the Al_2O_3 passivating layer is capped by a SiN_x:H to protect it from the Al-paste during the firing process and also serve as an internal reflector for the long wavelength light. Commercial PECVD and atomic layer deposition (ALD)-based systems are available for depositing Al_2O_3 with throughput of up to 4,800 wafers/h [39].

6. Metallization and solar cell characterization

6.1 Screen-printing-based metallization

The last processing step for solar cell fabrication is the FS and RS metallization to draw out the power with minimum resistive losses. Ag is a good contact material for the n-type emitter, while Al makes a very good contact with the p-type substrate. A combination of Ag/Al paste is used to print pads on the RS to facilitate interconnection of solar cells in a module. Screen-printing is a simple, fast and continuously evolving process for solar cell metallization.

A schematic representation of the screen-printing process is shown in **Figure 16**. The screens have an emulsion coated stainless steel mesh with openings as per the desired metallization pattern as illustrated in **Figure 17(a)**.

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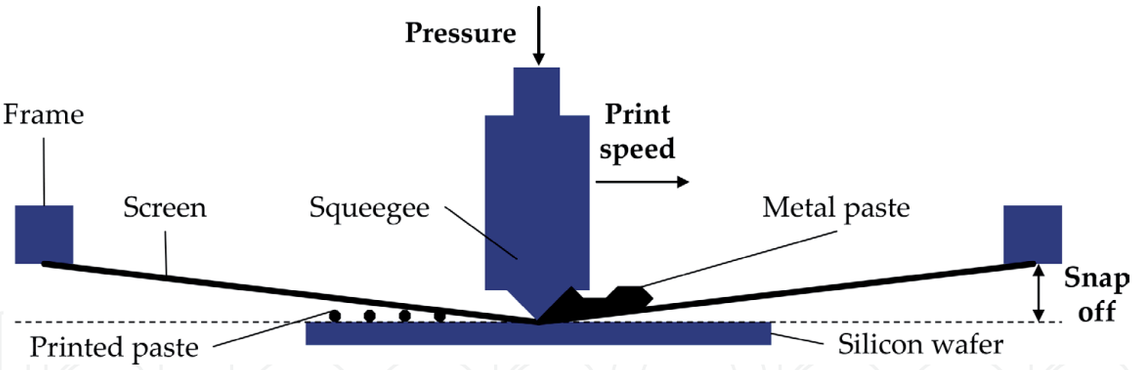

Figure 16.
Illustration of the screen-printing process for solar cell metallization.

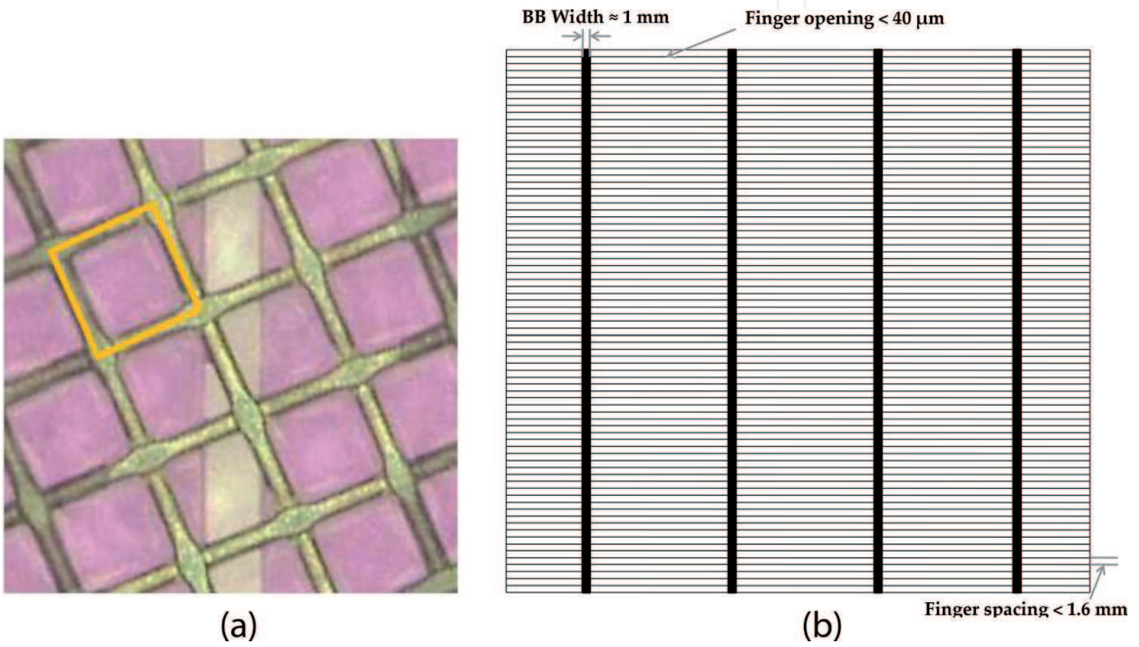

Figure 17.
(a) Mesh-emulsion screen with finger opening for FS Ag printing [40] and (b) representative FS metallization pattern.

The metal paste is spread over the screen via the flood and the squeegee movement that deposits the paste on the solar cell based on the screen-pattern. Snap-off is the distance the screen and the solar cell. The squeegee pressure and the snap-off distance are the critical parameters that determine the paste lay down and geometry of the Ag FS fingers.

Typical paste lay down for Ag/Al RS pads, RS Al and FS Ag are 35–45 mg, 1.1–1.4 g and 100–120 mg, respectively for a 6 inch Al-BSF multi-crystalline solar cell. An illustrative Ag FS metallization pattern is shown in **Figure 17(b)**. The Ag finger opening has reduced to below 30 µm, while application of 5 bus-bar is being increasingly adopted now. With such screen parameter and good paste lay down, consistent FF of >80% should be obtained for the Al-BSF solar cells with an optical shading loss of <6%.

6.2 Drying and fast firing of metallization pastes

The metallization pastes consist of metal powder, solvents and organic binders. In case of FS Ag paste, the paste also contains glass-frit while etches the SiN_x:H layer and makes contact with the n-type emitter [41]. The metal pastes

are dried after printing and finally they are sent through a fast-firing furnace for sintering and form the RS Al-BSF and FS Ag contact. An example of such a fast-firing furnace with the temperature profile is shown in **Figure 18**. The FS Ag finger sintering process is illustrated in **Figure 19**. When the solar cell passes through the fast-firing furnace, the organic binders are burnt, followed by melting of the glass frit and finally formation of Ag crystallites contacting the n-type emitter. The firing profile needs to be tuned based on the specific types of metallization pastes and emitter diffusion profile. As an example, the firing peak temperature could be low to not form a good ohmic contact on the FS, while a too high temperature can lead to diffusion of Ag through the junction and shunting of the p-n junction. Image of a complete multi-crystalline Al-BSF solar cell is shown in **Figure 20**.

6.3 Plating-based front-side metallization

The costing of various factors in solar cell processing have decreased over the years, while the contribution of front Ag is still the most significant [42]. Significant amount of work has been done to replace Ag by alternate metal like copper (Cu) which has a conductivity value of very close to that of Ag and also offers a potential significant cost advantage [43, 44]. Cu has high diffusivity and solubility in Si and hence a barrier-layer like nickel (Ni) is deposited on Si prior to Cu plating [42]. Light-induced plating (LIP) which is derived from conventional plating utilizes the photovoltaic effect of light to plate the desired metal and has many advantages compared to conventional plating [43, 44].

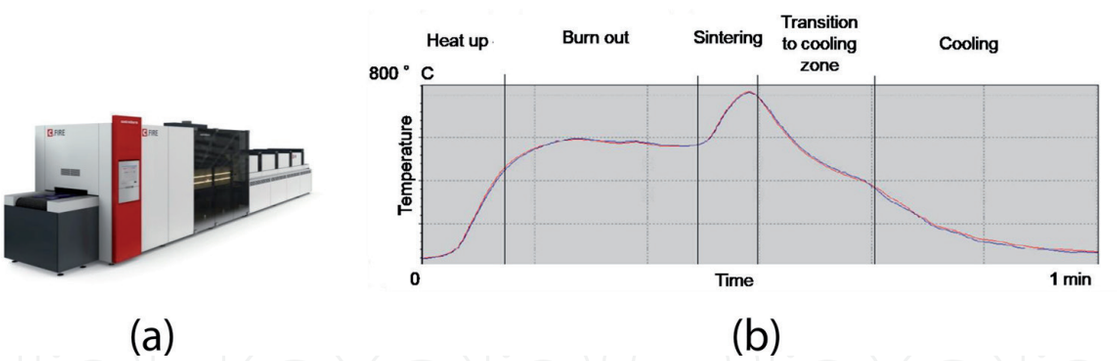

Figure 18.
(a) Example of a firing furnace for sintering metal contacts and (b) illustrative temperature profile of a firing furnace. Source: centrotherm GmbH.

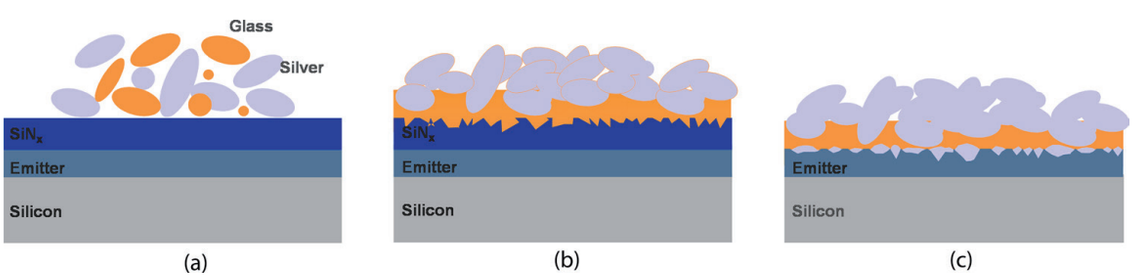

Figure 19.
Illustration of the firing process. (a) Burning out of the organic binders, (b) melting of glass frit which etches the SiN_x:H and (c) Ag crystallite formation at the emitter interface.

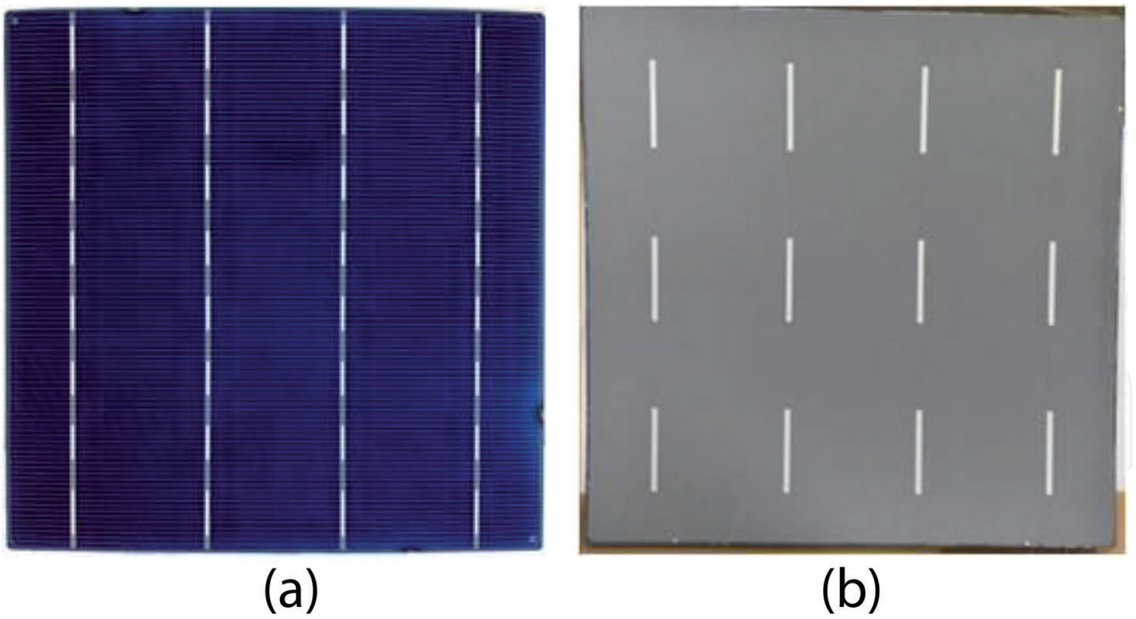

Figure 20.
(a) FS of a complete solar cell and (b) RS of a complete solar cell.

Ni-Cu-based front-side metallization requires an additional front-side ARC patterning step unlike the Ag paste-based metallization and in most cases also an additional Ni sintering step to reduce the contact resistance and have good adhesion of the metal stack [42]. Commercial DWS cut mc-Si solar cells based on Ni-Cu-Ag plated stack have been demonstrated with finger width of 22 μm, aspect-ratio of close to 0.5 and similar efficiency as that of reference screen-printed Ag-based solar cells [45].

Continuous improvement in the Ag FS pastes along with simplicity, reliability and high throughput of the screen-printing process has made it difficult for Ni-Cu-based metallization to compete with Ag-based FS metallization. However, high solar cell efficiency concepts like bifacial heterojunction solar cells, where Cu can be directly plated onto the transparent conducting oxide, the plating process is simplified and requires only a single tool [39]. Similarly, high efficiency concepts which require reduced amount of metal can achieve the same using plating-based metallization [42, 46].

6.4 I-V testing and characterization of solar cells

The final step is I-V testing of the complete solar-cells as per the standard test conditions (STC), i.e., AM 1.5G, 1000 W/m^2 with a Class AAA solar simulator. An example of FS probing of solar cell is shown in **Figure 21**. The typical parameters obtained from the I-V tester are indicated in **Table 3**. I-V testers have many characterization parameters which can be helpful for diagnosis of solar cell defects. Representative electroluminescence (EL) and thermal IR image of a solar cell with some defects are shown in **Figures 22(a)–(c)**. An EL image of a good solar cell with uniform intensity is shown in **Figure 22(a)**, while for a solar cell in which the FS fingers are not printed uniformly, a darker contrast can be seen in **Figure 22(b)**. **Figure 22(c)** shows a thermal IR image of a solar cell with a localized shunt which has been formed during one of the processing steps. In the end, the solar cells are sorted in different efficiency bins based on the selected classification.

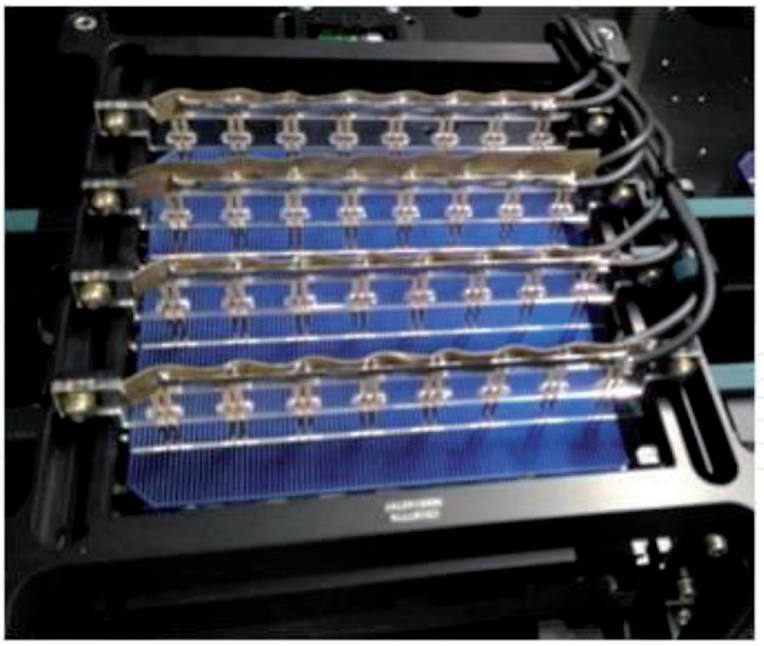

Figure 21.
I-V measurement FS probing for solar cell characterization.

Parameter	Comments
V_{oc} (V)	Good mc-Si Al-BSF solar cells have a value of >0.635 V
I_{sc} (A)	Good mc-Si Al-BSF solar cells have a value of >9.0 A
FF (%)	Good mc-Si Al-BSF solar cells have a value of >80%
Efficiency (%)	Good mc-Si Al-BSF solar cells have a value of >18.6%
V_{mpp} (V)	Corresponding voltage at the maximum power point
I_{mpp} (A)	Corresponding current at the maximum power point
R_s (Ω)	Good mc-Si Al-BSF solar cells have a value of <1.5 mΩ
R_{sh} (Ω)	Good mc-Si Al-BSF solar cells have a value of >100 Ω
I_{rev} (A)	Reverse current at a voltage of −12 V should be <0.5 A for good solar cells
FS BB-BB resistance (Ω)	Resistance measured between the BB's on the FS
RS BB-BB resistance (Ω)	Resistance measured between the BB's on the RS

Table 3.
Parameters for characterization of a solar cell obtained from I-V measurement.

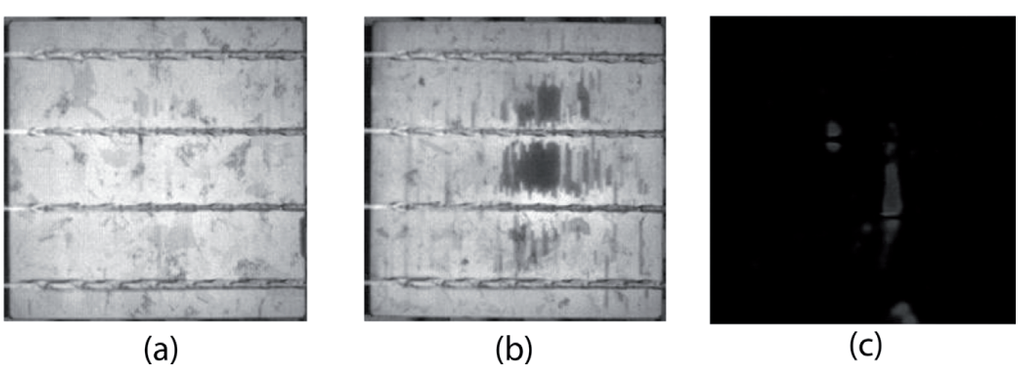

Figure 22.
(a) EL image of a good solar cell, (b) EL image of a solar cell with non-uniformity in Ag finger printing and (c) thermal IR image of a solar cell indicating presence of localized shunts.

7. Future trends

DWS has become the standard for mono-crystalline wafers, while it is expected to have a market share of >80% by 2022 for multi-crystalline wafers [2]. SWS for multi-crystalline wafers is expected to phase-out by that time. With DWS, the kerf loss would also become <80 μm by 2022, which would in turn reduce the poly-Si consumption per wafer below 15 g. 3BB design for front-contacts are expected to phase-out by 2020 with 50% share for 5BB design. With continuous improvements in Ag pastes and screens, the FS finger width is projected to reduce to 30 μm by 2022. Wet-chemical processing tools have crossed throughput of 8,000 wafers/h in 2018 and would touch 9,000 wafers/h by 2020. Thermal processing equipments have reached throughput of 5000 wafers/h in 2018 and expected to cross 7,000 wafers/h by 2020. The metallization and I-V testing/sorting section is expected to have a throughput of >7,000 wafers/h by 2022.

Al-BSF-based cell technology which has a market share of >60% in 2018 is expected to reduce to <20% by 2025. With more emphasis on high efficiency solar cells concepts, share of PERC technology is expected to be >50% by 2022. Production efficiency of Mono PERC is expected to be >22% by 2022, while for multi PERC it should touch 21% by the same time. An important aspect related to multi-PERC is the mitigation of LeTID-based problem to minimize the loss of efficiency after installations of the modules in the field. Si HJ cells with efficiencies of >22% in 2018 after expected to reach stable efficiency of 23% by 2020, with a market share of around 10% by 2022. High efficiency bifacial cells with an additional advantage of tapping the solar radiation from the rear-side is expected to have a market share of 20% by 2022. N-type back contact solar cells are expected to cross 24% efficiency by 2020.

8. Conclusions

Si solar cells have become an important part of the renewable energy domain over past decades with matured manufacturing technologies. P-type multi-crystalline wafers have become the main-stay for solar cell production. However, with higher efficiency and decreasing production costs, mono-crystalline solar cells have also gained a significant share and are expected to compete closely with multi-crystalline wafers in the near future. For standard Al-BSF technology, 19 and 20% has become the bench-mark for multi-crystalline and mono-crystalline solar cells, respectively. Mono-PERC and multi-PERC cells have reached stabilized efficiencies of 21.5 and 20%, respectively. In addition, PERC also provides a simpler approach for bifacial solar cells by having a grid pattern on the RS instead of the full area contact. High efficiency n-type and bifacial solar cells have a market-share of <10% which is expected to increase in the future. The manufacturing technologies have matured considerably over the past few years with further improvements to increase the throughput.

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