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# Double-Sided Passivated Contacts for Solar Cell Applications: An Industrially Viable Approach Toward 24% Efficient Large Area Silicon Solar Cells

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## Abstract

Tunnel layer passivated contacts have been successfully demonstrated for next-generation silicon solar cell concepts, achieving improved device performance stemming from the significantly reduced contact recombination of the solar cell contacts. However, these carrier-selective passivated contacts are currently deployed only at the rear side of the silicon solar cell, while the front side adopts a conventional diffused junction and contacting scheme. In this work, we report on the novelty and feasibility of deploying tunnel layer passivated contacts on both sides of a silicon wafer-based solar cell, featuring a textured front surface and a planar rear surface. In particular, we demonstrate that silicon solar cells incorporating our in-house developed electron-selective thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) and hole-selective thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) passivated contacts have a solar cell efficiency potential approaching 24%. Deploying contact passivation only at the rear side of the solar cell, we have reached a solar cell efficiency of 21.7%, using conventional screen printing for metallization. We present a systematic approach of evaluating our in-house developed electron-selective and hole-selective passivated contacts on both textured and planar lifetime test structures, as well as dark I–V test structures, to extract the recombination current density  $j_0$  and the contact resistance  $R_c$  of the passivated contact, which is used for process optimization as well as for subsequent efficiency potential prediction. The two key challenges aiming at a double-sided integration of passivated contacts are (1) parasitic absorption within the front-side highly doped poly-Si capping layer, requiring the processing of ultrathin ( $\leq 10$ -nm) contact passivation layers. This has been quantified by numerical simulation (using SunSolve™) and also solved experimentally, i.e., processing ultrathin 3-/10-nm hole/electron extracting SiO<sub>x</sub>/poly-Si(p<sup>+</sup>/n<sup>+</sup>) passivated contact layers, reaching an implied open-circuit voltage of 690/703 mV on a planar/textured silicon surface, which will even further enhance after SiN<sub>x</sub> capping. (2) Ensuring process compatibility with conventional screen printing: Screen printing on electron extracting poly-Si(n<sup>+</sup>) seems feasible; however, screen printing on hole-extracting poly-Si(p<sup>+</sup>) is still a challenge. Solar cell precursors have been processed, showing excellent pre-metallization results (implied- $V_{OC} \sim 713$  mV). According to

our efficiency potential prediction (using the measured  $j_0$  and  $R_c$  values of our developed contact passivation layers), bifacial double-sided passivated contact solar cells (efficiency potential of  $\sim 23.2\%$ , using our layers) can clearly outperform rear-side-only passivated contact solar cells (efficiency potential of  $\sim 22.5\%$ ).

**Keywords:** passivated contacts, contact passivation, silicon solar cells, double-sided passivated contacts

## 1. Introduction

To meet the future energy needs, there is a need to develop low-cost alternative energy sources to complement the conventional energy sources (e.g., oil, gas, coal) as well as to address the pressing environmental issues associated with the latter. Hence, energy-related technology roadmaps are actively being released and revised toward the future energy needs. One good example is the International Technology Roadmap for Photovoltaic (ITRPV) [1]. In general, a successful deployment of any selected solar cell technology will be mainly dominated by (i) cost-effectiveness of the material and processes, (ii) scalability to high-volume manufacturing, (iii) device performance, and (iv) long-term stability of product. To progress toward item (iii), ITRPV predicts a continuous reduction of recombination losses in the wafer as well as at the front and rear surfaces of the solar cell. According to Ref. [2–4], given the considerable improvements in the wafer bulk, and surface passivation layers, the main source of recombination losses in high-efficiency solar cells is now dominated by the metal contacts. Thus, the ability to greatly reduce the recombination losses underneath the solar cell metal contacts (i.e., contact passivation) coupled with other technological advancements will be instrumental toward attaining the increasing solar cell efficiency targets.

One of the earliest examples of contact passivation can be found in the heterojunction silicon wafer solar cells, which utilizes a stack of intrinsic and doped amorphous silicon (a-Si:H) heterojunction layers [5–7] on both surfaces of the silicon wafer. The ultrathin ( $< 5$  nm) intrinsic a-Si:H layer not only serves to passivate the silicon surface but also to selectively enable hole or electron transport across this “tunnel layer,” sandwiched between the overlying conductive a-Si:H layer and the crystalline silicon wafer. In this application, the contact-related recombination losses with the intrinsic/doped a-Si:H stack is significantly lower than utilizing the doped a-Si:H layers alone on the crystalline silicon wafers [5], hence establishing contact passivation for the former case. It can then be generalized that contact passivation can be established by deploying ultrathin passivating (and even in principal insulating, if thick) tunnel layers capped with a highly doped capping layer material with a suitable doping polarity or work function to form either hole-selective or electron-selective passivated contacts. Some examples of high/low work function capping layer materials such as transition metal oxides ( $WO_x$ ,  $VO_x$ , etc.) and doped organic materials had been reported [4, 8].

Some prominent examples of single-junction silicon wafer-based high-efficiency ( $\geq 25\%$ ) solar cell concepts which adopt contact passivation include the amorphous silicon heterojunction interdigitated back contact (IBC) solar cell by Kaneka (26.6%) [9], the tunnel layer passivated interdigitated back contact (IBC) solar cell by SunPower (25.2%) [10], the polysilicon on oxide (POLO) passivated contact interdigitated back contact (IBC) solar cell by ISFH (26.1%) [11], and the conventionally front- and rear-contacted tunnel layer passivated contact solar cell (TOPCon) by the Fraunhofer ISE team (25.7%) [12]. The excellent performance of the TOPCon cell (despite being conventional front- and rear-contacted, instead of

being contacted in an all-back-contact configuration) can be attributed to the highly effective and simplified full-area rear-side passivating contact scheme, which inserts an electron-selective tunnel layer passivated rear-side contact between the wafer and the full-area rear-side contact of the solar cell, comprising a wet-chemically formed silicon oxide tunnel layer (wet-SiO<sub>x</sub>) and a highly n-doped polysilicon capping layer. This achieves both excellent interface passivation toward the silicon wafer and a highly selective collection of excess electron charge carriers. Although this work was established on a small-sized (4 cm<sup>2</sup>) float-zone n-type silicon wafer, adopting a conventional front-side selective emitter, photolithography processes, and evaporated contacts, it has set the stage for immense research interests such as those reported in Refs. [12–26]. Contact passivation presents a clear advantage over the popular passivated emitter rear contact (PERC) solar cell concept by UNSW [27], which is currently a large scale adopted by the industry (as of Jan. 2019), as an even higher solar cell efficiency can be reached (i.e., by directly passivating the metal solar cell contacts instead of “only” reducing the metal contact area fraction).

An ideal tunnel layer, suited for contact passivation, (i) exhibits a tunneling relevant thickness (i.e., <2 nm) [14], (ii) exhibits excellent interface passivation toward the crystalline silicon wafer [28, 29], and (iii) contributes only minimally to the total contact resistance of the solar cell (in the order of maximal 1 Ω cm<sup>2</sup>) [30]. Furthermore, an ideal capping layer, suited for contact passivation, should be either (i) highly doped or (ii) exhibit a high/low work function [31] in order to ensure selective excess charge carrier extraction.

The already proven success on electron-selective passivated contacts is also generating huge interest and research activities on hole-selective passivated contacts now. Pertaining to the feasibility studies of different tunnel layer candidates for hole-extracting passivated contacts, most previous reports had focused on using silicon-based oxides formed via either wet-chemical approaches (wet-SiO<sub>x</sub>) or UV/ozone photo-oxidation (ozone-SiO<sub>x</sub>) approaches. In our published works [28, 29, 32–34], a comprehensive evaluation of passivation quality and interface properties of silicon-based oxides (SiO<sub>x</sub>) and atomic layer-deposited aluminum oxides (ALD-AlO<sub>x</sub>) had revealed a larger potential for ALD-AlO<sub>x</sub> to be integrated in hole-selective passivated contacts as compared to the commonly used wet-SiO<sub>x</sub> or ozone-SiO<sub>x</sub>. This stems from a significantly higher negative fixed interface charge density (~1 order of magnitude higher at  $-6 \times 10^{12} \text{ cm}^{-2}$ ) even at a tunneling relevant thickness (just a few ALD cycles) while maintaining a relatively low interface defect density ( $D_{it}$ ) of  $\sim 2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , which is comparable to the  $D_{it}$  of SiO<sub>x</sub>-based tunnel layers. The high negative fixed interface charges of the ALD-AlO<sub>x</sub> tunnel layer will accumulate holes at the c-Si interface, which will simultaneously enhance hole extraction probability and reduce surface recombination rates due to an efficient field-effect passivation in addition to the chemical passivation at the interface, as evident from the higher measured effective carrier lifetime (two orders of magnitude higher) than the passivation by either wet-SiO<sub>x</sub> or ozone-SiO<sub>x</sub> alone on symmetrically tunnel layer passivated n-type Cz wafers in our previous work [28]. These findings were consistent with literature for much thicker AlO<sub>x</sub> layers [35–39]. For hole-extracting capping layer materials, various candidates had been suggested, which includes highly p-doped polysilicon, transition metal oxide films with high work function such as molybdenum oxide (MoO<sub>x</sub>) [40–45], tungsten oxide (WO<sub>x</sub>), vanadium oxide (V<sub>2</sub>O<sub>5</sub>), cuprous oxide (Cu<sub>2</sub>O) [46], or alternatively organic polymers, such as poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) [47–49], among others. It is worthy to highlight that the transition metal oxide films exhibit a tunable work function between 4.7 and 7 eV [50, 51] by an appropriate combination of materials, while organic

polymers can also exhibit a tunable work function from 3.0 to 5.8 eV by chemical modification [8]. As an example, Zielke et al. [52] has demonstrated a cell efficiency of 18.3 and 20.6% for both n-type silicon and p-type silicon solar cells, respectively, which deploys a rear-side tunnel layer passivated hole-extracting metal contact using their specifically adapted organic PEDOT:PSS blend as capping layer. Such findings could open up new opportunities for potentially low-cost novel material integration for high-efficiency solar cell concepts in the future.

Regarding contact passivation, however, it is to be noted that in most of these reports, the carrier-selective passivated contacts were mostly deployed at the rear side of the solar cell, while the front side composes of a conventionally diffused silicon surface followed by the standard anti-reflection coatings and screen-printed fire-through metal contacts. Since the rear-side deployed passivated contacts can achieve an excellently low contact recombination loss, instinctively the next focus will be to reduce the contact recombination loss at the front side as well in order to improve device performance. With varying degrees of success using either electron-selective or hole-selective passivated contacts in a standalone configuration, the question arises on the feasibility to integrate both electron-selective and hole-selective passivated contacts together in a typical silicon solar cell architecture. Regardless of the technological advances, the fundamental driving factors toward industry adoption will still be the same as outlined earlier (i.e., cost-effectiveness of the material and processes, manufacturing scalability, device performance, and product stability). Hence, it is of keen interest in this paper to evaluate the feasibility of combining our optimized electron-selective and hole-selective passivated contacts obtained via industrial relevant processes onto an otherwise conventional front and rear screen-printed silicon solar cells and comparing that to solar cells with only a rear-side passivated contact scheme.

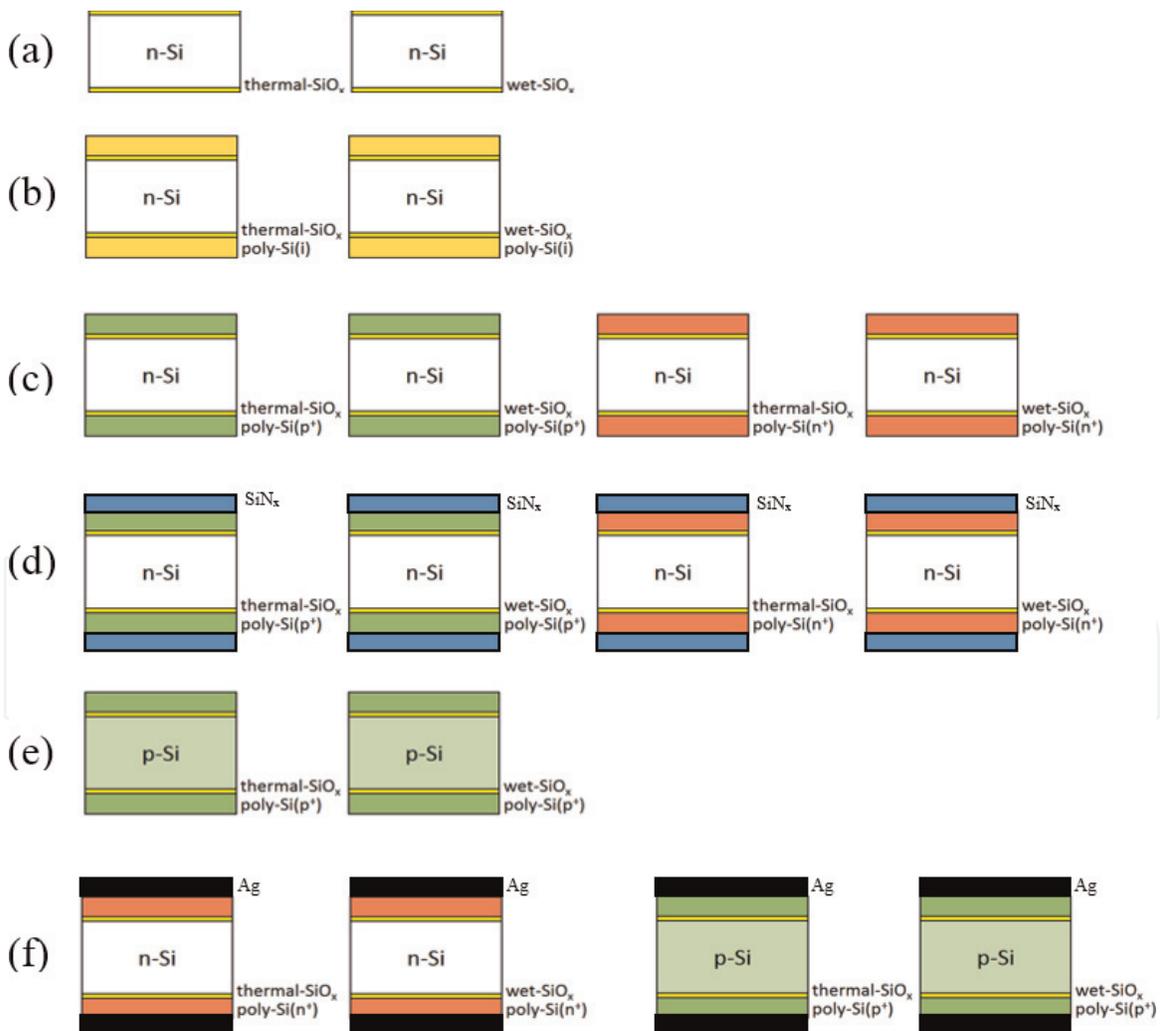
In this work, we will investigate “conventional”  $\text{SiO}_x$ /poly-Si passivated contacts to be deployed on both sides of the solar cell, instead of only being deployed rear side. Using different lifetime test structures and solar cell structures, the following topics are investigated: (i) the influence of the tunnel oxide choice on the passivation quality, comparing wet-chemically formed oxides (wet- $\text{SiO}_x$ ), UV photo-oxidation-formed ozone oxides (ozone- $\text{SiO}_x$ ), and in situ thermal oxidation-formed oxides (thermal- $\text{SiO}_x$ ); (ii) the impact on the contact passivation quality after doped silicon capping layers were applied upon the tunnel oxide layers on the same lifetime test structures (formed via tube diffusion doping of low-pressure chemical vapor deposition (LPCVD) of intrinsic polysilicon layers, to serve as either electron-selective or hole-selective capping layers); (iii) the influence of the surface conditions on the passivation quality by both types of electron- or hole-selective passivated contacts; (iv) the integration of the optimal passivated contacts onto a practical double-sided passivated contact solar cell structure and studies on the resulting passivation quality, both prior to and after subsequent anti-reflection passivation layers (i.e.,  $\text{SiN}_x$  layers) were applied; (v) the influence of the capping layer thickness on the absorbable cell current and various parasitic absorption losses via numerical analysis (SunSolve™) and our experimental approaches to realize ultrathin poly-Si capping layers; and (vi) the ability to apply screen-printed metal contacts on the developed electron-selective and hole-selective passivated contacts.

In addition, from the measured passivation quality results on lifetime test structures, a numerical calculation of the practical solar cell efficiency potential adopting both of our developed electron-selective and hole-selective passivated contacts was performed by utilizing the measured saturation current density  $J_0$  and the measured contact resistance  $R_c$  from our investigated tunnel layer passivated contact test structures. This work demonstrates the feasibility and attractiveness of using industrial relevant processes to develop device quality tunnel oxide/doped

polysilicon passivated contacts for effective contact passivation on both textured and planar silicon surfaces. A major highlight of this work is the demonstration of a practical solar cell efficiency potential approaching 24% on a large area (6-inch wafer), by deploying the in-house developed passivated contact layers on both sides of an otherwise conventionally processed silicon solar cells with industrial screen-printed contacts.

## 2. Experimental details

Firstly, the in-house development of device quality passivated contacts based on wet-SiO<sub>x</sub>/poly-Si(doped), ozone-SiO<sub>x</sub>/poly-Si(doped), or in situ thermal-SiO<sub>x</sub>/poly-Si(doped) stack was established using simple planar symmetrical lifetime test structures as sketched in **Figure 1**. Such structures are convenient for assessing (i) the resulting tunnel layer/doped capping layer stack thickness; (ii) the passivation quality, attributing from the passivated contacts alone (i.e., determining minority carrier lifetime  $\tau_{\text{eff}}$ , reverse saturation current density  $J_0$ , and implied open-circuit voltage  $iV_{\text{OC}}$ ); and (iii) the tunneling resistance (i.e., determining the contact resistance  $R_c$ ). Starting from bare diamond-wire cut Cz silicon wafers (NorSun, 190  $\mu\text{m}$  thick, and

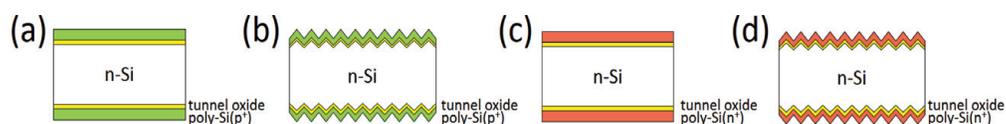


**Figure 1.** Schematic of the (a-e) symmetrical lifetime and (f) contact resistance test structures utilized for assessing/optimizing the passivation quality and minimizing the contact resistance of both, electron-selective and hole-selective passivated contacts, developed on either a wet-SiO<sub>x</sub>, ozone-SiO<sub>x</sub> or an in-situ thermal-SiO<sub>x</sub> tunnel layer. Using the sketched symmetrically passivated contact test structures, the developed SiO<sub>x</sub>/poly-Si passivated contacts were characterized in terms of their passivation quality, doping profiles, film uniformity and contact resistance.

wafer resistivity of  $3.4 \Omega \text{ cm}$ ), these wafers received a saw damage etch removal process, followed by a standard RCA and HF clean process. The next step is the deposition of the various tunnel oxide layers (see **Figure 1(a)**). For lifetime test samples that require the wet-SiO<sub>x</sub> tunnel layers, these samples were subjected to one more round of RCA2 process for 5 min (using deionized water, HCl, and H<sub>2</sub>O<sub>2</sub> in the volume ratio of 0.84:0.08:0.08) in order to form the wet-SiO<sub>x</sub> tunnel layer. Other selected lifetime test samples were deposited with a symmetrical ozone-SiO<sub>x</sub> (UVO-Cleaner® 42, Jelight Company Inc.). The samples planned for an in situ thermal-SiO<sub>x</sub> tunnel layer were processed using the low-pressure chemical vapor deposition (LPCVD) tool (TS-Series, Tempres) by flowing the oxidative gases prior to the deposition of the intrinsic poly-Si capping layers. Second, intrinsic poly-Si capping layers were deposited on top of all tunnel layers investigated, using LPCVD (TS-Series, Tempres) (see **Figure 1(b)**). These intrinsic poly-Si capped lifetime test structures were subsequently subjected to detailed doping optimization studies, using an industrial relevant high-throughput diffusion tool (Quantum, Tempres) to obtain device quality electron-selective and hole-selective passivated contacts (see **Figure 1(c)**). The increase in passivation quality after the deposition of an additional SiN<sub>x</sub> passivation layer was studied using test samples as sketched in **Figure 1(d)**. In order to assess the total contact resistance  $R_c$ , some selected samples as sketched in **Figure 1(c)** and **(e)** (now using a p-type wafer instead of an n-type wafer) were further symmetrically contacted by thermally evaporated silver (System Control Technologies), i.e., processing symmetric Ag/poly-Si(n<sup>+</sup>)/tunnel-oxide/n-Si-wafer/tunnel-oxide/poly-Si(n<sup>+</sup>)/Ag samples to study electron extraction and Ag/poly-Si(p<sup>+</sup>)/tunnel-oxide/p-Si-wafer/tunnel-oxide/poly-Si(p<sup>+</sup>)/Ag samples to study hole extraction (see **Figure 1(f)**). In such samples, an ohmic straight-line dark I–V curve can be obtained, from which the contact resistance  $R_c$  on each side can be determined (after subtracting the resistance contribution from the silicon bulk).

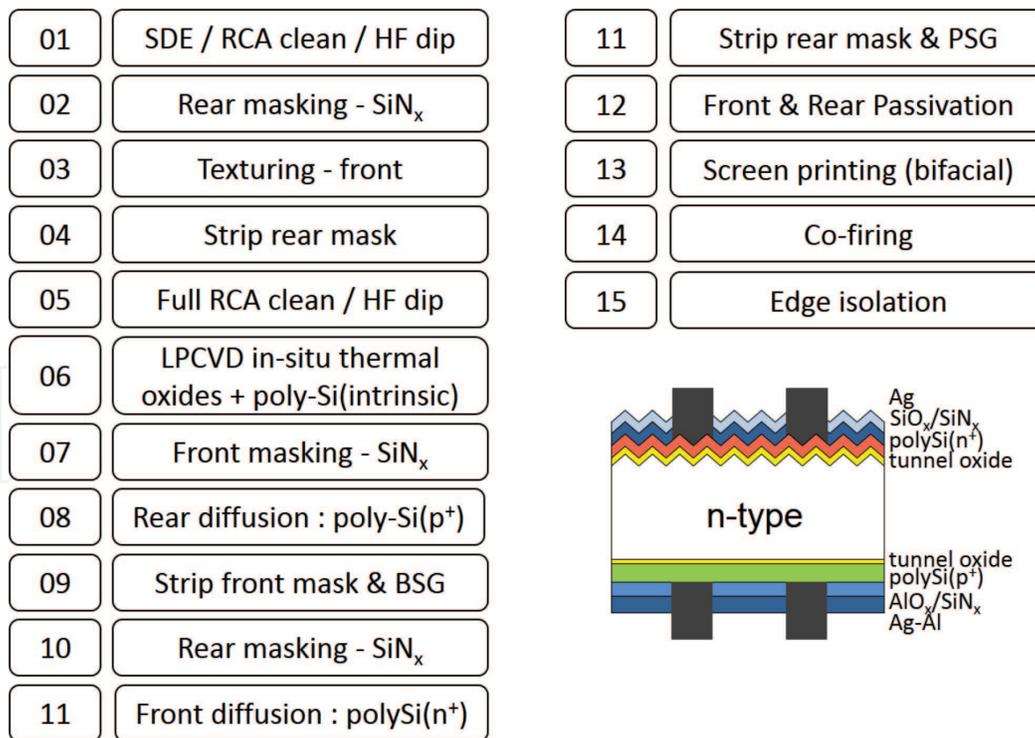
Next, considering that typical silicon solar cells are either single-sided textured or symmetrically textured, it is relevant to explore the passivation quality when these developed passivated contacts are deployed on textured surfaces as well, while comparing that to planar references, as sketched in **Figure 2**. The objective is to identify the suitability of our developed electron-selective and hole-selective passivated contacts for textured surfaces and to determine the optimum configuration for a silicon solar cell considering contact passivation for both the front and rear surfaces.

It will be shown in later sections that the optimum double-sided passivated contact scheme can be realized by deploying the electron-selective passivated contacts (i.e., poly-Si(n<sup>+</sup>)/tunnel oxide stacks) on the front textured surface while deploying the hole-selective passivated contacts (i.e., poly-Si(p<sup>+</sup>)/tunnel oxide stacks) on the rear planar surface. Subsequently, the silicon solar cell precursors with the optimum double-sided passivated contact scheme were experimentally realized according to the process flow shown in **Figure 3** and characterized in terms of the passivation quality and doping profile, both prior to and after the standard anti-reflection/passivation dielectric coatings were deposited (i.e., step. 11 and 12, respectively) via microwave PECVD (MAiA, Meyer Burger), while comparing that to the symmetrical lifetime test structures. Selected samples were then subjected to



**Figure 2.**

*Comparison of the passivation quality by both (a, b) hole-selective and (c, d) electron-selective passivated contacts on both planar and textured lifetime test structures.*



**Figure 3.** Potential process flow for a silicon solar cell adopting double-sided passivated contacts and bifacial metal contacts.

a conventional full-area or bifacial screen printing process using commercially available fire-through paste to contact the electron-selective and hole-selective passivated contacts, through a high-temperature co-firing process at  $\sim 740^{\circ}\text{C}$  in a fast-firing furnace (BTU) for 1 min. It is to be noted that the time of 1 min accounts for the total time spent within the fast-firing furnace, moving the intended sample across five temperature zones with increasing temperatures, with an estimated time of 5 seconds within the final peak temperature zone. As a final step, an edge isolation is carried out on the finished solar cell via a nanosecond laser process (ILS500LT, InnoLas), followed by electrical characterization.

One potential issue with replacing the conventional diffused regions with carrier-selective passivated contacts (such as the poly-Si(doped)/tunnel oxide stack in this work) is the presence of parasitic absorption, similar to the case of transparent conductive oxides or amorphous silicon layers in a heterojunction silicon wafer solar cell concept. Hence, there is an optimization potential toward simultaneously achieving excellent passivation quality of both textured and planar surfaces while minimizing the doped poly-Si capping layer thickness as much as possible in order to minimize the parasitic absorption issue.

Thus, it has been tested experimentally how thin our developed contact passivation layers can become while maintaining their excellent passivation quality. This has been realized by two different experimental approaches: (1) applying etch-back technology, thereby thinning down the already optimized thick layers, and (2) diffusion re-optimization for ultrathin LPCVD of intrinsic poly-Si layers.

To provide more insights into the influence of the doped capping layer thickness on the maximum absorbable current density  $J_{\text{absorbed, cell}}$  attainable in a silicon solar cell, the simulation program SunSolve™, available on PV Lighthouse [53], was utilized. The SunSolve™ calculator combines Monte Carlo ray tracing with thin-film optics to calculate the maximum potential photogeneration current in the solar cell for the standard AM1.5G spectrum, as well as the corresponding optical losses occurring elsewhere (i.e., front-reflected, front-escaped, rear-escaped, parasitic

absorption, edge absorption). Using SunSolve™, we provide a quantitative discussion of the influence of our doped poly-Si capping layer thickness on  $J_{\text{absorbed, cell}}$  and  $J_{\text{absorbed, parasitic}}$  which will ultimately affect the solar cell performance.

Finally, it is of keen interest to predict the impact of combining both of our developed electron-selective and hole-selective passivated contacts on the rear (and front side) of a silicon solar cell. To do this, we utilized Brendel's model [54] to predict the efficiency potential of a passivated contact and further enhanced the model to explicitly consider front-side conventional screen-printed contacts. This is done by additionally considering the combined front-side saturation current density  $J_{0, \text{front}}$  (contributed by both the front-side metal-contacted regions and metal-passivated regions) and the front-side contact resistance  $R_{c, \text{front}}$  of the screen-printed contacts. Thus, practical iso-efficiency contour plots (under a variation of the  $J_{0, \text{rear}}$  and  $R_{c, \text{rear}}$  values of the rear-side passivated contact) can be obtained, allowing us to predict a practical solar cell efficiency potential, given known  $J_{0, \text{front}}$ ,  $R_{c, \text{front}}$ ,  $J_{0, \text{rear}}$ ,  $R_{c, \text{rear}}$  values. Subsequently, our individually measured  $J_{0, \text{rear}}$  and  $R_{c, \text{rear}}$  values for our investigated passivated contacts in this work were inserted into this iso-efficiency contour plot, and a realistic prediction of the solar cell efficiency potential can be realized for both single-sided passivated contact scheme and double-sided passivated contact schemes.

Last but not least, the feasibility to contact our developed ultrathin contact passivation layers by an industrially suited method (i.e., aiming at conventional screen printing) is investigated, and the remaining issues, still to be solved in order to reach this goal, are addressed.

Concerning characterization metrology, we used the following tools: The average thickness and uniformity of the tunnel layers/doped poly-Si capping layers were determined by ellipsometry (SE-2000, Semilab) over a 9-point mapping measurement. The passivation quality was determined from the injection-dependent effective carrier lifetime measurements using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Consulting) operated in both transient and quasi steady-state modes (QSSPC), which adopts an intrinsic carrier concentration of  $8.6 \times 10^9 \text{ cm}^{-3}$  in the calculation of the saturation current densities. To provide further insights at the tunnel layer/silicon interface, the fixed interface charge density  $Q_f$  and the interface defect density distribution  $D_{\text{it}}(E)$  were determined using time-resolved contactless corona charge—Kelvin probe measurements (PV-2000, Semilab). Considering our ultrathin dielectrics, and its high potential for charge leakage, PV-2000 utilizes a “Self-Adjusting SteadyState Technique (SASS)” which takes into consideration the SASS voltage obtained using both positive and negative corona charges in order to calculate a leakage index (equivalently a correction factor) which accounts for the dielectric leakage when present and applicable to both ultrathin and thicker dielectrics, in order to produce a reliable representation of the  $Q_f$  and  $D_{\text{it}}(E)$  values across different samples. The film structure of the doped silicon capping layer was determined via Raman spectroscopy (SE-2000, Semilab). The light and dark I–V measurements were performed on an LED-based AAA-calibrated I–V tester (Sinus220, Wavelabs).

### 3. Results and discussion

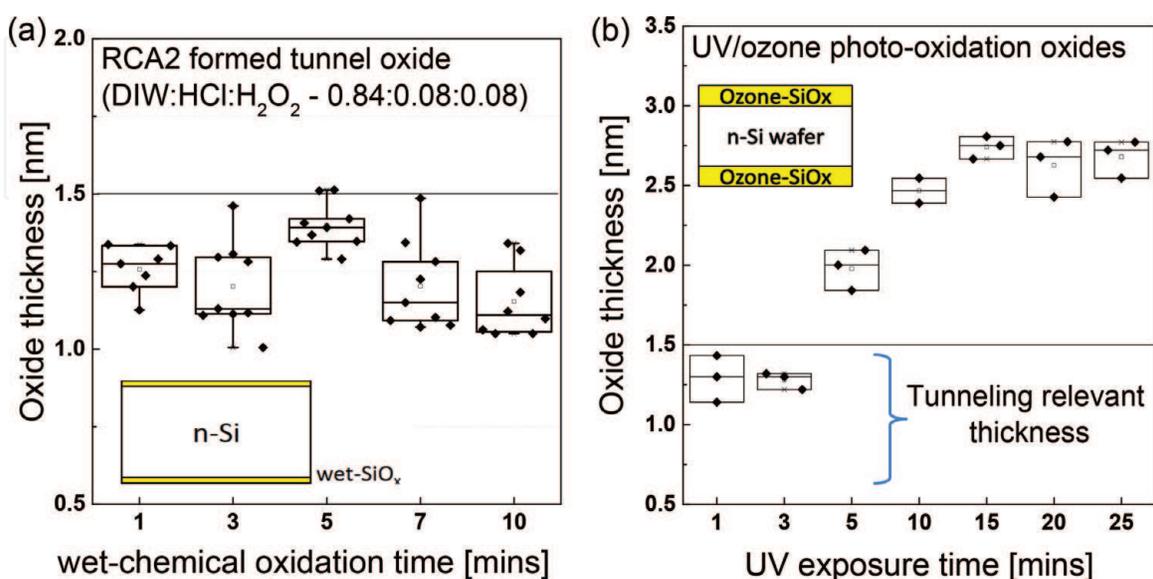
#### 3.1 Screening of tunnel oxide layers for contact passivation

As mentioned earlier, the development and optimization of contact passivation layer stacks were initiated on symmetrical planar lifetime test structures as sketched in **Figure 1**. Prior to deposition of the doped capping layer, various tunnel oxide candidates were screened (i.e., wet-SiO<sub>x</sub>, ozone-SiO<sub>x</sub>, and thermal-SiO<sub>x</sub>) in terms of

their deposition techniques as well as the time required to get tunneling relevant thicknesses. Starting from our wet-chemically formed oxides (wet-SiO<sub>x</sub>) via the standard RCA2 solution, **Figure 4(a)** shows that the resulting wet-SiO<sub>x</sub> tunnel oxide thickness is independent of the oxidation time utilized (1–10 min) and is well within the tunneling relevant thickness regime (~1.2–1.5 nm). These wet-SiO<sub>x</sub> tunnel oxide layers were also found to exhibit a highly leaky interface toward the silicon bulk, as attempts to determine the wet-SiO<sub>x</sub>/c-Si interface properties  $Q_f$  and  $D_{it}(E)$  were unsuccessful due to its inability to retain the deposited corona charges. Nonetheless, this is likely to be beneficial for the subsequent charge collection process, since the charge carriers to be collected can easily tunnel through such an oxide layer. It is also worthy to note that these symmetrical planar lifetime structures with only a wet-SiO<sub>x</sub> tunnel oxide do not passivate well ( $\tau_{eff} \sim 4 \mu s$ ) and are only effective when subsequently coupled with a highly doped capping layer to form a wet-SiO<sub>x</sub>/poly-Si(doped) passivated contact scheme, as will be shown in the coming sections.

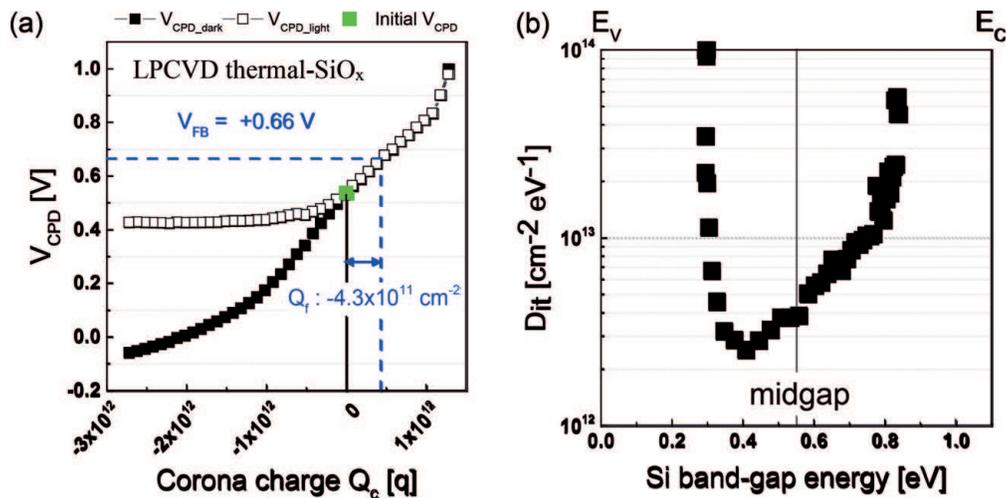
In contrast, for the investigated UV/ozone photo-oxidation-formed ozone-SiO<sub>x</sub> tunnel oxides, **Figure 4(b)** shows that the resulting ozone-SiO<sub>x</sub> layer thickness shows a time dependence of the photo-oxidation time, which increases from ~1.3 nm for an exposure time of 3 min to ~2.5 nm for 10 min. Beyond 10 min, the thickness of the ozone-SiO<sub>x</sub> layer saturates at ~2.7 nm (i.e., surface reaction limited). Hence, considering the need for tunneling relevant applications (<1.5 nm), the UV/ozone exposure time should be limited to  $\leq 3$  min. Similar to the wet-SiO<sub>x</sub> case, the ozone-SiO<sub>x</sub> tunnel oxides were also found to be leaky in the as-deposited state, evident from its inability to measure  $Q_f$  and  $D_{it}(E)$ . In terms of passivation, symmetrically ozone-SiO<sub>x</sub> passivated planar lifetime samples also do not passivate well ( $\tau_{eff} \sim 2 \mu s$ ) and should be coupled with a highly doped capping layer to form an effective contact passivation scheme as well.

Finally, our investigated in situ thermal oxides were also found to exhibit a deposition time dependence on the measured oxide thickness, in which an in situ oxidation time of 30 secs at 570°C was already sufficient to achieve a tunneling relevant thickness of 1.0 to 1.2 nm. At higher deposition timings (e.g., 5 min), the thickness increases to ~13 nm which is not suitable for tunneling relevant applications.



**Figure 4.**  
 (a) Comparison of the wet-chemical (RCA2) oxidation time on the measured wet-SiO<sub>x</sub> tunnel oxide thickness. The wet-SiO<sub>x</sub> thickness does not exhibit a time dependence (1–10 min) and has a thickness range of ~1.2–1.5 nm, relevant for device integration. (b) For ozone-SiO<sub>x</sub>, the UV exposure time directly affects the ozone-SiO<sub>x</sub> tunnel oxide thickness, with a recommended exposure time of 3 min to achieve tunneling relevant thickness.

Correspondingly, an in situ thermal oxide growth rate of  $\sim 2.4\text{--}2.6$  nm/min can be expected. Interestingly, in contrast to the wet-SiO<sub>x</sub> and ozone-SiO<sub>x</sub> tunnel layers, our as-deposited thermal-SiO<sub>x</sub> tunnel oxides were able to retain the deposited charges from the contactless corona charge—Kelvin probe measurements, allowing the fixed interface charge density and the interface defect density distribution to be determined (see **Figure 5**). At the first glance, this already suggests that the in situ thermal-SiO<sub>x</sub> exhibits a higher film quality (i.e., non-leaky) than both wet-SiO<sub>x</sub> and ozone-SiO<sub>x</sub>. It is also likely that the thermal-SiO<sub>x</sub> film structure is more dense, which can be beneficial when coupled with a highly doped silicon capping layer, which could reduce the out-diffusion of dopants into the c-Si bulk. **Table 1** summarizes the measured  $Q_f$  and  $D_{it}$  for our investigated tunnel oxides (wet-SiO<sub>x</sub>, ozone-SiO<sub>x</sub>, thermal-SiO<sub>x</sub>) and compares that to literature-reported values. As plotted in **Figure 5**, and summarized in **Table 1**, the as-deposited in situ thermal-SiO<sub>x</sub> ( $\sim 1.2$  nm) in this work exhibited a  $Q_f$  of  $-4.3 \times 10^{11}$  cm<sup>-2</sup> and a minimum  $D_{it}$  of  $\sim 2.5 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>. The energy distribution of the interface defect density  $D_{it}(E)$  as a function of the silicon band-gap energy for our in situ thermal-SiO<sub>x</sub> layers is plotted in **Figure 5(b)**, showing a minimum  $D_{it}$  closer to the valence band, instead of the midgap position. This could be due to the increase of surface micro-roughness from the processing conditions, leading to a higher density of dangling bond defects in the higher part of the silicon energy



**Figure 5.** The *in-situ* thermal silicon oxides deposited within the LPCVD process prior to the intrinsic poly-Si layers exhibited (a) a negative fixed interface charge density  $Q_f$  of  $-4.3 \times 10^{11}$  cm<sup>-2</sup> and (b) a minimum interface defect density  $D_{it(min)}$  of  $\sim 2.5 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>.

Tunnel oxide	Thickness (nm)	$Q_f$ (cm <sup>-2</sup> )	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> )	References
Thermal-SiO <sub>x</sub>	$\sim 1.2$	$-4.30 \times 10^{11}$	$2.50 \times 10^{12}$	This work
Wet-SiO <sub>x</sub>	$\sim 1.5$	Not measurable	Not measurable	This work
Ozone-SiO <sub>x</sub>	$\sim 1.3$	Not measurable	Not measurable	This work
Thermal-SiO <sub>x</sub>	$\sim 50\text{--}240$	$+3.00 \times 10^{11}$	$10^{10} \sim 7 \times 10^{11}$	[56–59]
Wet-SiO <sub>x</sub>	$\sim 1\text{--}2$	$+1.28 \times 10^{12}$	$5.17 \times 10^{12}$	[57, 60–64]
Ozone-SiO <sub>x</sub>	$\sim 1\text{--}2$	No data	$1.00 \times 10^{13}$	[55]
ALD-AlO <sub>x</sub>	$\sim 1.5$	$-6.10 \times 10^{12}$	$2.70 \times 10^{12}$	[28]

**Table 1.**

Comparison of the fixed interface charge density  $Q_f$  and the interface defect density distribution  $D_{it}(E)$  for different investigated tunnel oxides (thermal-SiO<sub>x</sub>, wet-SiO<sub>x</sub>, ozone-SiO<sub>x</sub>) in this work as compared to literature.

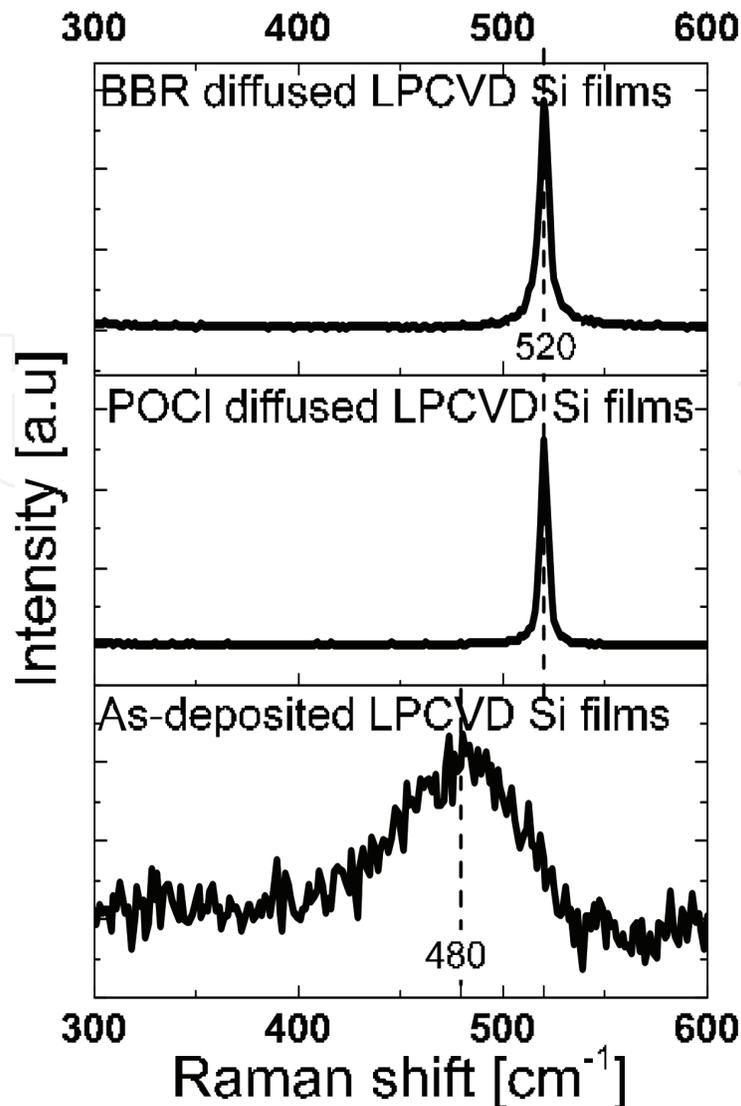
gap, similar to the observation by Angermann et al. [55] who observed a skewing toward the conduction band when p-type Si substrates are utilized.

As compared to other thermally grown silicon oxides [56–59] which exhibited significantly lower  $D_{it}$  values ( $\sim 1$ – $2$  orders), their film thickness was however also significantly higher at  $\sim 50$ – $240$  nm, making it inappropriate for tunnel layer applications. On the other hand, the wet-SiO<sub>x</sub> and ozone-SiO<sub>x</sub> tunnel oxides reported in Refs. [55, 57, 60–64] do exhibit measurable  $Q_f$  and  $D_{it}$  values, unlike our investigated samples, which can be attributed to the deposition method and the post-deposition annealing conditions. Our wet-SiO<sub>x</sub> and ozone-SiO<sub>x</sub> tunnel oxides were unable to retain the deposited corona charges due to its leaky interface, which nonetheless could be beneficial for the purpose of tunneling carrier transport. Another noteworthy tunnel oxide candidate is atomic layer deposition (ALD) of aluminum oxide (AlO<sub>x</sub>), whereby in one of our earlier publications [28], we experimentally realized ultrathin ALD-AlO<sub>x</sub> films in the tunneling regime ( $\sim 1.5$  nm) which is capable of exhibiting a significantly higher negative  $Q_f$  of  $-6 \times 10^{12}$  cm<sup>-2</sup> and a  $D_{it}$  of  $\sim 2.7 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>. This resulted in a  $\sim 110$ -fold increase in the initial passivation quality prior to the doped capping layers as compared to a conventional wet-SiO<sub>x</sub> tunnel oxide layer using our test structures (i.e., from 2 to 218  $\mu$ s) [28]. This finding positions ultrathin ALD-AlO<sub>x</sub> as a highly attractive tunnel oxide candidate for hole-extracting selective contacts. In contrast, although the  $D_{it}$  values of our in situ thermal-SiO<sub>x</sub> and ALD-AlO<sub>x</sub> films are comparable, the thermal-SiO<sub>x</sub> in this work exhibited one order lower negative fixed interface charge density which do suggest a reduced field-effect passivation and overall surface passivation prior to the doped capping layers, which is observed experimentally as well ( $\tau_{eff} \sim 4.7$   $\mu$ s). Nevertheless, this positions thermal-SiO<sub>x</sub> as a tunnel oxide candidate suitable for both electron-extracting and hole-extracting selective contacts.

### 3.2 Screening LPCVD poly-Si capping layers for contact passivation

As compared to the TOPCon approach by the Fraunhofer ISE's team, which deposited doped amorphous silicon films followed by a suitable annealing condition and hydrogenation process to convert the highly doped amorphous silicon to highly doped polysilicon capping layers, we implement an alternative approach by first depositing intrinsic silicon films via the LPCVD approach, followed by either a phosphorus or boron diffusion process to convert it to a highly doped poly-Si(n<sup>+</sup>) or poly-Si(p<sup>+</sup>) capping layer, respectively. The optimization goal is to incorporate as much active dopants within the poly-Si layers as possible while reducing or avoiding the out-diffusion of dopants into the c-Si wafer bulk, which will increase the surface recombination rates and reduce the device performance, as also reported in Ref. [65].

As a start, Raman spectroscopy was utilized to monitor the structural evolution of our in-house deposited silicon capping layers, both in the as-deposited intrinsic case and after the optimal diffusion process (boron or phosphorus doped). **Figure 6** shows that our LPCVD as-deposited intrinsic silicon films were amorphous in film structure, evident by a single Raman peak centered at a Raman shift of  $\sim 480$  cm<sup>-1</sup> [66]. Nonetheless, upon either a boron diffusion process or a phosphorus diffusion process, which takes place at temperatures between 850 and 950°C, these doped silicon films fully crystallize as evident by a single Raman peak centered at a Raman shift of  $\sim 520.5$  cm<sup>-1</sup> with a full width at half maximum (FWHM) of 5.3 and 4.0 cm<sup>-1</sup>, respectively. These findings were comparable to our crystalline silicon wafer reference (Raman shift centered at  $\sim 520.6$  cm<sup>-1</sup> and a FWHM of 3.5 cm<sup>-1</sup>). The slightly higher FWHM measured for our doped silicon films indicated a marginally higher structural disorder than a perfect crystalline silicon wafer bulk which



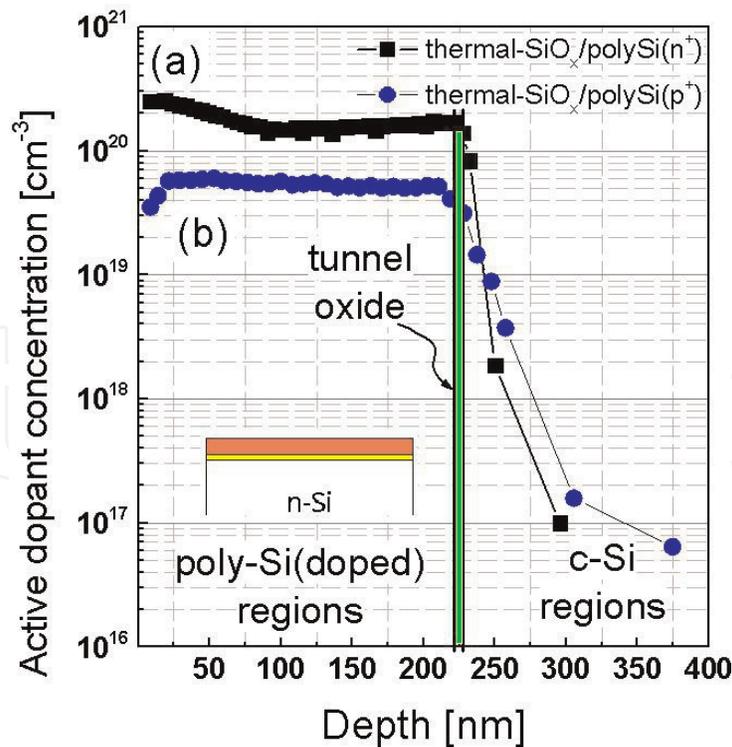
**Figure 6.**

*Raman spectra for our in-house LPCVD of silicon films ( $\sim 250$  nm), comparing the film crystallinity in the as-deposited state, post- $\text{POCl}_3$  diffusion process, and post- $\text{BBR}_3$  diffusion process.*

is not too surprising, given the high quantities of dopants ( $10^{19}$ – $10^{20}$   $\text{cm}^{-3}$ ) incorporated in the former.

The corresponding dopant profile within these highly doped silicon capping layers can be extracted from ECV measurements as shown in **Figure 7**. After an optimized diffusion doping process to convert the thermal- $\text{SiO}_x/\text{a-Si}$  (intrinsic) capping layer stack toward either an electron-selective passivated contact (i.e., thermal- $\text{SiO}_x/\text{poly-Si}(n^+)$  stack) or a hole-selective passivated contact (i.e., thermal- $\text{SiO}_x/\text{poly-Si}(p^+)$  stack), the ECV measurements revealed a peak doping concentration within the poly- $\text{Si}(n^+)$  and poly- $\text{Si}(p^+)$  capping layers as  $\sim 1.5 \times 10^{20}$  and  $\sim 5 \times 10^{19}$   $\text{cm}^{-3}$ , respectively.

The tunnel oxide in the passivated contact stack not only serves as passivation/tunneling purposes, but it also likely serves as a blocking layer to reduce the out-diffusion of dopants from the highly doped silicon capping layer into the crystalline silicon wafer bulk. The lower active dopant concentration within the poly- $\text{Si}(p^+)$  layer can be partially attributed to the lower doping efficiency of boron atoms than phosphorus atoms [67] based on the theoretical prediction of impurity formation energies and partially attributed to the higher diffusivity of the boron dopants [68] into the silicon bulk which resulted in a deeper boron-diffused junction (see **Figure 7**). Similar to other reports [65], we also observed experimentally that it is preferable to concentrate all the dopants within the poly-Si layers, as the



**Figure 7.**

ECV profiles for both (a) electron-selective passivated contacts comprising thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) stacks and (b) hole-selective passivated contacts comprising thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) stacks. The electron-selective passivated contacts exhibited a higher peak doping concentration than the hole-selective counterpart by a factor of ~2 times. Poly-Si(p<sup>+</sup>) layers also exhibited a higher out-diffusion of dopants into the c-Si bulk than the poly-Si(n<sup>+</sup>) layers, which was found to limit the potentially achievable implied-V<sub>OC</sub> values (see Table 3).

out-diffusion of dopants is expected to lead to increased surface recombination rates and a corresponding drop in the overall passivation quality as well.

Table 2 summarizes our measured passivation quality results on planar symmetrical lifetime test structures with the optimized doped poly-Si(n<sup>+</sup>) capping layers on various investigated tunnel oxide candidates (i.e., wet-SiO<sub>x</sub>, ozone-SiO<sub>x</sub>, thermal-SiO<sub>x</sub>). Table 2 shows that using planar symmetrical lifetime test structures, our wet-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) and ozone-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated samples were exhibiting implied-V<sub>OC</sub> values of ~719 mV and J<sub>0</sub> of ~6–9 fA cm<sup>-2</sup>, while the thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contact stack exhibited an even higher implied-V<sub>OC</sub> values of 729 mV, despite a similar J<sub>0</sub> of ~9 fA cm<sup>-2</sup>. The enhanced implied-V<sub>OC</sub> values for thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivation stack were consistent with the earlier discussion on the tunnel oxides, in which a thermal-SiO<sub>x</sub> tunnel oxide is likely more effective in reducing the out-diffusion of phosphorus dopants from the poly-Si(n<sup>+</sup>) into the c-Si wafer bulk, hence providing better overall passivation quality (implied-V<sub>OC</sub> increases by ~10 mV).

Since a typical silicon solar cell would be further coated with suitable anti-reflection layers (such as SiN<sub>x</sub> or AlO<sub>x</sub>/SiN<sub>x</sub> stacks) prior to metallization, the influence of these layers on our symmetrical lifetime samples were evaluated as well, by capping the passivated contacts with an additional ~70-nm-thick SiN<sub>x</sub> films symmetrically and its resulting passivation quality evaluated. As summarized in Table 2, the measured passivation quality further improves with the additional SiN<sub>x</sub> capping layers upon all three investigated lifetime test structures with electron-selective passivated contacts. In particular, the thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>)/SiN<sub>x</sub>-capped lifetime structure exhibits high implied-V<sub>OC</sub> approaching 740 mV, with single-sided J<sub>0</sub> values down to ~2.5 fA cm<sup>-2</sup>, which is already on par with the best results from the Fraunhofer ISE team [69]. Concurrently, similar studies were conducted on lifetime test structures with hole-selective passivated contacts, and

selected results are highlighted in **Table 3**, which demonstrates the potential of our developed hole-selective contact passivation layers as well (i.e., thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) or ALD-AlO<sub>x</sub>/poly-Si(p<sup>+</sup>) stacks) with implied- $V_{OC}$  approaching 700 mV in the as-deposited state and a further enhancement to 713 mV with single-sided  $J_0$  values down to  $\sim 4$  fA/cm<sup>-2</sup> after applying symmetrical SiN<sub>x</sub> capping layers. This can be attributed to the hydrogenation process which occurs spontaneously during the deposition of the SiN<sub>x</sub> capping layer, which helps to reduce the interface defect densities and directly improves the passivation quality [70]. Comparing our results to the excellent results from the Fraunhofer ISE team [69], which adopts PECVD of p-doped a-Si:H layers followed by sintering and SiN<sub>x</sub> capping (with a high implied- $V_{OC}$  values up to 732 mV and single-sided  $J_0$  values  $< 1$  fA/cm<sup>-2</sup>), we do identify optimization potential for our LPCVD of intrinsic silicon capping layer and the associated boron diffusion optimization thereafter.

Tunnel layer/capping layer	Method	$iV_{OC}$ (mV)	Total $J_0$ (fA cm <sup>-2</sup> )	References
Wet-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )	PECVD Centrotherm	719 ± 2	–	FhG-ISE
Wet-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )	PECVD RF-MAiA	740	–	[69]
Wet-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )	LPCVD Tempress	719	~9	This work
Ozone-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )	LPCVD Tempress	719	~6	This work
Thermal-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )	LPCVD Tempress	729	~9	This work
After a hydrogenation/anti-reflection coating step by SiN <sub>x</sub>				
Wet-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )/SiN <sub>x</sub>	LPCVD + MAiA	730	~5	This work
Ozone-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )/SiN <sub>x</sub>	LPCVD + MAiA	732	~4	This work
Thermal-SiO <sub>x</sub> /poly-Si(n <sup>+</sup> )/ SiN <sub>x</sub>	LPCVD + MAiA	737	~5	This work

The thickness of the tunnel oxides/doped poly-Si layer/SiN<sub>x</sub> layer is  $\sim 1.5/250/80$  nm, respectively.

**Table 2.**

Comparison of the passivation quality of electron-selective passivated contacts on planar Cz n-Si symmetrical lifetime samples, both prior to and after the additional hydrogenation process step via the symmetrical addition of the SiN<sub>x</sub> capping layers.

Tunnel layer/capping layer	Method	$iV_{OC}$ (mV)	Total $J_0$ (fA cm <sup>-2</sup> )	References
Thermal-SiO <sub>x</sub> /poly-Si(p <sup>+</sup> )	LPCVD Tempress	698	37	This work
ALD-AlO <sub>x</sub> /poly-Si(p <sup>+</sup> )	ALD Solaytec + LPCVD	697	~26	This work
After a hydrogenation/anti-reflection coating step by SiN <sub>x</sub>				
Thermal-SiO <sub>x</sub> /poly-Si(p <sup>+</sup> )/ SiN <sub>x</sub>	LPCVD +MAiA	713	~8	This work
Thermal-SiO <sub>x</sub> /poly-Si(p <sup>+</sup> )/ SiN <sub>x</sub>	PECVD Centrotherm	732	~1	[69]

The thickness of the tunnel oxides/doped poly-Si layer/SiN<sub>x</sub> layer is  $\sim 1.5/250/80$  nm, respectively.

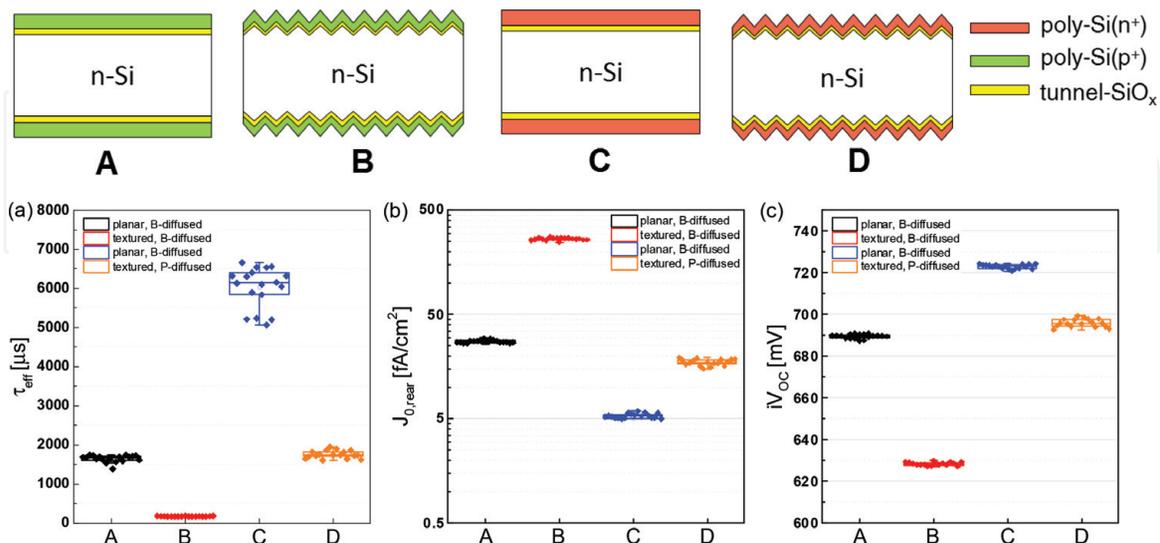
**Table 3.**

Comparison of the passivation quality of hole-selective passivated contacts on planar Cz n-Si symmetrical lifetime samples, both prior to and after the additional hydrogenation process step via the symmetrical addition of the SiN<sub>x</sub> capping layers.

### 3.3 Evaluation of developed contact passivation stacks on textured surfaces

Given the excellent passivation quality from our developed electron-selective and hole-selective passivated contacts on planar Cz silicon wafers, it is then of research and commercial interest to evaluate the performance of these layers on textured surfaces as well, to determine its viability for deployment on a conventional silicon solar cell structure which adopts a front-side textured surface and either a rear-side planar or textured surface. To evaluate that, the lifetime test structures as shown in **Figure 2** are utilized, featuring either symmetrical planar surfaces or symmetrical textured surfaces and symmetrically capped by either the electron-selective (thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>)) or hole-selective (thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>)) passivated contacts. The objective is to identify the suitability of our developed electron-selective and hole-selective passivated contacts for textured surfaces as well and to determine the optimum configuration for a silicon solar cell considering contact passivation for both the front and rear surfaces.

The highlight of this evaluation is plotted in **Figure 8**. Firstly, considering the influence of surface conditions on the passivation quality, it can be observed consistently from **Figure 8** and summarized in **Table 4** that both the electron-selective and hole-selective passivated contact stacks exhibited significantly better passivation quality on planar surfaces than on textured surfaces and which were consistent with the best results shown in **Tables 2** and **3**. Based on a batch average of 18 samples for each investigated lifetime test structure shown in **Figure 8**, the hole-selective passivated contacts on symmetrical planar lifetime test structures demonstrated an effective minority carrier lifetime  $\tau_{\text{eff}}$  of  $\sim 1650$   $\mu\text{s}$ , a single-sided  $J_{0, \text{rear}}$  of  $27.5$   $\text{fA cm}^{-2}$ , and an implied- $V_{\text{OC}}$  of  $689$  mV, which is a significant improvement over the textured case ( $\tau_{\text{eff}}$  of  $\sim 170$   $\mu\text{s}$ , single-sided  $J_{0, \text{rear}}$  of  $265$   $\text{fA cm}^{-2}$ , and implied- $V_{\text{OC}}$  of  $628$  mV). Effectively, upon deploying the hole-selective passivated contact on a textured surface, the  $\tau_{\text{eff}}$  and implied- $V_{\text{OC}}$  reduce by  $\sim 90$  and  $\sim 8.9\%$ , respectively. Similarly, while the electron-selective passivated contacts continued to exhibit excellent passivation quality on planar surfaces ( $\tau_{\text{eff}}$  of  $\sim 6030$   $\mu\text{s}$ , single-sided  $J_{0, \text{rear}}$  of  $5.4$   $\text{fA cm}^{-2}$ , implied- $V_{\text{OC}}$  of  $723$  mV), the passivation quality



**Figure 8.** Comparison of the passivation quality (i.e. (a) effective carrier lifetime at  $10^{15} \text{ cm}^{-3}$  injection level, (b) rear side  $J_0$  values and (c) implied- $V_{\text{OC}}$  values) by electron-selective (thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>)) and hole-selective (thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>)) passivated contacts on both symmetrical planar and symmetrical textured lifetime test structures. It can be observed that electron-selective passivated contacts are suitable for applications on both planar and textured surfaces (with implied- $V_{\text{OC}} > 720$  mV and  $> 695$  mV respectively), while the hole-selective passivated contacts are only suitable for planar surfaces at the moment (with implied- $V_{\text{OC}}$  approaching 700 mV, compare **Table 3**).

Structure	Surface	Pass. contact type	$\tau_{\text{eff}}$ ( $\mu\text{s}$ )	$J_{0, \text{rear}}$ ( $\text{fA cm}^{-2}$ )	$iV_{\text{OC}}$ (mV)
A	Planar	Hole-selective	1649	27.5	689
B	Textured	Hole-selective	170	265	628
C	Planar	Electron-selective	6030	5.4	723
D	Textured	Electron-selective	1756	17.4	696

**Table 4.**

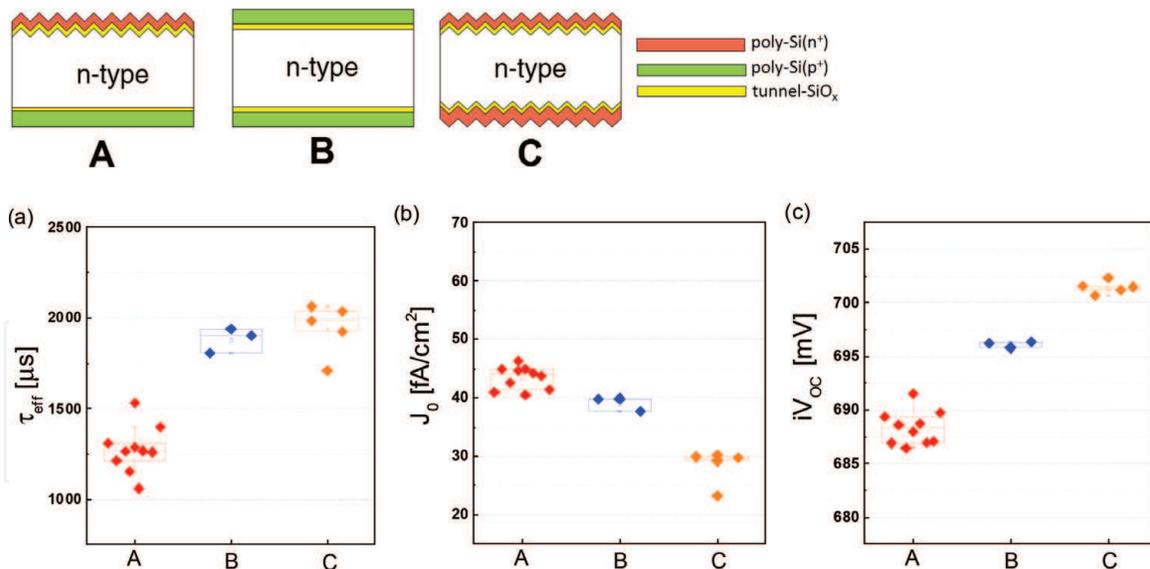
*Summary of the average measured passivation quality for both electron-selective and hole-selective passivated contacts deployed on both symmetrical planar and symmetrical textured silicon lifetime test structures.*

reduces on textured surfaces as well ( $\tau_{\text{eff}}$  of  $\sim 1750 \mu\text{s}$ , single-sided  $J_{0, \text{rear}}$  of  $\sim 17 \text{ fA cm}^{-2}$ , implied- $V_{\text{OC}}$  of 696 mV). Effectively, upon deploying the electron-selective passivated contact on a textured surface, the  $\tau_{\text{eff}}$  and implied- $V_{\text{OC}}$  reduce by  $\sim 71$  and  $\sim 3.7\%$ , respectively. Utilizing the same textured lifetime test structures, the electron-selective passivated contacts experience lower degradation of the passivation quality than the hole-selective passivated contacts by a factor of 2.4 times in terms of the implied- $V_{\text{OC}}$  values. The lower passivation quality measured on textured surfaces is not too surprising, given that similar observations were observed when evaluating silicon dioxide thin-film passivation on either planar or textured surfaces [71]. In particular, this reduced passivation quality can be attributed to (i) increased surface area ( $\sim 73\%$  more surface area for textured [111] surfaces than planar [100] surfaces), (ii) increased density of dangling bonds at a [111] surface, and (iii) a higher concentration of interface defects, which could originate from the mechanical stress in the dielectric-silicon interfaces at creases, edges, or vertices [72]. Despite this inherent limitation, we demonstrate in this work that our electron-selective (thermal- $\text{SiO}_x/\text{poly-Si}(n^+)$ ) passivated contacts have a great potential for being deployed on both planar and textured surfaces, while our hole-selective (thermal- $\text{SiO}_x/\text{poly-Si}(p^+)$ ) passivated contacts are currently only suited on planar surfaces, based on our current developments.

Thus, if a double-sided contact passivation scheme is to be considered, the results in this work suggest that it is preferable to implement a solar cell structure with a textured front surface and a planar rear surface, and adopting the electron-selective passivated contacts at the textured front surface and the hole-selective passivated contacts at the planar rear surface, as will be shown in the next section.

### 3.4 Deployment of double-sided passivated contacts at the solar cell level

Based on the findings from the previous section, the deployment of double-sided passivated contacts at the solar cell level had been experimentally realized on n-type silicon wafers with a textured front surface and a planar rear surface and adopting an electron-selective (thermal- $\text{SiO}_x/\text{poly-Si}(n^+)$ ) passivated contacts at the textured front surface and a hole-selective (thermal- $\text{SiO}_x/\text{poly-Si}(p^+)$ ) passivated contacts at the planar rear surface. This is further compared to reference lifetime test structures with either symmetrical planar surfaces with symmetrical hole-selective passivated contacts or symmetrical textured surfaces with symmetrical electron-selective passivated contacts, as sketched in **Figure 9**. As shown in **Figure 9** and summarized in **Table 5**, the lifetime test structures within this second batch of samples processed similarly to **Figure 8** were able to consistently deliver excellent passivation qualities for the planar and textured lifetime test structures. In particular, **Table 5** shows that structure B (symmetrically planar lifetime test structures with symmetrical hole-selective passivated contacts) was able to again demonstrate an implied- $V_{\text{OC}}$  of  $\sim 696 \text{ mV}$  and a single-sided  $J_{0, \text{rear}}$  value of  $\sim 19.5 \text{ fA cm}^{-2}$ , while structure C



**Figure 9.** Comparison of the passivation quality (i.e. (a) effective carrier lifetime at  $10^{15} \text{ cm}^{-3}$  injection level, (b) rear side  $J_0$  values and (c) implied- $V_{\text{OC}}$  values) when both the electron-selective (thermal- $\text{SiO}_x$ /poly-Si( $n^+$ )) passivated contacts and hole-selective passivated contacts (thermal- $\text{SiO}_x$ /poly-Si( $p^+$ )) are deployed on both solar cell structure A (front-side textured, rear-side planar silicon wafer), lifetime test structure B (symmetrically planar), and lifetime test structure C (symmetrically textured).

Structure	Surface (poly-Si thickness)	Pass. contact type	$\tau_{\text{eff}}$ (μs)	Total $J_0$ (fA cm <sup>-2</sup> )	$iV_{\text{OC}}$ (mV)
A	Front-textured (250 nm) Rear-planar (250 nm)	Front electron-selective Rear hole-selective	1273	43.4	688
B	Sym.-planar (250 nm)	Hole-selective	1883	39.1	696
C	Sym.-textured (250 nm)	Electron-selective	1943	28.5	701

**Table 5.** Summary of the average measured passivation quality for both electron-selective and hole-selective passivated contacts deployed on different wafer surfaces.

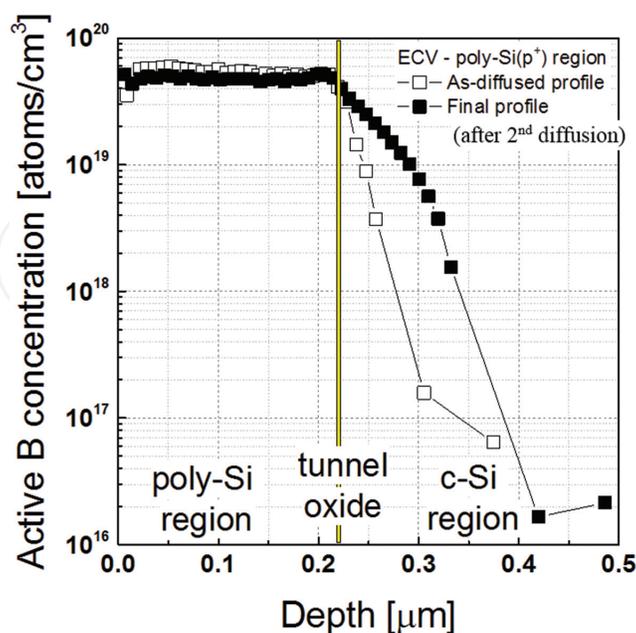
(symmetrically textured lifetime test structures with symmetrical electron-selective passivated contacts) was able to demonstrate an implied- $V_{\text{OC}}$  of  $\sim 701$  mV and a single-sided  $J_{0, \text{rear}}$  value of  $\sim 14 \text{ fA cm}^{-2}$ . At the first thoughts, we would expect structure A (the double-sided passivated contact solar cell precursors) to exhibit a measured passivation quality that lies between that exhibited by structure B and structure C. However, the actual measured results revealed that structure A exhibited a poorer passivation quality than both structure B and structure C. Nonetheless, structure A was able to demonstrate quite high implied- $V_{\text{OC}}$  of  $\sim 688$  mV and a total  $J_0$  value of  $\sim 43 \text{ fA cm}^{-2}$ , prior to any anti-reflection/passivation layers, which likely cannot be attained by conventional diffusion of silicon solar cell precursors.

With a closer look at the key process steps, the key difference between the symmetrical lifetime test structures and the solar cell structures is that the former structures can be done in a one-step diffusion process, while the latter structures would require a series of dielectric masking to achieve single-sided diffused poly-Si layers with different polarities, starting from the higher-temperature requirement first (i.e., boron diffusion toward poly-Si( $p^+$ ) in this work), followed by the diffusion process with a lower-temperature requirement (i.e., phosphorus diffusion toward poly-Si( $n^+$ )). The goal is to reduce the drive-in/out-diffusion of boron dopants from the poly-Si( $p^+$ ) layer into the silicon bulk which is expected to lead to an increased near-surface recombination and poorer passivation quality, as evident

from our measurements as well (see **Figure 9**). **Figure 10** shows a comparison of the ECV profiles done on the same poly-Si(p<sup>+</sup>) layer in the as-diffused state and after an additional diffusion masking and front-side phosphorus diffusion step. It can be clearly seen in the latter that the boron dopants have out-diffused from the poly-Si(p<sup>+</sup>) capping layer into the silicon bulk, which is consistent with the reduced passivation quality measured on the solar cell precursors. Unfortunately, this issue is inevitable for our current investigated approach of obtaining the doped silicon capping layers, although the dopant out-diffusion could be better controlled via diffusion recipe optimization.

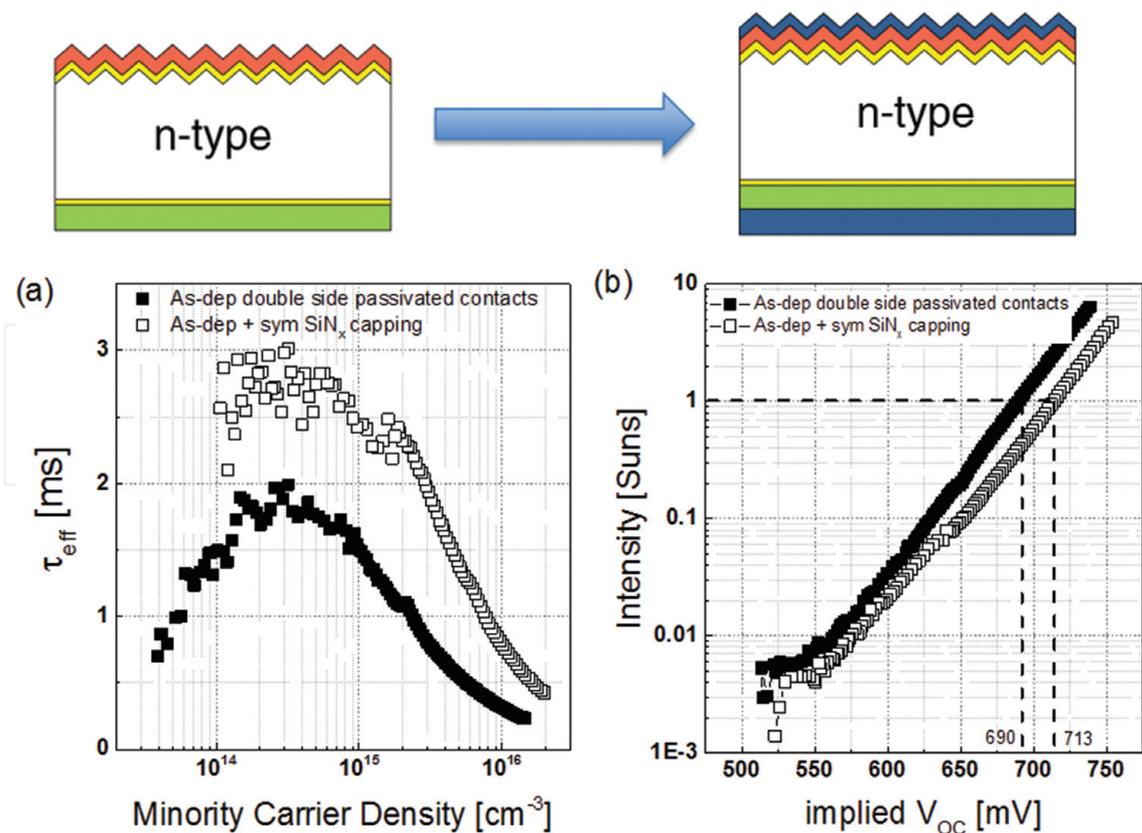
For a conventional silicon wafer solar cell, suitable dielectric thin films or stacks of thin films (such as SiO<sub>x</sub>, SiN<sub>x</sub>, AlO<sub>x</sub>) would be deposited on the silicon wafer surfaces to serve as anti-reflection/passivation prior to the metallization step. Similarly, in this work, the double-sided passivated contact solar cell precursors shown in **Figure 9** were symmetrically capped with PECVD of ~70-nm-thick SiN<sub>x</sub> films. The resulting passivation quality before and after additional SiN<sub>x</sub> capping is plotted in **Figure 11** and listed in **Table 6**.

It can be seen from **Figure 11** that upon the deposition of an additional symmetrical SiN<sub>x</sub> capping layer, there is a striking improvement in the pre-metallized solar cell precursors, in which the  $\tau_{\text{eff}}/J_0/iV_{\text{OC}}$  values improve from 1.5 ms/48 fA cm<sup>-2</sup>/690 mV to 2.4 ms/16.5 fA cm<sup>-2</sup>/713 mV. This improvement can be attributed to the hydrogenation effects from the overlying SiN<sub>x</sub> films, which is expected to further reduce the interface defect densities and improve its corresponding interface passivation quality, as evident from the measured lifetime results presented earlier. This observation was also consistently observed on the symmetrical lifetime test structures, in which the textured samples with electron-selective passivated contacts exhibited improvement in the  $\tau_{\text{eff}}/J_0/iV_{\text{OC}}$  values from ~1.9 ms/28.5 fA cm<sup>-2</sup>/701 mV to ~5.5 ms/13.3 fA cm<sup>-2</sup>/731 mV, while the planar samples with hole-selective passivated contacts exhibited improvement in the  $\tau_{\text{eff}}/J_0/iV_{\text{OC}}$  values from ~1.9 ms/39 fA cm<sup>-2</sup>/696 mV to ~3 ms/30.8 fA cm<sup>-2</sup>/710 mV.



**Figure 10.**

Measured ECV profile for the poly-Si(p<sup>+</sup>) region, comparing the as-diffused profile after the first rear-side boron diffusion (i.e., same compared to the lifetime test structure) and the final boron diffusion profile (i.e., after additional steps of masking, the second front-side phosphorus diffusion, and the chemical mask removal process). For the solar cell precursors, the additional high-temperature process step (second diffusion) causes out-diffusion of boron dopants from the poly-Si(p<sup>+</sup>) layer into the silicon wafer bulk, as evident from ECV measurements.



**Figure 11.** Measured passivation quality of the deployed double-sided passivated contacts on the solar cell structure sketched in Figure 10, both in the as-deposited state and after a symmetrical SiN<sub>x</sub> capping layer, was applied. With the symmetrical SiN<sub>x</sub> capping, which leads to the pre-metallized solar cell precursors, an excellent implied-V<sub>OC</sub> of 713 mV was obtained. The corresponding total J<sub>0</sub> values improved from 48 to 16.5 fA cm<sup>-2</sup>, an approximately threefold improvement.

Structure	Surface (poly-Si thickness)	Pass. contact type	$\tau_{\text{eff}}$ ( $\mu\text{s}$ )	Total J <sub>0</sub> (fA cm <sup>-2</sup> )	iV <sub>OC</sub> (mV)
Before SiN <sub>x</sub>	Front-textured (250 nm)	Front electron-selective	1500	48	690
	Rear-planar (250 nm)	Rear hole-selective			
After SiN <sub>x</sub>	Front-textured (250 nm)	Front electron-selective	2400	16.5	713
	Rear-planar (250 nm)	Rear hole-selective			

**Table 6.** Summary of the measured passivation quality of a double-sided passivated contact solar cell precursor, before and after additional SiN<sub>x</sub> capping.

### 3.5 Addressing the parasitic absorption issue for highly doped poly-Si layers

Despite the excellent passivation qualities from the developed passivated contacts, one of the key challenges identified for device integration is the issue of parasitic absorption by these highly doped poly-Si capping layers. This issue is found to be more critical when the layers are deployed at the front surface than the rear surface, as simulation studies will show in the later sections. Hence, in order to address the parasitic absorption issue, a thinning of the doped poly-Si thickness is necessary.

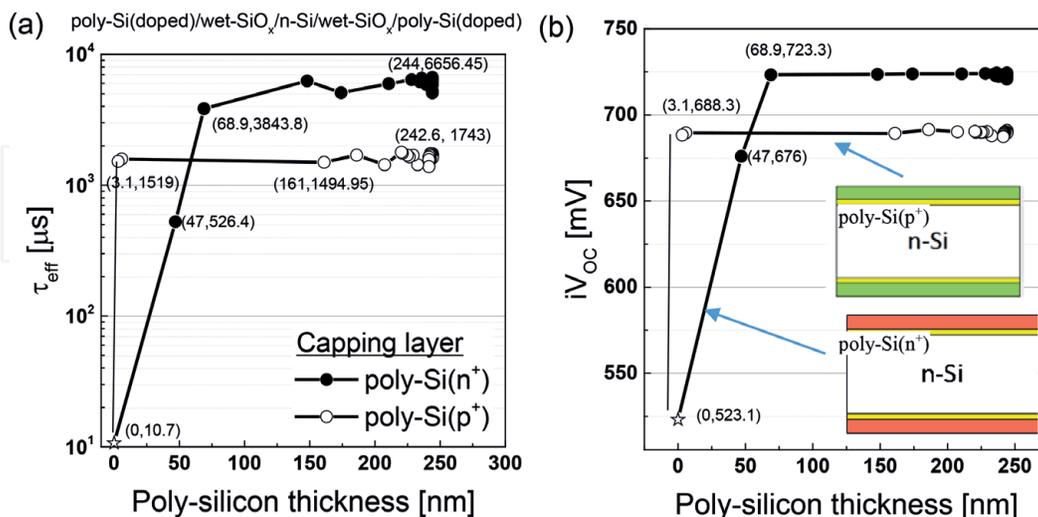
Two different experimental approaches have been investigated: (1) applying a slow silicon etch-back technology, thereby thinning down our already well-optimized thick layers, and (2) performing a diffusion re-optimization for ultrathin LPCVD of intrinsic poly-Si layers. The goal is to determine the threshold (lowest

thickness) of the poly-Si films necessary to achieve the same excellent passivation quality as the thicker counterparts while reducing the parasitic absorption issue as much as possible.

Using our slow silicon etch (SSE) solution (DIW:KOH (3.5%):NaOCl (63.25%) at 80°C), an etch rate of  $\sim 0.1$  nm/s was determined, which was consistently observed for both poly-Si( $n^+$ ) and poly-Si( $p^+$ ) capping layers. **Figure 12** highlights the influence of the resulting doped poly-Si capping layer thickness on the measured passivation quality.

Interestingly, for hole-selective passivated contacts, the passivation quality can be preserved for a poly-Si( $p^+$ ) thickness from a thick  $\sim 250$  nm down to ultrathin layers of approximately  $\sim 3$  nm, with measured  $\tau_{\text{eff}}$  of  $\sim 1.5$  ms and implied- $V_{\text{OC}}$  of  $\sim 690$  mV, respectively. This suggests that a simple SSE etch could be an effective approach to reduce the poly-Si( $p^+$ ) capping layer thickness to an ultrathin (i.e., some nm only) level. However, for electron-selective passivated contacts, the passivation quality was preserved only from  $\sim 250$  nm down to  $\sim 70$  nm, with measured  $\tau_{\text{eff}} > 6$  ms and implied- $V_{\text{OC}} > 720$  mV, respectively. A further thickness reduction ( $< 70$  nm) leads to a severe degradation of passivation quality. As an example, upon reduction of the poly-Si( $n^+$ ) layer from 69 nm to 47 nm, the measured  $\tau_{\text{eff}}$  and implied- $V_{\text{OC}}$  reduce by 86 and 6.5%, respectively. Hence, considering the preference to deploy electron-selective passivated contacts (thermal- $\text{SiO}_x$ /poly-Si( $n^+$ )) on the textured surface, we have to investigate alternative approaches (as outlined in the following) to obtain ultrathin poly-Si( $n^+$ ) capping layers suitable for device integration at the front textured surface of a double-sided passivated contact solar cell.

One of the alternative approaches to obtain ultrathin poly-Si( $n^+$ ) layers is to directly deposit an ultrathin intrinsic poly-Si capping layer, followed by a further optimization of the phosphorus diffusion conditions. The goal is to obtain a highly doped thin poly-Si( $n^+$ ) capping layer which can achieve excellent passivation quality similar to the thicker poly-Si( $n^+$ ) counterparts while minimizing the in-diffusion of phosphorus dopants into the silicon bulk. To achieve this, ultrathin ( $\sim 10$  nm)

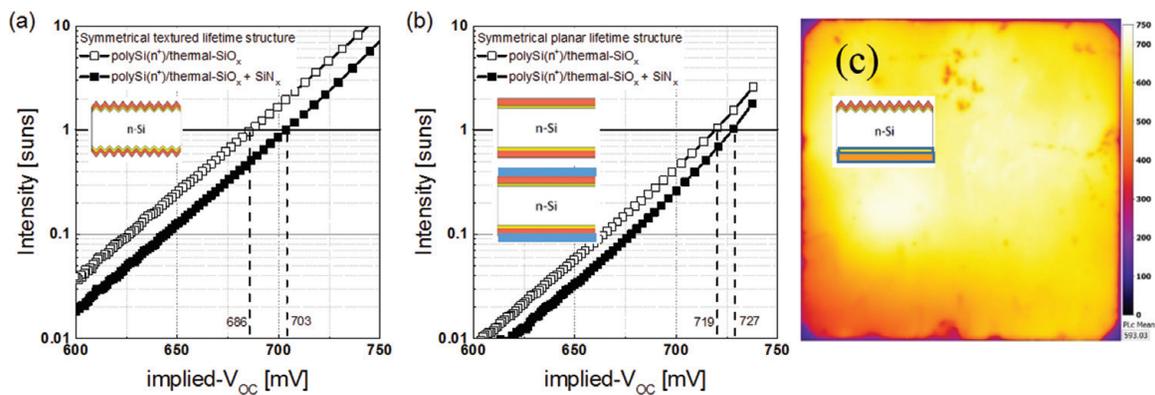


**Figure 12.**

Influence of the decreasing doped poly-Si capping layer thickness via the slow silicon etch process on the measured (a) minority carrier lifetime  $\tau_{\text{eff}}$  and (b) implied- $V_{\text{OC}}$  values for symmetrically planar lifetime test structures. Promising results are observed on hole-selective passivated contacts, in which the passivation quality is preserved for a poly-Si( $p^+$ ) capping layer thickness reduction from a thick  $\sim 250$  nm down to a thin  $\sim 3$  nm. In contrast, the passivation quality of the electron-selective passivated contacts with poly-Si( $n^+$ ) capping layer was preserved down to a thickness of  $\sim 70$  nm, beyond which there is a drastic drop in passivation quality. The “star” symbol refers to the case where there is no doped poly-Si capping layer (i.e., only the tunnel oxide  $\text{SiO}_x$  layer).

intrinsic LPCVD of poly-Si films was deposited on both symmetrical lifetime test structures (textured and planar) and solar cell precursors (i.e., front-side textured, rear-side planar surfaces), followed by the phosphorus diffusion optimization process as mentioned above. The best results from the optimization process are highlighted in **Figure 13** and **Table 7**.

Comparing these results to the thick ( $\sim 250$  nm) thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contacts (**Table 6**), the thin ( $\sim 10$  nm) thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contacts on similar lifetime test structures (textured and planar) also exhibited excellent passivation qualities, attaining an implied-V<sub>OC</sub> of 703 and 727 mV for the textured and planar case, respectively, after a symmetrical SiN<sub>x</sub> capping step. Excellent film and diffusion uniformity was observed from the photoluminescence images; an example is shown in **Figure 13(c)** for the solar cell precursor structure (i.e., front-side textured, rear-side planar) with an electron-selective passivated contact being deposited on both sides (no SiN<sub>x</sub> capping). However, it was observed that the absolute implied-V<sub>OC</sub> values are slightly lower (few millivolts) than the thicker counterparts.



**Figure 13.** Excellent passivation quality demonstrated from our in-house developed electron-selective (thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>)) passivated contact with thin ( $\sim 10$  nm) poly-Si(n<sup>+</sup>) capping layers applied on both (a) symmetrical textured lifetime test structures, with  $iV_{OC}$  reaching 686 mV, and (b) symmetrical planar lifetime test structures, with  $iV_{OC}$  reaching  $\sim 720$  mV, which further improves to 703 and 727 mV, respectively, after an additional standard SiN<sub>x</sub> capping layer. Good film and doping uniformity can be observed from the PL images for both the symmetrical lifetime test structures and solar cell precursors (i.e., front-side textured, rear-side planar) as shown in (c).

Structure	Surface (poly-Si thickness)	SiN <sub>x</sub> capped?	$\tau_{eff}$ ( $\mu$ s)	Total $J_0$ ( $fA\ cm^{-2}$ )	$iV_{OC}$ (mV)
A	Sym. planar (10 nm)	No	4229	16	719
A	Sym. planar (10 nm)	Yes	7277	10	727
B	Sym. textured (10 nm)	No	961	67	686
B	Sym. textured (10 nm)	Yes	1928	31	703
C	Asym. front txt., rear planar (10 nm)	No	2982	22	713
C	Asym. front txt, rear planar (10 nm)	Yes	6557	Inj. dep	741

**Table 7.** Summary of the measured passivation quality parameters ( $\tau_{eff}$ , total  $J_0$ , implied-V<sub>OC</sub>) for an electron-selective passivated contact comprising an in situ thermal-SiO<sub>x</sub> tunnel layer coupled with a thin ( $\sim 10$  nm) poly-Si(n<sup>+</sup>) capping layer, evaluated on lifetime test structures which are symmetrically planar (structure A), symmetrically textured (structure B), and front-side textured and rear-side planar solar cell precursors (structure C).

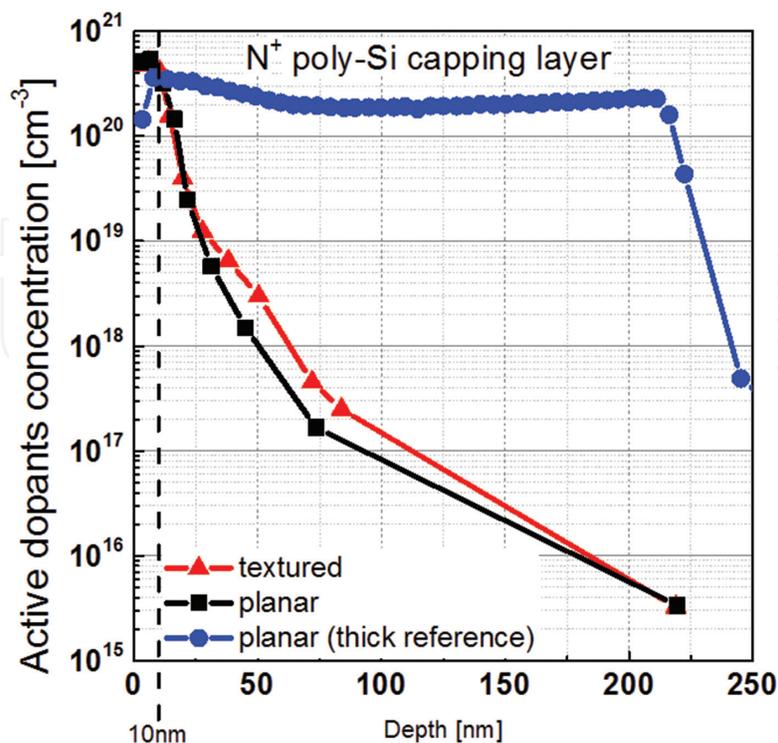
To provide more insights, ECV measurements were performed on the thin poly-Si( $n^+$ ) layers on both the textured and planar surfaces and compared to the thick reference as shown in **Figure 14**. The following observations can be made: (i) the thin poly-Si( $n^+$ ) layer exhibits a higher phosphorus dopant concentration ( $\sim 5 \times 10^{20} \text{ cm}^{-3}$ ) than the thicker counterpart ( $\sim 2 \times 10^{20} \text{ cm}^{-3}$ ); and (ii) the poly-Si( $n^+$ ) layer on the textured surface exhibits a higher dopants in-diffusion than the planar surface, which could partially explain the lower measured implied- $V_{OC}$  values for the former (i.e., 686 mV as compared to 719 mV).

Similar to the thick poly-Si( $n^+$ ) capped samples, an additional symmetrical  $\text{SiN}_x$  capping further enhances the overall passivation quality, such that the textured and planar lifetime structures now exhibit an improvement in the implied- $V_{OC}$  by 17 and 8 mV, which is a relative improvement of 2.5 and 1.1%, respectively.

To summarize, we have demonstrated on a textured silicon surface the ability to obtain an excellently passivating  $\text{SiN}_x$ -capped electron-selective passivated contact (thermal- $\text{SiO}_x$ /poly-Si( $n^+$ )) with sufficiently thin poly-Si( $n^+$ ) thickness ( $\sim 10 \text{ nm}$ ) to reduce the parasitic absorption issue while maintaining excellent passivation qualities (implied- $V_{OC}$  values exceeding 700 mV). Re-optimizing the diffusion recipe for an ultrathin LPCVD of intrinsic poly-Si layer therefore solves the limitations encountered when using slow silicon etch technology, which limited the obtainable poly-Si( $n^+$ ) layer thickness to  $\sim 70 \text{ nm}$  (i.e., observing a drastic drop in passivation quality for thinner layers).

### 3.6 Simulation studies: reducing parasitic absorption from highly doped poly-Si layers

The excellent results from the earlier sections clearly demonstrate the potential of deploying double-sided passivated contacts for next-generation silicon solar cell



**Figure 14.**

Comparison of the ECV profile for  $\sim 10\text{-nm}$ -thick poly-Si( $n^+$ ) layer on both planar and textured silicon surfaces. Additionally included is the ECV profile for a thick poly-Si( $n^+$ ) capping layer for comparison purpose. A higher dopant in-diffusion is observed for the textured surfaces, which partially explains the lower measured implied- $V_{OC}$  values.

concepts, which in this work had been entirely realized on commercially available industrial tools. However, as mentioned earlier, one of the key issues if contact passivation is to be applied front-side also is to minimize parasitic absorption within the highly doped front-side poly-Si capping layer. Highly doped poly-Si is similar to transparent conductive oxide (TCO) layers deployed for silicon heterojunction solar cells, non-zero extinction coefficients, resulting in the inevitable parasitic absorption. This is even more pronounced, if applied front-side, thereby directly reducing the absorbable photogeneration current in the silicon wafer bulk (as the incident light is then first entering the parasitically absorbing poly-Si capping layer before entering the silicon wafer).

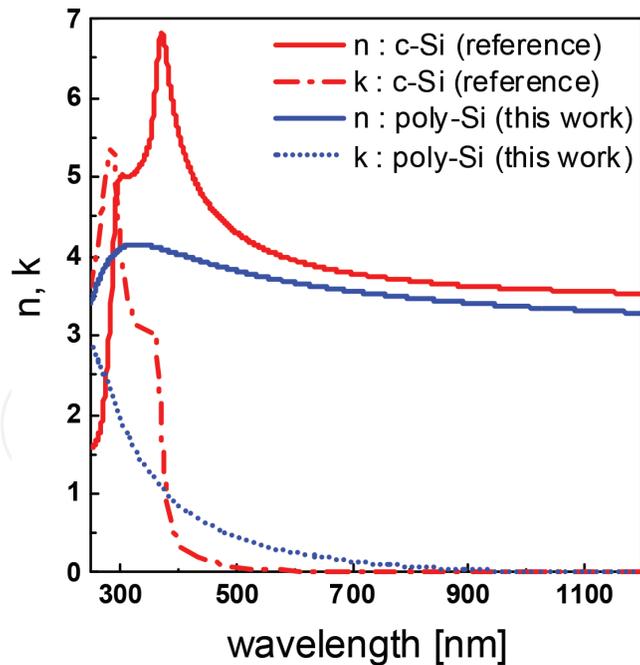
Hence, the objective of this section is to utilize an appropriate numerical calculation method to determine the parasitic absorption as a function of the (rear or front side) poly-Si capping layer thickness and then subsequently predict the corresponding solar cell efficiency potential of the correspondingly optimized passivated contact, being rear-side-only or front- and rear-side deployed in a solar cell. To address the above, the simulation program SunSolve™, available on PV Lighthouse [53], was utilized to study the impact of the doped poly-Si capping layer thickness on the maximum absorbable current density within the silicon wafer bulk  $J_{\text{absorbed, cell}}$ . Besides calculating  $J_{\text{absorbed, cell}}$ , the various optical losses can also be determined (i.e., front-reflected, front-escaped, rear-escaped, parasitic absorption in each layer, edge absorption) for the investigated solar cell precursors in this work.

To enhance the accuracy of the optical calculations, ellipsometry measurements were performed on all in-house fabricated samples, i.e., measuring our deployed dielectric films ( $\text{SiN}_x$ ,  $\text{SiO}_x$ ,  $\text{AlO}_x$ ) as well as our optimized doped poly-Si capping layers, followed by a fitting and extraction of the wavelength-dependent optical refractive indices ( $n$ ,  $k$ ). These wavelength-dependent refractive indices were then imported into the SunSolve™ simulation program for a more realistic prediction of the current loss analysis, based on our own developed contact passivation layers. As an example, **Figure 15** shows the fitted wavelength-dependent refractive indices for the doped poly-Si layers in this work, which is further compared to the crystalline silicon reference [73]. As seen, the doped poly-Si layers do exhibit a higher extinction coefficient ( $k$ ) compared to a c-Si reference within the visible to near-infrared region (400–900 nm). This again indicates that parasitic absorption is inevitable and should be minimized by thickness reduction while not compromising on the passivation quality. Further optimization work should also try to reduce the extinction coefficient of the poly-Si capping layers itself, i.e., by changing its chemical composition.

The current loss analysis results for a rear-side passivated contact solar cell (using SunSolve™) are shown in **Figure 16**. In order to account for internal back reflection, a local full-area metal contact scheme has been assumed (see **Figure 16**) (this can be realized by local laser ablation, forming contact openings in the  $\text{SiN}_x$  passivation layer and a subsequent full-area metallization).

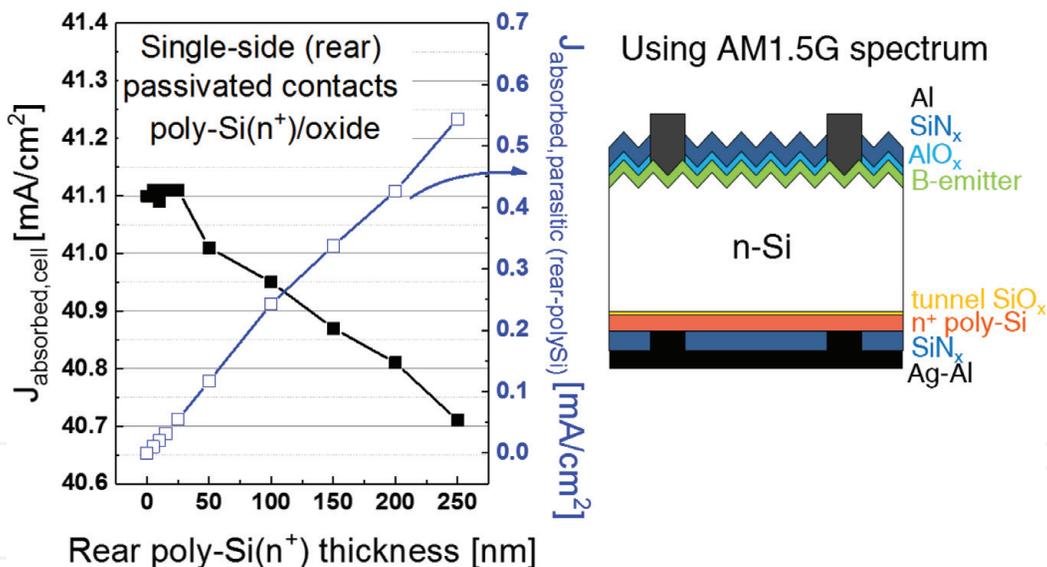
It can be seen that for a solar cell with a conventional front-side boron-diffused junction and a rear-side electron-selective passivated contact (thermal- $\text{SiO}_x$ /poly-Si( $n^+$ )), the parasitic absorption arising from the rear-side poly-Si( $n^+$ ) capping layer can be directly addressed by reducing the rear-side poly-Si film thickness (e.g., the parasitic absorption current loss reduces from  $0.55 \text{ mA cm}^{-2}$  for a 250-nm-thick poly-Si( $n^+$ ) layer to  $0.02 \text{ mA cm}^{-2}$  for a 10-nm-thick poly-Si( $n^+$ ) layer). The reduction in the parasitic absorption directly enhances the potentially absorbable current in the wafer bulk ( $J_{\text{absorbed, cell}}$ ), which in this case improves from  $\sim 40.7$  to  $\sim 41.1 \text{ mA cm}^{-2}$ .

Interestingly, it was observed that for a poly-Si capping layer thickness lower than 25 nm, the  $J_{\text{absorbed, cell}}$  saturates at  $\sim 41.1 \text{ mA cm}^{-2}$ . On hindsight, we would



**Figure 15.**

Optical indices extracted for the doped poly-Si layers in this work, based on ellipsometry measurements and its subsequent fitting by the Tauc-Lorentz model. Also included is the crystalline silicon optical index data for reference. The poly-Si films do exhibit higher extinction coefficient values than the c-Si wafer bulk within the visible to near-infrared regions (400–900 nm), clearly indicating the need to optimize the poly-Si capping layer thickness in order to reduce parasitic absorption.



**Figure 16.**

Numerically calculated absorbed photogeneration current in the silicon solar cell bulk ( $J_{\text{absorbed, cell}}$ ) and the parasitic absorption contributed by the rear-side poly-Si( $n^+$ ) capping layer ( $J_{\text{absorbed, parasitic (rear-polySi)}}$ ), as a function of its thickness from 250 nm down to 0 nm, for a rear-side passivated contact solar cell, adopting a conventional front-side boron-diffused emitter junction, and the investigated rear-side electron-selective passivated contacts (tunnel oxide/poly-Si( $n^+$ )). Reducing the rear-side poly-Si( $n^+$ ) layer thickness leads to a significant reduction on parasitic absorption (up to  $0.55 \text{ mA cm}^{-2}$ ) and a corresponding gain in the photogeneration current  $J_{\text{absorbed, cell}}$  (up to  $0.4 \text{ mA cm}^{-2}$ ). Interestingly,  $J_{\text{absorbed, cell}}$  saturates for a poly-Si( $n^+$ ) layer thickness lower than 25 nm, despite a further reduction of rear-side parasitic absorption (see text).

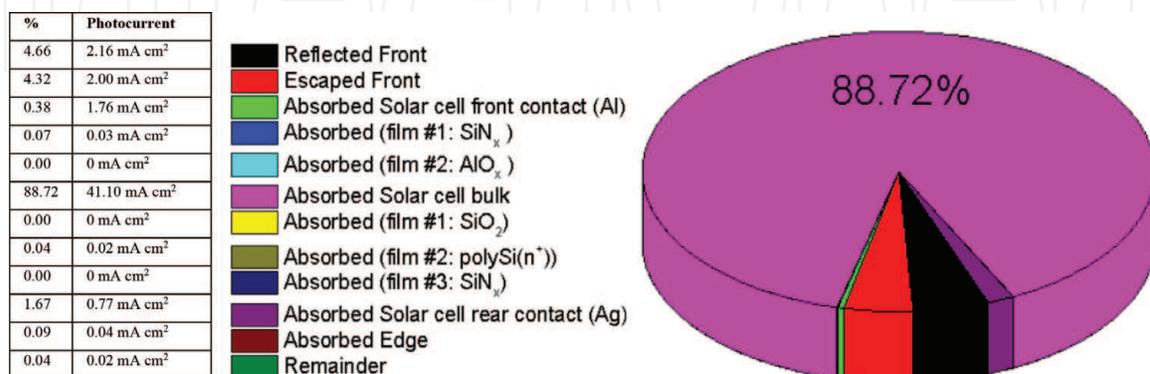
expect that as the poly-Si capping layer thickness reduces, photons which were not absorbed in the first pass within the cell bulk would now have an increased probability of being parasitically absorbed at the rear-side metal contacts. Indeed, the numerical calculations confirm that hypothesis in which the calculated parasitic absorption within the rear-side metal contacts increases from  $\sim 0.73 \text{ mA cm}^{-2}$  with

a 250-nm-thick poly-Si to  $\sim 0.78 \text{ mA cm}^{-2}$  with a 10-nm-thick poly-Si layer. Additionally, there was also a clear increasing trend in the front-escaped current density from  $\sim 1.91 \text{ mA cm}^{-2}$  with a 250-nm-thick poly-Si to  $\sim 2 \text{ mA cm}^{-2}$  with a 10-nm-thick poly-Si layer. These two effects were found to limit the potential  $J_{\text{absorbed, cell}}$  in case of deploying very thin rear-side poly-Si capping layers.

Hence, for the purpose of device integration, our numerical findings suggest that when considering tunnel oxide/poly-Si(doped) passivated contacts at the rear surface, it would suffice to shrink down the rear-side poly-Si thickness to 25 nm (thinner layers will not further improve the photogeneration current  $J_{\text{absorbed, cell}}$  within the silicon wafer). However, a thicker rear-side poly-Si layer may be more suited to accommodate screen-printed, industrial fire-through metal contacts, without damaging the interface passivation (see the next section). Hence, a trade-off of between these two requirements is needed and to be investigated in the future work.

**Figure 17** presents a pie chart summary for the current loss analysis of the simulated solar cell structure shown in **Figure 16**, which adopts a rear-side poly-Si( $n^+$ ) capping layer with an experimentally realizable thickness of 10 nm as mentioned in the earlier sections. Based on this single-sided (rear-side) passivated contact solar cell structure, the parasitic absorption contribution by the rear-side poly-Si( $n^+$ ) layer leads to a negligible low 0.04% of the total AM1.5G incident current density of  $46.32 \text{ mA cm}^{-2}$ , amounting to  $0.02 \text{ mA cm}^{-2}$  only. The bulk of the incident photon current density is absorbed by the silicon wafer (88.72%), although this could be further enhanced when better front-side anti-reflection coatings are available for deployment (currently, a front-reflected current density loss of 4.66% is calculated for our in-house deployed thin-film  $\text{AlO}_x/\text{SiN}_x$  anti-reflection stack). The second highest current loss channel is the front-escaped current density at 4.32%. Please note that this loss channel cannot be reduced: Photons which are desired to enter the silicon wafer will also be able to leave it. Actually, the higher the percentage loss due to front surface escape, the better the optical performance of the solar cell. The metal grid at the front and rear accounts for a total current loss of 2.05% based on our in-house available screen designs. Taking all optical current losses into account, the maximum absorbable photon current density in the silicon wafer is  $\sim 41.1 \text{ mA cm}^{-2}$ .

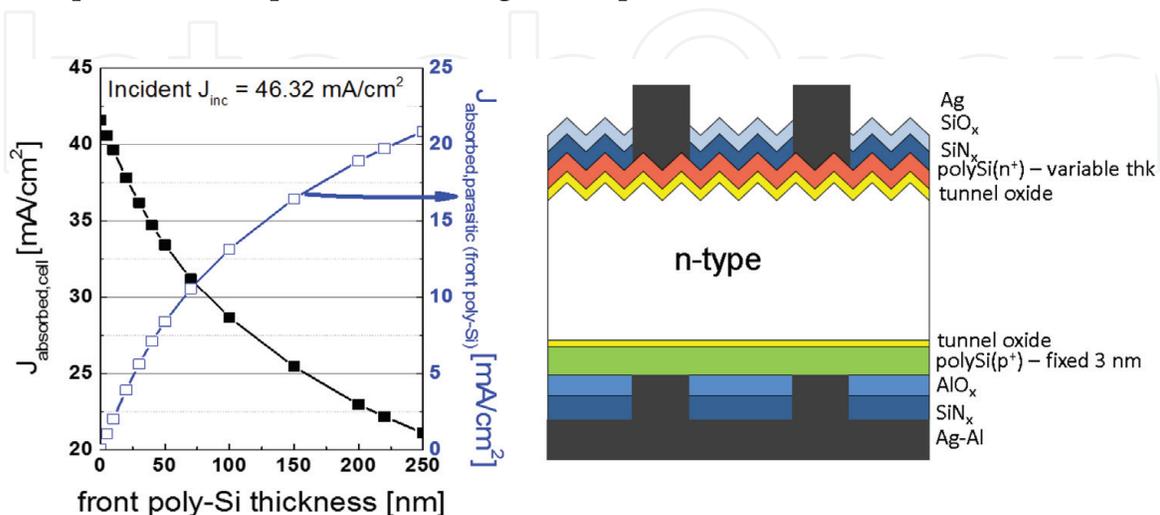
Extending the analysis from a solar cell with a single rear-side-only passivated contact toward double-sided passivated contacts, the same current loss analysis



**Figure 17.** Pie chart representing the SunSolve™ current loss analysis for the solar cell structure sketched in **Figure 16**, featuring an experimentally realizable rear-side poly-Si( $n^+$ ) capping layer thickness of 10 nm. In this case, the rear-side poly-Si( $n^+$ ) capping layer exhibits a negligible parasitic absorption of 0.04% at  $0.02 \text{ mA cm}^{-2}$ , out of the total incident current density of  $46.32 \text{ mA cm}^{-2}$  for the utilized AM1.5G solar spectrum. For a rear-side-only passivated contact solar cell, the maximum absorbable photocurrent density in the silicon wafer is  $\sim 41.1 \text{ mA cm}^{-2}$  (88.72% of the incoming solar spectrum).

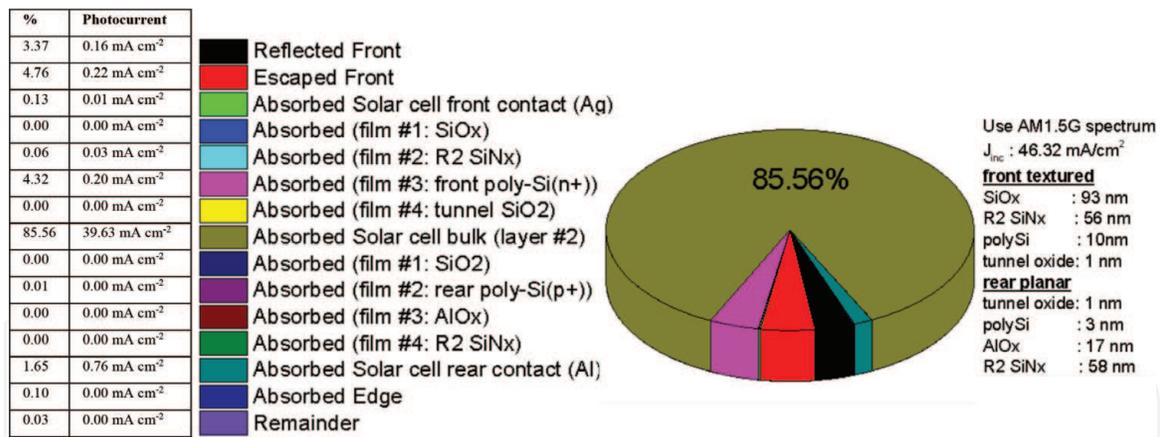
approach was applied to front- and rear-side passivated contact solar cells, exhibiting an optically negligible rear-side capping layer thickness of 3 nm, as experimentally realized. As sketched in **Figure 18**, this solar cell structure consists of a front-side textured surface with our developed electron-selective (tunnel oxide/poly-Si( $n^+$ )) passivated contacts, and a rear-side planar surface with our developed hole-selective (tunnel oxide/poly-Si( $p^+$ )) passivated contacts. This is followed by the standard dielectric coatings ( $\text{SiO}_x$ ,  $\text{SiN}_x$ ,  $\text{AlO}_x$ ) at both surfaces to serve both passivation and anti-reflection purposes, prior to the screen-printed fire-through metal contacts at both sides. Adopting an experimentally realizable rear-side poly-Si( $p^+$ ) capping layer thickness of 3 nm (see earlier section), the influence of the front-side poly-Si capping layer thickness on the  $J_{\text{absorbed, cell}}$  is investigated. **Figure 18** shows that the parasitic absorption by the front-side poly-Si capping layer has a much more severe and significant impact on the remaining absorbable current density in the solar cell bulk ( $J_{\text{absorbed, cell}}$ ). If contact passivation is applied front-side,  $J_{\text{absorbed, parasitic (front poly-Si)}}$  is as high as  $\sim 20.8 \text{ mA cm}^{-2}$  for a 250-nm-thick poly-Si( $n^+$ ) layer, and it reduces to  $\sim 1 \text{ mA cm}^{-2}$  for a 5-nm-thick poly-Si( $n^+$ ) layer. Front-side poly-Si layer thickness reduction therefore directly translates into a significant gain in  $J_{\text{absorbed, cell}}$ , approximately by the same amount (i.e., increasing from  $\sim 21$  to  $\sim 40.3 \text{ mA cm}^{-2}$ ).

Accordingly, the pie chart current loss analysis for the double-sided passivated contact solar cell structure depicted in **Figure 3** is shown in **Figure 19** for the case of an experimentally realizable front-side poly-Si( $n^+$ ) capping layer thickness of 10 nm and an experimentally realizable rear-side poly-Si( $p^+$ ) capping layer thickness of 3 nm. **Figure 19** shows that the presence of the 10-nm-thick front-side poly-Si( $n^+$ ) capping layer contributes to a comparatively higher parasitic absorption loss (4.32%) than the rear-side poly-Si( $p^+$ ) capping layer (0.01%), based on a total incident current density of  $46.32 \text{ mA cm}^{-2}$  (AM1.5G spectrum). The remaining potentially absorbable current density within the solar cell bulk stands at  $\sim 85.56\%$  ( $\sim 39.6 \text{ mA cm}^{-2}$ ), which is  $\sim 3.16\%$  lower than a rear-side-only passivated contact scheme. Hence, it is clear that although double-sided passivated contact solar cells could deliver excellent passivation on both sides of the wafer (thereby reaching higher open-circuit voltages  $V_{\text{OC}}$  than rear-side-only passivated contact solar cells or conventional diffused solar cells), there is still a trade-off with increased front-side parasitic absorption, demanding more optimization efforts.



**Figure 18.**

Numerically calculated photon current absorption for a double-sided passivated contact solar cell. The rear-side hole-selective poly-Si( $p^+$ ) capping layer thickness is fixed at 3 nm, while the front-side electron-selective poly-Si( $n^+$ ) capping layer thickness is varied from 0 nm to 250 nm. Front-side parasitic within the poly-Si( $n^+$ ) capping layer ( $J_{\text{absorbed, parasitic (front poly-Si)}}$ ) has a severe impact on the absorbable photon current density within the silicon wafer ( $J_{\text{absorbed, cell}}$ ).



**Figure 19.** Pie chart representing the SunSolve™ current loss analysis for the double-sided passivated contact solar cell structure sketched in Figure 18, featuring a rear-side poly-Si(p<sup>+</sup>) capping layer thickness of 3 nm and a front-side poly-Si(n<sup>+</sup>) capping layer thickness of 10 nm. The 10-nm-thin front-side poly-Si(n<sup>+</sup>) capping layer still contributes to the parasitic absorption (4.32% at 0.2 mA cm<sup>-2</sup>), whereas parasitic absorption within the 3-nm rear-side poly-Si(p<sup>+</sup>) capping layer can be neglected, based on a total incident current density of 46.32 mA cm<sup>-2</sup> for the utilized AM1.5G solar spectrum. For the double-sided passivated contact solar cell, the maximum absorbable photocurrent density in the silicon wafer is now ~39.6 mA cm<sup>-2</sup> (85.56% of the incoming solar spectrum).

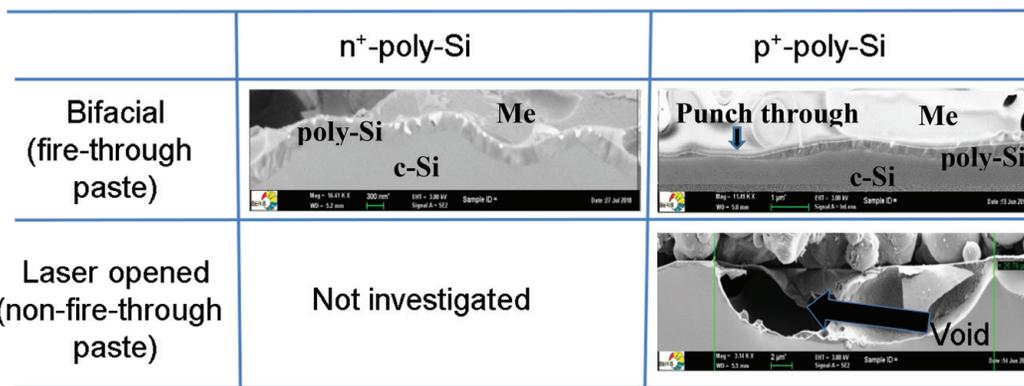
### 3.7 Compatibility of screen printing (using conventional screen-printing pastes) on our developed passivated contact layers

In earlier sections, the feasibility of the electron-selective and hole-selective passivated contacts has been demonstrated, both on symmetrical lifetime test structures and asymmetrical solar cell precursors as sketched in Figure 11 (in the as-deposited state and after an additional symmetrical SiN<sub>x</sub> capping). The remaining solar cell fabrication step would be the formation of metal contacts toward these thin-film passivated contacts, without damaging the passivation quality underneath these contacts. As a first attempt, conventional metal contacting schemes, i.e., screen printing, as commonly deployed for conventional silicon solar cells (exhibiting double-sided diffused junctions), were performed on our lifetime and solar cell precursors. In particular, we tested our industrial in-house fire-through and non-fire-through screen-printing pastes, based on Ag, Ag/Al, or Al material formulations. The corresponding results were compared to a nonindustrial research reference contact, deploying thermally evaporated Ag contacts.

In summary, so far, using conventional screen-printing pastes, screen printing works only on comparatively thick poly-Si(n<sup>+</sup>) layers, i.e., requiring a poly-Si(n<sup>+</sup>) thickness of 150 nm or larger. So far, it does not work on poly-Si(p<sup>+</sup>) layers. The SEM results presented in Figure 20 sum up these observations.

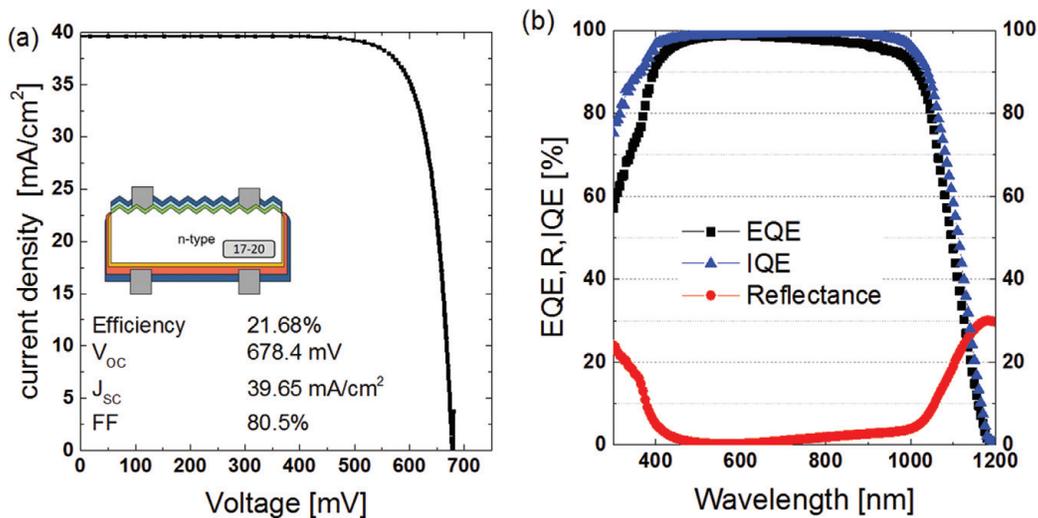
(I) A fire-through Ag paste (as conventionally used to contact n-doped silicon material) is able to contact our standard ~250-nm-thick poly-Si(n<sup>+</sup>) layers conformably, without any issues, i.e., exhibiting a low contact resistance (13 mΩ cm<sup>2</sup>) and no void issues or punch-through effects underneath the contact (see Figure 20 (top, left)). The investigated fire-through Ag paste is suitable for rear-side contacting poly-Si(n<sup>+</sup>) capping layers down to a thickness of 150 nm; however, it fails to contact our ultrathin ~10-nm poly-Si(n<sup>+</sup>) capping layer, as outlined in some more detail later.

Deploying industrial screen printing for rear-side-only passivated contact solar cells, we currently reach a solar cell efficiency of 21.7%, using our 250-nm “standard” rear-side SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) contact passivation layers (see Figure 21 and Table 8).



**Figure 20.**

SEM images taken for poly-Si(n<sup>+</sup>) and poly-Si(p<sup>+</sup>) layers contacted via conventional screen printing, using various commercially available pastes: (i) bifacial fire-through pastes, i.e., Ag paste for contacting n-doped Si and Al paste for contacting p-doped Si, and (ii) non-fire-through Ag/Al pastes, using laser ablation to form local contact openings prior to screen printing. Screen printing works only in case of contacting moderately thick (150–250 nm) electron-extracting poly-Si(n<sup>+</sup>) capping layers. In all other cases, issues like void formation or a local “punch through” of the metal paste (locally contacting the c-Si wafer instead of the poly-Si capping layer) occur.



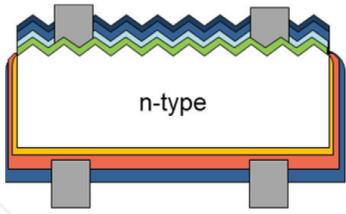
**Figure 21.**

(a) Measured I–V curve of our current rear-side passivated contact record efficiency cell, exhibiting a rear-side wet-chemically formed SiO<sub>x</sub> tunnel layer, a 250-nm poly-Si(n<sup>+</sup>) capping layer, and a conventionally formed (boron-diffused, AlO<sub>x</sub>/SiN<sub>x</sub> passivated and screen printed) front-side contact. (b) The correspondingly measured external/internal quantum efficiency, EQE, IQE, and the measured reflectance for the same cell.

Reducing the rear-side poly-Si(n<sup>+</sup>) capping layer thickness (separate batch, hereby only reaching 21.3% for the solar cell with the 250-nm-thick poly-Si reference layer), we were able to observe a clear increase in short-circuit current density (see **Table 9**). By thinning down the rear-side poly-Si(n<sup>+</sup>) capping layer thickness from 250 nm down to 150 nm, using etch-back technology, we gain  $\sim 0.4$  mA cm<sup>-2</sup> in short-circuit current density, reaching again a best cell efficiency of 21.7%. Up to a thickness of 150 nm, the poly-Si(n<sup>+</sup>) thinning did neither significantly affect the open-circuit voltage V<sub>oc</sub> nor the fill factor of the solar cell (compare **Table 8**). However, the samples with a 100-nm rear-side poly-Si capping layer exhibit a drop in V<sub>oc</sub> ( $\sim 15$  mV). This resulted from a local punch through of the screen-printed metal paste, similar to the SEM image as shown in **Figure 20** (top, right).

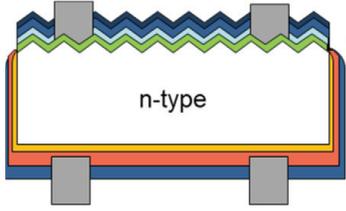
(II) A fire-through Ag/Al paste (as conventionally used to contact p-doped silicon material) could not contact our standard  $\sim 250$ -nm-thick poly-Si(p<sup>+</sup>) layers properly: There are several regions where the paste is observed to consume the poly-Si(p<sup>+</sup>) layer, causing a thinning of the poly-Si(p<sup>+</sup>) layer and some local

Cell type: thickness of rear poly-Si(n <sup>+</sup> )	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA cm <sup>-2</sup> )	FF (%)	Eff (%)
250 nm	678	39.7	80.5	21.7



**Table 8.**  
*I-V data of the rear-side passivated contact record cell, deploying conventional bifacial screen printing for metallization.*

Cell type: thickness of rear poly-Si(n <sup>+</sup> )	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA cm <sup>-2</sup> )	FF (%)	Eff (%)
250 nm	672	39.4	80.2	21.3
150 nm	676	39.8	80.7	21.7
100 nm	660	39.6	80.2	21.0



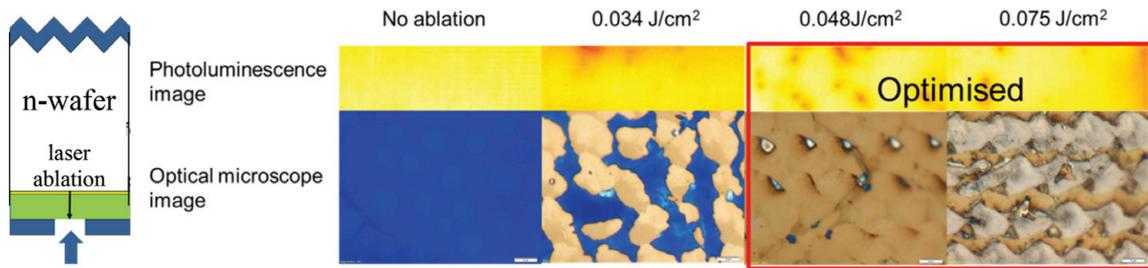
**Table 9.**  
*I-V data of rear-side passivated contact solar cells, with a varying rear-side poly-Si(n<sup>+</sup>) capping layer thickness.*

“punch-through” areas (see **Figure 20** (top, right)). This in turn leads to local shunting (in case of using an n-type wafer) and to a severe degradation of contact passivation quality, as evident from the final measured cell V<sub>oc</sub> values.

This issue can be likely attributed to the presence of the Al alloy within the paste, which is typically responsible for forming the back surface field regions in conventional silicon solar cells. Al alloying is known to partially consume crystalline silicon material: thus, our thin poly-Si(p<sup>+</sup>) capping layers will be consumed upon contact firing of the screen-printed Ag/Al paste, leading to the just outlined local “punch-through” effects.

(III) A non-fire-through pure Al paste (as conventionally used to contact a p-doped silicon wafer in order to form locally Al-alloyed back-surface-field (BSF) regions within the wafer) was found to create large voids in several regions (see **Figure 20** (bottom, right)) and to consume the entire poly-Si(p<sup>+</sup>) passivated contacts, leading to a drastic drop in contact passivation quality and measured device performance.

It is possible to use femtosecond laser ablation, in order to create damage-free local contact openings (i.e., locally ablating the overlying SiN<sub>x</sub> layer without damaging the underlying poly-Si(p<sup>+</sup>) capping layer). Using a femtosecond laser at an ultraviolet wavelength of 330 nm, the onset of laser fluence for optimized SiN<sub>x</sub> ablation is 0.08 J cm<sup>-2</sup>. Within the optimized process window, the lifetime is preserved after laser ablation (as indicated by photoluminescence imaging), and the SiN<sub>x</sub> is fully ablated (as indicated by optical microscope imaging) (see **Figure 22**). However, the paste composition of the screen-printing paste has to be altered, in order to enable a subsequent damage-free contacting of our (thick or ultrathin) poly-Si(p<sup>+</sup>) layers. Corresponding research activities, in cooperation with a paste manufacturer, are currently initiated.



**Figure 22.**

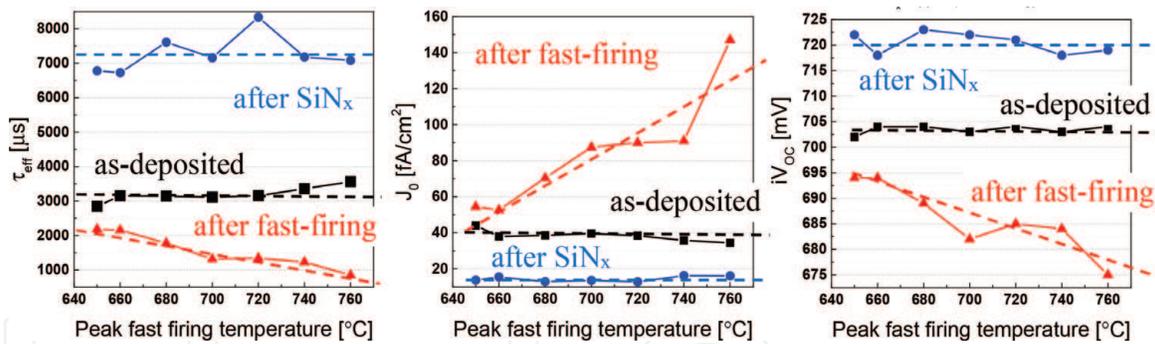
(Left) Sketch of the laser process to locally laser ablate  $\text{SiN}_x$  on top of thin-film poly-Si, in order to form local contact openings for further metallization, aiming at conventional screen printing, using a non-fire-through paste. (Right) Photoluminescence images and optical microscope images inside the opening, taken for a screened range of laser fluence.

(IV) As expected, our research reference thermal evaporated Ag contacts were able to form damage-free conformal low resistivity contacts to our developed  $\text{SiO}_x/\text{poly-Si}(\text{p}^+)$  and  $\text{ALD-AlO}_x/\text{poly-Si}(\text{p}^+)$  passivated contacts, thereby enabling a nonindustrial full-area reference contact on hole-extracting  $\text{poly-Si}(\text{p}^+)$  capping layers [34].

As just outlined above, using our conventional screen-printing metal pastes and fast-firing conditions, thus far we were not able to successfully contact hole-extracting  $\text{poly-Si}(\text{p}^+)$  layers as well as ultrathin 10-nm electron-extracting  $\text{poly-Si}(\text{n}^+)$  layers. Thus, a closer attention toward (i) an optimization of the metal paste itself, i.e., tuning its chemical composition, and (ii) an optimization of the fast-firing conditions, applied after screen printing, in order to form a low resistivity contact, is necessary.

To address the latter, an asymmetric lifetime test structure, featuring a textured front surface and a planar rear surface, symmetrically passivated contact by our ultrathin ( $\sim 10$  nm) electron-selective, thermal- $\text{SiO}_x/\text{poly-Si}(\text{n}^+)$  passivated contact layers, was utilized. The passivation quality of these samples in the as-deposited state was measured first, followed by a symmetrical deposition of the passivation/anti-reflective  $\text{SiN}_x$  film, and its passivation quality was remeasured. Then, the samples were subjected to different fast-firing peak temperatures (650, 660, 680, 700, 720, 740, 760°C), thereby mimicking different fast-firing conditions after screen printing, and the resulting final passivation quality was remeasured again (see **Figure 23**).

For our ultrathin 10-nm  $\text{SiO}_x/\text{poly-Si}(\text{n}^+)$  contact passivation layers, a severe degradation of passivation quality after fast-firing is observed (see **Figure 23**). In the as-deposited state, our asymmetrical lifetime test structures with electron-selective passivated contacts were exhibiting good passivation quality with average  $\tau_{\text{eff}}/J_0/iV_{\text{oc}}$  values of  $\sim 3.3$  ms /  $35.4$  fA  $\text{cm}^{-2}$  /  $704$  mV. Upon the subsequent symmetrical  $\text{SiN}_x$  capping, the passivation quality got further enhanced, i.e., reaching excellent average  $\tau_{\text{eff}}/J_0/iV_{\text{oc}}$  values of  $\sim 7.3$  ms /  $14.4$  fA  $\text{cm}^{-2}$  /  $720$  mV. However, after an additional short high-temperature treatment, in case of using our ultrathin 10-nm electron-extracting contact passivation layers, the passivation quality drops significantly. For example, if we adopt a fast-firing peak temperature of 740°C (which is currently utilized for our conventional double-sided diffused silicon solar cells), a drastic drop in passivation quality occurs, in which the  $\tau_{\text{eff}}/J_0/iV_{\text{oc}}$  values degrade to  $\sim 1.2$  ms /  $91$  fA  $\text{cm}^{-2}$  /  $684$  mV. This effect is less severe, but still significant, if lower fast-firing peak temperatures can be deployed (see **Figure 23**). It seems like our current ultrathin electron-selective passivation layers are not firing stable, especially if deploying high peak firing temperatures (they still do outperform conventionally diffused front-side contacts, though). Interestingly, this



**Figure 23.** Comparison of the measured passivation quality for the asymmetrical lifetime test structures comprising a textured front and a planar rear surface, passivated with electron-extracting thermal-SiO<sub>x</sub>/10 nm-poly-Si(n<sup>+</sup>) passivated contacts, in the as deposited state, after additional SiN<sub>x</sub> deposition and after a fast-firing belt furnace temperature treatment. The straight lines are a guide to the eyes.

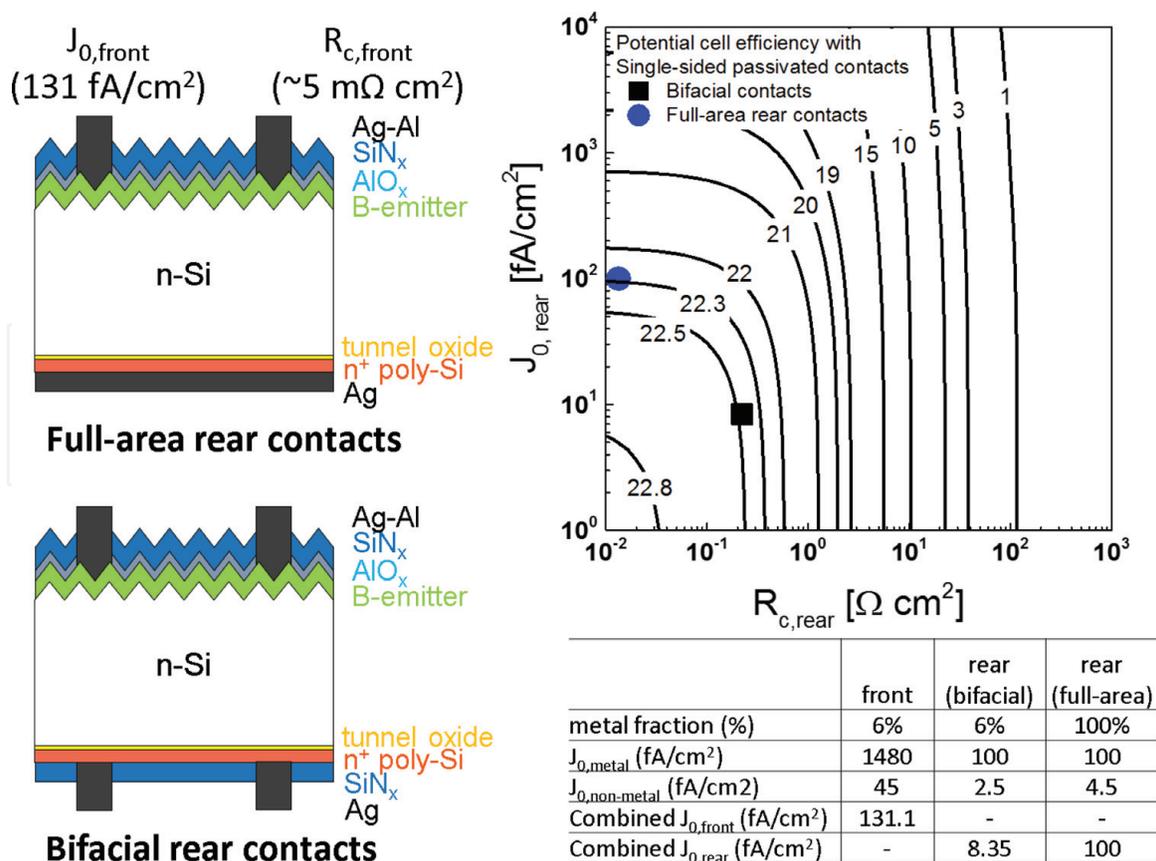
is not the case for the 250-nm-thick “standard” layers. ECV measurements confirm that after fast-firing, the dopants within the poly-Si(n<sup>+</sup>) capping layer have out-diffused into the silicon wafer bulk, thereby effectively reducing field-effect passivation and thus the observed lifetimes of the samples. More detailed investigations are currently ongoing.

Thus, more efforts to render our ultrathin contact passivation layers firing stable, i.e., by deploying lower peak firing temperatures and/or changing the chemical composition of the ultrathin LPCVD of poly-Si capping layers, are necessary. Furthermore, efforts to optimize the composition of the screen-printing paste itself, in order to be able to successfully contact ultrathin poly-Si layers using screen printing, will be undertaken. An alternative work plan is to investigate low-temperature inline plating, as a possible approach to contact our ultrathin SiO<sub>x</sub>/poly-Si contact passivation layers.

### 3.8 Cell efficiency potential prediction: single-sided versus double-sided contact passivation

As already indicated in the introduction part, we can determine a practical solar cell efficiency potential of our investigated solar cell structures, adopting either a rear-side-only passivated contact scheme or a double-sided passivated contact scheme. Using Brendel’s model [54], and explicitly considering measured front-side contact resistance and contact recombination parameters (i.e., the combined front-side saturation current density  $J_{0, front}$ , combining the contributions from both the non-metallized/passivated regions  $J_{0, non-metal}$  and from the metallized regions  $J_{0, metal}$ ), it is possible to calculate a practical solar cell efficiency potential as a function of the rear-side passivated contact layer properties, i.e., the rear-side recombination current density  $J_{0, rear}$  and the rear-side contact resistance  $R_{c, rear}$  of the rear-side passivated solar cell contact. By fixing the front-side  $J_{0, front}$  and  $R_{c, front}$  contributions, iso-efficiency contour plots can be calculated as a function of the rear-side  $J_{0, rear}$  and the rear-side  $R_{c, rear}$  (thereby generalizing Brendel’s model [54]). The goal of the cell efficiency prediction is twofold: (1) to determine if adopting a double-sided passivated contacts scheme is better than the single-sided (rear) passivated contact scheme and (2) to determine if a full-area rear-side contacting scheme is better than a bifacial contacting scheme.

Firstly, **Figure 24** shows a comparison of solar cells with a rear-side-only passivated contact scheme, comprising a conventional front-side textured surface with a boron-diffused emitter, passivated by a standard AlO<sub>x</sub>/SiN<sub>x</sub> double-layer



**Figure 24.**

Practical solar cell efficiency potential for a rear-side-only passivated contact solar cell (as a function of the quality of the rear-side passivated contact, i.e., its recombination current density  $J_{0, \text{rear}}$  and its contact resistance  $R_{c, \text{rear}}$ ), adopting a conventional front-side boron-diffused emitter and a rear-side electron-selective  $\text{SiO}_x/\text{poly-Si}(n^+)$  passivated contact, realized either in a full-area contact configuration or in a bifacial contact configuration. The measured current recombination densities  $J_{0, \text{rear}}$  and the correspondingly measured contact resistances  $R_{c, \text{rear}}$  of our developed rear-side  $\text{SiO}_x/\text{poly-Si}(n^+)$  electron-extracting passivated contacts are inserted within the iso-efficiency plot (blue dot, full-area contact; black square, bifacial contact). The corresponding practical solar cell efficiency potential using our developed  $\text{SiO}_x/\text{poly-Si}(n^+)$  passivated contacts is 22.3%, if a full-area rear-side contact is deployed, and 22.5%, if a bifacial contact is deployed.

anti-reflection coating and metallized by conventional screen printing (using a fire-through Ag-Al paste). The rear side composes of our developed electron-selective passivated contacts (thermal- $\text{SiO}_x/\text{poly-Si}(n^+)$ ), utilizing an experimentally achievable  $\sim 10$ -nm-thick poly-Si( $n^+$ ) layer and either a full-area Ag contact or a bifacial Ag contact with a contact area fraction similar to the front side (6%). For the efficiency potential prediction, a conservative, industrial feasible  $J_{0, \text{front}}$  value of  $131 \text{ fA cm}^{-2}$  and  $R_{c, \text{front}}$  value of  $\sim 5 \text{ m}\Omega \text{ cm}^2$  have been used. This corresponds to a  $J_{0, \text{front, pass}}$  value of  $45 \text{ fA cm}^{-2}$  underneath the  $\text{AlO}_x/\text{SiN}_x$  passivated B-diffused regions [74] and a  $J_{0, \text{front, metal}}$  value of  $1480 \text{ fA cm}^{-2}$  underneath the metal contacts [2, 75, 76], assuming a front-side metal contact area fraction of 6%.

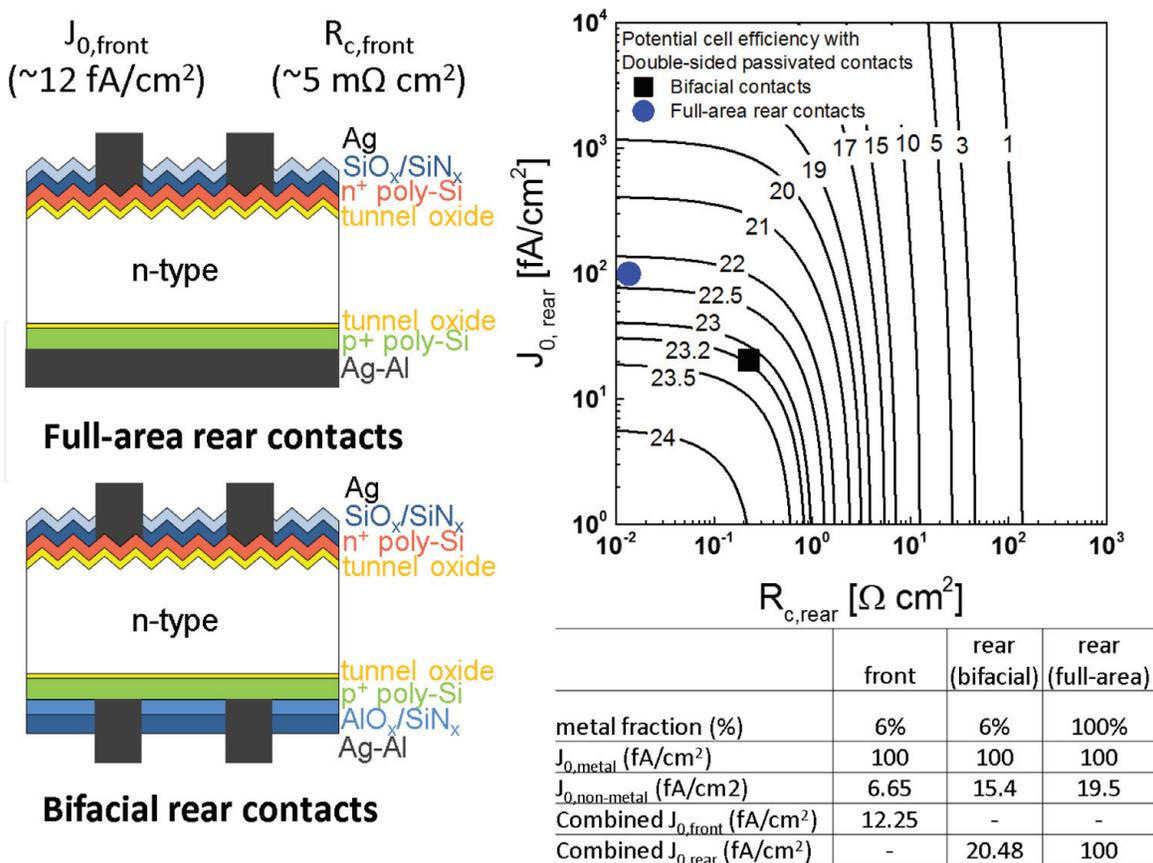
Regarding our developed rear-side  $\text{SiO}_x/\text{poly-Si}(n^+)$  contact passivation layers, the corresponding properties have been measured explicitly: Utilizing the symmetrical planar lifetime test structures with electron-selective passivated contacts discussed in earlier sections, the single-sided  $J_{0, \text{rear, pass}}$  values for the as-deposited and for the additionally  $\text{SiN}_x$ -capped samples were measured as  $4.5$  and  $2.5 \text{ fA cm}^{-2}$ , respectively. The recombination current density underneath the metal contact  $J_{0, \text{rear, metal}}$  has been determined separately as  $\sim 100 \text{ fA cm}^{-2}$ , using intensity-dependent PL imaging and our in-house developed Griddler software [77]. Please note that metal contact recombination after industrial screen printing is significantly reduced (more than one order of magnitude) if deploying contact passivation (i.e., comparing a  $J_{0, \text{front, metal}}$  value of  $1480 \text{ fA cm}^{-2}$  to a  $J_{0, \text{rear, metal}}$  value of

$\sim 100 \text{ fA cm}^{-2}$ ). Thus, a combined  $J_{0, \text{ rear}}$  value can be determined to be 8.35 and  $100 \text{ fA cm}^{-2}$  in case of a rear-side bifacial contact scheme or a full-area rear-side contact scheme, respectively (see **Figure 24**).

As discussed in Brendel's paper [54], in case of a rear-side bifacial contact, the recombination current density  $J_{0, \text{ rear}}$  scales with the rear-side contact area fraction, whereas the effective rear-side contact resistance  $R_{c, \text{ rear}}$  scales inversely with the rear-side contact area fraction. Again, regarding our developed rear-side  $\text{SiO}_x/\text{poly-Si}(n^+)$  contact passivation layers, the contact resistance  $R_{c, \text{ rear}}$  of our developed tunnel layer passivated contact has been measured explicitly: Based on our dark I-V test structures, as described in the introduction part of this paper and outlined in **Figure 1(f)**, the values for the bifacial and full-area rear-side contacts were measured to be  $0.22 \Omega \text{ cm}^2$  and  $13.3 \text{ m}\Omega \text{ cm}^2$ , respectively. These  $J_{0, \text{ rear}}$  and  $R_{c, \text{ rear}}$  values were then inserted into our calculated iso-efficiency contour plot in **Figure 24**, allowing a realistic prediction of the efficiency potential for a rear-side passivated contact solar cell in a bifacial or full-area configuration: As can be seen, the practical solar cell efficiency potential of a solar cell, adopting a conventional front-side boron-diffused emitter and a simple full-area rear-side passivated contact, is 22.3%. In case a bifacial contact is deployed, the practical solar cell efficiency potential is 22.5%. Using a rear-side bifacial contact instead of a full-area rear-side contact can therefore slightly enhance the solar cell efficiency by a relative gain of 0.9%.

The corresponding calculation of the practical efficiency potential for double-sided passivated contact solar cells is shown in **Figure 25**. As discussed in earlier sections, this solar cell concept features an optimized solar cell architecture considering our experimental finding, i.e., featuring a textured front surface with an electron-selective passivated contact (thermal- $\text{SiO}_x/\text{poly-Si}(n^+)$ ) and a planar rear surface with a hole-selective passivated contact (thermal- $\text{SiO}_x/\text{poly-Si}(p^+)$ ). The front surface of these cells is capped by a double-layer anti-reflection/passivation coating ( $\text{SiO}_x/\text{SiN}_x$ ) and assumed to be contacted via screen-printed fire-through Ag contacts. The rear-side hole-selective passivated contacts are assumed to be either contacted by a full-area Ag contact or to be capped by a double-layer anti-reflection/passivation coating ( $\text{AlO}_x/\text{SiN}_x$ ), forming a screen-printed bifacial fire-through Ag-Al contact.

Accordingly, in order to equate the rear-side  $J_{0, \text{ rear}}$  and  $R_{c, \text{ rear}}$  values for these two different contact schemes, we apply measured values, and we then plot the practical efficiency potential as a function of the quality of the front-side passivated contact ( $J_{0, \text{ front}}$  and  $R_{c, \text{ front}}$ ). The rear-side  $J_{0, \text{ rear}}$  value underneath the hole-selective passivated contact region was determined from the symmetrical lifetime test structures mentioned in earlier sections, while the rear-side  $R_{c, \text{ rear}}$  value was determined using the dark I-V test structures sketched in **Figure 1(f)** for the full-area case (using thermal evaporated Ag instead of screen printed Ag) and correspondingly inversely scaled with the contact-area fraction in case of the bifacial contact. It is to be noted that for our developed poly-Si( $p^+$ ) capping layers, the conventional screen-printing pastes were observed to consume the relatively thin poly-Si capping layer, thereby significantly degrading the rear-side  $J_{0, \text{ metal}}$  and  $R_{c, \text{ rear}}$  values (as reported in the former section). Nonetheless, in order to predict the practical efficiency potential of double-sided passivated contact solar cells, we assume this problem to be solved, i.e., we assume that applying a screen-printed contact on a hole-extracting poly-Si( $p^+$ ) capping layer will degrade our measured contact properties only in the same way as we observe it in case of an electron-extracting contact. Thus, as a first order of approximation, we assume the same  $J_{0, \text{ metal}}$  values for a metal contacting the hole-selective passivated contact as we measured it in case of a 250-nm-thick screen-printed  $\text{SiO}_x/\text{poly-Si}(n^+)$



**Figure 25.**

Practical solar cell efficiency potential for a double-sided passivated contact solar cell (as a function of the quality of the rear-side hole-extracting passivated contact, i.e., its recombination current density  $J_{0, rear}$  and its contact resistance  $R_{c, rear}$ ), adopting an ultrathin 10-nm electron-selective SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contact on the textured front-side and a hole-selective SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) passivated contact on the planar rear-side, realized either in a full-area contact configuration or in a bifacial contact configuration. The adopted  $J_{0, metal}$ ,  $J_{0, non-metal}$  and  $R_c$  values are based on own measurements (see text). The estimated current recombination density  $J_{0, rear}$  and the correspondingly estimated contact resistance  $R_{c, rear}$  of our developed hole-extracting passivated contact (assuming that the observed screen-printing issues have been solved) are inserted within the iso-efficiency plot (blue dot, full-area contact; black square, bifacial contact). The corresponding practical solar cell efficiency potential using our developed electron- and hole-extracting SiO<sub>x</sub>/poly-Si passivated contacts is 22.3%, if a full-area rear-side contact is deployed, and 23.2%, if a bifacial contact is deployed.

electron-selective passivated contact (100 fA cm<sup>-2</sup>), and we utilized measured  $R_{c, rear}$  values which we extracted using a thermal evaporated Ag contact instead of a screen-printed contacts, i.e., obtaining  $R_{c, rear}$  values of 0.225 and 13.5 mΩ cm<sup>2</sup> for the bifacial and full-area rear-contacts, respectively. The corresponding practical efficiency potential, as a function of the quality of the rear-side hole-extracting passivated contact ( $J_{0, rear}$  and  $R_{c, rear}$ ), is shown in **Figure 25**.

Comparing a front-side electron-extracting passivated contact to a conventionally applied front-side hole-extracting diffused contact (front-side boron-diffused emitter, passivated with AlO<sub>x</sub>/SiN<sub>x</sub> and metallized by bifacial screen printing) greatly improves the front surface passivation quality, reducing the  $J_{0, front}$  value from ~131 to ~12 fA cm<sup>-2</sup>, respectively. This can be (1) attributed to the excellent passivation quality of the developed electron-selective passivated contacts itself (6.65 fA cm<sup>-2</sup> on a textured silicon surface), which cannot be attained by conventional boron diffusion and AlO<sub>x</sub>/SiN<sub>x</sub> capping (~45 fA cm<sup>-2</sup>). Furthermore, the metal front-side contacts are now passivated (assuming  $J_{0, metal}$  ~100 fA cm<sup>-2</sup>, after industrial screen printing, as measured on 250-nm-thick poly-Si(n<sup>+</sup>) capping layers) instead of directly touching the doped silicon wafer ( $J_{0, metal}$  ~1480 fA cm<sup>-2</sup>). Therefore, a double-sided passivated contact solar cell has a good potential to obtain higher  $V_{OC}$  values at the cell level than a rear-side-only passivated

contact solar cell. To give an example, a bifacial double-sided passivated contact solar cell exhibits much lower total surface recombination ( $J_{0, \text{front}} + J_{0, \text{rear}}$  values of  $32.7 \text{ fA cm}^{-2}$ ) than a bifacial rear-side-only passivated contact solar cell ( $J_{0, \text{front}} + J_{0, \text{rear}}$  values of  $\sim 139.5 \text{ fA cm}^{-2}$ ), which is  $\sim 4$  times lower. The improved surface passivation should also directly translate to higher cell efficiencies, which is clearly shown comparing **Figure 25** to **Figure 24**. According to **Figure 25**, a double-sided passivated contact solar cell, using our developed  $\text{SiO}_x/\text{poly-Si}(n^+)$  and  $\text{SiO}_x/\text{poly-Si}(p^+)$  passivated contacts, exhibits a practical solar cell efficiency potential of  $\sim 22.3$  and  $\sim 23.2\%$ , respectively, using full-area or bifacial rear-side contacts. To recap, the corresponding practical efficiency potential in case of a rear-side-only passivated contact solar cell was 22.3 and 22.5%, respectively. Thus, in case of adopting a bifacial metallization scheme, a double-sided passivated contact solar cell is able to clearly outperform a rear-side-only passivated contact solar cell (practical efficiency potential of  $\sim 23.2\%$  as compared to 22.5%, using our developed contact passivation layers).

Again, the bifacial contact scheme appears more advantageous than deploying full-area rear-side contacts, exhibiting a significant 0.9% absolute (4% relative) increase in practical efficiency potential (analyzing double-sided passivated contact solar cells). If we compare bifacial silicon solar cells with a double-sided passivated contact scheme to rear-side-only passivated contact scheme, a respectable gain in cell efficiency by 0.7% absolute ( $\sim 3\%$  relative) is attainable. Interestingly, if we compare silicon solar cells which utilized full-area rear-side metal contacts, the practical cell efficiency potential for the double-sided passivated contact cell appears to be comparable to the rear-side-only passivated contact cell (both efficiency potentials are in the range of 22.3%). Given comparable  $J_{0, \text{rear}}$ ,  $R_{c, \text{rear}}$  and  $R_{c, \text{front}}$  values between the two schemes, it seems to indicate that a solar cell adopting a full-area rear-side passivated contact scheme exhibits a low sensitivity of the  $J_{0, \text{front}}$  values on the potential cell efficiency over a range of  $12\text{--}131 \text{ fA cm}^{-2}$  (i.e., the full-area rear-side contact is then limiting the cell efficiency). However, when bifacial contacts are considered, the performance gain by applying additional front-side passivation is substantial. This can be mainly attributed to the reduced recombination underneath the front-side solar cell contacts (further suppressing front-side recombination from 131 to  $12 \text{ fA cm}^{-2}$  while maintaining a low front-side contact resistance, i.e., comparing  $5\text{--}13 \text{ m}\Omega \text{ cm}^2$ ).

One suggestion to further improve the cell efficiency is to utilize laser-assisted local openings into the rear-side dielectrics (as demonstrated in **Figure 22**) and apply a full-area non-fire-through metal contact, which is expected to improve the rear interface reflectance and the corresponding collectable photocurrents.

To summarize, the net surface passivation quality on both the solar cell front-side and rear-side can be significantly improved by incorporating our in-house developed carrier-selective passivated contacts. A double-sided passivated contact scheme is predicted to deliver a  $\sim 3\%$  relative improvement of solar cell performance, as compared to a rear-side-only passivated contact scheme. Using a rear-side-only passivated contact scheme, i.e., deploying our in-house developed  $\text{SiO}_x/\text{poly-Si}(n^+)$  passivated contact layers and applying conventional bifacial screen printing, we have realized a solar cell efficiency of 21.7% (exhibiting a practical efficiency potential of 22.5%, using our standard boron-diffused front-side contact). The still prevailing challenge is to realize an industrial feasible metallization scheme on hole-extracting  $\text{poly-Si}(p^+)$  contact passivation layers, i.e., to develop suitable pastes to contact p-doped  $\text{poly-Si}$  by means of screen printing.

## 4. Conclusion

In this work, we demonstrate the potential of incorporating our in-house developed industrial relevant electron-selective (thermal-SiO<sub>x</sub>/poly-Si(n<sup>+</sup>)) and hole-selective (thermal-SiO<sub>x</sub>/poly-Si(p<sup>+</sup>)) passivated contacts into double-sided passivated contact solar cells. Using measured properties of our developed contact passivation layers (i.e., determining the recombination current density  $j_0$  and the contact resistance  $R_c$ ), we predict a practical efficiency potential approaching 24%, if device integrating them into a front-side textured, electron-extracting, and rear-side planar, hole-extracting solar cell architecture, applying conventional screen printing for contact formation (using a n-type 6-inch Cz wafer with a resistivity of 3.4 Ω cm). Thus far, we have reached a solar cell efficiency of 21.7%, rear side only integrating an electron-extracting SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contact and using conventional screen printing.

Our methodology of developing/optimizing (ultrathin) contact passivation layers is outlined as follows: First, we were comparing different tunnel oxides for their suitability to form passivated contacts when capped with highly doped poly-Si, i.e., we analyzed ultrathin (<1.5 nm) industrial relevant SiO<sub>x</sub> tunnel layers (i.e., wet-chemically formed silicon oxide (wet-SiO<sub>x</sub>), UV/ozone photo-oxidation-formed silicon oxides (ozone-SiO<sub>x</sub>), and in situ formed thermal silicon oxides, using low-pressure chemical vapor deposition (LPCVD) (thermal-SiO<sub>x</sub>)). Combining specifically designed lifetime and dark I–V test structures, we were able to extract the single-sided saturation current density  $j_0$  and its associated contact resistance  $R_c$  for our developed electron-selective and hole-selective passivating contacts. A subsequent optimization of the LPCVD of intrinsic poly-Si capping layers followed by conventional tube diffusion was undertaken, maximizing doping efficiency while minimizing in-diffusion of dopants from the poly-Si capping layer through the SiO<sub>x</sub> tunnel layer (which can act as a diffusion barrier) into the silicon wafer. After a subsequent standard SiN<sub>x</sub> passivation step, we reached implied open-circuit voltage  $iV_{oc}$  values exceeding 730 mV for electron-selective SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contacts and exceeding 710 mV for hole-selective SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) passivated contacts, formed on a planar silicon surface, using an in situ LPCVD-grown thermal-SiO<sub>x</sub> tunnel layer prior the LPCVD of the (intrinsic) poly-Si capping layer, and a subsequent tube diffusion. Applying these layers on a textured silicon surface, the electron-extracting SiO<sub>x</sub>/poly-Si(n<sup>+</sup>) passivated contact still performed well ( $iV_{oc} > 700$  mV), whereas the hole-extracting SiO<sub>x</sub>/poly-Si(p<sup>+</sup>) passivated contact showed unsatisfying performance on a textured surface ( $iV_{oc} \sim 630$  mV).

Subsequently, an asymmetric, front-side textured electron-extracting, rear-side planar hole-extracting passivated lifetime structure was processed, reaching an  $iV_{oc}$  of 713 mV. Two key challenges have been identified when aiming at a double-sided passivated contact device integration of these layers:

- (I) *Parasitic absorption*: There is always a significant amount of parasitic absorption within the poly-Si capping layer, which reduces the absorbed photogeneration current within the silicon wafer, and therefore the maximum possible short-circuit current of the solar cell. Thus, the poly-Si capping layers have to be designed to be as thin as technologically possible. This issue is even by far more important, if aiming at an additional front-side (i.e., double-sided) device integration of passivated contact. Numerical simulations (calibrated toward our developed contact passivation layers) indicate that a 10-nm-thin poly-Si layer still leads to a photogeneration

(i.e., short-circuit current) loss of  $\sim 1 \text{ mA/cm}^2$ , if front-side integrated, whereas the photogeneration loss saturates at  $0.05 \text{ mA/cm}^2$  for thicknesses lower than 25 nm, if rear-side integrated. A 25-nm-thin, front-side integrated passivated contact will already exhibit a parasitic absorption loss of  $5 \text{ mA/cm}^2$ , which is no longer suited for device integration (please note that the relation between the parasitic absorption loss and the thickness of the front-side integrated poly-Si contact passivation layer is rather exponential than linear in this case). In order to develop ultrathin ( $\leq 10 \text{ nm}$ ) contact passivation layers, two different process methodologies have been developed: (1) using etch-back technology that is starting from 250-nm-thick poly-Si “standard” layers (as described above) and applying a slow silicon etch (SSE) to reduce the thickness in a controlled way. Using this technology, we were able to obtain ultrathin 3–4-nm hole-extracting  $\text{SiO}_x/\text{poly-Si(p}^+)$  passivated contacts, which are basically maintaining the passivation properties of the thick layers (our corresponding 3–4-nm-thin  $\text{SiO}_x/\text{poly-Si(p}^+)$  contact passivation layers reached an implied open-circuit voltage  $iV_{oc}$  of  $\sim 690 \text{ mV}$  on a planar silicon surface). However, etch-back technology for electron-extracting passivated contacts was possible only down to a thickness of 70 nm. (2) Therefore, we re-optimized the diffusion conditions for ultrathin (10 nm) LPCVD of intrinsic poly-Si layers, which were subsequently subjected to phosphorous tube diffusion in order to obtain 10-nm-thin poly-Si( $n^+$ ) electron-extracting capping layers suitable for front-side device integration. Our 10-nm  $\text{SiO}_x/\text{poly-Si(n}^+)/\text{SiN}_x$  contact passivation layers reached an implied open-circuit voltage  $iV_{oc}$  of 720 mV on a textured silicon surface.

- (II) *Compatibility with conventional screen printing*: For “thick” (250–150 nm) electron-extracting  $\text{SiO}_x/\text{poly-Si(n}^+)/\text{SiN}_x$  contact passivation layers, conventional screen printing creates no issue. Correspondingly, rear-side-only passivated contact solar cells have been processed, reaching a solar cell efficiency of 21.7% (exhibiting a wet-chemically formed  $\text{SiO}_x$  tunnel layer and a 250-nm poly-Si( $n^+$ ) capping layer further passivated by  $\text{SiN}_x$  at the rear side of the solar cell and exhibiting a conventional boron-diffused,  $\text{AlO}_x/\text{SiN}_x$  passivated standard emitter at the front side of the solar cell, subsequently being metalized by conventional bifacial screen printing).

However, contacting hole-extracting poly-Si( $p^+$ ) layers or ultrathin electron-extracting poly-Si( $n^+$ ) layers is a challenge. Trying to contact hole-extracting poly-Si( $p^+$ ) layers by screen printing, using conventional fire-through Ag/Al pastes (as used to contact p-doped silicon material), we observe several local “punch-through” contact regions, where the paste is completely consuming the underlying poly-Si( $p^+$ ) capping layer, causing a severe degradation of contact passivation quality underneath the metal contact (i.e., there is no more contact passivation). This issue can be attributed to local aluminum alloying processes, which take place during fast-firing of Al containing screen-printing pastes: Al alloying is known to partially consume crystalline silicon material; thus, our thin poly-Si( $p^+$ ) capping layers will be consumed upon contact firing, leading to the just outlined local “punch-through” effects. Therefore, the chemical composition of the screen-printing paste itself has to be altered, in order to enable a subsequent damage-free contacting of our (thick or ultrathin) poly-Si( $p^+$ ) capping layers. Corresponding research activities, in cooperation with a paste manufacturer, are currently initiated.

Furthermore, it seems that our current ultrathin, 10-nm electron-extracting poly-Si(n<sup>+</sup>) layers are not firing stable, especially if deploying high peak firing temperatures (they still do outperform conventionally diffused front-side contacts, though). Interestingly, this is not the case for our “standard” 250-nm-thick layers. ECV measurements confirm that after contact firing (fast-firing in order to form low resistivity contacts), the dopants within the poly-Si(n<sup>+</sup>) capping layer have out-diffused into the silicon wafer bulk, thereby effectively reducing field-effect passivation and thus the observed implied open-circuit voltage of the samples after contact firing. Thus, more efforts to render our ultrathin contact passivation layers firing stable, i.e., by deploying lower peak firing temperatures and/or changing the chemical composition of the ultrathin LPCVD of poly-Si capping layers itself, are necessary.

An alternative work plan is to investigate low-temperature metallization approaches, like inline plating.

Nevertheless, despite still having to solve a suited industrial metallization scheme for our ultrathin ( $\leq 10$ -nm) in-house developed industrial electron- and hole-selective SiO<sub>x</sub>/poly-Si/SiN<sub>x</sub> passivated contact layers, due to their excellent passivation and contact resistance properties, these layers have a huge potential to get device integrated into a double-sided passivated contact solar cell architecture, which exhibits a practical efficiency potential of 23.2%, using our measured layer properties for a corresponding numerical prediction. Double-sided passivated contact solar cells deploying bifacial contacts are definitely able to outperform rear-side-only passivated contact solar cells in the near future.

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