Chapter

Room-Temperature Formation of Intermixing Layer for Adhesion Improvement of Cu/Glass Stacks

Mitsuhiro Watanabe and Eiichi Kondoh

Abstract

Reliable and high-precision Cu/glass stacks are particularly desirable for micro-electromechanical systems and packaging technologies. One solution for improving the adhesion strength of Cu/glass stacks is to form adhesion layers between the Cu films and the glass substrate. Many studies have shown that a strong adhesion layer is formed at the interface by high-temperature annealing when a Cu alloy is used instead of pure Cu. It is important to reduce the temperature and process time in order to reduce the thermal budget and fabrication cost. Therefore, the room-temperature process for fabrication of Cu/glass stack is desirable. In this chapter, typical advanced low-temperature processes including room-temperature process are introduced.

Keywords: adhesion improvement, low-temperature process, room-temperature process, intermixing, Cu/glass stack

1. Introduction

In microelectromechanical system (MEMS) and packaging technologies, high reliability of Cu metallization of glass substrates is strongly required. In the field of structural materials, fusion welding such as arc welding and laser welding is usually applied for dissimilar-metal or dissimilar-material welding, but in these welding methods, extremely high energy are needed for melting of metals, and it is difficult for joining of micrometer-scale or nanometer-scale precision. Recently, solid-state welding methods such as friction stir welding and magnetic pulse welding are developed. These methods have no high energy comparing with the fusion welding because these methods are achieved for joining at solid state. However, atomic diffusion for achievement of joining needs to be accelerated at solid state. For acceleration of the atomic diffusion, friction is usually generated between the welding materials. Therefore, brittle materials such as glass and silicon wafer are broken when the solid-state welding methods are applied for the MEMS stacks. Also, these fusion welding and solid-state welding methods usually produce thick brittle intermixing layer such as intermetallic compound with a scale of micrometers or larger. The brittle layer produced at the interface lowers the mechanical strength of the joint. Therefore, atomically scaled interface bonding is demanded for fabricating a highly reliable Cu/glass structure.

One of the solutions for strengthening the interface bonding is the formation of an adhesion layer between a Cu film and a glass substrate. It is a common sense in vacuum engineering to insert a reactive metal such as Al or Ti between Cu and glass. However, this technique is not very useful in three-dimensional MEMS/packaging, because

these metals must be deposited with sequential high-vacuum deposition methods, which do not give a good step coverage. In addition, reactions between Cu and those metals can lead to a significant increase in resistance when the Cu film is thin.

Koike et al. have investigated the interfacial properties of the annealed Cu-Mn/glass structure and reported that adhesion improvement was observed by formation of a several nm thick Mn oxide layer at the interface [1, 2]. Yi et al. reported the formation of interfacial layer by annealing in Cu-Mg/glass and showed that the adhesion strength improved by formation of a Mg oxide layer at the interface [3]. Other elements, such as Al, Ti, and Cr, added to Cu were studied previously, and they were reported to improve the adhesion strength between Cu and various substrates (not only glass) [4–6]. These studies mentioned above indicate that the effective adhesion layers contain elements that are easily oxidizable and miscible in Cu. However, it should be noted that these studies required heat treatment during/after deposition. For achieving the general trend of temperature reduction during microelectronic fabrication, room-temperature or lower-temperature adhesion improvement is required.

2. Low-temperature bonding using ion beam etching

For bonding at lower temperature, surface refresh is one of the effective methods, because contamination such as oxide scale and inclusion is formed at material surface exposed in the atmosphere. The contamination usually prevents from bonding of the materials. High-energy ion beam irradiation is useful for cleaning of the contaminated material surface. When the ion beam irradiation and the bonding of materials having the refreshed surface are done at same high-vacuum environment (without exposing atmosphere), bonding of both activated surfaces is achieved without suing a high temperature. This method is usually called "surface activation method" (**Figure 1**) [7].

Research group of Suga has studied several combination of similar- and dissimilar-material bonding (Si/Si [8, 9], Al/Al [10], Cu/Cu [8], Si/SiO_2 [11]) using the surface activation method. Especially, aluminum always has strong oxide scale at the surface, but smooth and clear bonding interface without voids is formed by using this method (**Figure 2**) [10]. This indicates that ion beam irradiation is an effective

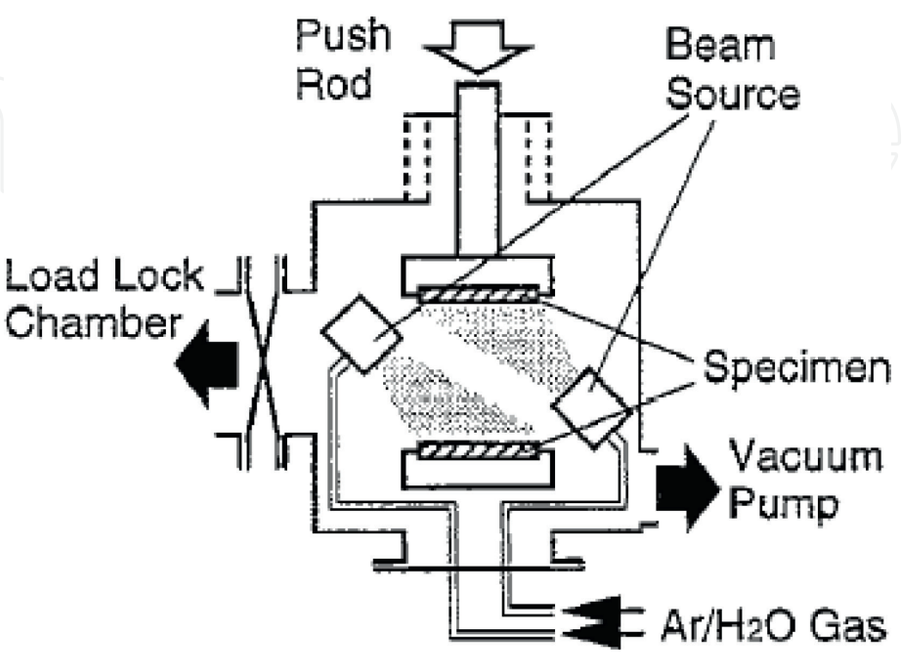

Figure 1.
Surface activation bonding method [11].

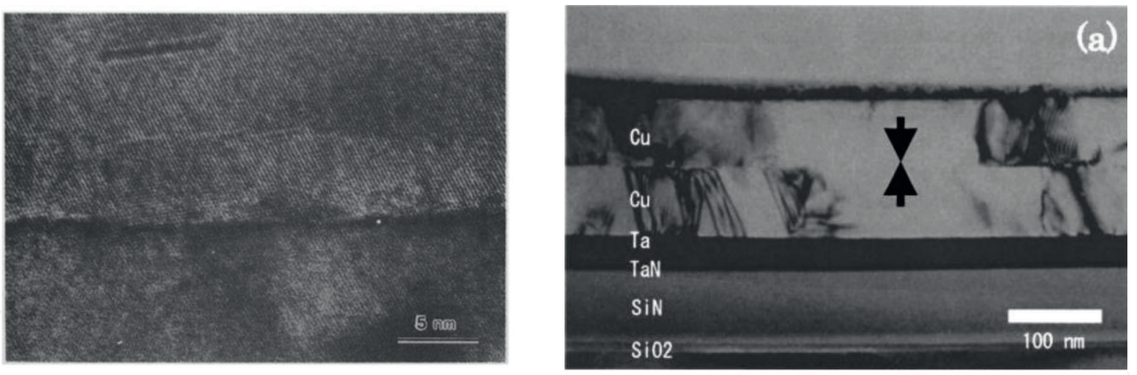

Figure 2.
TEM images of (a) Al/Al [10] and (b) Cu/Cu [8] interfaces fabricated by surface activation bonding.

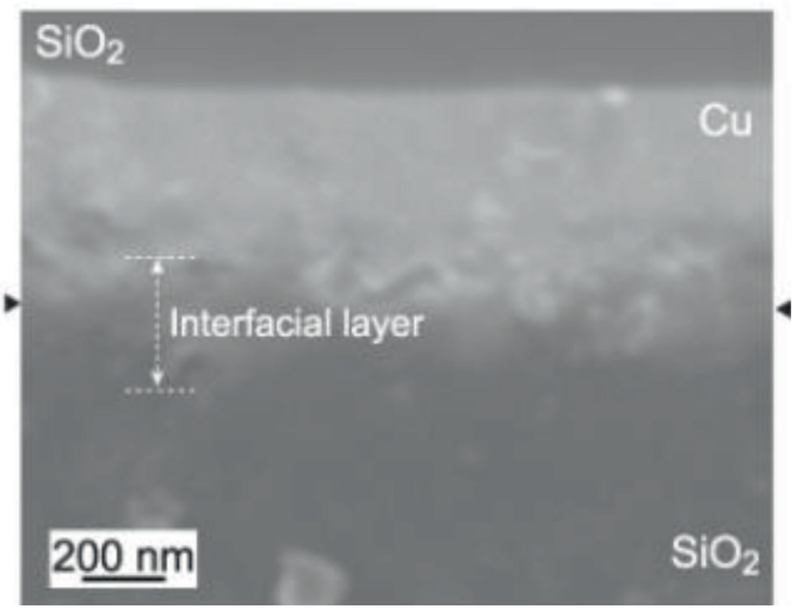

Figure 3.
Cu/SiO_2 interface fabricated by surface activation bonding [12].

method for removing the oxide scale. Also, achievement of bonding of Si and Si suggests that this method can be used for brittle materials. In addition, Takagi et al. reported the bonding of Si and SiO_2 using the surface activation method [11]. This indicates that this method can be achieved by the dissimilar-material bonding. A report on Cu/glass (Cu/SiO_2) bonding using the surface activation method also existed [12]. When the bonding temperature is increased to 423 K, good adhesion is obtained (**Figure 3**). The process temperature is very low than that of conventional diffusion bonding. This is considered to indicate that the surface cleaning by the ion beam irradiation is effective for the lower-temperature bonding.

3. Room-temperature formation of adhesion layer utilizing for adhesion improvement of Cu/glass stacks

As mentioned in Section 1, formation of adhesion layer at Cu/glass interface is an effective method for improvement of adhesion. Recently, we demonstrate room-temperature formation of Cu/glass stack with high adhesion strength [13, 14]. This adhesion improvement is due to effect of ZnO-based adhesion layer formed at room

temperature. The formation process is simple and affordable and is similar to that of electroless plating (ELP) of Cu. The research process leading to the development of this fabrication process is described below.

ZnO has gained considerable attention in microelectronics as an alternative transparent conductor [15, 16], because Zn is a recyclable, abundant, and affordable element. ZnO can be deposited by various techniques such as sputtering (SPT) [17, 18], sol-gel [19], chemical vapor deposition [20, 21], and supercritical fluid chemical deposition [22, 23]. In addition, Zn is miscible in Cu up to 38.27 at% Zn [24], and ZnO generally shows good adhesion to glasses or oxides [25, 26], indicating that ZnO is a potential adhesion layer in Cu/glass structures. Indeed, past research studies demonstrated that a ZnO layer works as an effective adhesion layer between Cu and glass [27, 28]. However, the films employed in those studies had micrometer thicknesses and a high-roughness surface topography, obviously inappropriate for micro-/nanoelectronic applications. Recently, we demonstrated that thin ZnO layers improve the adhesion between Cu and glass.

The relationship between the adhesion strength evaluated by a microscratch tester following JIS R3255 specifications and the Cu deposition method is shown in **Figure 4**. No delamination was observed in stack in which Cu was deposited by electroless plating (ELP) on a ZnO/glass substrate (ELP-Cu/ZnO/glass), whereas the adhesion strength of stack in which Cu was deposited using vapor deposition (VD) on a ZnO/glass substrate (VD-Cu/ZnO/glass) was low as well as that of the Cu/glass structure. Note that the glass substrate is fractured at the applied load of 500 mN; namely, the fracture of glass substrate occurred before the delamination in ELP-Cu/ZnO/glass stack. This means that the ELP-Cu/ZnO/glass stack has excellent adhesion.

Figure 5 shows the cross-sectional scanning transmission electron microscope (STEM) images and STEM-EDX (energy dispersive X-ray spectrometer equipped with STEM) maps of (a) the VD-Cu/ZnO/glass and (b) ELP-Cu/ZnO/glass stacks. In the VD-Cu/ZnO/glass stack, the Cu film, ZnO layer, and glass substrate were separately observed. At the Cu/ZnO interface, several voids were formed, as indicated by

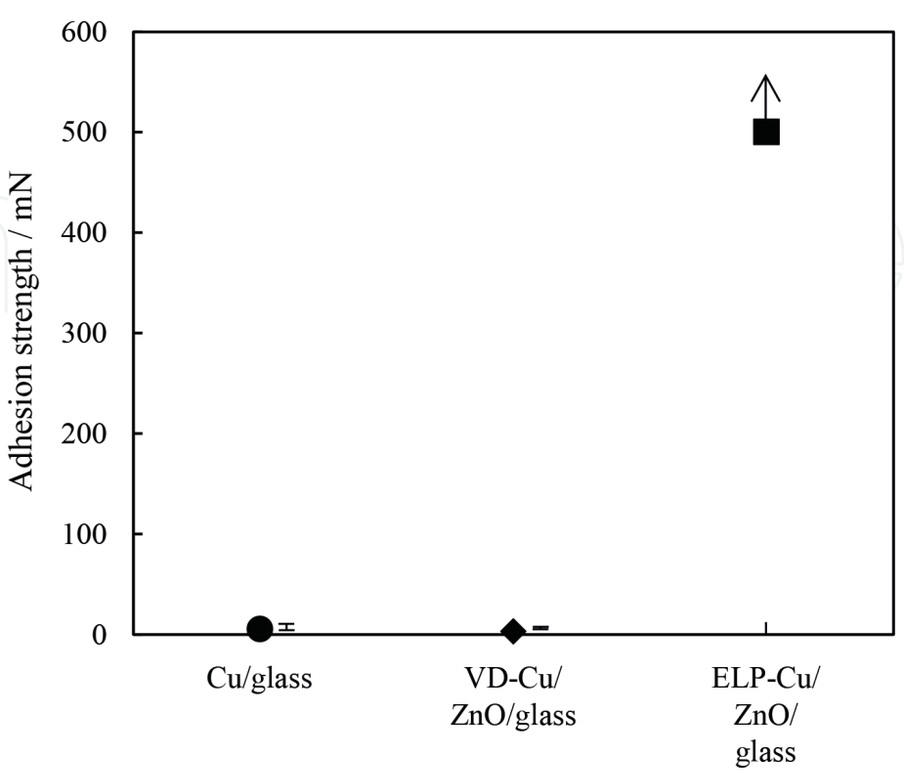

Figure 4.
Relationship between adhesion strength and deposition method.

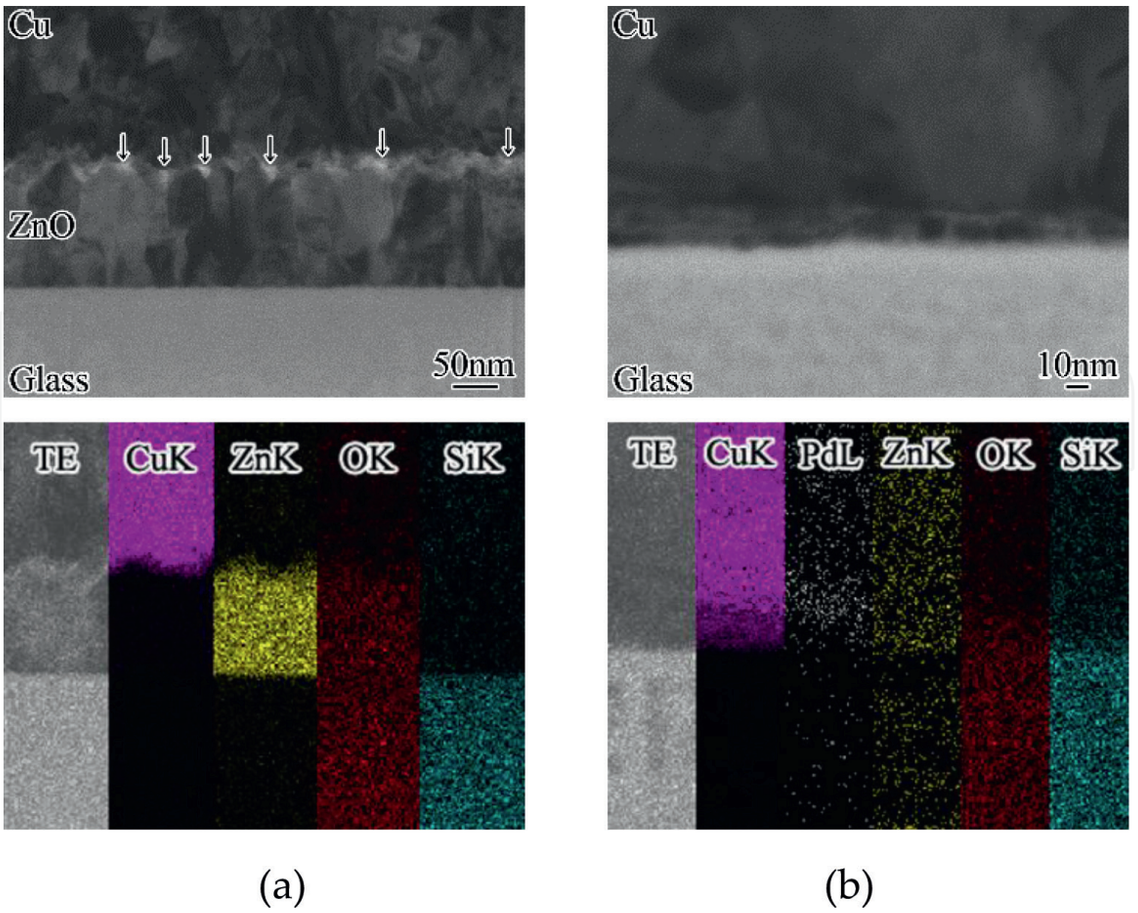

Figure 5.
Cross-sectional STEM images and STEM-EDX maps of (a) VD-Cu/ZnO/glass and (b) ELP-Cu/ZnO/glass stacks.

arrows in STEM image, indicating that the low adhesion strength is due to no intermixing at each interface. In contrast, the ELP-Cu/ZnO/glass stack exhibited a smooth interface, but no clear ZnO layer was observed. Careful observation revealed that the formation of an approximately 10-nm-thick layer was produced at Cu/glass interface. Strong Cu signals were obtained over the entire ELP-Cu film region, whereas a slight low Cu intensity was observed in the 10-nm-thick layer. Zn was detected at all regions of Cu film, 10-nm-thick layer, and glass substrate. Pd is a catalyst element used in the ELP, and it was observed in the 10-nm-thick layer. This indicates that Pd diffused into the ZnO layer during the ELP process, losing its original particulate shape (**Figure 6**). O and Si signals were detected in the 10-nm-thick layer. That is, the 10-nm-thick layer consists of Cu, Pd, Zn, O, and Si. The formation of such an intermixing layer at the Cu/glass interface significantly improved the adhesion.

When the VD process (processed at room temperature) was used to deposit the Cu films, an intermixing layer was not formed, and the ZnO layer was clearly observed, and voids were formed at the Cu/ZnO interface. On the other hand, it should be considered that the intermixing layer was formed during the ELP process, which was carried out at a deposition/plating temperature of almost room temperature (308 K). Also, ZnO layer was removed after Cu electroless plating. In addition, the SPT-Cu/ZnO/glass stack has also high adhesion strength like the ELP-Cu/ZnO/glass stack when pretreatment of Cu electroless plating was applied to the ZnO/glass substrate. In general, high temperatures were used to form such a reaction layer. The accelerated diffusion reaction is considered to be due to effect of catalytic role of Pd. We assume that the thinning of the ZnO layer decreased the diffusion distance of Cu and Si, which enhanced the Pd-promoted intermixing of Cu, Zn, O, and Si.

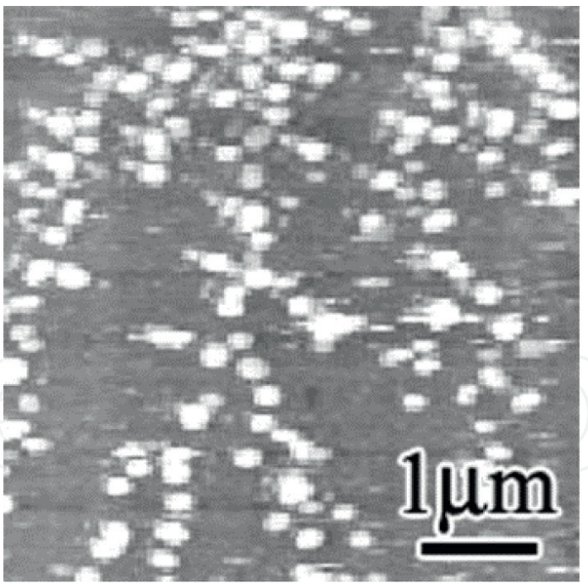

Figure 6.
Surface morphology of Pd-catalyzed ZnO/glass stack.

As mentioned above, the formation of intermixing layer at Cu/glass interface was found to result in adhesion improvement of Cu/glass stack. The intermixing layer is formed at room temperature, but reaction between Cu and glass does not occur at room temperature in general. For understanding the formation mechanism of intermixing layer at room temperature, the interfacial reaction at each process is necessary to be investigated.

At first, in order to confirm the incorporation of Zn into the glass (SiO_2) surface, the interfaces of ZnO/SiO_2 were examined before removing the ZnO layer [14]. This is because ZnO layer deposited at 673 K by metal organic chemical vapor deposition (MOCVD) was used in the results shown so far. **Figure 7** shows transmission electron microscope (TEM) images and Zn, Si, and O maps of the interfaces of (a) as-deposited MOCVD-, (b) as-deposited MBE-, and (c) annealed MBE-ZnO/glass stacks. Deposition temperatures of MOCVD- and MBE-ZnO were 673 K and room temperature, respectively. The MBE-ZnO/glass stack was then annealed at 623 K for 60 min. In the as-deposited MOCVD- and the annealed MBE-ZnO/SiO_2 stacks, approximately 5-nm-thick layer formation was observed at SiO_2 side of the ZnO/SiO_2 interfaces, whereas no reaction layer was observed at the as-deposited MBE-ZnO/SiO_2 interface. The Zn and Si signals were observed in the interfacial layer regions in the as-deposited MOCVD- and the annealed MBE-ZnO/SiO_2 stacks, whereas the as-deposited MBE-ZnO/SiO_2 stack showed very sharp transition between the Zn and Si intensities. These results indicate that Zn was diffused approximately 5 nm into the SiO_2 when the stacks were processed at high temperatures; i.e., the SiO_2 surface was doped with Zn by heat treatment during or after ZnO deposition.

Figure 8 shows a high-resolution TEM (HRTEM) image of the ZnO/SiO_2 interface. A typical amorphous structure having no fringe contrast can be observed in the glass substrate region. The lattice image is clearly observed in the interfacial layer regions as in the ZnO layer region, obviously proving that the interfacial layer is crystalline. **Figure 9(a)** shows a high-angle annular dark-field (HAADF) image of the ZnO/SiO_2 interface. The interfacial layer was composed of high-contrast regions (A in **Figure 9(b)**) and low-contrast regions (B in **Figure 9(b)**). TEM-EDX revealed that the A-region is Zn-containing SiO_2 (SiO_2(Zn)) and the B-region is an equilibrium Zn_2SiO_4 phase (**Table 1**).

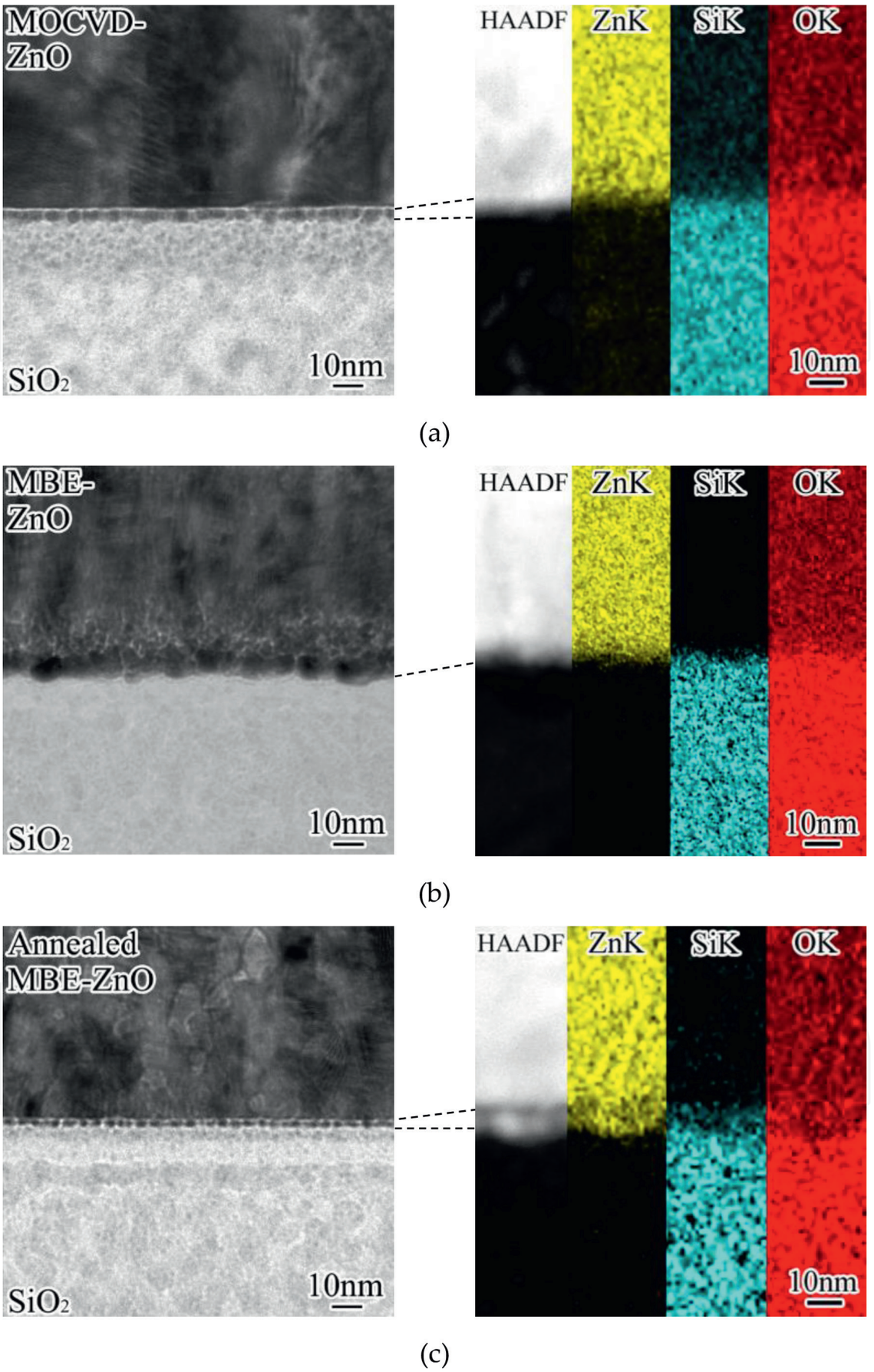

Figure 7.
TEM images and TEM-EDX maps of the interfaces of (a) as-deposited MOCVD-, (b) as-deposited MBE-, and (c) annealed MBE-ZnO/SiO_2 stacks. MBE means molecular beam epitaxy.

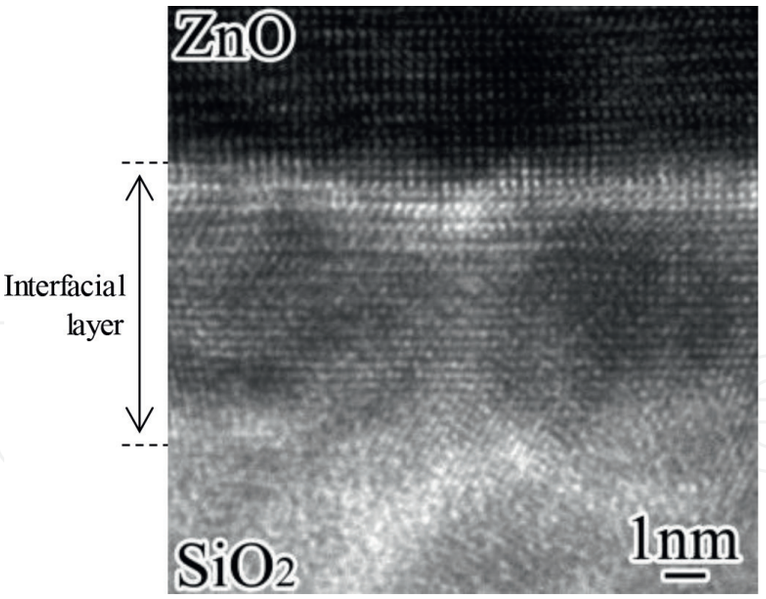

Figure 8.
HRTEM image of ZnO/SiO_2 interface.

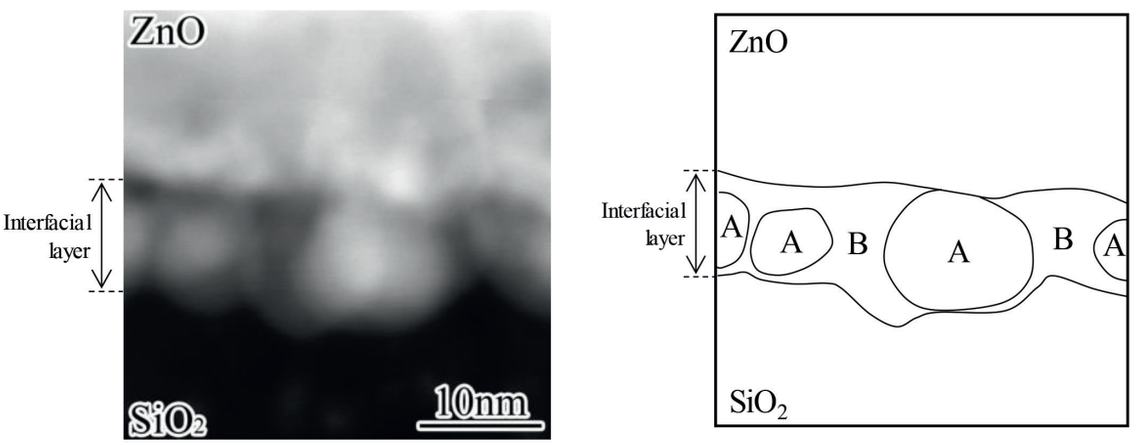

Figure 9.
(a) HAADF image of the ZnO/SiO_2 interface and (b) schematic illustration of (a).

	Atomic percentage		
	Zn	**Si**	**O**
A-region (higher-contrast region)	42	18	40
	46	16	38
	36	21	43
B-region (lower-contrast region)	27	17	56
	29	19	52
	33	17	50

Table 1.
TEM-EDX results of higher- and lower-contrast regions formed in interfacial layer.

The effect of dip to acid solution of ZnO/SiO_2 substrate was investigated. The dip to acid solution of substrate is surface treatment for substrate in conventional pretreatment of electroless plating. This process results in removing the ZnO layer.

TEM observation of the ZnO/glass stack after removing ZnO layer revealed the presence of an extremely thin surface layer (**Figure 10(a)**). Zn, Si, and O maps indicate that the surface layer consists of Zn, Si, and O (**Figure 10(b)**), and this composition distribution was similar to that of the interfacial layer formed at the ZnO/SiO_2 interface by heat treatment. This means that the interfacial layer remained at the SiO_2 surface as a Zn-doped layer even after the original thick ZnO layer being removed.

The relationship between noble metal particle and Zn-surface-doped layer was investigated. The noble metal particles (Pt in this case) and Cu films were deposited on the Zn-surface-doped SiO_2 and non-doped SiO_2, and the adhesion strength was investigated. When the Zn-surface-doped SiO_2 was used, remarkable adhesion improvement (>500 mN) was observed, whereas adhesion improvement was insufficient (26 mN) when the nondoped SiO_2 was used. This indicates that the doping of SiO_2 surface with Zn was effective for improving the adhesion at Cu/glass interface.

In order to know the effect of the noble metal particle on adhesion improvement, Cu was sputtered on the Zn-doped SiO_2 with/without Pt, Pd, or Pt-Pd particles, and the adhesion strength was evaluated. Remarkable adhesion improvement (>500 mN) was observed when Pt, Pd, or Pt-Pd particles were employed. This proves that Pt, Pd, and Pt-Pd particles are effective catalysts and, moreover, the combination of the Zn dope and the noble metal catalyzation enhances the adhesion between Cu films and SiO_2 substrate.

Figure 11 shows cross-sectional TEM image and EDX maps of the Cu/Pt/Zn-doped SiO_2 stack. The results were similar to that of the Cu/Pd/Zn-doped glass stack (**Figure 5(b)**). An extremely thin intermixing layer was clearly formed at the interface, and its composition was $Cu_{42}Pt_{18}Zn_{0.8}Si_{15}O_{22}$. From these observations, it is safely said that the formation of this intermixing layer results in the adhesion improvement. In the previous study, the formation of such an intermixing layer was observed when we used Pd as a catalyst, which shows the intermixing acceleration [13].

The effect of the kind of glass substrate on adhesion strength was investigated [29]. Each stack was fabricated by using each glass substrate (borosilicate glass, soda glass, SiO_2, SiO_2 thermal oxide growth on Si), SPT-ZnO layer, Pt as a catalyst, and SPT-Cu deposited at room temperature. Adhesion strengths were higher than 500 mN in any stacks, and no film delamination occurred even when any glass substrates were used. This means that Zn-doped layer was formed at each glass surface and that intermixing at room temperature occurred at Cu/glass interface. It is found that this adhesion enhancement is not influenced by the kind of glass substrate.

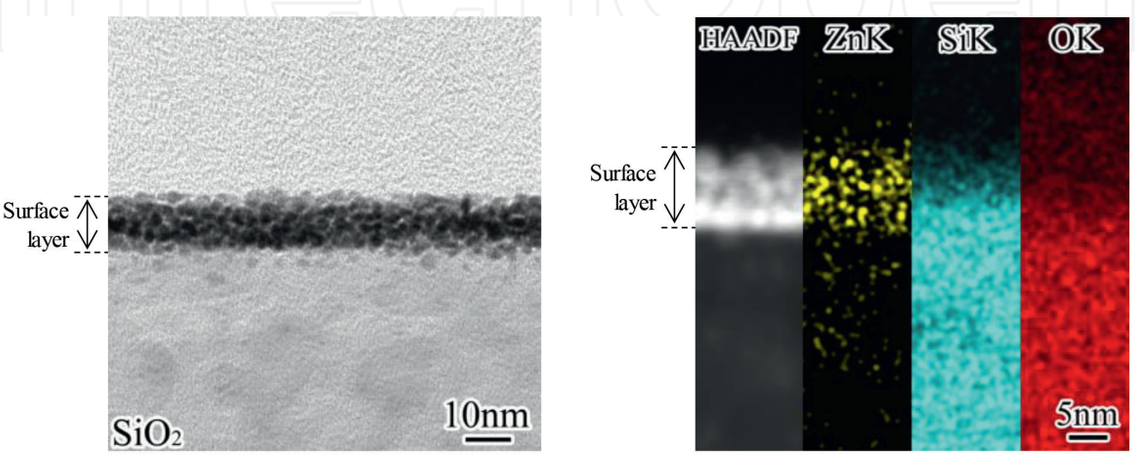

Figure 10.
(a) TEM image and (b) TEM-EDX maps of SiO_2 surface after the removal of ZnO layer.

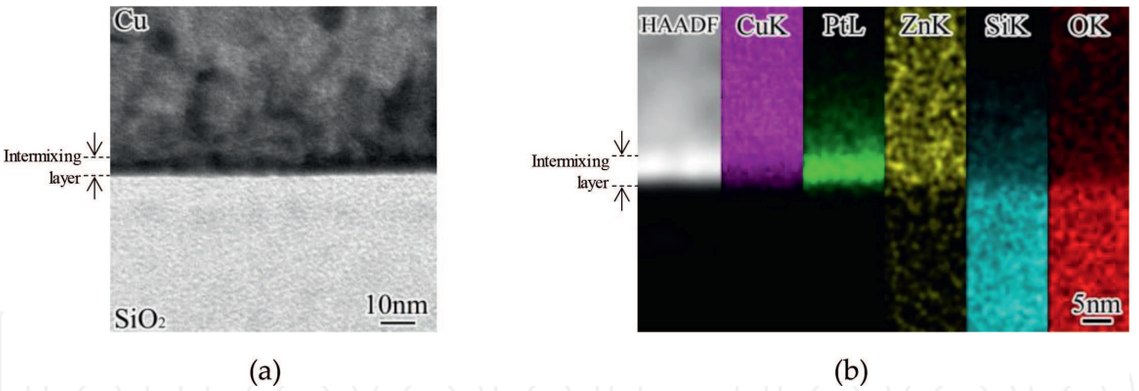

Figure 11.
(a) TEM image and (b) TEM-EDX maps of the interface of a Cu/Pt/Zn-doped SiO_2 stack.

The influence of the kind of ZnO layer on adhesion strength was examined [30, 31]. ZnO layer was fabricated by sol-gel method, metal organic decomposition (MOD), and supercritical fluid chemical deposition (SFCD), and we investigated whether these ZnO layers improve the adhesion of Cu/glass stacks. Adhesion strengths of Cu/glass stacks fabricated by using sol-gel-ZnO or MOD-ZnO were higher than 500 mN. When SFCD-ZnO was employed, adhesion strength (21 mN) was almost 20 times stronger than that of the Cu/non-treated glass stacks. The sol-gel- and MOD-ZnO layers were transparent as well as MOCVD- and MBE-ZnO layers, but the SFCD-ZnO layer had brown or white color. The color of the ZnO layer is considered to show crystallinity of ZnO. These results suggested that sol-gel-, MOD-, and SFCD-ZnO layers are effective for improving the adhesion of Cu/glass stacks and that the degree of improvement depends on the film quality.

From the above results, fabrication process of Cu/glass stack for significant adhesion improvement is shown in **Figure 12**. This process is simple and allows conventional Cu electroless plating or any other common Cu deposition methods, such as SPT and VD, to be used. **Figure 13** shows surface images of (a) VD-Cu/non-treated glass stack and (b) VD-Cu/glass stack fabricated using the process indicated in **Figure 12** after crosscut test (JIS K5600-5-6). It is clearly found that no Cu film delamination was observed in VD-Cu/glass stack fabricated using the process indicated in **Figure 12**, whereas Cu films were completely delaminated from glass substrate in VD-Cu/non-treated glass stack. The key in this process is the combination of Zn doping and noble metal catalyzation, which accelerates atomic intermixing at the Cu/glass interface. For obtaining the Zn-doped glass surface, annealing of the ZnO/glass stack during or after ZnO deposition was effective treatment.

Based on the observed results, interfacial reaction during fabrication process indicated in **Figure 12** is discussed. **Figure 14** shows schematic illustrations of the reaction at the ZnO/SiO_2 interface at 573–673 K. SiO_2(Zn) and Zn_2SiO_4 phases were produced at the interface (**Table 1**) by annealing of ZnO/SiO_2 stack at 623–673 K. This layer remained as the surface layer after ZnO removal. According to the ZnO/SiO_2 phase diagram [32], Zn_2SiO_4 is formed over 1573 K. This temperature is much higher than our process temperature. This indicates that the formed Zn_2SiO_4 phases were produced by diffusion reaction.

The reaction between ZnO and SiO_2 does not produce other compounds ($2ZnO + SiO_2 \rightarrow Zn_2SiO_4$). Therefore, based on our observations, we formulated a possible overall reaction as follows:

$$4ZnO + 2SiO_2 \rightarrow Zn_2SiO_4 + SiO_2(2Zn) + 2O \quad (1)$$

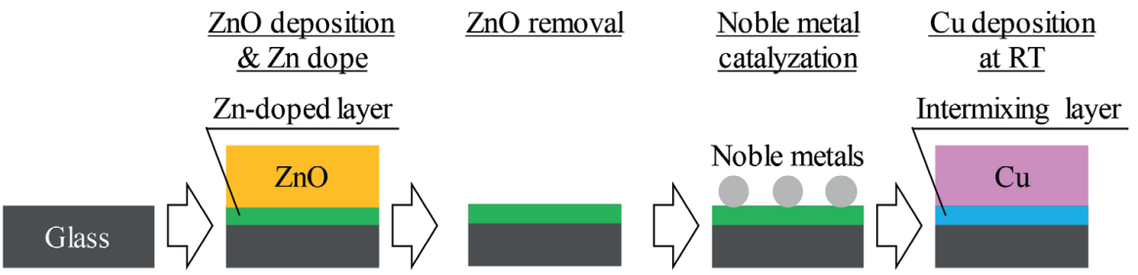

Figure 12.
Schematic diagrams of process for high-adhesion Cu/glass stack. RT means room temperature.

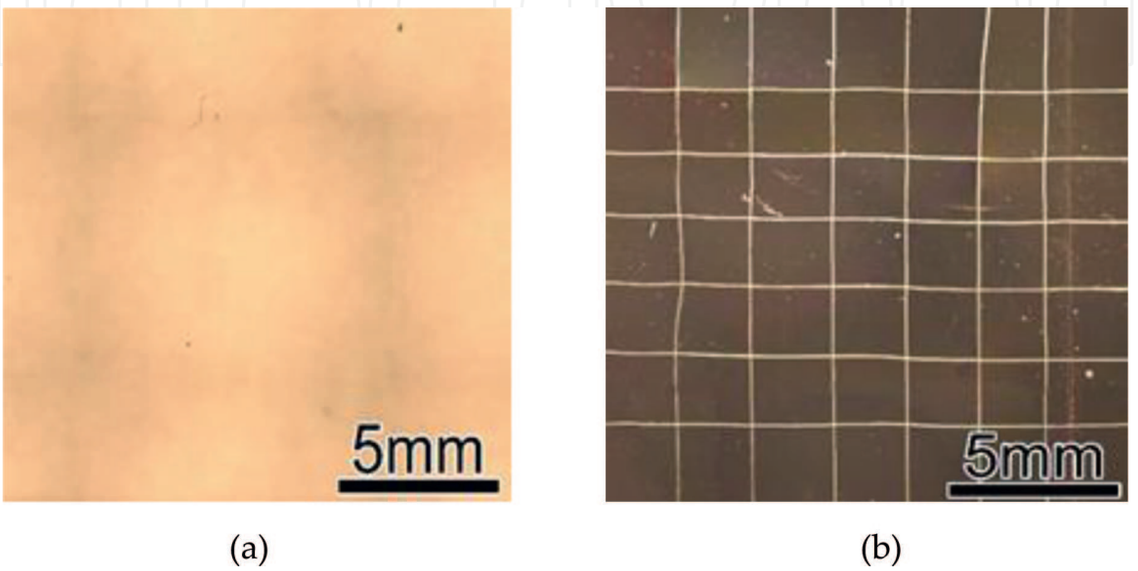

Figure 13.
*Macroscopic appearances of (a) VD-Cu/non-treated glass stack and (b) VD-Cu/glass stack fabricated by using the process for high-adhesion Cu/glass stack (**Figure 12**).*

where the coefficient of Zn is introduced as 2Zn to satisfy the stoichiometry of Zn. The bracket of Zn shows that Zn is free metal and dissolves in or coexists with the SiO_2.

The formula (1) indicates that the molar ratio of the formed Zn_2SiO_4 and the SiO_2(Zn) is 1:1 and that more ZnO is consumed in the reaction than SiO_2. Indeed, from the TEM-EDX analyses, the volumes of these phases are almost identical apart from the molar density of these phases. The stoichiometry also shows that free Zn forms and dissolves in SiO_2. As a result, as observed (**Table 1**), the Zn_2SiO_4 and the SiO_2(Zn) coexist at the interface.

Elementary reactions of reaction (1) can be expressed as follows:

$$ZnO + SiO_2 \rightarrow Zn_2SiO_4 \quad (2)$$

$$ZnO \rightarrow 2Zn + 2O \quad (3)$$

$$SiO_2 + 2Zn \rightarrow SiO_2(2Zn) \quad (4)$$

The above formulae simply indicate that ZnO is decomposed to Zn and O. Presumably, the formula (2) ignites these reactions to proceed. Once Zn diffuses into SiO_2, oxygen in ZnO becomes less and promotes oxygen diffusion.

Next, interfacial reaction of the formation of the intermixing layer is discussed. **Figure 15** shows schematic illustrations of the reaction at the Cu/Zn-surface-doped SiO_2 interface at room temperature. From the observation and analysis results, an extremely thin intermixing layer was formed at the interface at room temperature, and the composition of the layer was $Cu_{42}Pt_{18}Zn_{0.8}Si_{15}O_{22}$ (**Figure 11**). The composition ratio of Zn, Si, and O is Zn:Si:O = 2.1:39.7:58.2. This composition has a Si/O ratio close to 2:3. Therefore, we can safely say that this phase is an oxygen-deficient silicon oxide, presumably Si_2O_3 (SiO_2·SiO) that contains impurity Zn. The reactions can be expressed as the following formulae:

$$Zn_2SiO_4 + SiO_2(2Zn) \xrightarrow{Pt} SiO_2 \cdot SiO + 3O + 4Zn \quad (5)$$

$$Cu + Zn \rightarrow Cu(Zn) \quad (6)$$

The formula (5) is a Pt-catalyzed reaction. The catalytic reaction generates free oxygen and free Zn. As shown in **Figure 11(b)**, Zn was detected in Cu film. Therefore, the repelled Zn dissolves into the depositing Cu (**Figure 15**), because Zn is well miscible in Cu according to the Cu/Zn binary phase diagram [24]. The formula (6) expresses the dissolution of Zn in Cu.

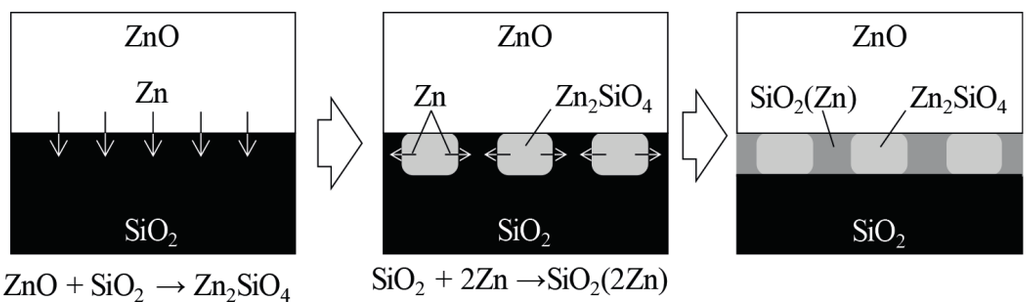

Figure 14.
Schematic illustrations of reaction at ZnO/SiO_2 interface at 573–673 K.

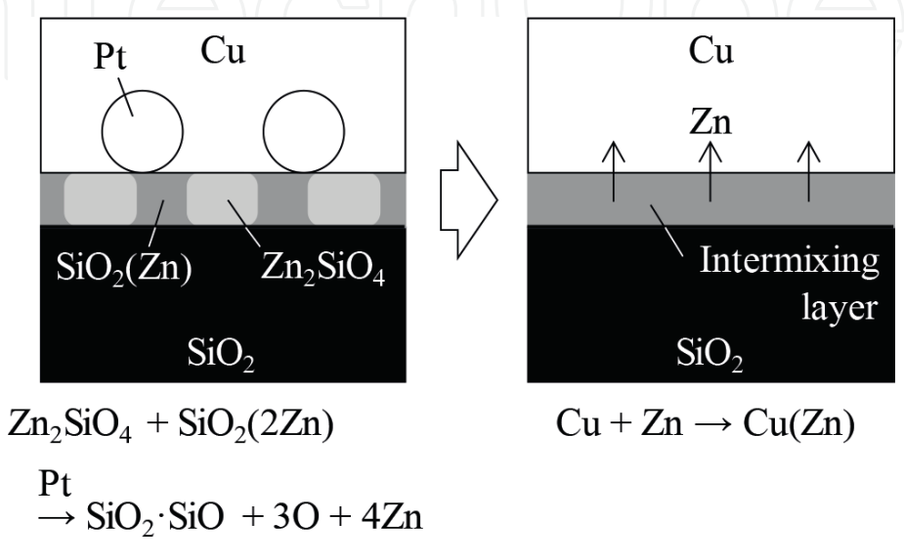

Figure 15.
Schematic illustrations of reaction at Cu/Zn-doped SiO_2 interface at room temperature.

4. Summary of this chapter and prospect for fabrication of the next-generation microelectronic devices

In this chapter, lower-temperature process for fabrication of high-adhesion Cu/glass stack was introduced. The surface activation bonding is one of the lower-temperature processes for similar- and dissimilar-material bonding. Also, room-temperature formation process of intermixing layer is also introduced. A nanoscale ZnO layer improves the adhesion strength between Cu and glass even if metallization was carried out at room temperature. A Cu/glass stack with a high adhesion strength is successfully fabricated by the combination of Zn dope and noble metal catalyzation. This remarkable adhesion improvement is due to the effect of formation of an intermixing layer at interface. As well-known, Cu and SiO_2 do not generally react at room temperature. Obviously, the noble metals lead to the intermixing acceleration, very likely by their catalytic effect.

These room-temperature/low-temperature processes achieve temperature reduction during microelectronic fabrication. In addition, it leads to formation of extremely thin (several nm thick) adhesion layer at the interface. The thickness reduction of adhesion layer can increase the area of the interconnection, and resistance of interconnection can be reduced. Therefore, these adhesion improvement processes at room temperature/low temperature is considered to be important for fabrication of a next-generation microelectronic device.

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Author details

Mitsuhiro Watanabe[1*] and Eiichi Kondoh[2]

1 Department of Precision Machinery Engineering, College of Science and Technology, Nihon University, Funabashi, Japan

2 Interdisciplinary Graduate School, University of Yamanashi, Kofu, Japan

*Address all correspondence to: watanabe.mitsuhiro@nihon-u.ac.jp

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