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On-Chip Interconnects of RFICs

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1. Introduction

Boosted by the demands of the rapidly growing wireless communication market, there is an increasing interest in the development of the radio frequency integrated circuits (RFICs). As highlighted by the International Technology Roadmap for Semiconductors (ITRS) annually, interconnect has become one of the most critical factors affecting the performance of ICs (ITRS, 2008). Thereafter, incorporating interconnect effects into the RFIC design flow becomes increasingly essential.

Because of the mature technology, low fabrication cost and high packing density, CMOS technology is deemed as a strong contender compared with other available technologies (Shi et al., 2005). Therefore, this chapter will mainly focus on the analysis of interconnects using conventional CMOS technology. Nevertheless, the authors would also like to shed some lights on some emerging interconnect concepts and technologies in the last part of the chapter.

1.1 Physical background

When an electric field, E, is applied, free electrons of the conductor begin to accelerate in the opposite direction to the applied E. Thus the average electron movement is in one direction. The movement of the charges and the established electric and magnetic fields are the basis for information transfer in interconnects. In order to understand interconnect behaviours in the RF ranges, several physical phenomena must be taken into consideration.

1.1.1 Inductive effect

The movement of the charges results in a magnetic field and hence the storage of the magnetic energy. The ability of a conductor to store the magnetic energy is described by its inductance.

At low frequencies, the impact of the magnetic field is often neglected, and interconnects are usually characterized by the conventional RC model (Kleveland et al., 2002). However, when the frequency increases beyond multi-Gigahertz, the inductive reactance of the interconnects becomes comparable to or dominant over the resistance. Therefore, the inductance and the magnetic field must be considered (Gala et al., 2002) in the Gigahertz frequency range. Hence, it becomes a major concern of the current interconnect modelling.

1.1.2 Skin effect

At low frequencies, current flow is uniformly distributed over the cross section of the conductor. The resistance of an interconnect with length l (m), width W (m) and thickness t (m) is given by (Plett & Rogers, 2003):

Source: Solid State Circuits Technologies, Book edited by: Jacobus W. Swart,
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$$R = \rho \frac{l}{tW} = R_s \frac{l}{W} \ (\Omega) \tag{1}$$

where ρ (Ω·m) is the resistivity of the interconnect material and R_s (Ω) is the sheet resistance based on DC measurements.

However, at high frequencies, say above 5 GHz, the EM fields attenuate substantially when they pass through the conductor. The current crowds to the surface of the conductor, as shown in Fig. 1. This is known as skin effect.

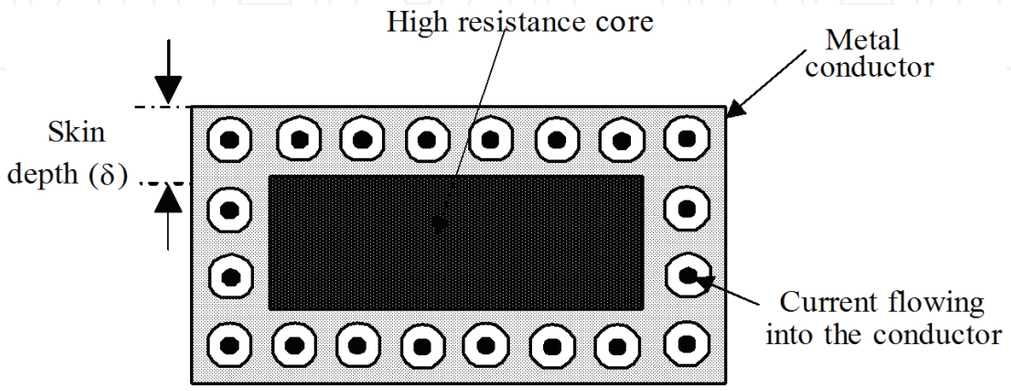


Fig. 1. Illustration of skin effect

The mechanism of skin effect can be explained either from an electrical circuit perspective or an electromagnetic perspective. From the circuit perspective, the currents in the conductor always flow in a way, which has the least impedance, i.e., $R+j\omega L$. For direct current, the imaginary part of the impedance is zero. The currents are distributed uniformly. This way of distribution has the least resistance or impedance. As the frequency increases, the imaginary part becomes more and more significant. While the current crowds to the surface of the conductor, the average distance between the currents is more than that of the currents which are distributed uniformly. Consequently, the magnetic coupling and the inductance are minimal, so is the impedance. From electromagnetic perspective, the electromagnetic waves are attenuated when they pass through the conductor. At a sufficient depth, all electric and magnetic fields are negligible and there is no current flow. The high-frequency voltage between the two terminals of the conductor creates a high-frequency electric field and a high-frequency current in the conductor and thus creates a magnetic field. This is equivalent to the situation where electromagnetic waves penetrate the conductor. Those fields are attenuated as they passing into the conductor. The currents inside the conductor weaken with the attenuation of the electric field.

At a sufficient depth, all the fields are negligible and there is no current. Hence, the effective cross section of the conductor shrinks with the increase of the frequency. Skin depth δ is defined in Eq. 2 in (Plett & Rogers, 2003). It refers to the depth from the surface of a conductor, where the currents are confined to flow.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \frac{1}{\sqrt{f\pi\mu\sigma}} \ (\text{m}) \tag{2}$$

where μ (H/m) and σ (S/m) are the permeability and the conductivity of the conductor respectively. ω (rad/s) represents the angular frequency, which is the product of 2π and the operating frequency f (Hz).
We now need to modify the conventional calculation of the resistance in Eq. 1 by replacing the geometrical cross-sectional area with the effective one. When $\delta << W$, t, the resistance formula could be approximated as Eq. 3 (Plett & Rogers, 2003):

$$R = \frac{\rho l}{Wt - (W - 2\delta)(t - 2\delta)} \ (\Omega) \tag{3}$$

As the skin depth decreases with the increasing frequency, the resistance of the conductor becomes frequency-variant. It increases along with the frequency. On the contrary, the inductance reduces. The reason is that at low frequencies, the magnetic energy is stored inside as well as outside the conductor. However, as frequency increases, the current flow is mostly concentrated near the surface of the conductor. Hence, the magnetic field becomes confined to the region outside the conductor.

1.1.3 Substrate effect

In current CMOS technologies, low-resistivity (1 to 20 Ω /cm (Marsh, 2006)) substrate is commonly used to improve yields and suppress the latchup. However, in RF ranges, the low-resistivity substrate causes significant high frequency losses. The silicon substrate therefore appears to be a major concern of the use of CMOS in multi-Gigahertz applications. Therein, its mechanism must be studied thoroughly and its effect must be considered.

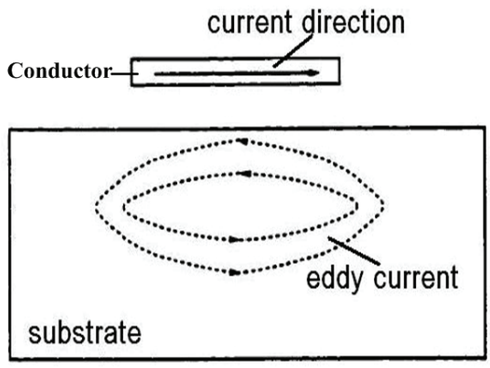


Fig. 2. Eddy currents in the substrate (Zheng, 2003)

The substrate affects interconnects in two ways: eddy current losses and substrate losses induced by the displacement currents injecting into the substrate (Chiprout, 1998). Fig. 2. illustrates the eddy currents in the substrate which are induced by the current flowing through the conductor. The eddy-current, in turn, will change the magnetic field and the inductance of the conductor. Particularly, if a high conductivity substrate is used at high frequencies, the eddy currents are strong and crowded near the surface of the substrate, the inductance is reduced and there are significant eddy current losses (Zheng, 2003). The impact of the eddy current is frequency dependent. For direct current, no eddy current is induced. The inductance is equivalent to that in the free space. As the frequency increases, the eddy current becomes stronger and more crowded to the surface.

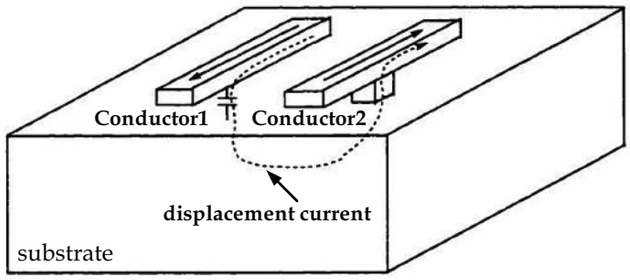


Fig. 3. Displacement current injected into the substrate (Zheng, 2003)

Fig. 3 illustrates the procedure of substrate losses derived from the injection of the displacement currents. The displacement currents flowing through the capacitance terminating on the substrate result in additional resistive losses. The capacitance to the substrate is also frequency-dependent. It is larger at higher frequencies because of skin effect of both the conductor and the substrate, as well as the frequency dependence of the effective permittivity (Zheng, 2003).

1.1.4 Corner effect

In most cases, straight-line interconnects are not adequate for on-chip interconnections. Interconnects with bends are often required. These bends are usually with angles of 90° or 45°. As mentioned in Section 1.1.2, the currents tend to flow in a path with the least impedance. Hence, in consequence of the appearance of the bends, the current distribution is different from that in straight-line interconnects. Fig. 4 illustrates the current distribution in the corners. This difference is known as the corner effect (Edwards & Steer, 2000).

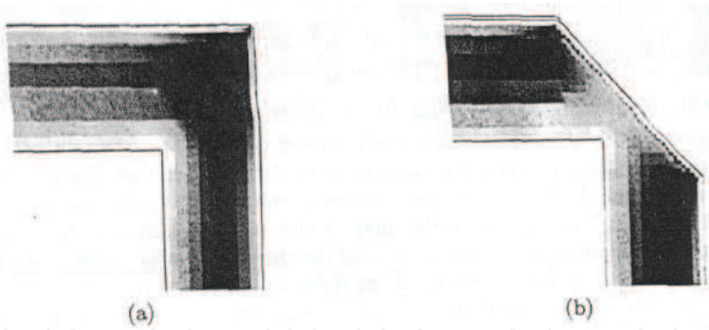


Fig. 4. Magnitude of the current densities at 10 GHz (a) right-angled bend; (b) an optimally mitred bend (Edwards & Steer, 2000).

1.1.5 Distributed effect

When the length of the interconnect is less than $\frac{1}{20}$ of the wavelength λ, the signal can be deemed as reasonably constant along the entire length of the interconnect. Hence it can be characterized with lumped components. However, when the length of the conductor is longer than $\frac{1}{10}$ of λ, the capacitance and inductance are distributed throughout the

interconnect. They cannot be confined to a lumped element. This effect is called distributed effects (Edwards & Steer, 2000).

1.2 Model development

Due to increased circuit complexity and higher operating frequency, the circuit performance becomes more and more subjected to interconnect behaviors. Inappropriate decision of interconnects in the design stage may lead to either over-design or excessive design iterations after tapeout. Therefore, there is an increasing need of adequate electronic design automation (EDA) tools for interconnect models from the industry. SPICE (simulation program with integrated circuit emphasis), developed by the University of California, Berkeley has become the industry standard simulation tool. With accurate models and precise model parameters, useful simulation results can be achieved to aid the IC design and significantly shorten the product-to-market time.

Besides SPICE-like circuit simulators, there are also electromagnetic (EM) simulators based on numerical solutions of Maxwell's equations that describe the EM behaviors of physical structures. EM simulators are capable of precisely analyzing the high frequency effects of the devices. However, they take up extremely high computing power and are very time consuming. Moreover, in-depth EM knowledge is required for using those EM simulators (Azadpour & Kalkur, 2002). Therefore, SPICE-compatible circuit models represented in capacitance, resistance and inductance, for instance, which are much easier to handle, are preferred by circuit designers.

In order to develop a desired equivalent circuit model for on-chip interconnects, there are mainly three stages to follow, namely, model construction, parameter extraction and model verification (Shi et al., 2008).

In the first stage, the model structure is established. The constructed interconnect model should be capable of characterizing the high frequency effects as well as incorporable with conventional EDA tools. The main challenge in this stage is that the interconnect behavior becomes frequency-variant at high frequencies. Although behavioral models, which can characterize the frequency-dependent characteristics, can be used in SPICE-like simulators, it is much slower than those only involve frequency-independent components. Therefore, characterizing the frequency dependent characteristics with frequency independent components would be more desirable.

In the second stage, model parameters are extracted. Essentially, the problem in parameter extraction is a multi-parameter and multi-target optimization. The accuracy, convergency and efficiency of the extracted data strongly depend on the chosen algorithm. Therefore, the algorithm should be selected, developed and applied appropriately.

Finally, the proposed model is verified with on-wafer measurements to ensure its accuracy.

2. Interconnect models

2.1 RC model

In many EDA tools, the interconnects are modelled as resistance and capacitance (RC) components (Celik et al., 2002; Shin et al., 2004), as shown in Fig. 5.

The calculation of the resistance for this model is straightforward. For a uniform structure with a rectangle cross-section the resistance can be calculated by Eq. 3. For the nonuniform or nonrectagle structures, the resistance calculation is more difficult. One aproach is to split the conductor into simple regions so that Eq. 3 can be applied to each region. Another approach is to formulate and solve the problem in terms of Laplace equations (Celik et al., 2002).

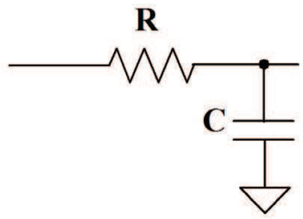


Fig. 5. RC model

For capacitance extraction, many techniques can be used, varying from simple 2-D analytical models to 3-D EM solvers (Celik et al., 2002).
This RC model is simple and straight forward. However, it becomes inadequate in the RF ranges.

2.2 Transmission line model

As stated in Section 1.1, when the operating frequency reaches multi-Gigahertz, inductive effect and distributed effect must be considered. Therefore, transmission line models are mostly studied and employed. The transmission line characteristics of an interconnect line can be mathematically formulated with the Telegrapher's equations (Pozar 1998) as listed below,

$$\begin{aligned} \frac{dV(x,t)}{dx} &= -(R + j\omega L)I(x,t) \\ \frac{dI(x,t)}{dx} &= -(G + j\omega C)V(x,t) \end{aligned} \tag{4}$$

where the voltage V and the current I along the line are both functions of position x and time t. R is per-unit-length (PUL) resistance, L is PUL inductance, G is PUL conductance and C is PUL capacitance. The RLGC model of the classical transmission line is shown in Fig. 6.

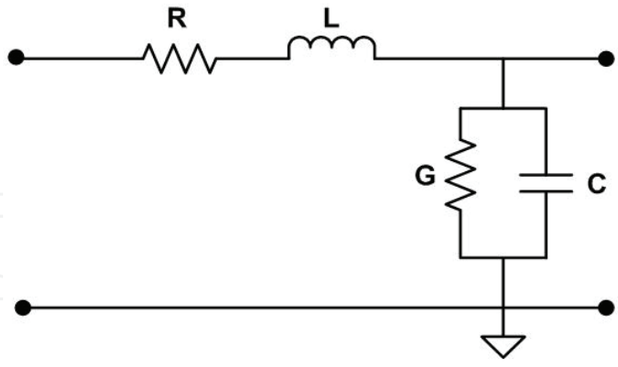


Fig. 6. Classical transmission line RLGC model

The standard solution to the Telegrapher's equations is

$$\begin{cases} V = V^{+}e^{-\gamma x} + V^{-}e^{+\gamma x} \\ I = \dfrac{1}{Z}(V^{+}e^{-\gamma x} + V^{-}e^{+\gamma x}) \end{cases} \tag{5}$$

where

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{6}$$

is the complex propagation constant and

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \ (\Omega) \tag{7}$$

is the characteristic impedance of the interconnect.
The line parameters (γ, Z, R, L, G and C) can be extracted from S-parameter measurements (Eisenstant & Eo 1992).

$$e^{-\gamma x} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \tag{8}$$

where

$$K = \sqrt{\frac{(1 + S_{11}^2 - S_{21}^2)^2 - (2S_{11})^2}{(2S_{21})^2}} \tag{9}$$

$$Z^2 = Z_o{}^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \tag{10}$$

where Z_o denotes the reference impedance of the S-parameter measurement system, which is usually 50 Ω. During the extraction of γ and Z from $e^{-\gamma x}$ and Z^2, extracted parameters with values that are not physically real, such as negative attenuation constants are ignored (Eisenstant & Eo 1992).
The line parameters R, L, G and C are extracted from S-parameter measurements as follows:

$$R = \mathrm{Re}\{\gamma Z\} \ (\Omega) \tag{11}$$

$$L = \frac{\mathrm{Im}\{\gamma Z\}}{\omega} \ (\mathrm{H}) \tag{12}$$

$$G = \mathrm{Re}\left\{\frac{\gamma}{Z}\right\} \ (\mathrm{S}) \tag{13}$$

$$C = \frac{\mathrm{Im}\left\{\frac{\gamma}{Z}\right\}}{\omega} \ (\mathrm{F}) \tag{14}$$

Since the characteristics of interconnects are frequency-variant, the extracted parameters are also frequency dependent. In order to fully describe the behaviour of high frequency interconnects with frequency independent components, the classical transmission line model is modified. Several model structures could be found in the literature, as shown in Fig. 7 to Fig. 10.

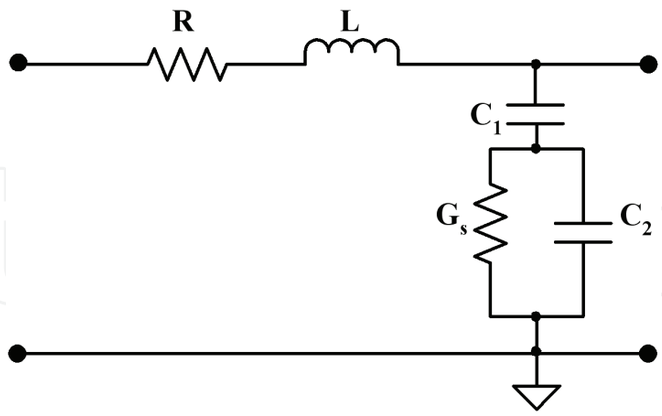


Fig. 7. Improved transmission line model 1 (Eo & Eisenstadt, 1993)

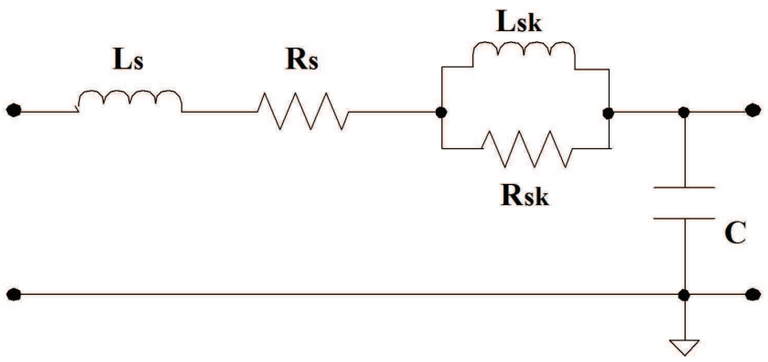


Fig. 8. Improved transmission line model 2 (Deutsch et al., 2001)

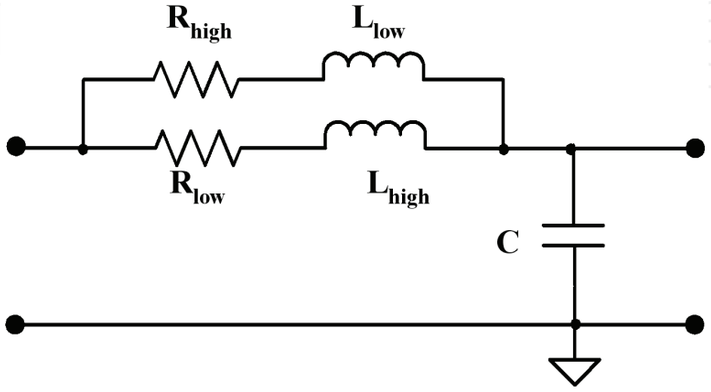


Fig. 9. Improved transmission line model 3 (Kleveland et al., 2002)

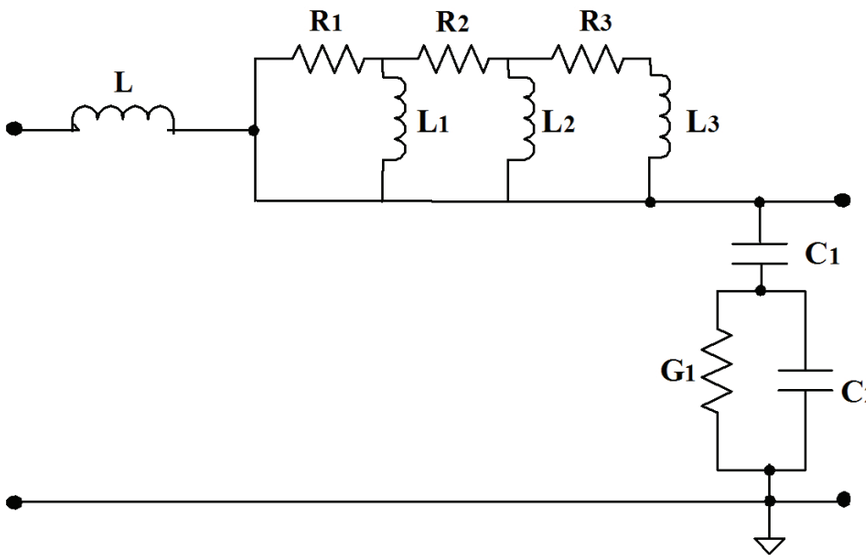


Fig. 10. Improved transmission line model 4 (Zheng et al., 2000)

2.3 Lumped element model

The RLGC parameters of the transmission line model characterize the PUL property. Therefore, the model complexity is proportional to the physical dimension of the interconnects. On the other hand, the on-chip RF interconnects can also be characterized by deliberately proposed lumped element models.

2.3.1 Straight-line interconnects

The function of interconnects is to connect different devices or blocks together. In the low frequency ranges, interconnects can be characterized by frequency-independent resistors (R) and capacitors (C). However, this RC model is not applicable at high frequencies. The reason is that as the frequency increases, the inductive effect, skin effect, substrate effect and distributed effect begin to have significant influences on the characteristics of the interconnects. All these effects are dependent on the frequency. In other words, the characteristics of RF interconnects are frequency-variant. Ideally, frequency-variant models should be used in the simulation. However, behavioural models which can characterize the frequency-dependent elements are much slower than models only involve frequency-independent components.

According to the notion described by Edwards and Steer in (Edwards & Steer, 2000), when the length of the interconnect is less than $\frac{1}{20}$ of the wavelength λ, the signal can be deemed to be reasonably constant along the entire length. Hence a lumped one-Π model shown in Fig. 11 is adequate. This one-Π model topology is widely used in the modelling of on-chip inductors.

With the increase in the length of the interconnect, the distributed effect begins to show its impact. When the length is longer than $\frac{1}{10}$ of λ, the transmission line model should be used (Edwards & Steer, 2000). λ can be calculated using Eq. 15.

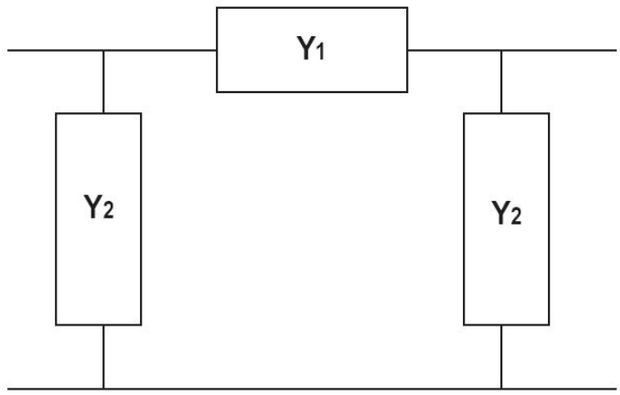


Fig. 11. Schematic block diagram of one-Π model

$$\lambda = \frac{c}{\sqrt{\mu_r \varepsilon_r} f} \quad \text{(m)} \tag{15}$$

where c is the speed of light in free space (3×10^8 m/s), f is the frequency under consideration, μ_r and ε_r are the relative permeability and permittivity of the material in which the signal propagates.

The transmission mode in the on-chip interconnect is not a pure transverse-electromagnetic (TEM) mode but a hybrid of transverse electric (TE) and transverse magnetic (TM) mode, known as a quasi-TEM mode (Marsh, 2006). Therefore, in order to apply Eq. 15, "effective" relative permittivity, which has a value between those of the substrate, the dielectric layer and the air, should be used. Here μ_r =1 and ε_r= (11.9+4.5+1)/3=5.8, where 11.9 is the relative permittivity of the silicon substrate, 4.5 is that of silicon dioxide and 1 is that of air, are used as a rough estimation of the CMOS process.

The criteria for choosing the model topology at various operating frequencies are summarized in Table 1.

Frequency (GHz)	0.3	5	15	30
lumped element model (μm)	20764.1	1245.9	415.3	207.6
Transmission line model (μm)	41528.2	2491.7	830.6	415.3

Table1 Critical Length of various frequencies

From Table 1, it reveals that for the intended frequency range, i.e., from 300 MHz to 30 GHz, the selection of the model topology is complicated. For example, at 30 GHz, the one-Π model is suitable only when the length of the on-chip interconnect is less than 207.6 μm, otherwise the validity of the model cannot be guaranteed. At 300 MHz, the transmission line model is appropriate only when the length is longer than 41528.2 μm; otherwise, it is not necessary to employ this topology. For typical RF circuit sub-blocks, such as low noise amplifier (LNA), voltage controlled oscillators (VCO) and mixer, the total die size is always smaller than 800 μm by 800 μm. Therefore, 800 μm is considered as the maximum length for on-chip interconnects of RFICs. Thus, both the lumped one-Π model and the transmission line model are not viable. The optimal model should be capable of characterizing high frequency behaviours of interconnects while keeping the model simple.

In order to maintain the simplicity, a two-Π model is developed based on the one-Π model. The problem of the one-Π model is that it cannot characterize the distributed effect which is significant at high frequencies. By strategically cascading two-Π lumped blocks together, as illustrated in Fig. 12, the distributed effects can be represented. In order to simplify the model construction and parameter extraction, the series blocks and shunt blocks are made to be identical of the two Πs. This optimization is physically acceptable due to the symmetrical structure of the straight-line interconnect.

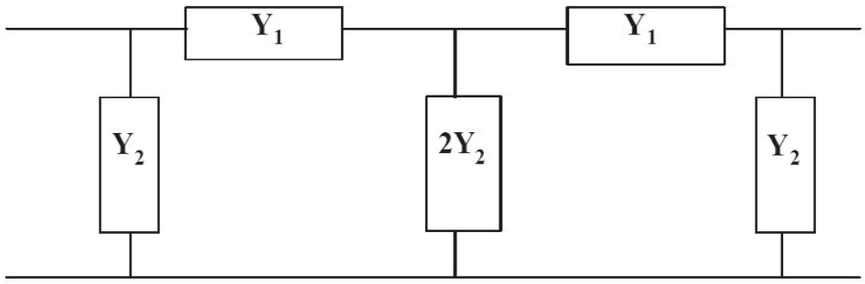


Fig. 12. Schematic block diagram of two-Π model

As shown in Fig. 13, based on the schematic block model, the two-Π equivalent circuit model is proposed from a physical point of view (Shi et al., 2005).

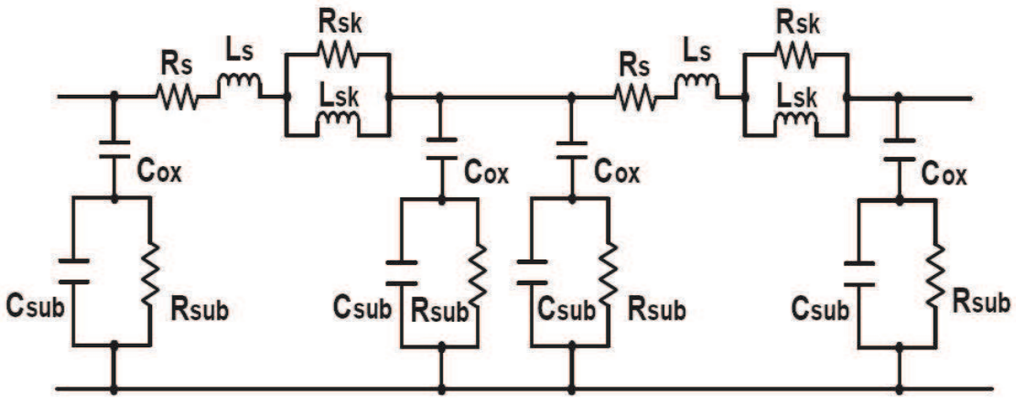


Fig. 13. Equivalent circuit model for straight-line interconnects (Shi et al., 2005)

With the significant increase of the operating frequency, the impact of the magnetic field and the magnetic coupling becomes one of the most emergent concerns of the RFIC design. In the two-Π model, the inductance is introduced by L_s, which represents the ideal series inductance. R_s represents the ideal series resistance. In RFICs, as the operating frequency approaches multi-Gigahertz, the skin effect becomes very significant. Although it must be included in the simulation, frequency-variant components are not supported by conventional circuit simulators. Hence, mimicking the frequency-variant skin effect with frequency-independent components becomes the straightforward solution.

In Fig. 13, the series components R_{sk} and L_{sk} connected in parallel are used to characterize the skin effect. Due to the skin effect, the behaviour of the interconnect becomes more resistive rather than inductive at high frequencies. In this parallel branch at low frequencies, most of the currents pass through L_{sk}. When the operating frequency rises, more currents

shift to the path of R_{sk}. With these two frequency-independent components, the frequency-variant skin effect characteristics are thus well captured.

Besides the skin effect, at Gigahertz frequencies the substrate losses are also substantial. In current CMOS RF technologies, high frequency losses are caused by the low-resistivity substrate (Chiprout, 1998; Zheng et al., 2000). As stated in 1.1.3 the substrate affects interconnects in two ways: eddy current losses and displacement current losses. The eddy currents in the substrate are induced by the current flowing through the conductor. The eddy currents, in turn, change the magnetic field and the inductance of the conductor. Particularly, if a high conductivity substrate is used at high frequencies, strong eddy currents will crowd near the surface of the substrate. As a result, the inductance is reduced and significant eddy current losses occur. This effect is characterized by L_{sk} and R_{sk} as well. As the frequency increases, the flow of the current shifts from L_{sk} to R_{sk}. Hence, the equivalent inductance reduces and the loss increases.

Another part of the substrate losses is derived from the substrate injection of the displacement currents. The displacement currents flow through the capacitance which terminates on the substrate. This results in additional resistive losses. The capacitance in the substrate is frequency-variant as well. It is larger at higher frequencies because of skin effect of both the conductor and the substrate, as well as the frequency dependence of the effective permittivity (Edwards & Steer, 2000). This effect is modelled by the resistor and capacitors in the shunt block. As shown in Fig. 13, C_{ox} represents the oxide layer capacitance, R_{sub} represents the substrate resistance and C_{sub} represents the capacitance of the substrate.

In the parameter extraction stage, an objective function is formulated to which an optimization algorithm is applied. Essentially, it is a multi-parameter and multi-target optimization. Optimizations can be made based on on-wafer measurements of the test structures to ensure the silicon verified accuracy.

At very high frequencies, measuring the voltages and currents is difficult in practice, since direct measurements usually involve the magnitude and phase of wave travelling in a given direction, or of a standing wave. Thus equivalent voltages, currents, related impedance and admittance matrices become somewhat of an abstraction (Pozar, 1998). Therefore, S-parameter is generally employed at radio frequencies.

The parameter extraction process is summarized as follows. Firstly, the admittance of each sub-block in Fig. 13 is derived as a function of the circuit components, as illustrated in Eq. 16 and Eq. 17.

$$Y_1 = \frac{1}{j\omega L_s + R_s + \dfrac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}} \tag{16}$$

$$Y_2 = \frac{1}{\dfrac{1}{j\omega C_{ox}} + \dfrac{R_{sub}}{j\omega C_{sub} R_{sub} + 1}} \tag{17}$$

The Y-parameters are presented as functions of the admittance of each sub-block Y_1 and Y_2, as illustrated in Eq. 18 to Eq. 21:

$$Y_{11} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2Y_1 Y_2} \tag{18}$$

$$Y_{12} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \tag{19}$$

$$Y_{21} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \tag{20}$$

$$Y_{22} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2Y_1Y_2} \tag{21}$$

On the other hand, the measured S-parameters are converted into Y-parameters, based on the equations from Eq. 22 to Eq. 25 (Pozar, 1998) as follows:

$$Y_{11} = \frac{1}{Z_o} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{22}$$

$$Y_{12} = \frac{1}{Z_o} \times \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{23}$$

$$Y_{21} = \frac{1}{Z_o} \times \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{24}$$

$$Y_{22} = \frac{1}{Z_o} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{25}$$

where Z_0 is the reference impedance of the S-parameter measurement system, which is usually 50 Ω.

By combining Eq. 18 - Eq. 21 with Eq. 22 - Eq. 25, Eq. 26 - Eq. 29 are obtained. By solving Eq. 26 - Eq. 29, the values of Y_1 and Y_2 can be obtained from the measurement results.

$$\frac{1}{Z_o} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2Y_1Y_2} \tag{26}$$

$$\frac{1}{Z_o} \times \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = \frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \tag{27}$$

$$\frac{1}{Z_o} \times \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \tag{28}$$

$$\frac{1}{Z_o} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2Y_1Y_2} \tag{29}$$

Therefore, the model parameter extraction becomes an optimization problem. The objective function $F_0(X)$ (Shi et al., 2005) of the optimization in Eq. 30 can be divided into two parts by the plus sign. The first part is the average error between the derived admittances and those obtained from the measurements. The second part is the variance of the error.

$$F_0(X)|_{X=(X_1,X_2,...,X_n)} = \sum_{i=1}^{m} \left\{ f_i(X)^2 + [f_i(X) - F_{mean}] \right\}^2 \tag{30}$$

In Eq. (30), the vector $X = (X_1, X_2, \ldots, X_n)$ represents the component values to be extracted, i.e., L_s, R_s, L_{sk} and R_{sk} of sub-block Y_1 and C_{ox}, C_{sub} and R_{sub} of sub-block block Y_2. n is the total number of parameters in each sub-block. m is the total number of frequency points under consideration. $f_i(X)$ is the error between the simulated admittance and the ones obtained from measurement results at each frequency point. The definition of $f_i(X)$ is given in Eq. 31. F_{mean} as defined in Eq. 32 is the mean error of the whole frequency range under consideration.

$$f_i(X) = \left| \frac{Y_{simulated(i)} - Y_{measured(i)}}{Y_{measured(i)}} \right| \tag{31}$$

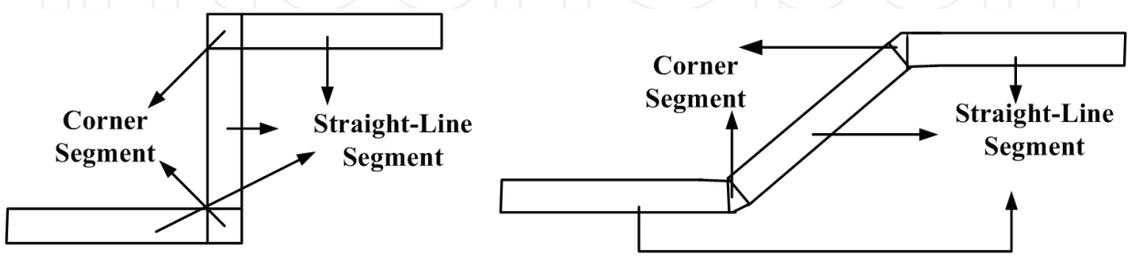
$$F_{mean} = \frac{\sum_{i=1}^{m} f_i(X)}{m} \tag{32}$$

The values of L_s, R_s, L_{sk} and R_{sk} of sub-block Y_1 and C_{ox}, C_{sub} and R_{sub} of sub-block Y_2 can be determined by searching for the minimum values of $F_0(X)$, starting from the reasonable initial guess.

2.3.2 Interconnects with bends

The interconnect shapes on a real chip are very complicated. Interconnect models which handle straight lines only are far from sufficient. Interconnects with bends are often required. These bends are usually with angles of 90° or 45°.

According to the physical configuration, the entire trace of the interconnects with bends can be divided into different sub-segments, i.e., straight-line segments and corner segments. The structural analysis and nomenclatures are illustrated in Fig 14.



a. interconnect with 90 degree bends **b. interconnect with 45 degree bends**

Fig. 14. Structural analysis of interconnect with bends (Shi et al., 2008)

Henceforth, the model development methodology can be proposed. Firstly, a complex-shaped interconnect is decomposed into sub-segments as shown in Fig. 15. Secondly, equivalent circuit models are developed for these sub-segments. Lastly, the sub-segments are cascaded to form the model of the entire interconnect.

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Fig. 15. Schematic block model of interconnect with bends (Shi et al., 2008)

A T-network as shown in Fig. 16 is used to characterize the interconnect bends of the CMOS process.

Fig. 16. Equivalent circuit model of the corner segment (Shi et al., 2008)

It is known that currents flowing round the corners distribute unevenly, such that most of the flows crowd around the inner edge (Edwards & Steer, 2000). Given in (Baker et al., 1997), the sheet resistance of straight lines is R_{square}, and the sheet resistance of corners is approximately $0.6 \times R_{square}$

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The construction of the complex-shaped interconnect model seems quit straightforward. However, simply connecting the sub-segments together will not lead to a precise model. The reason is that the inductance of a curved interconnect does not equal to the sum of the inductances of the straight-line sub-segments. Due to the mutual inductance cancellation of different sub-segments, the general trend is that the larger curvature an interconnect has, the smaller is the inductance. In order to characterize this effect, the series inductance in the Π-network of the straight-line segments which is connected to the corner segment should be modified. An additional parameter α (0< α <1), i.e., the multiplication factor, is introduced to represent this variation of the inductance. As illustrated in Fig. 18, inductance L_s in the second Π-network of *Straight-line Segment 1*, L_s in both of the two Π-networks of *Straight-line Segment 2*, and L_s in the first Π-network of *Straight-line Segment 3* are multiplied with the multiplication factor α. The influences of the corner can be omitted in the shunt blocks of the straight-line segments, so that the parameters are kept unchanged.

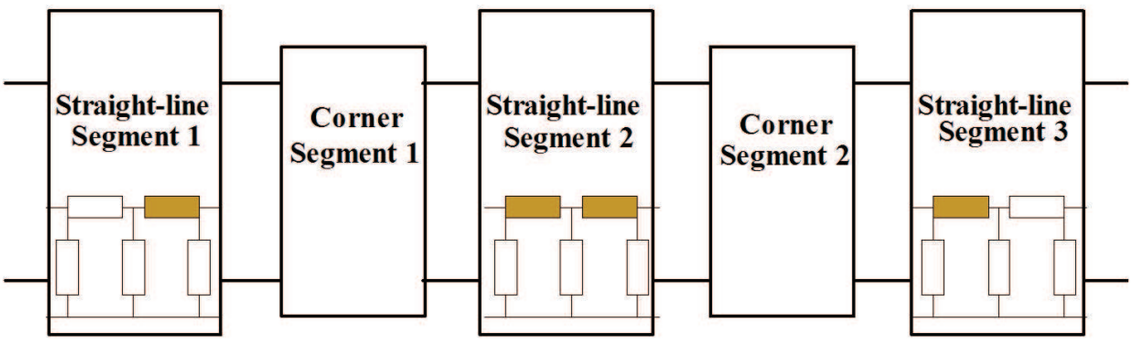


Fig. 18. Illustration of the application of factor α (Shi et al., 2008)

The parameter extraction of the interconnect with bends can also be formulated as an objective function. As shown in Fig. 18, three straight-line segments and two corner segments are cascaded in a sequence. Therefore, in order to get the ABCD matrix of the whole trace, five corresponding ABCD matrixes of each segment are multiplied (Eq. 33).

$$T_{wire} = T_{\Pi} T_{\Pi corner} T_{corner} T_{\Pi corner} T_{\Pi corner} T_{corner} T_{\Pi corner} T_{\Pi} \tag{33}$$

where T_{π} denotes the ABCD matrix of each Π-network of the equivalent circuit model in Fig. 13; $T_{\pi corner}$ denotes the ABCD matrix of the Π-network, which is influenced by the corner; and T_{corner} denotes the ABCD matrix of the corner segment.

T_{corner}, as shown in Eq. 34, can be derived as a function matrix of the circuit components L_b, R_b and C_b, based on the model shown in Fig. 17. The elements of T_{corner} are presented in Eq. 35 - Eq. 38.

$$T_{corner} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{34}$$

$$A = 1 + \frac{j\omega L_b}{\frac{1}{j\omega C_b} + R_b} \tag{35}$$

$$B = 2j\omega L_b - \frac{\omega^2 L_b^2}{\frac{1}{j\omega C_b} + R_b} \tag{36}$$

$$C = \frac{1}{\frac{1}{j\omega C_b} + R_b} \tag{37}$$

$$D = 1 + \frac{j\omega L_b}{\frac{1}{j\omega C_b} + R_b} \tag{38}$$

Tπ is defined based on Eq. 39 - Eq. 43. The derived ABCD matrix elements are functions of the equivalent circuit components L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub} and R_{sub}.

$$T_{\Pi} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{39}$$

where

$$A = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{cox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \tag{40}$$

$$B = j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \tag{41}$$

$$C = \frac{2j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} + (j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}) \left[\frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \right]^2 \tag{42}$$

$$D = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega \alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{cox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \tag{43}$$

The matrix elements presented in Eq. 40 to Eq. 43 are for the Π-networks without corner influence. For the corner-influenced Π-networks, $T_{\Pi corner}$ is similar to T_{Π}. We just have to replace the item L_s with αL_s to account for the corner effect as illustrated in Eq. 44 - Eq. 48.

$$T_{\Pi corner} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{44}$$

where

$$A = 1 + \frac{j\omega C_{ox}\left(j\omega C_{sub} + \frac{1}{R_{sub}}\right)\left(j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}\right)}{j\omega C_{cox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \tag{45}$$

$$B = j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \tag{46}$$

$$C = \frac{2j\omega C_{ox}\left(j\omega C_{sub} + \frac{1}{R_{sub}}\right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} + \left(j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}\right)\left[\frac{j\omega C_{ox}\left(j\omega C_{sub} + \frac{1}{R_{sub}}\right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}}\right]^2 \tag{47}$$

$$D = 1 + \frac{j\omega C_{ox}\left(j\omega C_{sub} + \frac{1}{R_{sub}}\right)\left(j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}\right)}{j\omega C_{cox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \tag{48}$$

The values of all the components in the straight-line segment, namely L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub} and R_{sub} are obtained from the previous section. Thereafter, the ABCD matrix of the entire wire are interpreted as functions of L_b, C_b, R_b and α. Corresponding S-parameters are expressed as functions of these variables under the following transformation formulas from Eq. 49 to Eq. 52.

$$S_{11} = \frac{A + \frac{B}{Z_o} - CZ_o - D}{A + \frac{B}{Z_o} + CZ_o + D} \tag{49}$$

$$S_{12} = \frac{2(AD - BC)}{A + \frac{B}{Z_o} + CZ_o + D} \tag{50}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_o} + CZ_o + D} \tag{51}$$

$$S_{22} = \frac{-A + \frac{B}{Z_o} - CZ_o + D}{A + \frac{B}{Z_o} + CZ_o + D} \tag{52}$$

The objective function $F_0(X)$ can then be obtained as Eq. 53.

$$F_o(X)\big|_{X=(\alpha,L_b,C_b,R_b)}=\sum_{i=1}^{m}\left\{f_{1i}^2(X)+\left[f_{1i}(X)-F_{1mean}\right]^2+f_{2i}^2(X)+\left[f_{2i}(X)-F_{2mean}\right]^2\right\} \quad (53)$$

where m is the total number of the frequency points under consideration. f_{1i} is the error between the simulated S_{11} and those acquired from the measurement results at each frequency point i, which is stated in Eq. 54. f_{2i} is the error between the simulated S_{21} and the measurement results at each frequency point i, which is stated in Eq. 55. F_{1mean} and F_{2mean} defined in Eq. 56 and Eq. 57 are the mean errors of S_{11} and S_{21} at each frequency point i. Given the symmetry of the interconnect test structures as shown in Fig. 14, it is known that $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$. We apply the average values of the measured S_{11} and S_{22} and S_{12} and S_{21} as follows. They are denoted by $S'_{11}$and S'_{21}, respectively.

$$f_{1i}(X)=\left|\frac{S_{11-i_simulated}-S'_{11-i_measured}}{S'_{11-i_measured}}\right| \quad (54)$$

$$f_{2i}(X)=\left|\frac{S_{21-i_simulated}-S'_{21-i_measured}}{S'_{21-i_measured}}\right| \quad (55)$$

$$F_{1mean}=\frac{\sum_{i=1}^{m}f_{1i}(X)}{m} \quad (56)$$

$$F_{2mean}=\frac{\sum_{i=1}^{m}f_{2i}(X)}{m} \quad (57)$$

The values of α, L_b, C_b and R_b of the corner segment can be determined by searching for the minimum values of $F_0(X)$ as shown in Eq. 53, starting from the reasonable initial guess. Therefore, the model of the complex shaped interconnect can be constructed.

3. Emerging on-chip interconnect concepts and technologies

The previous sections have emphasized on interconnects in the conventional metal/dielectric system. In this section, the authors would like to shed some lights on some emerging interconnect concepts and technologies. According to ITRS, these interconnect renovations are going to play the key role in satisfying the requirements of performance, reliablility and power consumption of the IC designs in the long run.

3.1 Optical interconnects

Optical interconnects (OIs) have been proposed to overcome the communication bottleneck by replacing electrical wires with optical waveguides (Haurylau et al., 2006). The major advantages of the OIs are speed-of-light signal propagation, large bandwidth and minimum crosstalk between signal transmission paths (ITRS, 2008).

While board--to-board and chip-to-chip of OIs have been actively under development, the feasibility of on-chip OIs is still an open question (Haurylau et al., 2006). The compatibility with CMOS technology is the biggest challenge for on-chip OIs and therefore gaining ever

increasing interest from both academia and industry. The block diagram of an on-chip OI system is illustrated in Fig. 19. It consists of the following components (ITRS, 2008; Haurylau et al., 2006):

- Light sources: From the modulation perspective, light source can be either directly modulated or non-modulated. For the non-modulated case, the light source must be used with modulators that can be controlled by electrical signals. From the location point of view, lasers can be either off-die or on-die. Key parameters of the light sources are output power, efficiency, cost, thermal stability, cooling requirements and speed for directly modulated sources. Up to date, high speed, electrically driven, on-chip monolithic light sources are still far from reality.
- Modulators: Modulators are used together with a non-modulated light source, typically off-die. The light provided by the laser is fed into the modulator. The main function of a modulator is to transducer electrical data supplied from the electrical driver into a modulated optical signal. The key parameters are coupling efficiency, operation voltage, switching time, waveguide loss, overall power, modulation depth/extinction ratio and area.
- Waveguides: waveguides are the paths through which light is propagated on-chip with minimum losses. Key parameters of waveguides include loss per unit length, refractive index contrast and pitch.
- Photo detectors: photo detectors are used to converts the incoming optical signal to small output current proportional to the input optical power. Key parameters of photo detectors are responsivity, bandwidth, switching speed and noise performance (Dagli, 2006). The two most widely used semiconductor photo detectors are P-Insulator-N (PIN) photodiodes and avalanche photodiodes (APDs).
- Transimpedance amplifiers (TIAs): TIAs acts as the electrical front-end of an optical receiver. It converts the small current signal generated by the photo detector to voltage signal. Key parameters of TIAs are the input referred noise, the overload current, the transimpedance gain, the bandwidth and the group delay.

The primary challenge for optical interconnects is to develop low-cost, low-power and CMOS-compatible components.

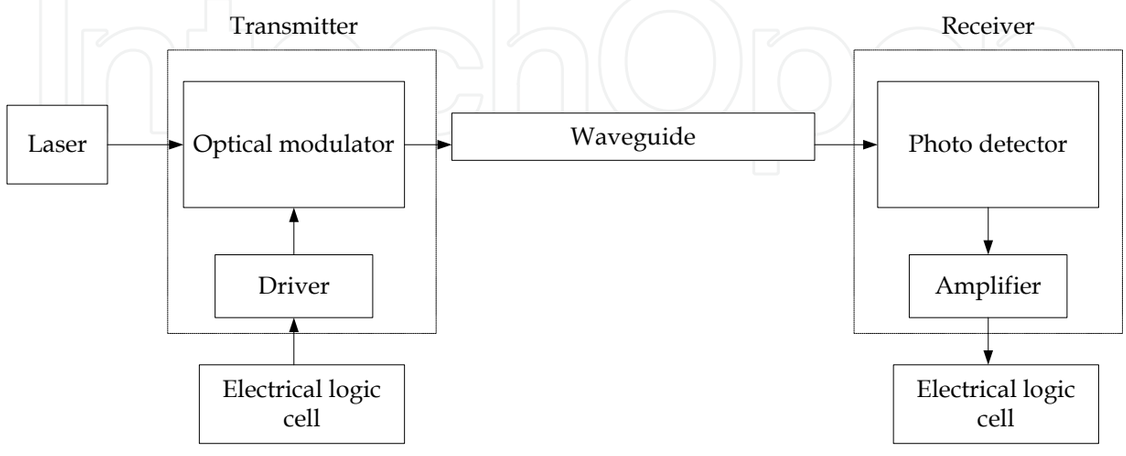


Fig. 19. Block diagram of OI system (Haurylau et al., 2006)

3.2 RF/Microwave interconnects

The basic idea of RF/microwave interconnect is to replace on-chip wires with integrated on-chip antennas to realize communication from one part of a chip to another part via RF or microwaves. RF/microwave signals are transferred either through free space or guided mediums (Chang et al, 2001). In the first case, it essentially takes the form of an on-chip LAN (local-area network), with transmitters, receivers, antennas and appropriate signal generation and signal detection circuitry (ITRS, 2008). The biggest challenge comes from the antenna design. Free space transmission and reception of RF/Microwave signals requires the antenna size comparable to its wavelength. Even at near 100 GHz operating frequency and cut-off frequency, the optimal aperture size of the antenna is of the order of one mm^2, which is too large to be implemented on-chip. In the later case, the RF/microwave signals are transmitted in guided mediums, such as the microstrip transmission line (MTL) or coplanar waveguide (CPW). Microwave transmission in MTLs and CPWs has much lower attenuation as compared with traditional wires. Moreover, since the communication distance is relatively short (several centimetres), the conventional large "far-field" antenna can be replaced by much smaller "near-field" capacitive couplers (Chang et al, 2001).

RF/Microwave interconnect technology is still in the early state of development. According to ITRS, there are four most critical questions must be solved (ITRS, 2008). First of all, in order to compare it with alternative interconnect solutions, characterization of the RF/Microwave interconnect system in terms of cost and performance must be completed. Secondly, full design rules for the electrical and electromagnetic portions of RF/microwave interconnect must be set up. Thirdly, the associated power and design complexity trade-offs must be fully understood. Last but not least, appropriate IC substrate and packaging materials for optimized transmission of RF and microwaves must be identified.

3.3 Carbon nanotubes

As the physical dimension of on-chip interconnects keeps on shrinking with the scaling of CMOS, the increased resistivity and electromigration issues of the conventional metal interconnects have caused serious concern. Carbon nanotubes (CNTs) have been proposed as a replacement for metal interconnects for their high mechanical and thermal stability, high thermal conductivity and large current carrying capacity (Naeemi et al, 2005; Raychowdhury& Roy, 2006).

CNTs are sheets of graphite rolled into cylinders with diameter of the order of one nanometer. Depending on the direction in which CNTs are rolled up (chirality), they demonstrate either metallic or semiconducting properties (Srivastava & Banerjee, 2005).

There are mainly two categories of CNTs, i.e., single-wall (SWCNT) or multi-wall (MWCNT). SWCNTs consist of only one graphene shell, while MWCNTs consist of several concentric graphene cylinders. MWCNTs are predominantly metallic. However, it is more difficult to achieve ballistic transport over long distance as compared to SWCNTs (Srivastava & Banerjee, 2005). Therefore, metallic SWCNTs are determined as preferred candidates as interconnects.

Research has shown a promising outlook for CNTs as a possible alternative to traditional metal interconnects. However, there are still numerous technical challenges to be addressed (ITRS, 2008), such as achieving a high-density integration with CNTs, selective growth of

metallic SWCNTs, directional growth in CNTs, achieving low-resistance metal-CNT contacts, achieving defect free CNTs and back-end-of-the-line compatible CNT growth.

4. Conclusion

Boosted by the great demand from the wireless telecommunication market, RFICs are gaining more and more attention. As circuit performance is getting increasingly dependent on interconnects, the RFIC design faces a big challenge that is the interconnect. In this chapter, the physical background of on-chip interconnects and the basic ideas of model development have been introduced. Various existing interconnect models have been presented. Extractions of model parameters have been discussed. Three of the most promising on-chip interconnection technologies, i.e., optical interconnects, RF/microwave interconnects and carbon nanotubes have also been introduced.

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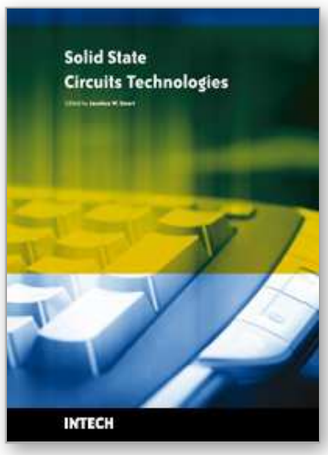
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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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