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Thermal Noise in Modern CMOS Technology

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1. Introduction

Because of the high cut-off frequency (f_T) in hundreds of gigahertz resulting from the aggressive reduction of physical size and the enhancement of carrier mobility, metal-oxide-semiconductor field effect transistors (MOSFETs) become widely used in radio-frequency (RF) and high-speed integrated circuits (ICs). However, when working at high frequencies and high speed, thermal noise becomes a critical issue preventing these circuits from their anticipated performance. This chapter presents how thermal noise is characterized, how it is modeled, and what is its trend in future CMOS technology.

2. Noise characterization

Because the thermal noise is overwhelmed by the $1/f$ noise in devices at low frequencies, it is usually evaluated at high frequencies, at least above the $1/f$ corner frequency. Different from the low-frequency noise characterization, which can be directly conducted using a spectrum analyzer, thermal noise characteristics has to be evaluated by its noise factor (or noise figure in dB) and/or its four noise parameters, namely minimum noise factor (F_{min}) or minimum noise figure in dB, (NF_{min}), equivalent noise resistance (R_n), and optimized source admittance ($Y_{opt} = G_{opt} + j \cdot B_{opt}$). We describe how noise factors and noise parameters are measured in 2.1, how to remove the parasitic effects of probe pads and metal interconnections in a device-under-test (DUT) in 2.2, and how to extract the noise sources of interest in 2.3.

2.1 Noise measurement

Noise parameters are commonly used parameters in the microwave noise characterization of a linear noisy two-port network. One of its applications is to calibrate a noise measurement system (Chen et al., 2007), and another example is to remove the parasitic effects of metal interconnections in a DUT (Chen & Deen, 2001). They are also used to extract the noise sources of interest in devices (Chen & Deen, 2001; Chen & Deen, 2000; Asgaran et al., 2007), which assist in device noise modeling (Chen & Deen, 2002; Asgaran, Deen & Chen, 2004; Deen et al., 2006). In this section, we present the setup of a noise measurement system and different algorithms to improve the measurement accuracy.

The conventional set of noise parameters are based on Rothe and Dahlkes' work (Rothe & Dahlke, 1956). In this work, a noisy two-port network is represented by voltage or current sources connected to the noiseless network. Haus et al. expanded this concept and

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developed the four well-known noise parameters – minimum noise factor F_{min}, equivalent noise resistance R_n, optimal source conductance G_{opt} (i.e., the real pat of Y_{opt}), and optimal source susceptance B_{opt} (i.e., the imaginary part of Y_{opt}) (Haus et al., 1960). This representation allows easy calculation of noise figures for a noisy two-port network. The intuitive, impedance-based representation of the noisy two-port network also demonstrates the dependence of noise factors on the source admittances attached to the input of the network. Since the introduction of this two-port noise representation, many measurement and extraction methods have been introduced (Lane, 1969; Mitama & Katoh, 1979; Vasilescu, Alquie & Krim, 1988; O'Callaghan & Mondal, 1991).

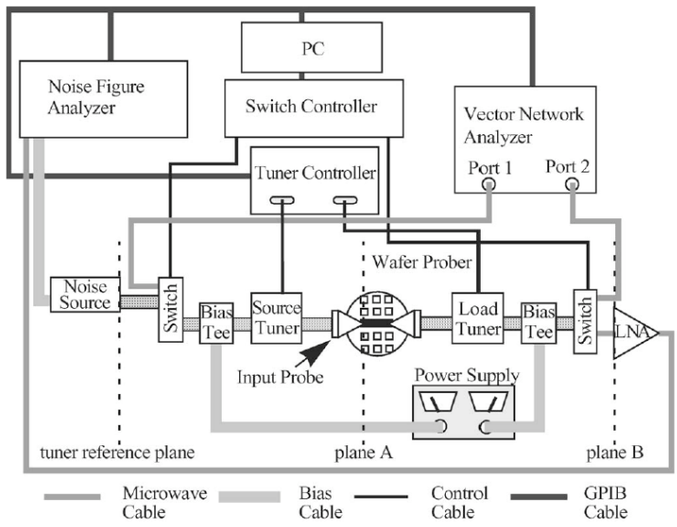

Fig. 1. System configuration for microwave noise measurements (Chen et al., 2007).

For a commonly-used a noise measurement system (see Fig. 1), it consists of a noise source, a vector network analyzer, a noise figure analyzer (NFA), microwave impedance tuners, a low-noise amplifier (LNA), and other peripheral components (e.g., PC). This system can be furthered simplified using a PNA-X (with noise option) from Agilent to replace both VNA and NFA (Simpson, 2009). The noise source is to generate two noise outputs with different equivalent noise temperatures, namely hot (T_h) and cold (T_c) temperatures during the noise measurements. The source tuner is to provide different source admittances for the receiver, and the load tuner is to match the output of the DUT for a maximum power transfer. The LNA is to boost the weak noise signal to increase the accuracy of the measured noise power. It also helps to reduce the noise factor of the receiver to increase the noise factor accuracy of the DUT, especially when Friis's equation (Friis, 1944) is applied to remove receiver's noise contribution. However, the gain of the LNA has to be carefully selected in order not to saturate the receiver in the NFA.

For noise parameter measurements, in general, they can be divided into two different categories. The first category involves the forward and reverse noise measurements based on the concept of noise wave. It was first introduced by Penfield in 1962 (Penfield, 1962). Instead of representing the internal noise of the two-port network by voltage or current sources, Penfield's method uses noise waves. Such wave-based representation allows the use of the scattering parameters, which are widely used in the microwave frequency range. Unlike the conventional noise parameters, wave-based noise parameters represent the

intrinsic noise behavior of a noisy two-port network. They do not necessarily depend on the reflection coefficient seen by the input of the two-port. Since a noisy two-port can also be represented by other combinations of voltage or current sources, Hillbrand and Russer provided a more general treatment using waves to replace these sources (Hillbrand & Russer, 1976). Using the wave-based noise analysis technique, Meys developed a measurement method to characterize a linear two-port's noise properties (Meys, 1978). With Meys' formulation of the wave-based noise parameters, Valk et al. developed a method to de-embed the two-port noise parameters from a cascaded two-port network (Valk et al., 1988). Using different noise-wave definitions, Hecken developed a different set of noise parameters for noisy multi-ports (Hecken, 1981). Wedge developed a set of two-port noise parameters by modeling the intrinsic noise as noise waves leaving each port (Wedge & Rutledge, 1992; Wedge & Rutledge, 1991). From a practical point of view, the purpose of a set of noise parameters should help designers decide how to terminate a noisy two-port for optimal noise or power performance. Engen and Wait presented a set of noise parameters with physical meanings for the ease of this application (Engen, 1970; Wait & Engen, 1991). Based Wedge's noise parameters and using a similar approach to Engen's work, Randa presented a method in which the available noise temperature for the input port of the device can be also obtained (Randa & Walker, 2007; Randa, 2002). A reverse measurement is still necessary, but this more generalized approach removes the assumption that the reverse available power gain of the two-port is negligible (Chen, Wang & Bakr, 2008). The major issue stopping the wave-based approach from the on-wafer noise measurements in practice is the requirement of the reverse measurements.

In the second category, however, only the forward measurements are conducted to obtain the noise powers (or noise factors) at different source admittances/impedances. Under this catagory, there are two approaches to obtain these crucial noise parameters. In the first approach, four (or more) noise factors are obtained first using the Y-factor method (Agilent Application Note 57-1). The four noise parameters are then calculated by solving the linearized noise factor equations with algorithms or methods to take care of the experimental errors in the noise factors and the source admittances (IRE Subcommittee 7.9 on Noise, 1963; Lange, 1967; Lane, 1969; Gupta, 1970; Caruso & Sannino, 1978; Mitama & Katoh, 1979; Sannino, 1979; Pospieszalski, 1986; Vasilescu, Alquie & Krim, 1988; Davidson et al., 1989; O'Callaghan & Mondal, 1991; Archer & Batchelor, 1992; Boudiaf & Laporte, 1993; Tiemeijer et al., 2005; Wiatr & Walker, 2005). The second approach, on the other hand, directly solves the noise parameters using the power equation (Adamian & Uhlir, 1973; Tutt, 1994). This method leads to the so-called "cold-only" method in which the noise power in the hot state is only measured during the system calibration, but not in the measurement of the DUT (Adamian & Uhlir, 1973; Tutt, 1994; Meierer & Tsironis, 1995; Kantanen et al., 2003). Recently, two methods to improve the measurement accuracy by taking care of the impedance difference between the hot and cold states are presented by Kantanen (Kantanen et al., 2003) for Y-factor based approach and by Chen (Chen et al., 2007) for power equation based approach, respectively.

2.2 Noise parameter de-embedding

Because the physical size of devices is small, probe pads and interconnections are usually designed to access devices when performing noise measurements. With the continuous downscaling of the device dimensions, the impact of the surrounding parasitics on the

device characteristics has steadily gained importance in the a.c. and noise measurements of a DUT, which includes a transistor, probe pads, and metal interconnections between the probe pads and the transistor. Since the probe pads and interconnections introduce additional parasitics including resistances, inductances, and capacitances, de-embedding procedures for both measured scattering and noise parameters must be performed prior to analyzing the performance of an intrinsic transistor to isolate the intrinsic performance from that due to extrinsic parasitic effects for on-wafer measurements.

In 1987, van Wijnen et al. presented a method to remove the capacitive parasitics of probe pads from the on-wafer s-parameter measurements by measuring an additional "OPEN" dummy structure (van Wijnen, Claessen & Wolsheimer, 1987). In 1991, Koolen et al. improved the de-embedding procedure with the consideration of the influence of the interconnections by measuring another "SHORT" dummy structure (Koolen, Geelen & Versleijen, 1991). Lee et al., in 1994, modified the "SHORT' structure and the de-embedding method presented by Koolen et al. so as to extract the parasitic inductances of the interconnections (Lee, Ryum & Kang, 1994). In 2000, Kolding presented a procedure to predict the series losses and coupling parasitics (Kolding, 2000). In these de-embedding methods, in general, a parallel-series configuration which assumes that the impedance of interconnections is in series with the transistor, and the admittance of probe pads is in parallel with the interconnections and the transistor is used to model the DUT.

In the parallel-series configurations, it is assumed that the capacitive effect of interconnections is negligible, and the inductive and resistive effects are dominant at the frequencies of interest. However, this might not be true for the designs with long interconnections or at operating frequencies at several tens of GHz, where the distributive effects of the interconnections become important. Therefore, the interconnections cannot be modeled as an inductor in series with a resistor, and the DUT has to be modeled as probe pads, interconnections, and the transistor connected in a cascade configuration. The de-embedding procedure presented by Biber in 1998 (Biber et al., 1998) is based on cascade configurations, but it still neglects the capacitive effect of the interconnections. In addition, it requires specific equivalent circuit models for both probe pads and the interconnections. In 2002, Chen and Deen presented a general de-embedding procedure based on the cascade configurations without the requirement of any equivalent circuit models for probe pads and interconnections (Chen & Deen, 2001). Cho et al. improved Chen and Deens' method by presenting a scalable noise de-embedding technique for the characterization of devices in various sizes without designing their corresponding dummy structures (Cho et al., 2005). This can save a lot of wafer space in designing microwave test structures.

2.3 Noise source extraction

Behavior of physical noise sources in MOSFETs, namely channel thermal noise, induced gate noise, and their correlation, is needed when we develop any physics-based compact noise model. Obtaining the spectral densities of these noise sources of interest as a function of frequency, bias condition, and device geometry directly from the intrinsic noise and s-parameters is the key step in the noise modeling. The extracted noise spectral densities of these desired noise sources can provide important insights on the noise characteristics of devices and serve as a useful guide for noise modeling. There are several methods for the noise source extraction (Chen & Deen, 2000; Knoblinger, Klein & Baumann, 2000; Chen et al., 2001; Knoblinger, 2001). Both methods by Chen (Chen & Deen, 2000) and Knoblinger

(Knoblinger, Klein & Baumann, 2000) published in year 2000 only extract the channel noise. In 2001, both of them presented new methods to extract channel noise, induced gate noise, and their correlation (Chen et al., 2001; Knoblinger, 2001). Fig. 2 shows the extracted channel noise, induced gate noise, correlation noise, and cross-correlation coefficient as a function of frequencies for devices with different channel lengths (Chen et al., 2001). It is observed that the channel noise is about frequency independent, the induced gate noise and the correlation term are proportional to f^2 and f, respectively, where f is the operating frequency (solid lines in the figures). In addition, when the channel length decreases, both induced gate noise and its correlation with the channel thermal noise also decrease because of the reduction of the gate-to-source capacitance.

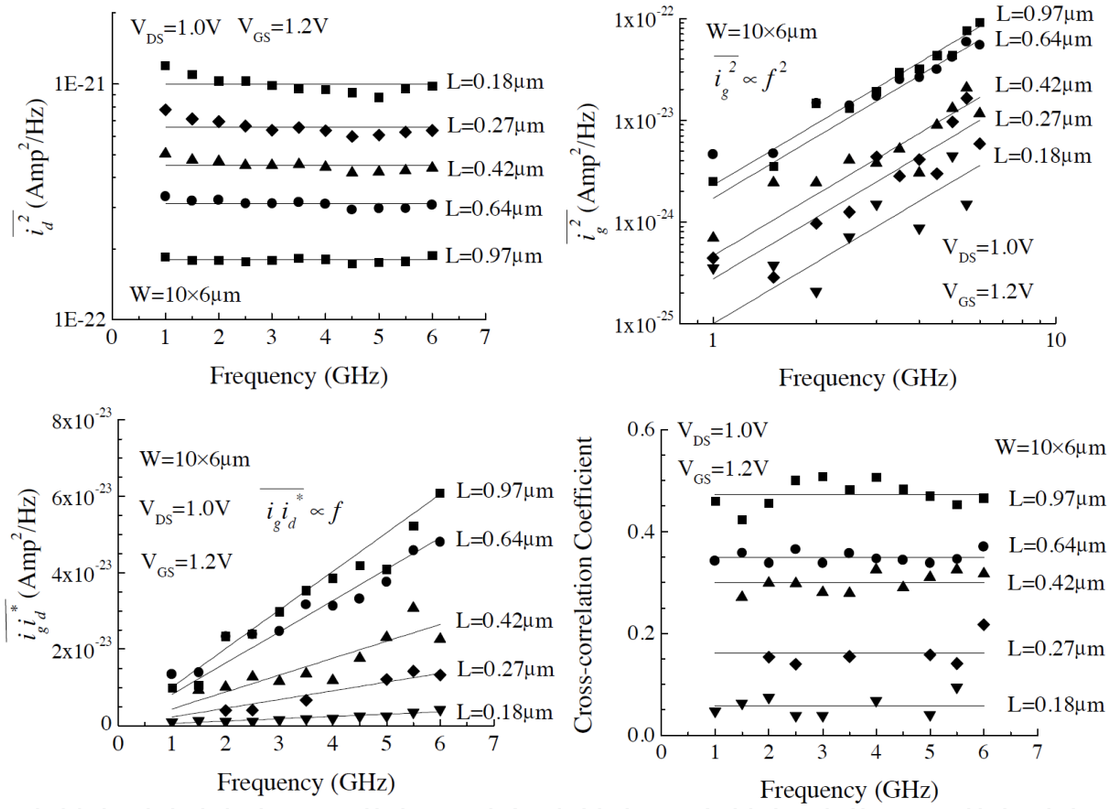

Fig. 2. Extracted channel noise, induced gate noise, correlation noise, and cross-correlation coefficient as a function of frequencies for devices with different channel lengths (Chen et al., 2001).

According to Chen and Deens' analytical equation (Chen & Deen, 2000), it is shown that among these noise parameters - NF_{min}, R_n, and Γ_{opt}, only the equivalent noise resistance R_n extrapolated at low frequencies provides a direct insight for the channel noise. Therefore, any proposed channel noise model should compare the calculated and measured R_n versus frequency characteristics. It is not sufficient to verify the channel noise model by just comparing the NF_{min} only, which is affected by the induced gate noise as well. Fig. 3 shows the measured (symbols) and calculated (lines) NF_{min} and r_n (R_n normalized to 50Ω) versus frequency characteristics for an n-type MOSFET with L = 0.97 µm and W = 10 × 6 µm (ten 6

μm fingers connected in parallel) biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V using different combination of these noise sources. It is shown that the induced gate noise has strong impact on the NF_{min}, especially for long channel devices, but little influence on r_n. In addition, it seems that the correlation noise has little impact on NF_{min} and r_n.

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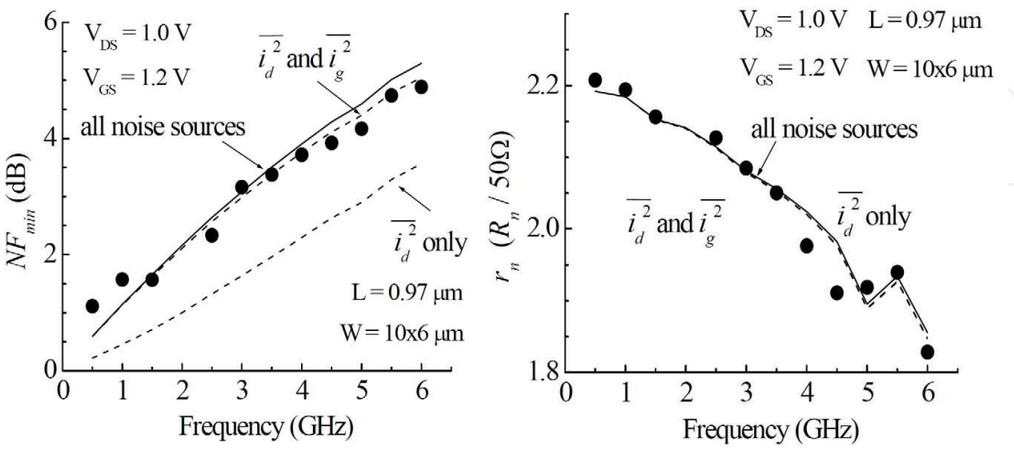

Fig. 3. Impacts of noise sources on NF_{min} and r_n (R_n normalized to 50Ω).

Another example to illustrate this idea is shown in Fig. 4. The solid lines are obtained using the extracted channel noise, induced gate noise and their correlation, and the dashed lines are obtained by replacing the extracted channel thermal noise with the thermal noise models commonly used by analog IC designers (i.e., $8kTg_{do}/3$ and $8kTg_m/3$). It is shown that although the conventional channel noise models agree well with the measured NF_{min}, they predict lower r_n.

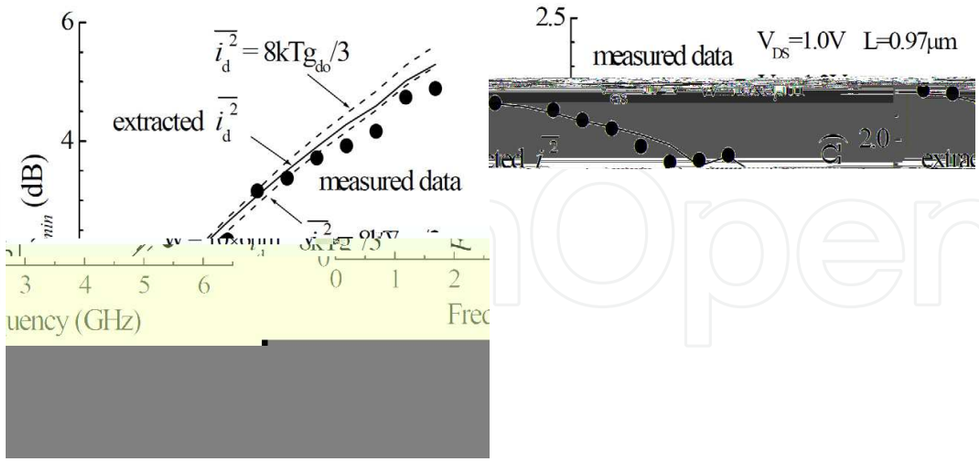

Fig. 4. Verification of channel thermal noise based on NF_{min} and r_n (R_n normalized to 50Ω).

3. Noise modeling

Physics-based noise models for channel thermal noise, induced gate noise, and their correlation are important when examining experimental results. It also provides circuit

designers some guidelines in designing low-power, low-noise ICs. This section presents thermal noise modeling in 3.1 and how they can be implemented into commercial circuit simulators in 3.2.

3.1 Thermal noise modeling

Due to the enhancement in CMOS technology, new noise phenomena emerge. This section discusses the impacts of channel length modulation effects, hot carrier effects, and velocity saturation effects down to 65 nm technology node.

Starting from van der Ziel, Jordan, and Jordans' pioneering work back to 1962 and 1965 (van der Ziel, 1962; Jordan & Jordan, 1965), the modeling of the channel thermal noise in field-effect transistors has been continuous since then. In 1967, Klaassen and Prins derived an equation to calculate the power spectral density of the channel thermal noise as (Klaassen & Prins, 1967)

$$S_{i_d^2} = \frac{4kT}{L_{eff}^2}\int_0^{L_{eff}} g(V(x))dx = \frac{4kT}{I_D L_{eff}^2}\int_{V_{seff}}^{V_{deff}} g(V)dV \tag{1}$$

where k is Boltzmann's constant, T is the lattice temperature, L_{eff} is the effective channel length, $g(V(x))$ is the channel conductance at the position x, and I_D is the d.c. drain current. Here V_{seff} and V_{deff} are the effective source and drain voltages, respectively. In order to treat a MOSFET as a resister-like element, van der Ziel presented a simpler equation as (van der Ziel, 1970)

$$S_{i_d^2} = 4kTg_{do}\gamma \tag{2}$$

where g_{do} is the output conductance at $V_{DS} = 0$, and the value of γ is 1 and 2/3 in the triode and saturation regions, respectively. The parameter γ in (2) is widely used later in the literature to demonstrate the enhanced channel noise in short-channel transistors. Another frequently used equation for the channel thermal noise proposed by Tsividis was given by (Tsividis, 1987)

$$S_{i_d^2} = \frac{4kT}{L_{eff}^2}\mu_{eff}\,|Q_{inv}| \tag{3}$$

where μ_{eff} is the effective mobility and Q_{inv} is the total inversion layer charge. These models, (1) to (3) are considered as the conventional models which worked well for long-channel transistors. In 1986, Adibi reported that the γ value of a 0.7 μm transistor is higher than 2/3 when working in the saturation region (Abidi, 1986). Different theories were then proposed to discover the origin of the enhanced channel thermal noise.

- Chen and Deens' model

Before Chen and Deen proposed their model in 2002 (Chen & Deen, 2002), all of the theories (Triantis, Birbas & Kondis, 1996; Klein, 1999; Scholten et al., 1999; Jin, Chan & Lau, 2000; Park & Park, 2000; Knoblinger, Klein & Tiebout, 2001) attributed the enhanced channel thermal noise to the hot carrier effect, following the similar arguments for the excess noise in field-effect transistors (Klassen, 1970; Baechtold, 1971; Takagi & Matsumoto, 1977; Jindal, 1986). Chen and Deen, however, considered the channel length modulation (CLM) effect and proposed the spectral density of the channel noise as (Chen & Deen, 2002)

$$S_{i_d^2} = \frac{4kT}{L_{elec}^2}\mu_{eff}\,|Q_{inv}| + \delta\frac{4kTI_D}{L_{elec}^2 E_{crit}^2}V_{DSsat} \tag{4}$$

where E_{crit} is the critical electrical field, Q_{inv} is the total inversion charge in the gradual channel region, and L_{elec} is the electrical channel length of the device ($L_{elec} = L_{eff} - \Delta L$, where ΔL is the channel length of the velocity saturated region). The second term in (4) is used to account for the carrier heating effect. However, in the experimental verification (see Fig. 5), very good agreements with measured data are achieved without including the hot carrier effect (i.e., $\delta = 0$) (Chen & Deen, 2002). Based on this observation, it was argued that no carrier heating is needed to model the channel thermal noise, and that the lattice temperature should be used for the temperature T in (4). In addition, the noise generated from the velocity saturated region in the channel, measured at the drain terminal, is assumed to be negligible.

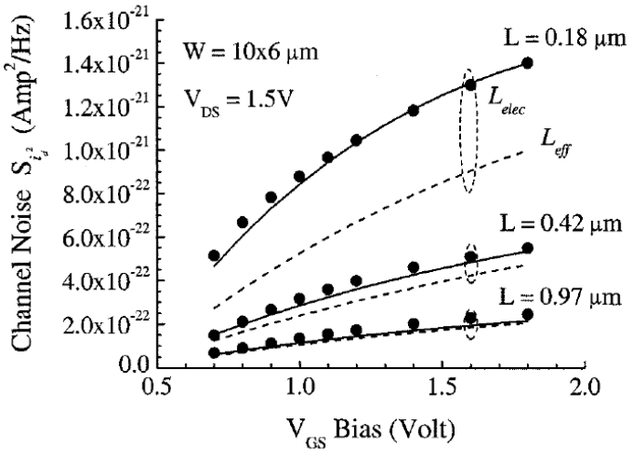

Fig. 5. Extracted (symbols) and calculated (lines) spectral densities of the channel thermal noise of n-type MOSFETs in a 0.18 μm COMS technology (Chen & Deen, 2002).

- Paasschens, Scholten & van Langeveldes' model

As indicated by Paasschens et al. (Paasschens, Scholten & van Langevelde, 2005), the limitation in (1) is that it cannot be applied to those devices whose channel conductance is a function of both position and voltage, i.e., $g = g(x, V)$ like LDMOS. In this case, Paasschens et al. separated the position and voltage dependence for the channel conductance as

$$g(x,V) = \frac{h(V)}{r(x)}. \tag{5}$$

Then, the channel thermal noise can be obtained by

$$S_{i_d^2} = 4kT\frac{\int_0^{L_{elec}} h(V(x))r(x)dx}{(\int_0^{L_{elec}} r(x)dx)^2} = \frac{4kT}{I_D}\frac{\int_{V_{seff}}^{V_{deff}} h(V)^2 dV}{(\int_0^{L_{elec}} r(x)dx)^2}. \tag{6}$$

Fig. 6 shows the normalized channel thermal noise for a ring-MOSFET biased at $V_{DS} = V_{GS} - V_{TH} = 1$ V. Both conventional Klaassen-Prins equation in (1) (i.e., $g = g(V)$) and thermal noise equation for resisters (i.e., $g = g(x)$) predict wrong results in the case of ring-MOSFETs.

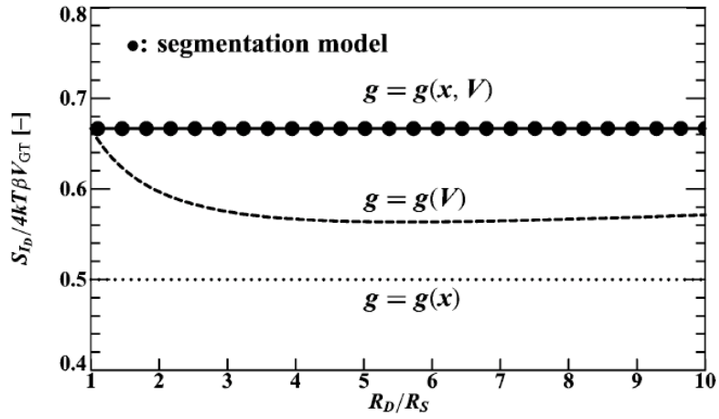

Fig. 6. Normalized channel thermal noise for a ring-MOSFET based on the classical Klaassen-Prins equation (dashed), the thermal noise equation for resistors (dotted), and the modified Klaassen-Prins equation (solid) (Paasschens, Scholten & van Langevelde, 2005).

For the velocity saturation effect due to the lateral electrical field, Paasschens et al. proposed a modified Klaassen-Prins equation as (Paasschens, Scholten & van Langevelde, 2005)

$$S_{i_d^2} = 4kT \frac{\int_0^{L_{elec}} (g_o / g)^{2p} g dx}{(\int_0^{L_{elec}} (g_o / g)^p dx)^2} = \frac{4kT}{I_D L_{vsat}^2} \int_{V_{seff}}^{V_{deff}} g_c^2 dV \tag{7}$$

with g_o and g_c defined in Paasschens et al.'s paper. Here p is the parameter to include the velocity saturation effect. Fig. 7 shows the calculated channel thermal noise with and without the velocity saturation effect. We can see that the velocity saturation effect reduces the channel thermal noise appeared at the drain terminal of the transistor.

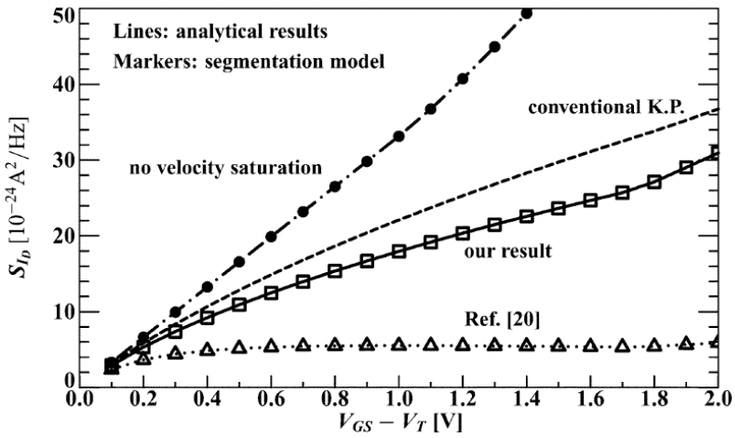

Fig. 7. Calculated channel thermal noise with and without the velocity saturation effect (Paasschens, Scholten & van Langevelde, 2005).

- Roy and Enzs' model

The carrier heating and mobility degradation are the two major concerns after Chen and Deens' model. Roy and Enz proposed a model for the channel noise as (Roy & Enz, 2005)

$$S_{i_d^2} = \frac{4kT_l W_{eff} \int_0^{L_{eff}} \frac{\mu_o |Q_{inv}|}{\mu_{eff} + \mu'_{eff} \cdot E} dx}{L_{elec}^2 (1 + \frac{1}{L_{elec}} \int_{V_s}^{V_{deff}} \frac{u'_{eff}}{\mu_{eff} + \mu'_{eff} \cdot E})^2 dV} \tag{8}$$

where

$$\mu_{eff} = \frac{\mu_o}{\sqrt{1 + (\frac{dV/dx}{E_c})^2}} \sqrt{\frac{T_c}{T_l}}, \ \mu'_{eff} = \partial \mu_{eff} / \partial E, \tag{9}$$

T_c and T_l are the carrier and the lattice temperatures, respectively, E is the lateral electrical field in the gradual channel region, W_{eff} is the effective channel width, μ_o is the mobility without the velocity degradation result from E. Roy and Enz reported in their paper that the carrier heating and mobility reduction have an opposite effect on the power spectral density of the channel thermal noise. The mobility reduction decreases it, whereas the carrier heating enhances it. They believed that as Chen and Deens' model does not consider the carrier heating, the effect of mobility reduction gets largely compensated. They also believed that this is why Scholten et al. (Scholten et al., 2003) were able to match the experimental result without considering carrier heating. Jeon et al. also reported that the hot-carrier effect should be taken into account when modeling their 0.13 μm transistors (Jeon et al., 2007). On the contrary, Schenk et al. used device simulators to calculate the hot-electron effect for 0.25 μm transistors and concluded that the hot-electron effect on the channel thermal noise is not important under the normal operation conditions (Schenk et al., 2003). Fig. 8 shows the calculated γ value as a function of gate bias for models proposed by Chen (Chen & Deen, 2002), Han (Han, Shin & Lee, 2004), and Roy (Roy & Enz, 2005), respectively.

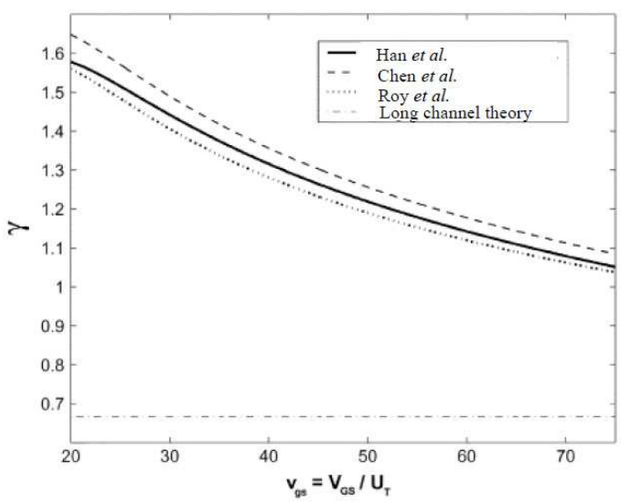

Fig. 8. Simulated γ values versus normalized v_{gs} bias for different models (Roy & Enz, 2005).

For the range of γ values, Fig. 9 shows the measured γ values from different technologies published in the literature (Dronavalli & Jindal, 2006). In general, the majority of the published γ values vary between 2/3 and 3 for channel length down to 120 nm.

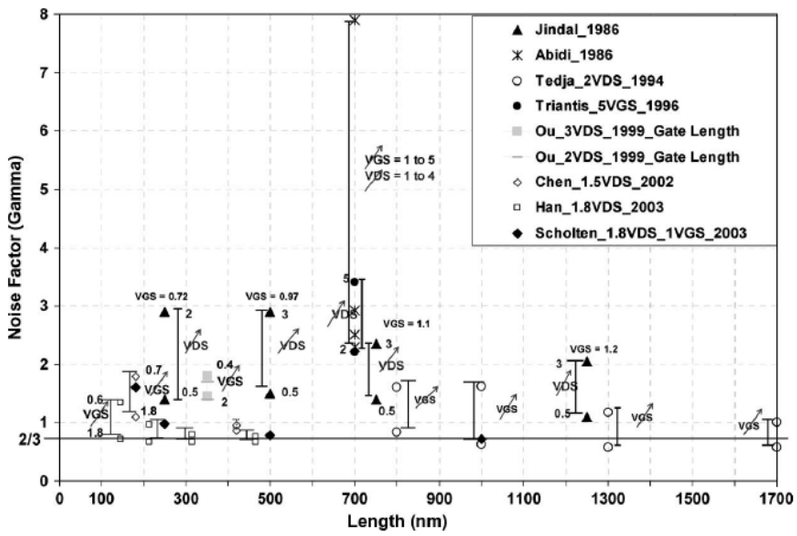

Fig. 9. Measured γ values for different technologies reported in the literature (Dronavalli & Jindal, 2006).

For the state-of-the-art 65 nm CMOS technology, Fig. 10 shows the measured (symbols) and simulated (lines) γ values for transistors fabricated by United Microelectronics Corporation (UMC) with W = 32×4 μm, and L = 60 nm, 80 nm, 120 nm, and 180 nm, respectively biased at V_{DS} = 1.2 V (Chen et al., 2008). We can see that the γ value could be as high as 4 for the 65 nm CMOS technology now.

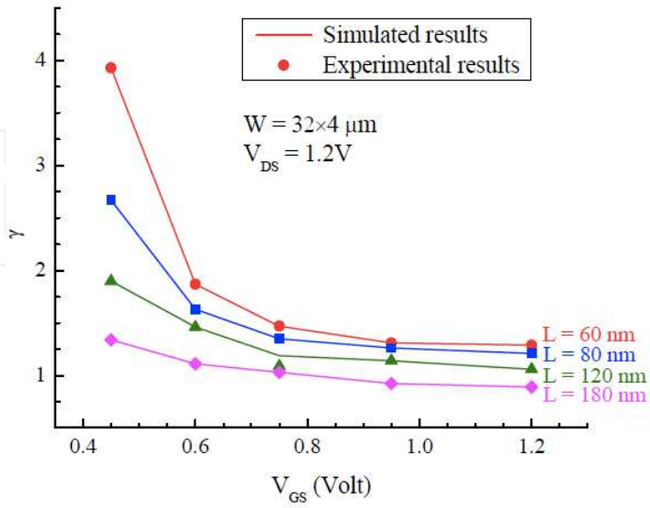

Fig. 10. Measured (symbols) and simulated (lines) γ values versus V_{GS} characteristics for transistors with W = 32×4 μm, and L = 60 nm, 80 nm, 120 nm, and 180 nm, respectively biased at V_{DS} = 1.2 V (Chen et al., 2008).

3.2 Thermal noise implementation

Any physics-based noise model has to be implemented into the circuit simulators before they can be used by IC designers. This is usually done through the software vendor or model developers, which might take long time to accomplish. Assuming that the noise spectral densities of channel thermal noise and induced gate noise are obtained from either theoretical calculation based on any noise model mentioned in previous sections or experimental results, Chen et al. provided a simple method to implement the enhanced channel noise and the induced gate noise for RF IC applications using a subcircuit approach (Chen, Li & Cheng, 2004). This approach is general and can work with any compact model (e.g., BSIM, MOS 11 or EKV model) and circuit simulator (e.g., SpectreRF or ELDO). Fig. 11 shows an equivalent circuit to demonstrate the implementation method. Because most of the circuit simulators cannot handle correlated noise sources, the correlation noise is not implemented at this point.

- Enhanced channel thermal noise

The enhanced channel thermal noise i_{de} shown in Fig. 11 is implemented using a Current Controlled Current Source (CCCS), and its value is determined by the noise current generated by the reference resistance R_{de} as shown in Fig. 12(a). Its resistance value is determined by (Chen, Li & Cheng, 2004)

$$R_{de} = \frac{4kT}{\overline{i_d^2} - \overline{i_{dcom}^2}}, \tag{10}$$

where k is Boltzmann's constant, T is the absolute temperature, and $\overline{i_{dcom}^2}$ is the channel thermal noise generated by the compact model.

- Induced gate noise

The induced gate noise can be naturally generated by using the segmentation method as presented in Scholten's paper (Scholten et al., 2003). However, the disadvantage of this approach is that it increases the number of transistors and therefore the simulation complexity, especially for the distortion analysis. In Chen's paper, the induced gate noise i_g shown in Fig. 11 is implemented by using another Current Controlled Current Source (CCCS), whose power spectral density is generated by the noise reference circuit shown in Fig. 12(b) with C_{ind} and R_{ind} selected by (Chen, Li & Cheng, 2004)

$$C_{ind} = 100 \cdot \frac{P_{ind} \cdot f_{max}}{8kT\pi} \tag{11}$$

and

$$R_{ind} = \frac{P_{ind}}{16kT\pi^2 C_{ind}^2} \tag{12}$$

where f_{max} is the maximum frequency up to which the simulation will be valid, and P_{ind} represents the coefficient in the induced gate noise vs. frequency characteristics, i.e.,

$$P_{ind} = \frac{\overline{i_g^2}}{f^2}. \tag{13}$$

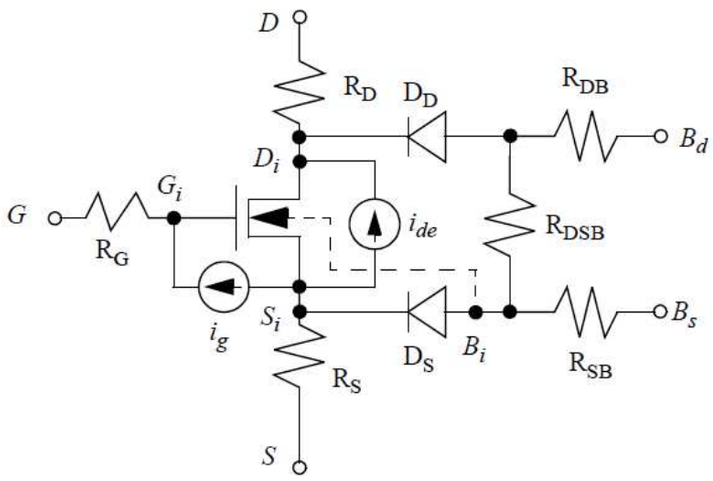

Fig. 11. Noise equivalent circuit of a MOSFET including parasitic resistance (R_D, R_G, and R_S), substrate network (D_D, D_S, R_{DB}, R_{SB}, and R_{DSB}), enhanced channel noise (i_{de}), and induced gate noise (i_g) for RF IC applications (Chen, Li & Cheng, 2004).

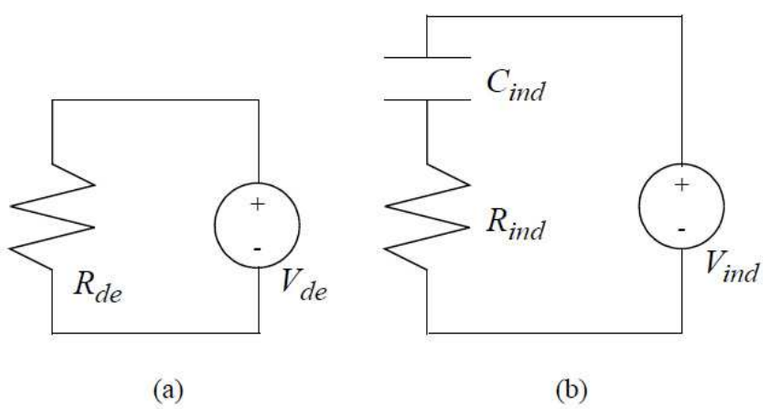

Fig. 12. Noise reference circuits to generate the noise currents for (a) the enhanced channel noise i_{de} and (b) the induced gate noise i_g shown in Fig. 11 (Chen, Li & Cheng, 2004).

4. Future work

As presented in the paper, all of the recent channel noise models focus on the noise from the gradual channel region, and how to characterize the noise contribution from the velocity saturation region in the nanometer MOSFETs is an area for future research. On the other hand, the design of integrated circuits with low power consumption is the trend for future circuit designs. In some cases, transistors might work in the moderate or weak inversion region. Therefore, the channel noise models for transistors working in these regions will become important for low-power applications. Finally, the scaling issues and the temperature characteristics of the active noise sources in the transistor are other research areas for future studies.

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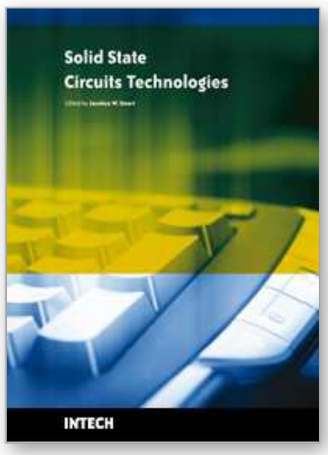

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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