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Electrostatic Discharge Protection and Latch-Up Design and Methodologies for ASIC Development

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Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/intechopen.81033>

Abstract

Electrostatic discharge (ESD) has been an issue in devices, circuits, and systems for electronics for many decades, as early as the 1970s, and continued to be an issue until today. In this chapter, the issue of ESD protection design and methods for Application-Specific Integrated Circuits (ASICs) will be discussed. The chapter will discuss ESD design in an ASIC environment. The discussion will address ESD design layout, design rules and practices, and the method of integration of ESD protection into the ASIC design practice. Part of the methodology is the floor planning of an ASIC design, I/O library, integration of ESD into I/O cells, power distribution, and placement of power pads, in both array and peripheral design methodologies. As part of the ASIC I/O design, guard rings and latch-up interactions will be highlighted.

Keywords: electrostatic discharge, latch-up, ASICs, ASIC I/O integration, ASIC power distribution

1. Introduction

Electrostatic discharge (ESD) design, practices, and methods are a fundamental to the implementation of an ASIC design environment [1–28]. The integration of ESD and latch-up in an ASIC environment is typically a top-down design flow. In the ASIC environment, the chip size, the number of I/O circuits, the bus location, placement of the I/O cells, and integration of the ESD elements and power are all synthesized. The top-down design flow is as follows:

- Functional definition
- Technology decision

- I/O definition with ESD network and guard ring definition
- Power pad definition with ESD power clamp and guard ring definition
- Core function placement
- Number of I/O
- I/O placement
- Power pads and number of ESD power clamps required
- Core to core ESD networks
- Core to core guard rings
- I/O to core guard rings

2. Electrostatic discharge

Electrostatic discharge (ESD) is a common form of component-level failure from manufacturing, shipping, and handling in an ASIC environment [1–8]. Two of the tests used in the qualification and release process of an ASIC design system are the human body model (HBM) and the charged-device model (CDM) standards [1–8].

2.1. Human body model

The human body model (HBM) is the most widely established standard for the qualification and release of semiconductor components in the semiconductor industry [1–4, 6–8]. The HBM test is integrated into the qualification and release process of the quality and reliability teams for components in ASIC organizations, corporations, and foundries. The model was intended to represent the interaction of the electrical discharge of a human being, who is charged, with a component or an object. The charged source then touches a component or an object using a finger. The physical contact between the charged human being and the component or object allows for current transfer between the human being and the object.

HBM failure mechanisms typically are associated with failures on the ASIC peripheral circuitry of a semiconductor chip that are connected to signal pins. HBM ESD networks are used to establish an alternative current path to avoid failure of the ASIC peripheral circuitry. HBM failures can also occur on the power rails due to inadequate bus widths and ESD power clamps between the power rails. HBM failures can occur in both passive and active semiconductor components. The failure signature is typically isolated to a single device or a few elements in a given current path where the current exceeded the power to failure of the circuit elements. ESD circuits are designed to be responsive to HBM pulse widths; specifically, the RC-triggered ESD power clamp is a vulnerable ESD circuit.

An example of an ESD protection network is known as a dual-diode network [1–4, 7, 8]. The dual-diode ESD network is a commonly used network for complementary metal-oxide

semiconductor (CMOS) technology. A first p-n diode element is formed in an n-well region where the p-anode is the p-diffusion implant of the p-channel MOSFET device and the n-cathode is the n-well region connected to the power supply V_{DD} . This is sometimes referred to as the “up diode.” A second p-n diode element is formed in a p-well or p-substrate region where the n-cathode is the n-diffusion implant of the n-channel MOSFET device or the n+/n-well implant, and the p-anode is the p-well region or p-substrate region connected to the power supply V_{SS} . This is sometimes referred to as the “down diode.” This circuit provides a “forward bias” ESD protection solution for positive and negative ESD pulse events to the two power rails V_{DD} and V_{SS} . An advantage of the dual-diode ESD network for ASIC environments is that it is easy to migrate from technology generation to technology generation and is scalable.

In an ASIC design methodology, the ESD network is integrated within the I/O library element. The I/O cell can contain a bond pad, guard rings, ESD network, receiver, and off-chip driver (OCD) elements [2, 3, 7, 8].

2.2. Charged-device model

The charged-device model (CDM) is an electrostatic discharge (ESD) test method that is part of the qualification of semiconductor components in an ASIC design system [6]. The CDM event is associated with the charging of the semiconductor component through different charging processes. Charging of the package can be achieved through direct contact charging or field-induced charging processes. The field-induced charging method is called the field-induced charged-device model (FI-CDM).

Charged-device ESD solutions utilize an additional circuit element local to the receiver network. For CDM protection, an additional resistor and second dual diode are added, where the second stage element is adjacent to the MOSFET receiver. The purpose of the second stage element is to divert the electric charge in the substrate adjacent to the MOSFET receiver to the bond pad without destruction of the receiver dielectric and circuitry.

2.2.1. CDM and long-narrow ASIC I/O

In an ASIC environment, each generation attempts to squeeze in as many I/O circuits on the periphery, by reducing the width of the I/O cell, and compensate by increasing the height of the ASIC I/O cell [11–15]. With the long-narrow ASIC I/O cell, the receiver network is moved farther away from the bond pad and the first stage of the ESD network. As a result, the second dual-diode stage is even more necessary to achieve excellent CDM ESD results.

3. ASIC requirements

In an ASIC environment, there are rules and requirements that are established in the design methodology. These rules and requirements for ESD design, latch-up design layout, to application issues of placement of power, placement of grounds. Additionally, the power sequencing for power down and power up is specified in the methodology. These fundamental ASIC rules have

a significant influence on the ESD circuits, ESD design methodology, and ESD circuit placement. Additionally, the ASIC system must achieve latch-up specification objectives.

3.1. ESD protection-level requirements

In a release of an ASIC system, there are qualification expectations of ESD protection levels. Each ASIC I/O cell is tested for ESD and CDM test processes, and the entire I/O library is to achieve above the desired protection levels for qualification. In the past, the desired protection levels for HBM and CDM were >4000 V HBM and > 500 V CDM; with technology scaling, these objectives have been changed to lower levels.

3.1.1. ESD design rules

ESD design rules of the physical dimensions of the ESD networks are typically contained within the technology design manual. The ASIC library is required to fulfill the technology ESD design manual rule set. The ESD design rules provide the circuit, layout, and physical dimensions.

3.2. Latch-up requirements

Latch-up requirements are also needed for the qualification of an ASIC design system [5]. The latch-up requirements used in all corporations and foundries are in the JEDEC latch-up specification and test method.

3.2.1. Latch-up design rules

As ASIC systems became more complex with integration of system on chips (SOC), the number of latch-up design rules has increased. Historically, latch-up rules consisted of four rules—(1) the distance between a PFET and its corresponding n-well contact, (2) the distance between an NFET and its closest substrate contact, (3) spacing of PFET to n-well edge, and lastly (4) spacing of NFET to n-well edge [5]. With scaling, there were many additional rules established between ESD and I/O, I/O to I/O, PFET to core logic, and NFET to core logic. With complexity, more guard rings were added to isolate the different regions of an ASIC implementation.

3.3. ASIC application requirements

In the definition of an ASIC system, there are many application rules and requirements that are established. These include area requirements, power distribution, and power sequencing.

3.3.1. Area requirements

In an ASIC system, there is a given chip area specified for the I/O circuitry [9–15]. This is planned as a certain percentage of the total chip area. Additionally, the ESD networks also can only be a certain defined percentage of the I/O cell. Typically, the ESD area desired is less than 20–25% of the total I/O cell area.

3.3.2. Power-up: sequence dependent

ASIC system can define the sequencing requirements for the power and the signal pins. Some ASIC systems can have a sequence-dependent power up and shutdown. In these systems, the ESD networks are not to be “on” during power up or power down.

3.3.3. Power-up: sequence independent and hot plugging

ASIC system can define the sequencing requirements for the power and the signal pins. Some ASIC systems require sequence-independent power up and shutdown. In these systems, the ESD networks are not to be “on” during power-up or power down. In this case, the ESD networks must not be forward biased in power up or power down. As a result, new sequence-independent ESD networks that do not forward bias were required. A sequence-independent ESD network was implemented into a 0.5-um ASIC system with significant success with a floating well control network [2, 3, 9].

3.3.4. Power distribution and placement requirements

ASIC methodologies establish requirements for the frequency of placement of “power cells” and “ground cells” to support the I/O and core circuitry. For example, some corporations stated that their ASIC system must be a power cell for every fourth or fifth I/O location. This provided a significant opportunity for ESD protection, since an “ESD power clamp” can be placed in the area allocating for the VDD and VSS power pins. As the frequency of placement of the ESD power clamps increases, the series resistance loss of the power bus or ground bus decreases; this allows for a lower resistance path for the current to flow through the complete network, providing improved ESD robustness [2, 3, 7, 8].

3.3.5. Frequency bandwidth

As ASIC technology transitions to advanced technology nodes, the application frequency is increased. From an ESD perspective, the expectation from ASICs is that the capacitance loading of the ESD network must be reduced to not impact the frequency bandwidth of the I/O networks. This can be achieved through semiconductor process modification, layout and design, and reduction of the size of the ESD networks. Through ESD novelty and innovation, the frequency bandwidth of signal inputs can be realized without reduction of ESD reliability concern.

3.3.6. Input leakage and IDD limitations

An additional concern is the input leakage requirements and IDD limitations. Input leakage can be minimized through proper design of ESD networks through process, circuit topology, and layout innovations. A larger concern is the ESD power clamps on the VDD power supply. It is critical to limit the number of ESD power clamps to not impact the IDD leakage limit for the application.

4. ASIC I/O

In ASIC I/O design, ESD protection is integral in the definition and methodology. In the following section, this will be discussed.

4.1. I/O and ESD integration

In the definition of an ASIC I/O, the off-chip driver (OCD), the receiver, and ESD circuitry are co-designed to integrate the networks into a common physical space [7]. This requires planning in the methodology to allocate the right percentage of area for each of these elements. Different methodologies are used depending on the foundry or corporation.

4.2. I/O and ESD design integration and synthesis

In one methodology, the ASIC system supported different off-chip driver (OCD) sizes by adjusting the number of MOSFET fingers that were connected. The number of MOSFET fingers used was the maximum driver strength for the I/O library providing different impedance as well. There are many options on what can be done in this methodology.

For example, there can be a 20, 30, and 50 Ω impedance OCD circuit offering, by attaching a different number of MOSFET fingers in a given I/O cell. In one method, the residual MOSFET OCD fingers were grounded and used as a “grounded gate NMOS” ESD network. In this case, the residual MOSFET fingers act as a natural ESD protection and utilize the “unused” section of the OCD. The advantage of this method is that the unused portion of the I/O is utilized. In a second embodiment, instead of grounding the residual MOSFET fingers, a dummy inverter load was attached to keep the residual fingers “off” or in a low logic state. Using a dummy inverter, the MOSFET gates that are not grounded, and “turn-on” from MOSFET snapback at the same impedance state as the MOSFET OCD. In this fashion, both the active and residual elements work together for ESD protection [7, 8].

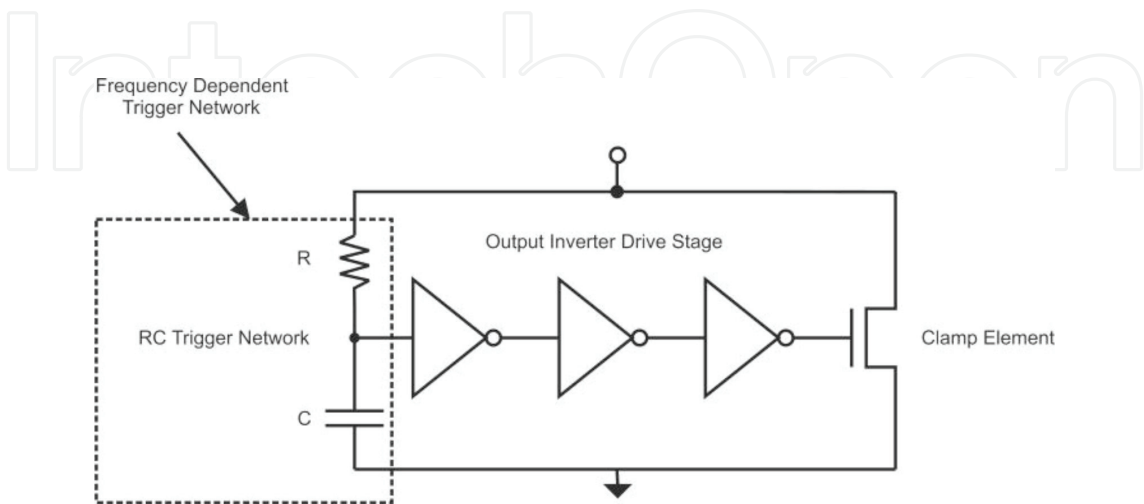


Figure 1. RC-triggered ESD power clamp.

4.3. I/O and ESD power clamp integration

ASIC methodologies establish requirements for the frequency of placement of “power cells” and “ground cells” to support the I/O and core circuitry [2–4, 7, 8, 11–15]. This provided a perfect opportunity for ESD protection, since an “ESD power clamp” can be placed in the area allocating for the power pins, the VDD pin location (**Figure 1**).

At one time, prior to the invention of ESD power clamps, it was just as empty areas; it was realized that the ESD power clamps can be placed in these regions. As the frequency of placement of the ESD power clamps increases, the series resistance loss of the power bus or ground bus decreases; this allows for a lower resistance path for the current to flow through the complete network, providing improved ESD robustness.

4.4. Ground-to-ground ESD networks

ESD networks are required between ground power rails for every independent domain. In an ASIC system, analog and digital circuits are in separate power domains [7, 8, 11–18]. These domains must be interconnected through ground-to-ground ESD networks. These networks must be bidirectional to allow current to flow in both directions. These networks do not have to be symmetric (e.g., m diodes in one direction and n diodes in the opposite direction). These ground-to-ground ESD networks can be placed in the VSS pin location.

4.5. Master/slave ESD systems

In some ASIC embodiments, the ESD power clamps are integrated across the entire system. In this type of system, there is one “master,” which triggers the set of ESD power clamps on all in parallel (**Figure 2**) [2, 3, 7, 8]. A “master ESD power clamp” contains the trigger network that then sends a signal to turn on all the “slave ESD power clamps.” This system has the advantage of turning on all ESD power clamps in parallel across the entire ASIC system, significantly lowering the “on-resistance” of the single ESD power clamp. The disadvantage of this system is an ESD signal bus (from the master clamp to the slave clamps) must be distributed with the ASIC power busses around the complete chip (**Figure 3**).

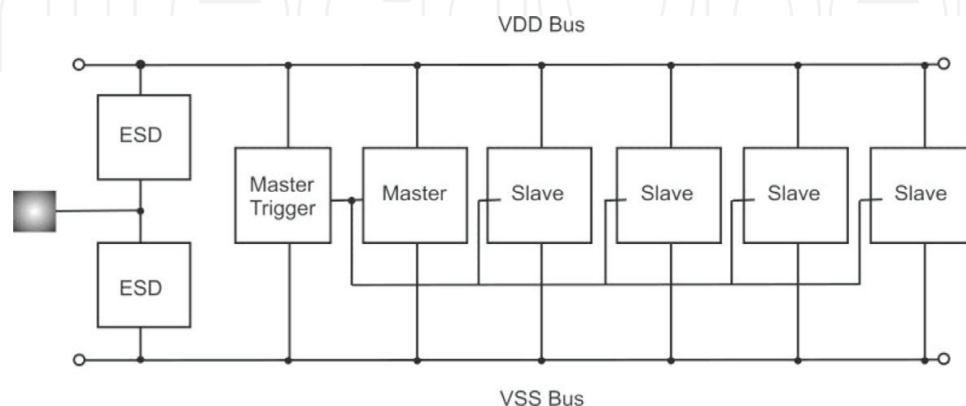


Figure 2. Master/slave ESD system.

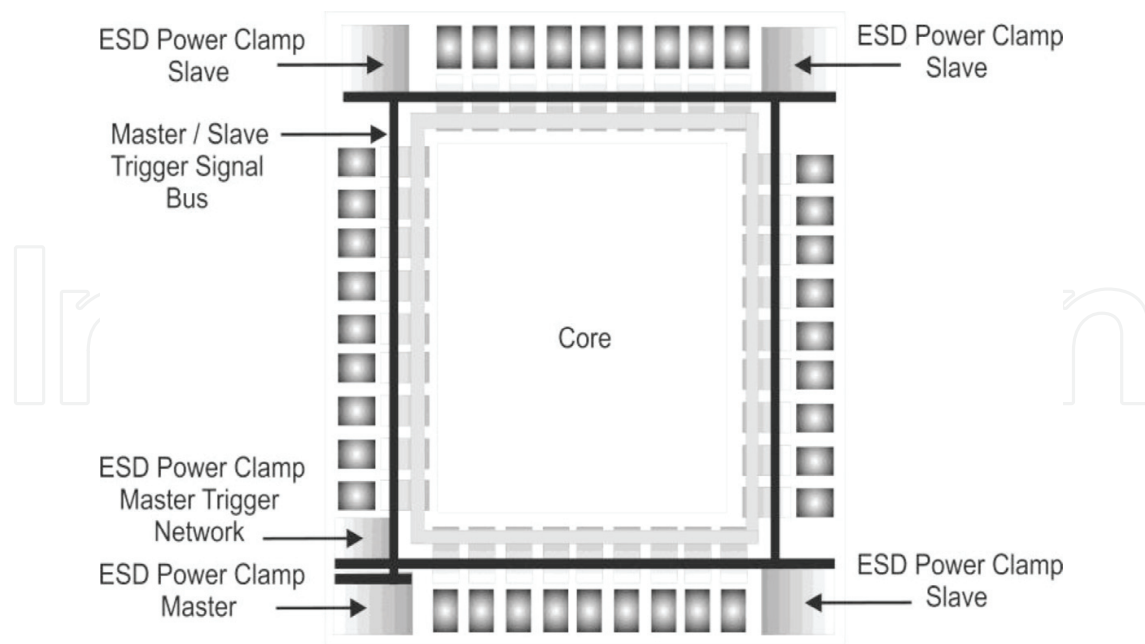


Figure 3. Master/slave ESD system floor plan.

5. ASIC I/O and latch-up: guard ring integration

In ASIC design methodologies, the I/O must address both ESD and latch-up [11–15]. Latch-up of the ASIC I/O can occur with improper design of the outer guard rings and internal guard rings in a given ASIC I/O cell.

5.1. I/O outer guard ring

In some ASIC methodologies, a guard ring is placed around the entire I/O cell region. This leads to a natural “frame” for the circuit. It serves as a source to collect internal current injected from inside the I/O circuit or external current being injected from outside the I/O circuit. In other methodologies, this outer guard ring is overlapped or integrated with the adjacent I/O cell; this is not detrimental and saves space [7, 8].

Additionally, even further methodologies, there is no “ring” around the entire circuit but only on the top and bottom. This can lead to I/O to I/O interaction, which is not desirable.

5.2. I/O circuit to adjacent I/O circuit

In ASIC I/O design, ESD and latch-up problems can occur when the design is “fully populated” versus “partially populated.” In digital applications, typically the design is fully populated and is “I/O limited.” But, in some analog applications, in core-dominated designs, the core establishes the chip size (e.g., core-dominated design), leading to a partially populated periphery.

5.2.1. Fully populated I/O periphery

In the case of a chip perimeter that is fully populated by I/O cells, concerns about latch-up events between adjacent I/O can be evaluated and tested (**Figure 4**). In this case, guard rings can be placed between the I/O cells, and latch-up interaction can be quantified [7, 8].

5.2.2. Partially populated I/O periphery

In the case of a chip perimeter that is not fully populated, concerns about latch-up events between I/O and adjacent cells can occur. In many ASIC systems, decoupling capacitors can be placed adjacent to an I/O cell. An n-well decoupling capacitor has a large n-well region that can serve as a cathode to a lateral pnpn formed by an adjacent PFET to form a pnpn. In this low populated system, new latch-up rules are needed to avoid CMOS latch-up in ASIC environments without full populated I/O cells.

5.2.3. Adjacency latch-up rules

In some design methodologies, it is necessary to verify what the adjacent circuit is [11–15]. In a fully populated I/O ring, the adjacent circuit will be another I/O cell. In this case, it is well understood. But, in cases where it is not populated, additional rules may be required to avoid latch-up between adjacent circuits. The most common failure was latch-up between an I/O cell and a decoupling capacitor [7–8].

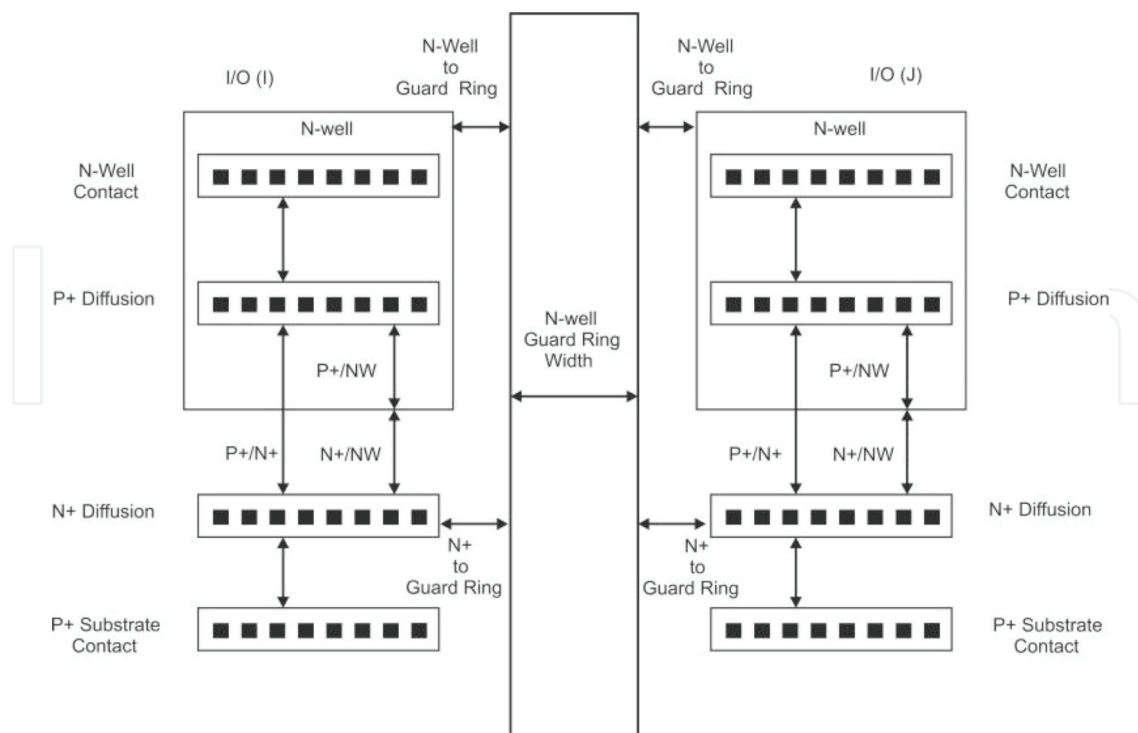


Figure 4. I/O to I/O latch-up test structure.

5.3. ESD to I/O circuit

Proper isolation between the ESD circuit contained within the I/O cell and the I/O circuit itself is necessary to avoid CMOS latch-up. The I/O circuit may contain an NFET pull-down, a PFET pull-up, and ballasting resistor bank. This is achievable by proper guard rings around the ESD network and the choice of what elements are placed adjacent to the ESD device. Note that there are multiple elements in an I/O circuit, and the choice of what is placed adjacent to the ESD network has to be co-synthesized with the power bus placement for the I/O cell (e.g., bond pad, VDD, VSS, AVDD, and AVSS). Since the ESD network typically has an element for positive and negative polarity pulse events, both the VDD and the VSS must be local to the ESD network and likewise for the PFET and NFET OCD elements.

For negative polarity ESD events, the n-diffusion or n-well resistor banks will be in parallel with the ESD elements, and the adjacency to their respective guard rings is key to provide “current sharing” and avoid “current robbing” of the ESD event. It was found by matching the space between n-type elements, and the guard rings provided maximum ESD results.

5.4. I/O to core circuitry

To avoid interaction between the I/O circuitry and the core circuitry, additional guard rings have been placed to isolate the I/O from the core circuits. The core circuits are very sensitive to CMOS latch-up since they have no guard rings surrounding the MOSFETs. To avoid latch-up issues between the I/O and core circuitry, additional requirements are established [5]:

- Latch-up space design rule between PFET OCD circuit and core circuits
- Latch-up space design rule between NFET OCD circuit and core circuits
- N+ guard ring of specified width between I/O region and core circuitry
- P+ substrate guard ring of specified width between I/O region and core circuitry

5.5. Core-to-core circuitry

Latch-up can occur between different core regions. This occurs when cores are placed adjacent to each other, where there is no design rule check, and when there is no history of the cores being adjacent in prior designs. An example is between a PFET-dominated core and a bank of decoupling capacitors with an n-well plate (**Figure 5**) [7, 8].

To avoid latch-up interaction between the circuitry of cores, additional guard rings, moats, substrate contacts, and space can be added in the design (**Figure 6**) [7, 8].

5.6. Digital, analog, and RF core circuitry

Latch-up and noise can occur between digital, analog, and radio frequency (RF) cores placed on the same substrate in an ASIC design. This occurs when cores are placed adjacent to each other, where there is no design rule check, and when there is no history of the cores being

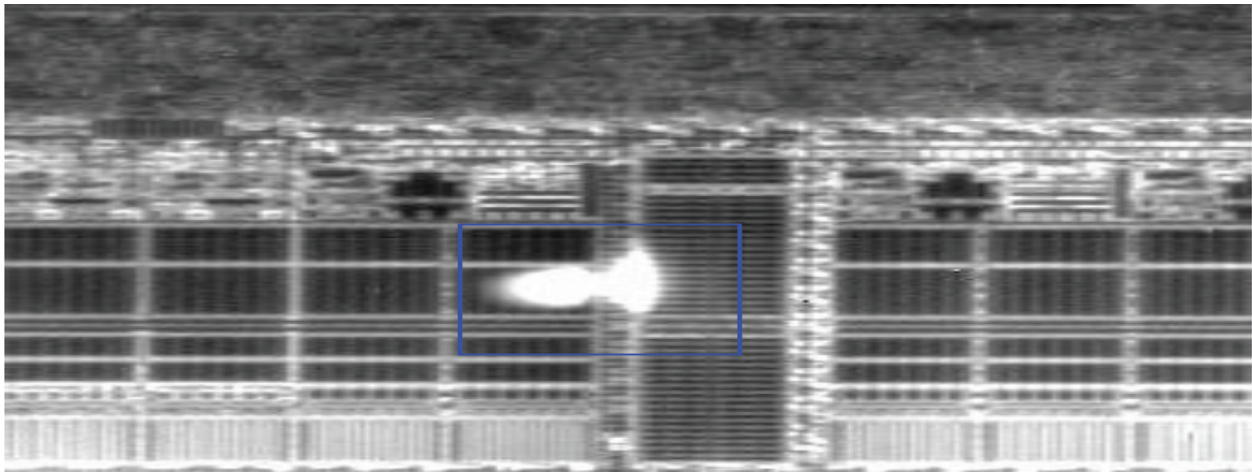


Figure 5. Latch-up between peripheral I/O and adjacent decoupling capacitors.

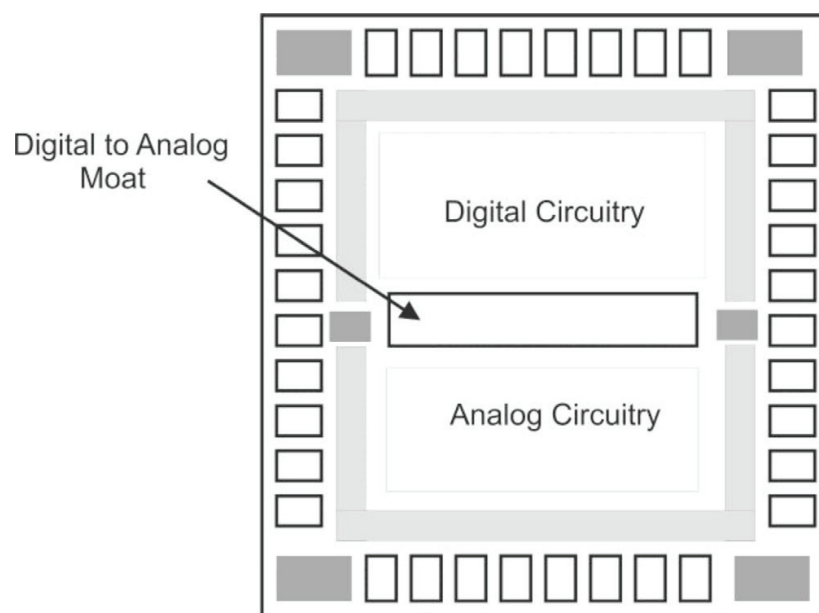


Figure 6. Digital to analog integration with moa.

placed close together. To avoid latch-up and noise interaction between digital and analog circuits, large guard rings, moats, substrate contacts, and spaces are added. The space between the digital and analog cores can be significant and as large as 40 to 100 μm . In these designs, the power grids and grounds are also separated and spatially isolated [7, 8].

5.7. Internal ESD networks: digital to analog signals

In mixed signal (MS) and system-on-chip (SOC) ASIC designs, there are signal lines that transfer from the digital core to the analog core. The power grids and ground planes are physically isolated to improve noise isolation. Digital core driver circuits transmit signals to analog core receiver networks in the analog section of the semiconductor chip. With the

separation of the digital and analog grounds, and physical space separation, overvoltage of the analog receiver can occur due to the voltage drops in the signal line and the ground connections (**Figure 7**).

One of the solutions is to place an “internal ESD network” on the internal signal line between the digital driver circuit and the analog receiver. This can be achieved by adding a resistor to the signal line and a grounded gate NMOS prior to the analog receiver (**Figure 8**).

A second solution is to place “third part” inverter stages and ground-to-ground connections between the digital and analog cores. This methodology has less performance or signal impact and is a more migratable solution (**Figure 9**) [7–8].

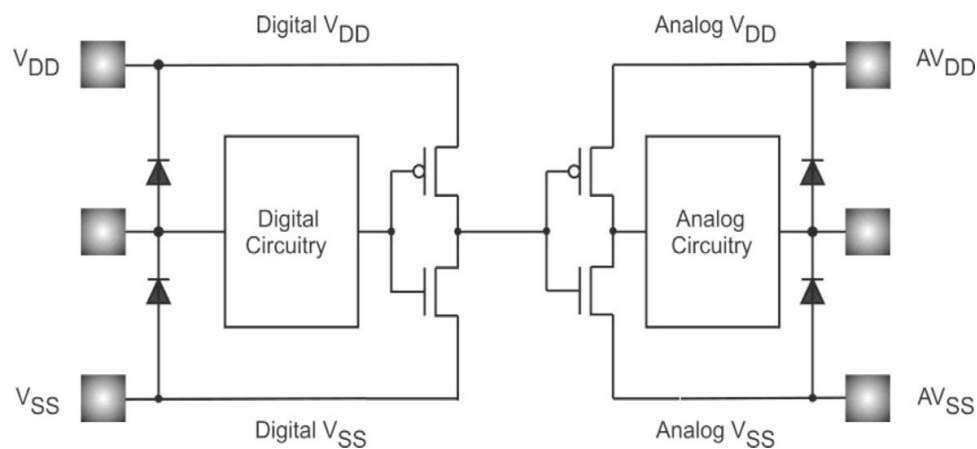


Figure 7. Digital to analog core internal signal lines requiring internal ESD.

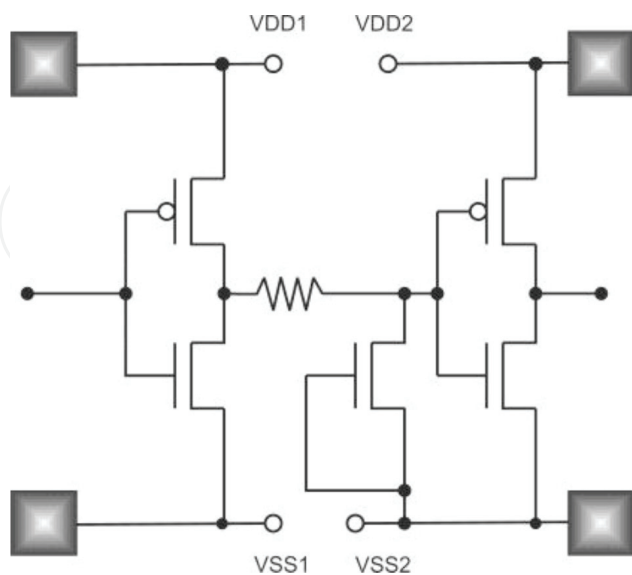


Figure 8. Internal ESD networks between cores.

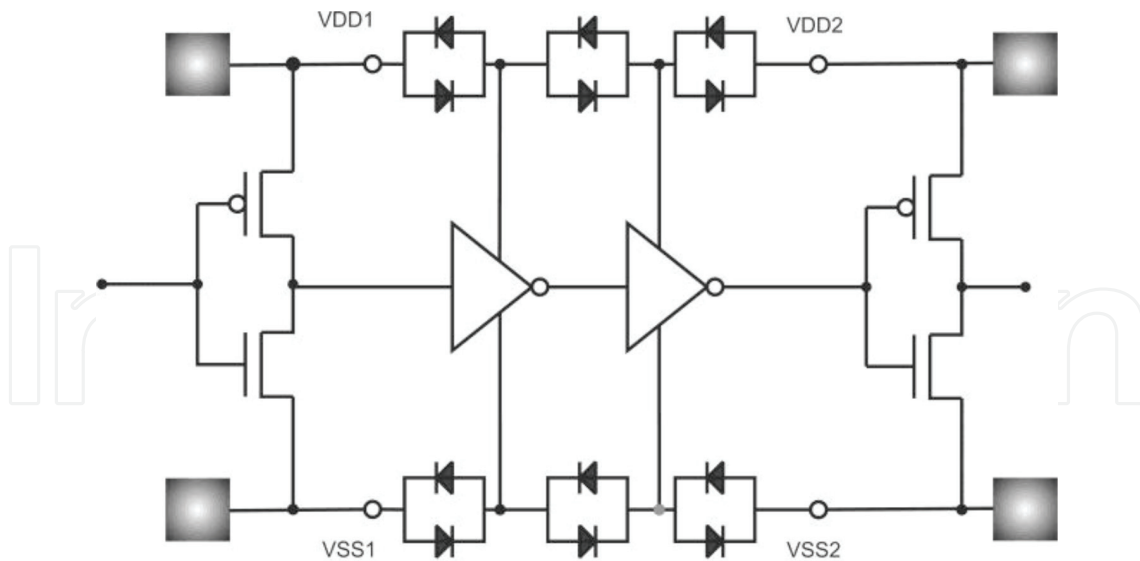


Figure 9. Third-party circuits between digital and analog cores.

6. Array I/O versus peripheral I/O architectures

In high pin count environments, the I/O networks can be distributed with the core of a semiconductor chip instead of the periphery. This is referred to as “array I/O” where the I/O cells are placed in an array fashion throughout the core. This has a large advantage for wiring, and performance, but alters the ESD and latch-up methods and needs.

6.1. Array I/O and ESD

In an array I/O environment, the I/O and ESD are co-integrated into the same I/O cell within the semiconductor chip and ASIC core. A significant change in the ESD results is that the ESD failure distribution is dependent on the wire width from the bond pad to the I/O cell. In this fashion, a “transfer wire” extends from the bond pad to the I/O cell. The ESD failure mechanism can be the wiring itself and may limit the robustness of the system. The wiring choices on how to get from the bond pad to the ESD network are also key to the robustness of the ASIC system. The ESD robustness of the system can be “wiring limited.”

6.2. Array I/O and latch-up

A key issue in an array I/O environment is the onset of latch-up [7, 8]. All the circuitry surrounding the I/O cell is core circuitry with no guard rings placed around them. Latch-up can occur from the injection of carriers into the substrate from the ESD network into the surrounding circuitry (**Figure 10**). Solutions to avoid this issue are as follows:

- Wider guard rings around the I/O cell to capture carriers

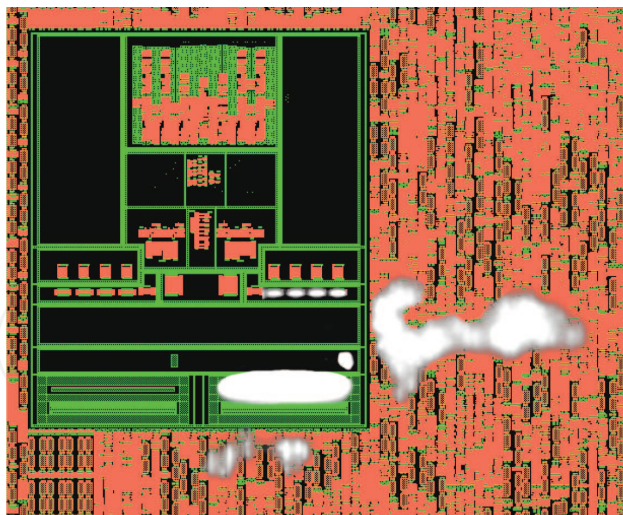


Figure 10. An example of array I/O and latch-up propagation in the core circuitry.

- Different guard ring structures with higher efficiency of carrier capture (e.g., trench, moats, etc.)
- Decreasing the n-well and p-well contact placement in the core circuitry adjacent to the I/O cell

7. Advanced technology nodes

Electrostatic discharge (ESD) will be an issue in ASIC technology as we evolve to new technologies, new devices, and 2.5D and 3D systems. These transitions will have a significant effect on ESD protection in the future.

7.1. 2.5D and 3D ASIC systems

In today's applications, migration to 2.5D and 3D systems has begun. In 2.5D applications, there are a significant number of wire bonds that interconnect the stacked chips. This has implications to electrical overstress (EOS) and wire-bond reliability. In 3D applications, the introduction of through-silicon via (TSV) technology changes the interrelation of how current flows through the multi-chip design; this has an influence on power grid design, placement of the TSV structure, and ESD devices. ESD design may require co-design with the power and ground placement of the multi-chip ASIC system.

7.2. Silicon on insulator (SOI)

Silicon on insulator (SOI) has been a mainstream technology since 2000 [1–3]. Microprocessors have been designed with excellent ESD protection levels in partially depleted SOI technology. From an ESD perspective, new SOI ESD structures were integrated, as well as addressing new SOI failure mechanisms, since these structures behaved differently than bulk ESD elements [29, 30].

7.3. FinFET

Presently, the FinFET device is being integrated into advanced sub-25 nm technologies [31–33]. With the FinFET structure, the layout and guard ring strategy will be influenced leading to different ESD layouts and designs. In the future, the direction may include both bulk and SOI FinFETs, which will respond differently for ESD and for latch-up. With the scaling of the FinFET structure, the shallow trench isolation (STI) will be scaled leading to higher parasitic bipolar current gain in the FinFET technology [33].

8. Closing comments and summary

Electrostatic discharge (ESD) has been a crucial issue in ASIC design flow and release and will continue to be an issue as semiconductor devices are scaled below 20 nm in both future and present-day nanotechnology era. As technologies migrate to sub-25 nm technology, ESD, latch-up, and EOS will be an issue for both bulk and SOI FinFET technologies.

Acknowledgements

I would like to thank the IBM ASIC I/O development team for the many years of collaboration and integration of ESD and latch-up solution into four generations of ASIC design methods. Special thanks to team lead Douglas Stout, James Pequignot, and Jeffrey Sloan. I would also like to thank the IBM Cadence™ software development of Susan Strang, Don Jordan, and C.N. Perez for implementing the ESD hierarchical parametrized cell system.

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