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Interface Control Processes for Ni/Ge and Pd/Ge Schottky and Ohmic Contact Fabrication: Part Two

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Abstract

We examine the reported interface-based processes used in the modulation of Schottky barrier heights at the nickel germanide/n-type germanium and palladium germanide/n-type germanium junctions. Various sample preparation and characterization methods are discussed. Stable Ni/Ge and Pd/Ge structural phases are identified, and their temperature range of stability is established. Current-voltage (I-V) and capacitance-voltage (C-V) characteristics are analyzed to study the effect of various interface control processes. Sheet resistivity and its stability over various annealing temperature ranges are analyzed. The fundamental mechanisms at play in order to achieve ohmic characteristics are observed and analyzed using various interface control processes. Some interfacial and structural factors that pin the Fermi level are analyzed in relation to experimental results. The different interfacial control processes are analyzed, and their effectiveness is compared. Recommendations are made for the improvement of Ni and Pd contacts in the next generation of n-type germanium-based nanoelectronic devices.

Keywords: thin film, Schottky barrier, ohmic contact

1. Introduction

The fact that ohmic contacts provide an almost unimpeded transfer of majority carriers across an interface makes them an essential part of nanoelectronic device fabrication. The interface control processes of producing ohmic contacts in germanium-based technology, such as the local incorporation of dopant atoms at the metal-germanium interface and the insertion of an interlayer into the interface, result in contacts that have values of resistivity which are very sensitive to the interlayer thickness and the temperature of annealing used during the fabrication process. These aspects of the interface control processes will be examined in this chapter.

We present a review of some of the novel interface control processes developed for the fabrication of NiGe/*n*-Ge and PdGe/*n*-Ge Schottky and ohmic contacts.

2. Results and discussion

2.1. Phase-formation sequences

There has been a lot of work reported on the solid-state interactions in the Ni/Ge system [1–5] but interactions in the Pd/Ge system have not been as extensively reported on [6–8]. The available reports agree on the second and the final phase NiGe formed in the Ni/Ge system, but there is some disagreement on the first phase. There is agreement that Pd_2Ge is the first phase to be formed in the Pd/Ge system, the second and final phase to be formed is also agreed upon to be PdGe. These phases are generally reported to form sequentially [7, 9]. Our results [10, 11] for the phase-formation sequences, formation temperatures, and dominant diffusing species (DDS) during reactive diffusion in the Ni/Ge and Pd/Ge systems, obtained using in-situ (real-time) Rutherford Backscattering Spectrometry (RBS) and particle induced X-ray emission (PIXE) are summarized in **Table 1**.

We see from **Table 1** that in order to produce NiGe at an interface, the annealing temperature needs to be above 250°C. Below that temperature, Ni_5Ge_3 is produced. We also see that PdGe needs to be formed above an annealing temperature of 180°C, below which Pd_2Ge is formed. One positive aspect from these results in terms of device fabrication is that the two phases of interest, which are NiGe and PdGe, are the final phases to be formed in the Ni/Ge and Pd/Ge systems, respectively. What this means is that annealing at temperatures above 250°C and 180°C in the Ni/Ge and Pd/Ge systems respectively would effectively avoid the formation of the other phases of the systems.

Phases observed	Ni_5Ge_3, NiGe, Pd_2Ge, PdGe	
Phase-formation sequence	1st	Ni_5Ge_3, Pd_2Ge
	2nd	NiGe, PdGe
Phase-formation temperatures	Ni_5Ge_3	150°C
	Pd_2Ge	140–150°C
	NiGe	250°C
	PdGe	180°C
Diffusing species	Ni_5Ge_3	Ni
	NiGe	Ni is the DDS; Ge diffusion observed during the early stages of growth.
	Pd_2Ge	60% Pd and 40% Ge
	PdGe	65% Pd and 35% Ge

Table 1. Summary of our results for the thin film couple phase-formation sequences, phase-formation temperatures, and dominant diffusing species during the respective phase growths in the Ni/Ge and Pd/Ge systems [10, 11].

2.2. NiGe contacts

2.2.1. Cyclically stacked NiGe contacts

One of the concerns regarding NiGe contacts on n-type Ge substrates is that other phases of the Ni/Ge system apart from NiGe are formed below 250°C. Another concern is the reaction of the deposited Ni film and the Ge substrate, which increases the interface roughness. Suppression of this interface reaction by the use of cyclic stacking, as explained in Section 2.1.3 of the previous chapter, is advantageous in obtaining a flat interface between NiGe and the Ge substrates. This was done in an investigation carried out by Motoki [12]. The wafers used in this study were n-type Ge (100) with a doping density of 4.0×10^{16} cm^{-3}. These substrates were treated with HF after which sets of Ni/Ge (0.5 nm/1.3 nm) layers were cyclically stacked eight times using RF magnetron sputtering. The thickness of the layers corresponded to an atomic ratio between Ni and Ge of 1 to 1, as in the phase NiGe. As explained in Section 2.1.3 of the previous chapter, the concept behind this process is to suppress the interface reaction, upon annealing, between the deposited Ni and the Ge substrate, hence reducing the number of interface electron energy states. The samples configuration is illustrated in **Figure 1**.

Two samples of cyclically stacked Ni/Ge were produced, one with 8 Ni/Ge cycles (referred to as sets in the figures) and the other with 16 cycles. In order to see if cyclic stacking produces improved results, two other samples were prepared with Ni films of thickness 3.0 and 5.5 nm respectively on Ge substrates without cyclic stacking, for comparison. The four types of samples, including the cyclically stacked ones, were annealed in nitrogen (N_2) gas at annealing temperatures that ranged from 200 to 500°C for 1 min. Four-terminal sheet resistance measurements were carried out on the samples as explained in Section 2.3 of the previous chapter. **Figure 2** shows experimental results of the sheet resistivity (ρ_{sh}) of the films as a function of the annealing temperature. We see a large decrease in sheet resistivity for the sample with a 3.0 nm-thick Ni film and no cyclic stacking within the temperature range from 200 to around 300°C. This is attributed to the formation of the NiGe phase. When the annealing temperature is over 350°C, the sheet resistivity shows a large increase owing to thermal instability. In the sample with a 5.5 nm-thick Ni layer and no cyclic stacking, the temperature range of the NiGe thermal phase stability is wider than that for the
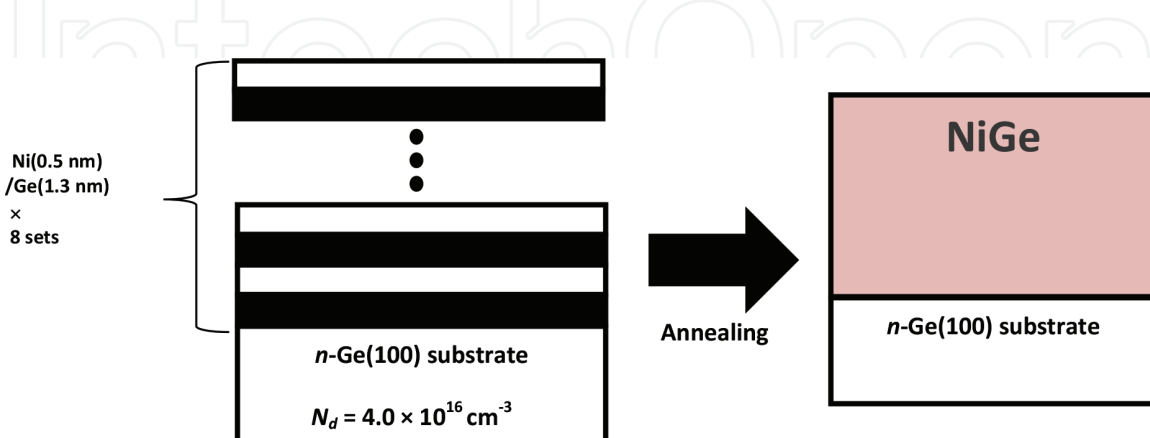

Figure 1. Cyclically stacked samples to suppress the interface reaction, upon annealing, between the deposited Ni and the Ge substrate.
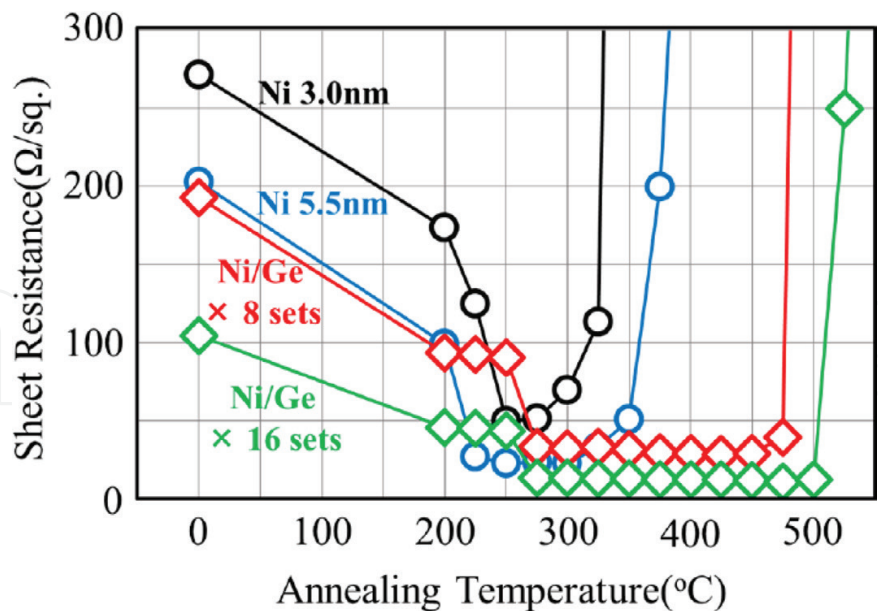
Figure 2. Experimental results of the sheet resistivity (ρ_{sh}) of Ni/Ge films as a function of the annealing temperature [12].
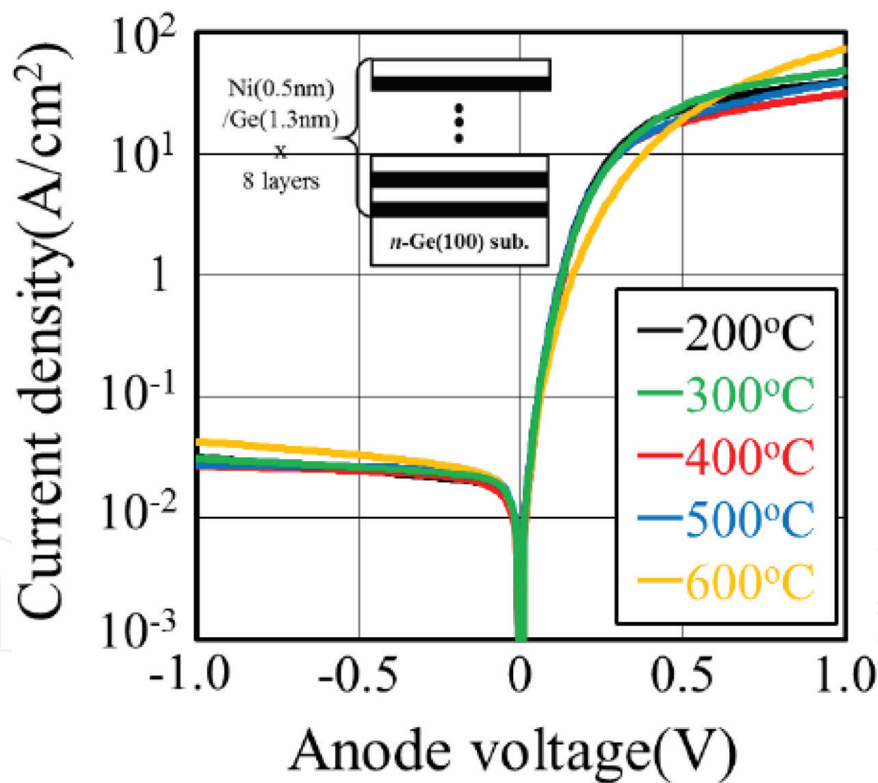

Figure 3. Current-voltage characteristics of the cyclically stacked NiGe at various annealing temperature from 200 to 600°C [12].

sample with the 3.0 nm-thick Ni layer. On the other hand, for the samples with cyclic stacking, a reduction in ρ_{sh} was observed over 250°C, and the value became stable at annealing temperatures from 275 to around 500°C. This demonstrates that cyclic stacking produces improved results.

Figure 3 shows the current-voltage characteristics of the cyclically stacked NiGe at various annealing temperature from 200 to 600°C. It is seen that the current density profile on a

semilogarithmic scale in the reverse bias directions (negative anode voltage region) are very small compared to those in the forward bias direction, showing that the contacts are rectifying, which is typical Schottky diode behavior.

The height of the Schottky potential barrier, Φ_{Bn} and the ideality n-factor were extracted from the I-V characteristics of the Schottky diodes at various annealing temperatures using the thermionic emission model, as explained in Section 1.1.4 of the previous chapter. Equations (11) and (12), of the previous chapter, were used to extract Φ_{Bn} and the ideality n-factor respectively. The value of the effective Richardson constant, A^* used in this study was 133 A/cm^2 K^2. The results for the sample with a 5.5 nm-thick Ni layer (no cyclic stacking) and the Ni/Ge cyclically stacked sample with eight layers are shown in **Figure 4**, for annealing temperatures up to 600°C.

It is seen in **Figure 4** that the determination of both Φ_{Bn} and the ideality n-factor was repeated a number of times at each temperature, showing some experimental scattering errors, but the general trends are clear. The values of Φ_{Bn} that are determined for the sample with a 5.5 nm Ni film and the cyclically stacked Ni/Ge sample, annealed up to 600°C were within 0.54–0.57 and 0.53–0.55 eV, respectively. The ideality factor showed values of less than 1.3 for the cyclically stacked sample. We see in **Figure 4** that in this sample, the ideality factor could be maintained at values lower than 1.2 up to a temperature of 500°C, and it increases slightly at 600°C. In the
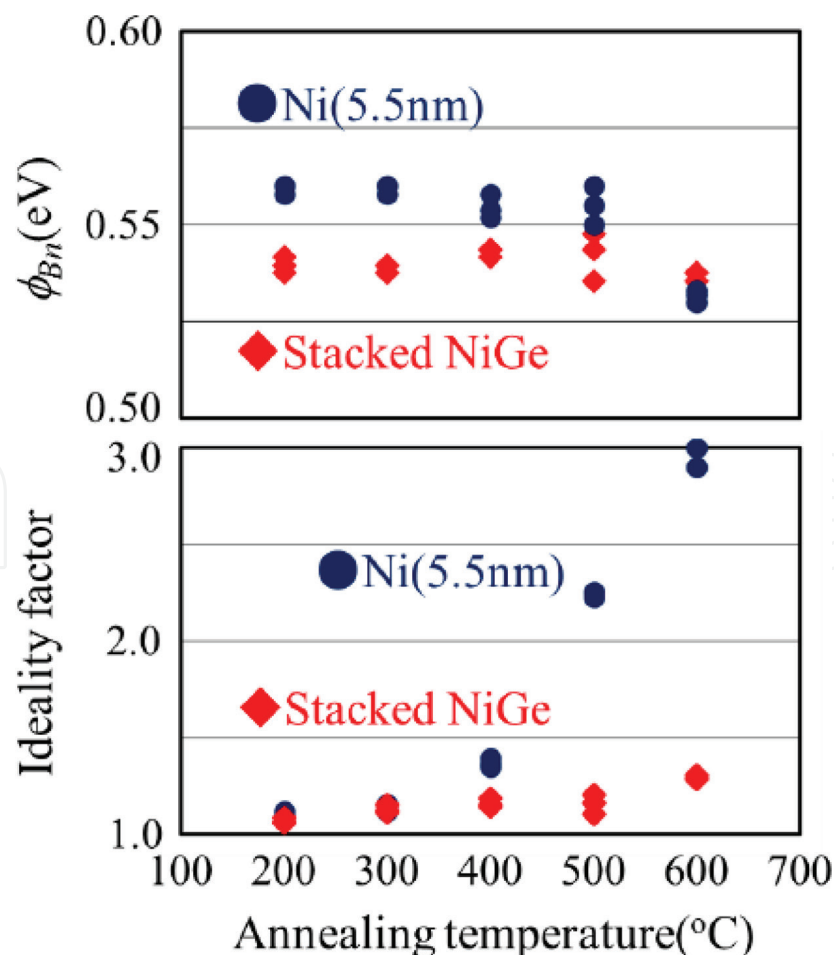

Figure 4. Heights of the potential barrier and the ideality n-factors for the Schottky contacts with stacked NiGe and with a 5.5 nm-thick Ni film, at various annealing temperatures [12].

sample with a 5.5 nm Ni film and no cyclic stacking, the values of the *n*-factor were very large for temperatures above 400°C, owing to thermal instability of NiGe films in this sample. This result is consistent with the sheet resistivity result presented in **Figure 2**. In **Figure 2**, we see that the sheet resistivity for this sample rises rapidly around 400°C.

2.2.2. Interface dopant incorporation

A sample with 22 nm of Ni on an *n*-type Ge substrate and another with 30 nm of Ni_3P on an *n*-type Ge were prepared by plasma deposition. **Figure 5** shows a schematic illustration of the two samples.

Current-voltage characteristics were obtained at various annealing temperatures (for 1 min) for the two samples in order to extract the Schottky potential barrier heights, Φ_{Bn} using the thermionic emission model. The results are shown in **Figure 6**.

The ideality *n*-factor for the sample with a 22-nm-thick Ni film was also determined and is presented in **Figure 6**. It can be seen in **Figure 6** that the determination of Φ_{Bn} and the *n*-factor was repeated a number of times at each temperature, showing some experimental scattering error. It is clear that the values of Φ_{Bn} for the Ni/*n*-Ge sample remained almost constant over the whole temperature range of annealing. It is however seen that the values of Φ_{Bn} for the Ni_3P/*n*-Ge sample gradually decreases with increased temperature and the lowest Φ_{Bn} value is achieved at 600°C, after which the value increases. The ideality factor of the Ni/*n*-Ge sample gradually increases but does not go above the value of 1.5.

Since we see from **Figure 6** that the values of Φ_{Bn} for the Ni_3P/*n*-Ge sample are the lowest at 600°C, we now focus on the current-voltage characteristics at this temperature alone for both the Ni/*n*-Ge and Ni_3P/*n*-Ge samples, the results are shown in **Figure 7**.

We see in **Figure 7(a)** that the current density profiles on a semilogarithmic scale for the forward and reverse bias (negative voltage region) directions are symmetric about the zero anode voltage axis for the Ni_3P/*n*-Ge sample, suggesting Ohmic characteristics. On the other hand, for the Ni/*n*-Ge samples, in the reverse bias direction, the current density is very small compared to that in the forward bias direction, showing that the contact is rectifying. In **Figure 7(b)**, the current density profile is presented on a linear scale. For the Ni_3P/*n*-Ge sample, we get a straight line which confirms that this is an ohmic contact. The corresponding result for the Ni/*n*-Ge sample clearly shows that it is not an ohmic contact. It shows Schottky diode
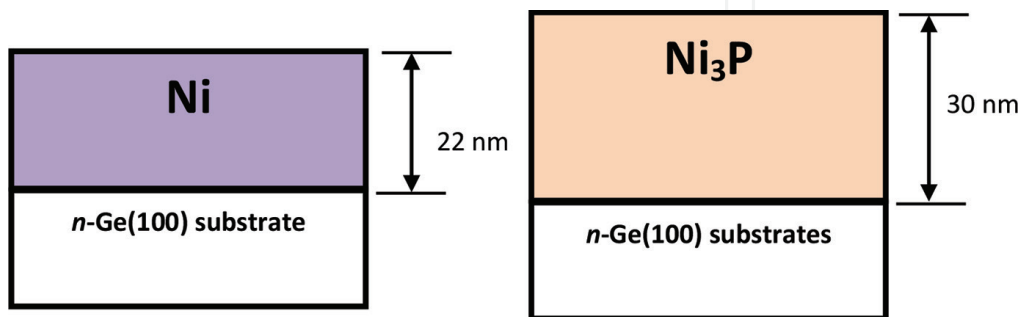

Figure 5. Schematic illustration of a sample with 22 nm of Ni on an *n*-type Ge substrate and another with 30 nm of Ni_3P on *n*-type Ge.
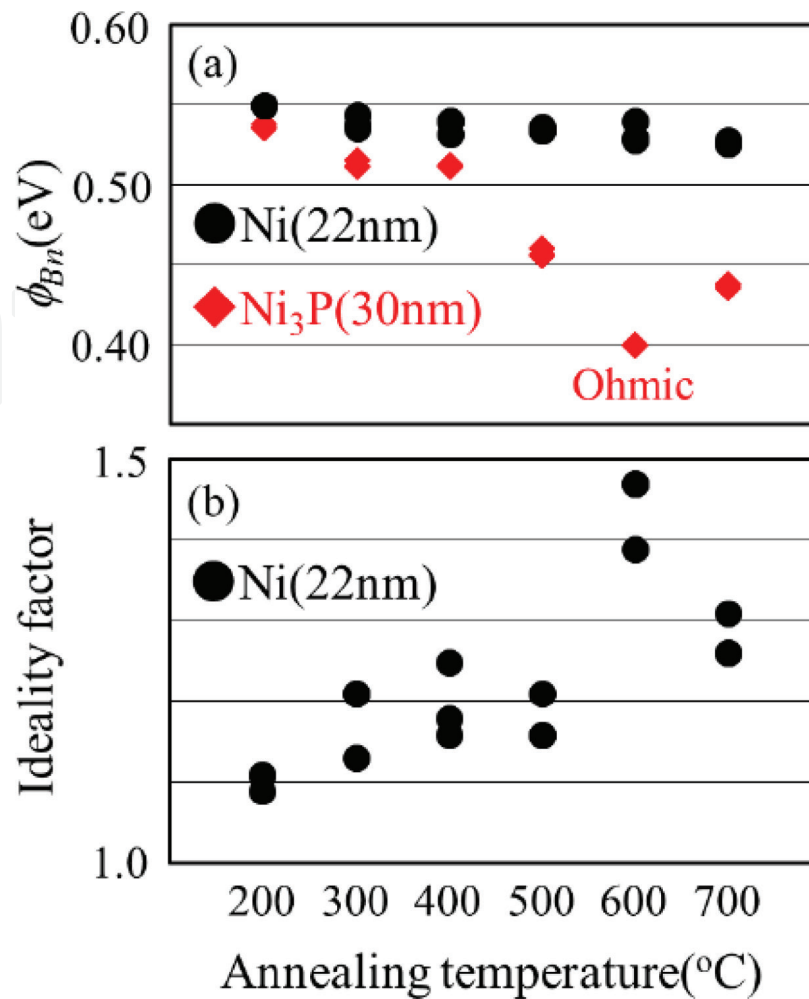
Figure 6. (a) Potential barrier heights at various annealing temperatures (for 1 min) for Ge Schottky contacts with a 30 nm-thick Ni_3P film and with a 22 nm-thick Ni film. (b) The ideality n-factor for the sample with a 22 nm-thick Ni film at various annealing temperatures [12].

characteristics as was illustrated schematically in **Figure 11** of the previous chapter. **Figure 8** shows a cross-sectional scanning electron microscope (SEM) image of the Ni_3P (30 nm)/n-Ge contact in the as-deposited state, (a) and after annealing at 600°C for 1 min, (b).

The SEM micrograph in **Figure 8(a)** shows a regular thickness of Ni_3P in the as-deposited contact. **Figure 8(b)** shows a much thicker reaction region up to a depth of 77.8 nm below the original interface. We saw in **Figure 6** that ohmic behavior was not achieved for annealing temperatures that were less than 600°C. It appears that at 600°C, the P atoms penetrated enough into the n-Ge substrate to form an interface region inside the substrate which is heavily doped by P atoms. This facilitates for the ohmic characteristics observed at 600°C.

2.2.3. Cyclically stacked NiGe contacts with interface dopant incorporation

A thin 0.68 nm film of Ni_3P was plasma deposited on an n-type Ge substrate after which sets of Ni/Ge (0.5 nm/1.3 nm) layers were cyclically stacked seven times. **Figure 9** shows a schematic illustration of the sample.
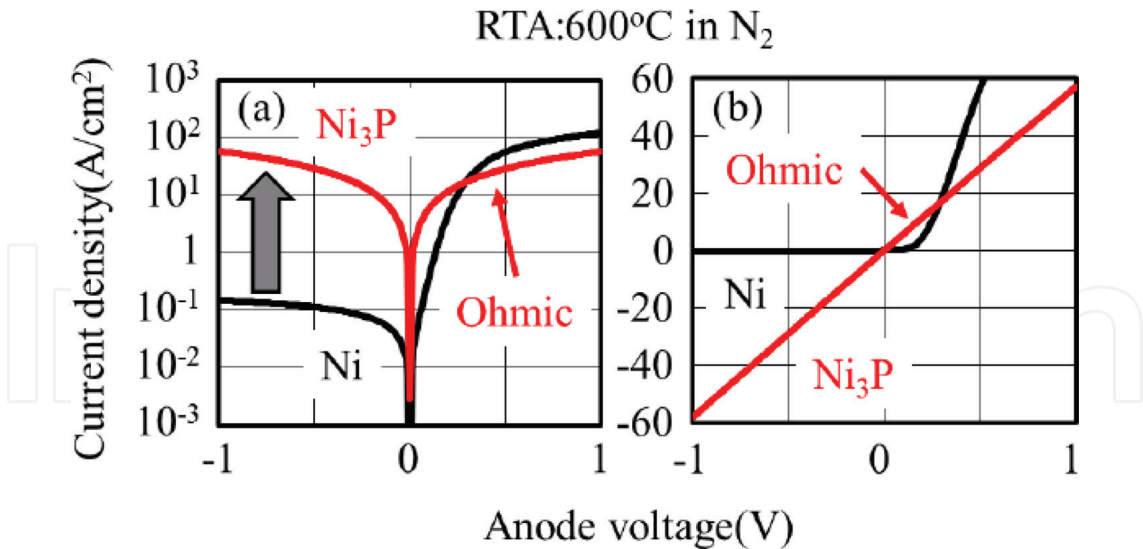
Figure 7. (a) Current density profile on a semilogarithmic scale for the forward and reverse bias directions for Ni/n-Ge and Ni$_3$P/n-Ge samples. (b) Current density profile of the same samples on a linear scale [12].
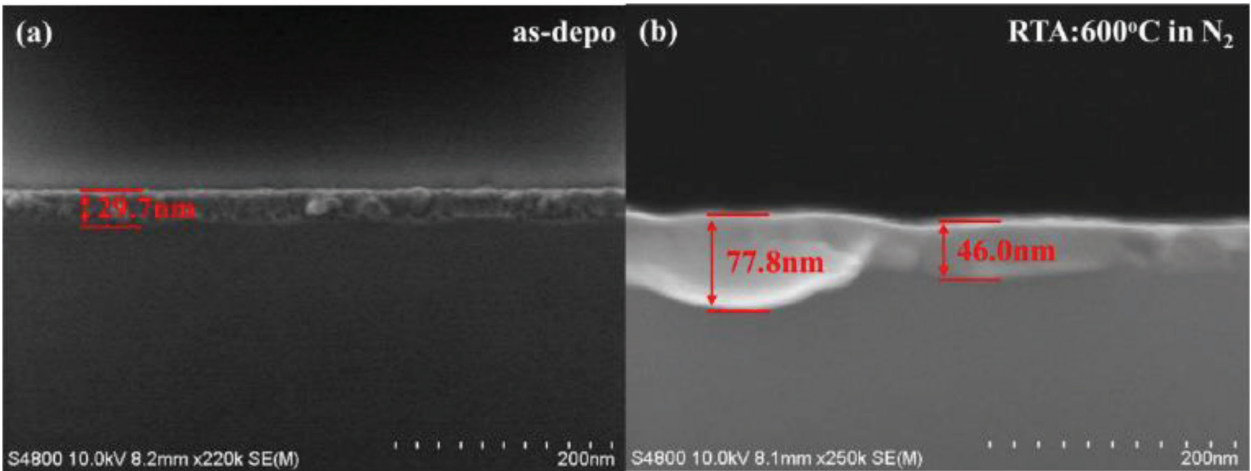

Figure 8. (a) A cross-sectional scanning electron micrograph of an as-deposited Ni$_3$P/n-Ge contact. (b) A micrograph similar to the one presented in (a) but after annealing at 600°C [12].

Current-voltage characteristics were obtained at various annealing temperatures for 1 min. The potential barrier heights, Φ_{Bn} were extracted using the thermionic emission model, as explained earlier. The results are shown in **Figure 10**, and results for cyclically stacked NiGe without a thin 0.68 nm film of Ni$_3$P are also included in **Figure 10** for comparison.

It is seen in **Figure 10** that the Ni$_3$P film reduces the barrier height by about 0.51 at 500°C. We now focus on the current-voltage characteristics at the temperatures of 400 and 500°C for both the cyclically stacked samples with and without an Ni$_3$P film. The results are shown in **Figure 11**.

The sample without an Ni$_3$P film is used as a control to compare with the one with an Ni$_3$P film, the results from this sample are therefore labeled as "control" in **Figure 11**. It can be seen
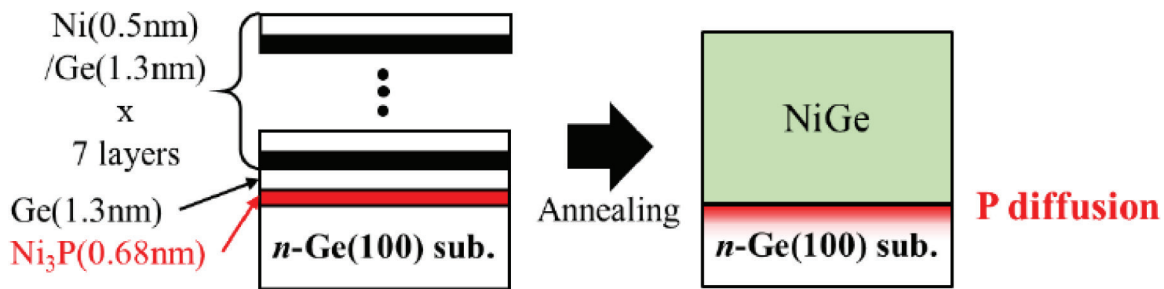
Figure 9. Schematic illustration of sets of Ni/Ge (0.5 nm/1.3 nm) layers cyclically stacked seven times over a thin 0.68 nm film of Ni$_3$P on an *n*-Ge(100) substrate [12].
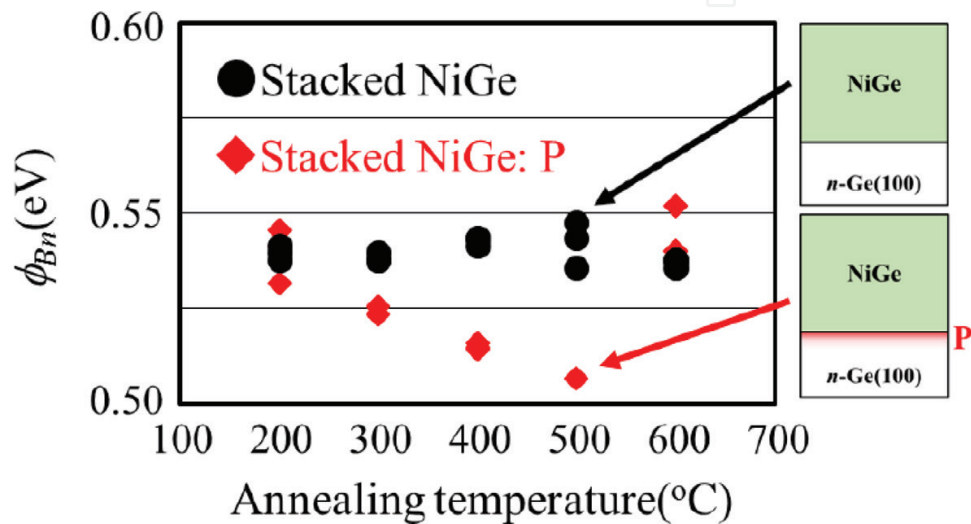

Figure 10. Potential barrier heights extracted at various temperatures for cyclically stacked NiGe with and without a thin 0.68 nm film of Ni$_3$P [12].

that both contacts are rectifying. Despite the reduction in the barrier height seen in **Figure 10**, the incorporation of a Ni$_3$P film does not result in an ohmic contact in this case.

2.2.4. Interface insertion of a silicon film

A silicon film with a varying thickness, x, is deposited on an *n*-type Ge substrate after which sets of Ni/Ge (0.5 nm/1.3 nm) layers were cyclically stacked seven times. Samples were prepared in this way for four different values of the Si film thickness, which are: x = 0.1, 0.3, 0.6 and 1.0 nm. Another set of similar samples were prepared with the only difference being the introduction of a 0.68-nm-thick Ni$_3$P film between the Si film and the sets of Ni/Ge (0.5 nm/1.3 nm) layers. **Figure 12** shows a schematic illustration of the two types of sample configuration.

The current-voltage characteristics for samples without P incorporation (w/op) and with P incorporation (w/p), annealed at a temperature of 400°C for 1 min, are shown in **Figure 13** for the different values of Si thickness, x.

It can be seen in **Figure 13** that ohmic characteristics are observed for the contact with P incorporation (w/p) and a silicon film thickness of 0.1 nm. Current-voltage characteristics
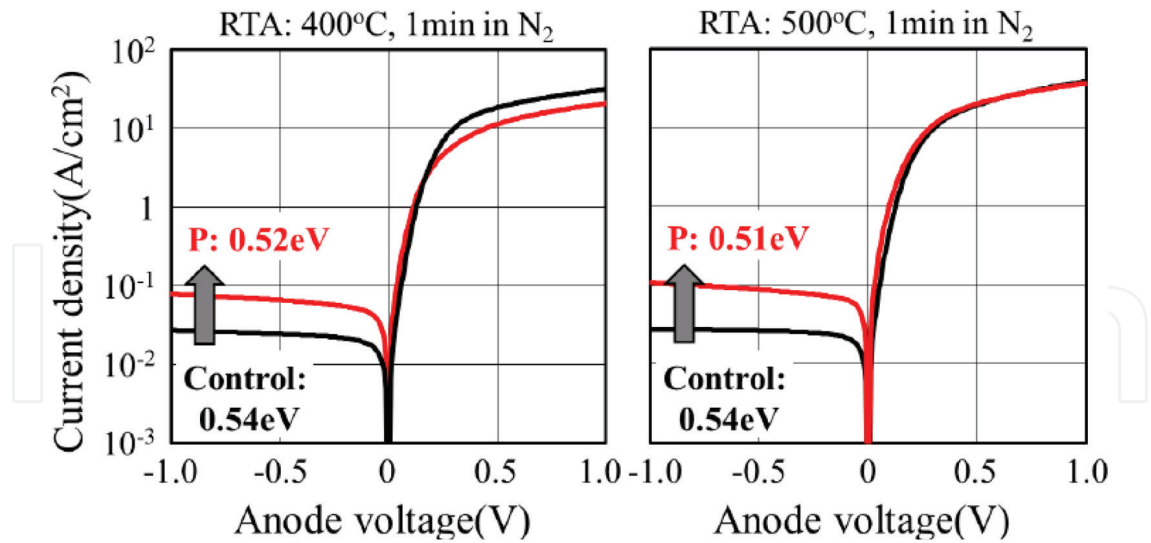
Figure 11. Current-voltage characteristics at the temperatures of 400 and 500°C for both the cyclically stacked samples with and without an Ni₃P film [12].
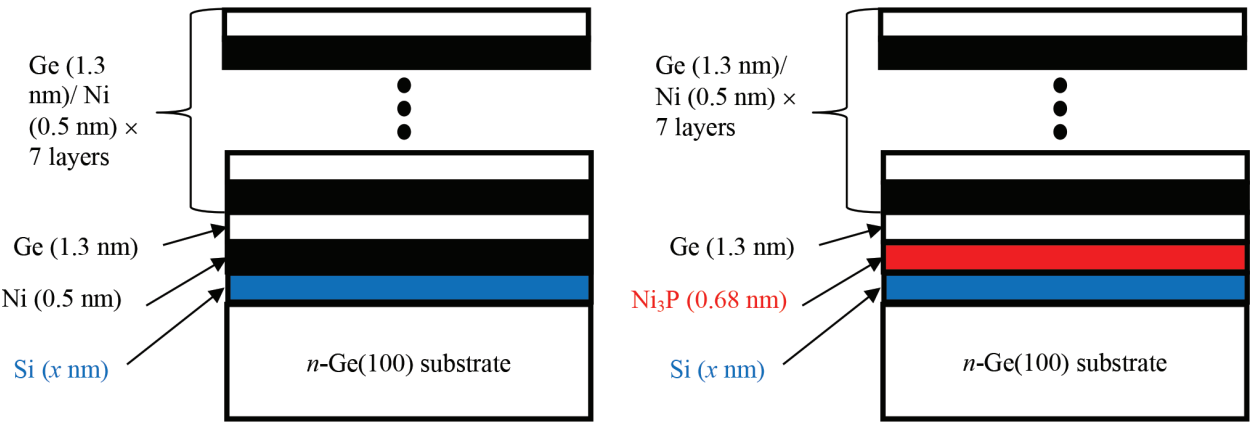

Figure 12. Schematic illustration of two types of cyclically stacked sample configurations with the insertion of a silicon film.

were obtained for annealing temperatures between 200 and 600°C. The barrier heights were determined at these temperatures of annealing and are presented in **Figure 14**.

We see in **Figure 14** that a silicon thickness of 0.1 nm gives the lowest barrier height for both types of samples. However, ohmic characteristics are only observed when P is incorporated and at an annealing temperature of 400°C, as seen in **Figure 13**. An annealing temperature of 300°C with $x = 0.1$ nm gives characteristics that are nearly ohmic as indicated in **Figure 14**.

The four materials, Si, NiGe, n-type Ge, and P doped n-type Ge have different work functions. These four materials therefore have individual energy band structures with the respective Fermi levels being at different positions relative to the vacuum level. After a contact between any of these materials is made, the Fermi level becomes constant throughout the system at equilibrium, and the energy bands, which should have continuous characteristics, therefore bend.
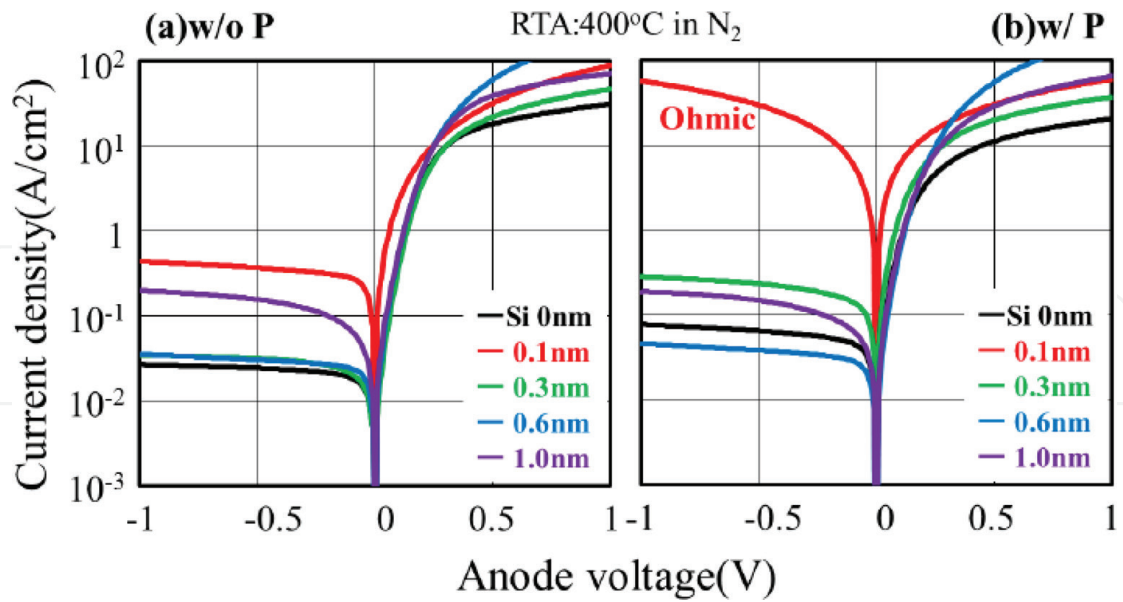
Figure 13. Current-voltage characteristics for samples without P incorporation (a) and with P incorporation (b), annealed at a temperature of 400°C for 1 min and different values of Si thickness, x [12].
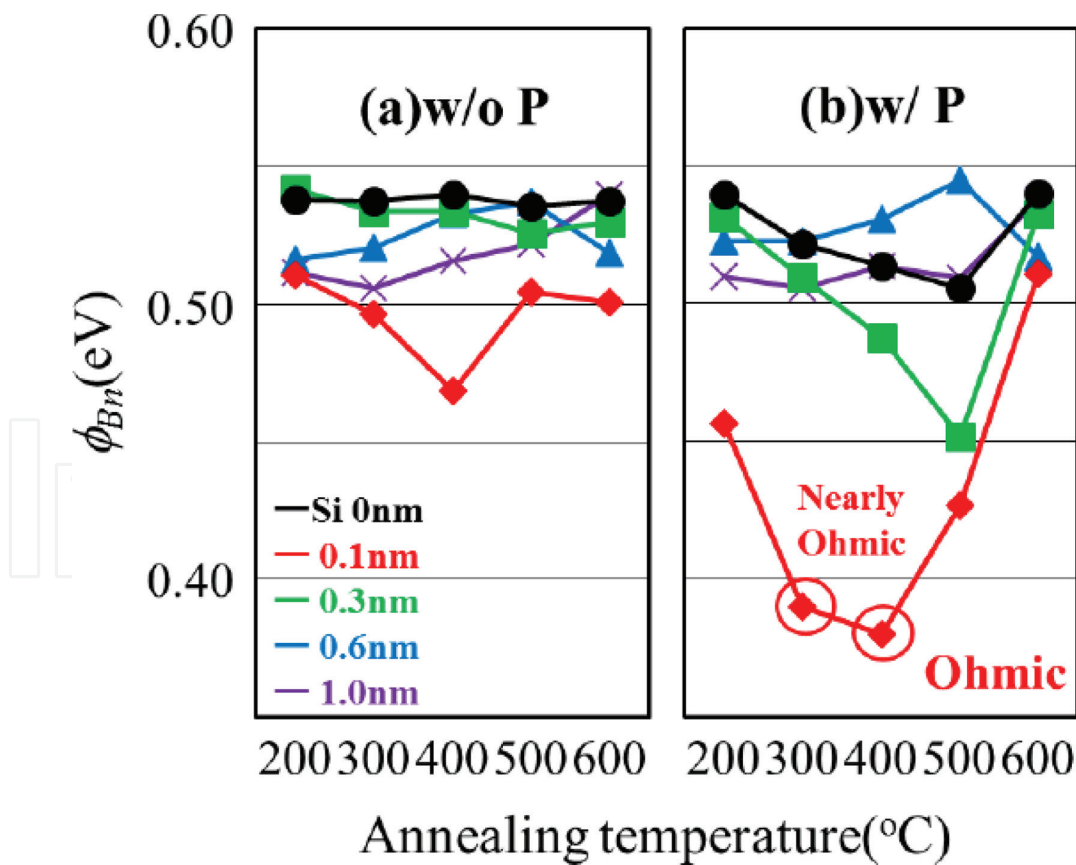
Figure 14. (a) Barrier heights at various temperatures of annealing and varying thickness of the Si film inserted, without the incorporation of P atoms. (b) A plot of results similar to the ones in (a) but with the incorporation of P atoms [12].

Figure 15(i) shows this energy band bending at the NiGe/*n*-Ge interface. **Figure 15(ii)** and **(iii)** show the energy band bending at the NiGe:P/*n*-Ge and NiGe:P/Si/*n*-Ge interfaces respectively. We see the successive reduction in the Schottky potential barrier heights from 0.54 to 0.51 eV in **Figure 15(i)** and **(ii)** respectively and then 0.42 eV in the ohmic contact of **Figure 15(iii)**. The energy band bending due to the doping by diffused P atoms is shown in **Figure 15(ii)** and **(iii)**. **Figure 15(i)** shows that the Fermi level is pinned. As explained in Section 1.1.5 of the previous chapter, this Fermi-level pinning is caused by dipole formation due to the large amount of interface states. The diameter of a silicon atom is approximately 0.1 nm and the thickness of the silicon layer in **Figure 15(iii)** is also 0.1 nm, meaning that it was essentially a monolayer deposition of silicon which released the Fermi-level pinning and achieved an ohmic contact. The large modulation of the Schottky potential barrier height due to the insertion of a 0.1-nm-thick Si monolayer is explainable by considering that the Si atoms caused the formation of chemical bonds between NiGe, Si, and *n*-Ge, thereby reducing the number of dangling bonds (valence mending) that are responsible for the dipole formation which is explained in Section 1.1.5 of the previous chapter.
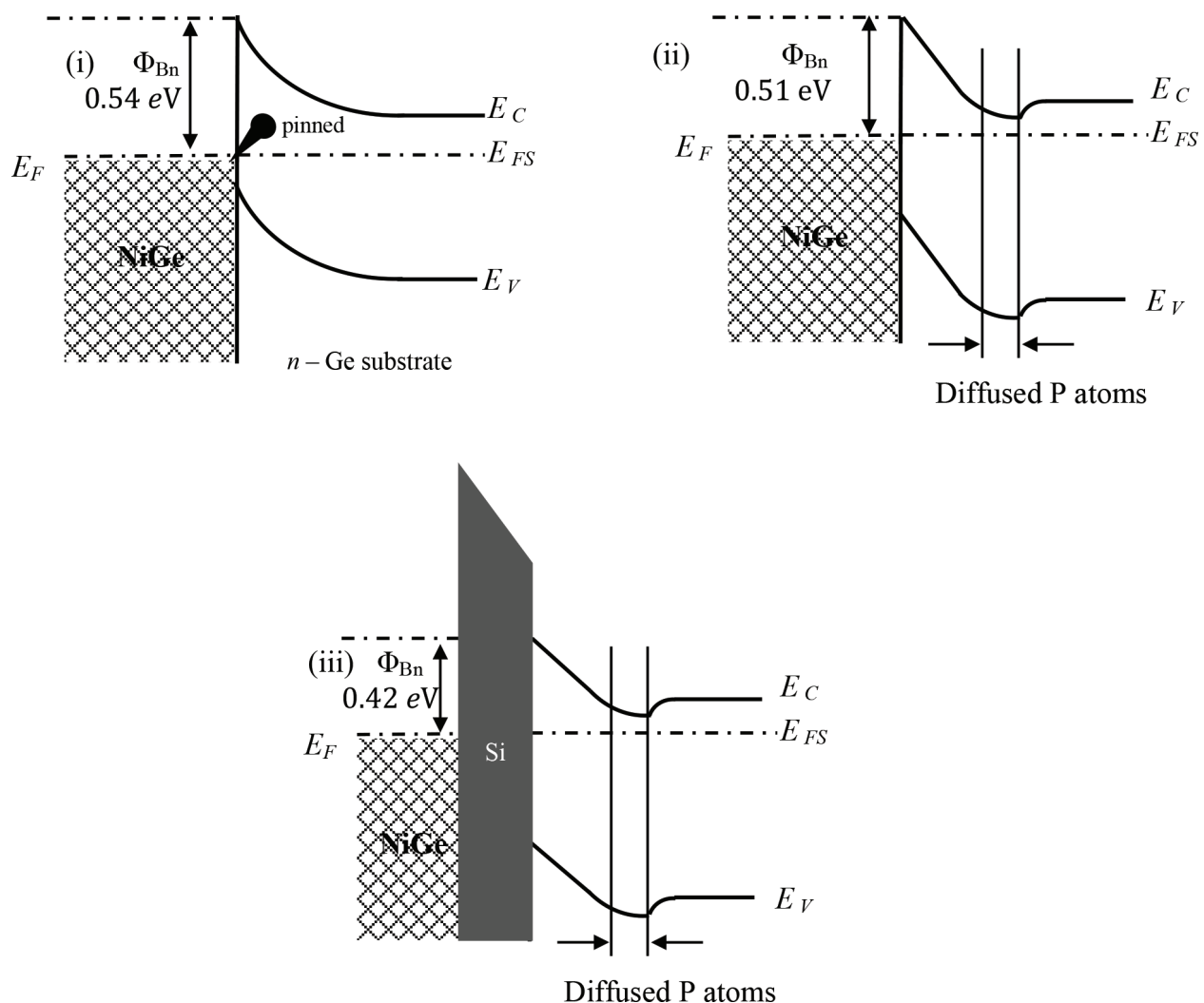

Figure 15. Schematic energy band diagrams of: (i) an NiGe/*n*-Ge interface; (ii) an NiGe/*n*-Ge interface with the incorporation of P atoms; (iii) an NiGe/*n*-Ge interface with the incorporation of P atoms and the insertion of a silicon layer.

2.3. PdGe contacts

Chawanda et al. [13] used *n*-type Ge(111) doped with antimony (Sb) at a density of 2.5×10^{15} cm^{-3}. Pd was deposited onto the substrates by vacuum resistive evaporation as explained in Section 2.1.1 of the previous chapter. This was done through a mechanical mask which had circular windows of diameter, 0.6 ± 0.05 mm. In this way, 24 circular contacts were prepared in a single evaporation. The thickness of each deposited layer of Pd was 30 nm. Room temperature forward and reverse bias current-voltage characteristics were obtained for five of the Pd/*n*-Ge contacts, which acted as Schottky barrier diodes. The results are shown in **Figure 16**.

Rectifying characteristics are seen for all samples in **Figure 16**. The height of the Schottky potential barrier, Φ_{Bn} and the ideality *n*-factor were extracted from the forward bias I-V characteristics of the Schottky diodes at room temperature using the thermionic emission model, as explained in Section 1.1.4 of the previous chapter. This was done for several samples and a histogram was produced to show the statistical distribution of the effective potential barrier heights from the forward bias I-V characteristics, and this is presented in **Figure 17**.

The effective potential barrier heights obtained from the I-V characteristics varied from 0.492 to 0.550 eV. A Gaussian distribution function was used to obtain fits to the histogram. The statistical analysis yielded a mean Schottky potential barrier height value of 0.529 eV with a standard deviation of 0.019 eV.

A histogram was also produced for the values of the ideality factors determined from the I-V characteristics. **Figure 18** shows the statistical distribution of ideality factors from the forward bias I-V characteristics.
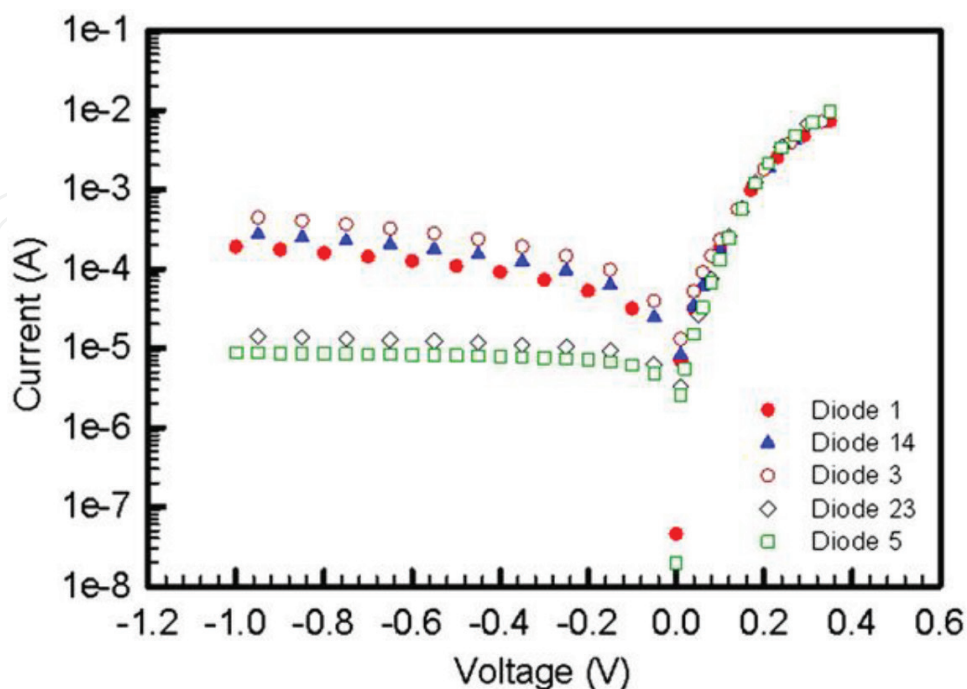

Figure 16. Room temperature forward and reverse bias current-voltage characteristics obtained for five of the Pd/*n*-Ge contacts [13].
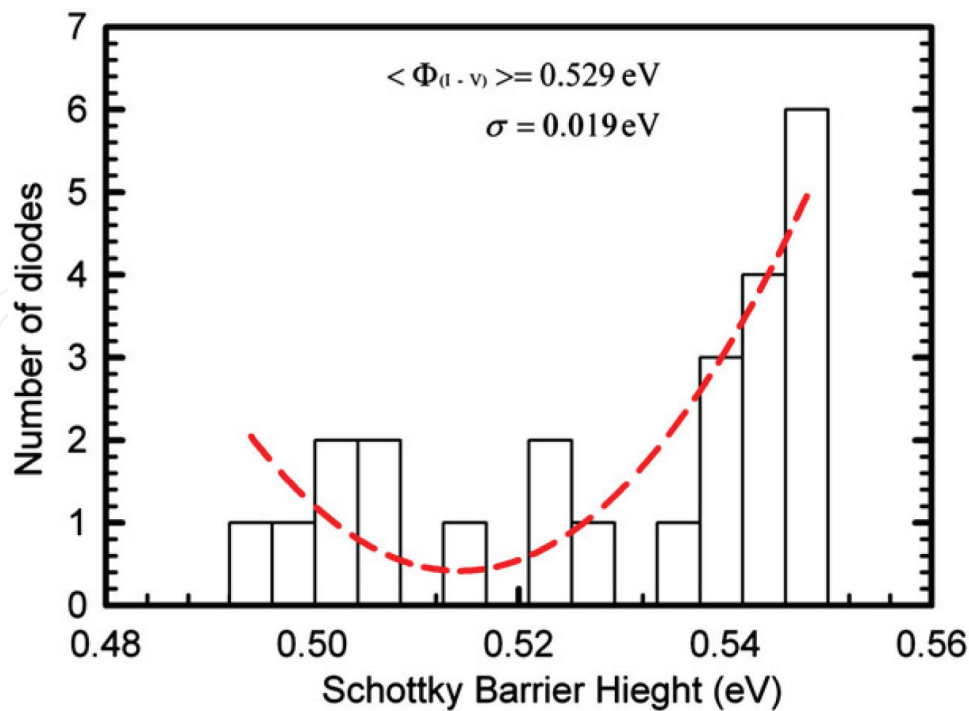
Figure 17. Room temperature Schottky potential barrier height distribution derived from forward bias I-V characteristics [13].

The ideality factor ranged from 1.140 to 1.950. A Gaussian distribution function was used to obtain a fit to the histogram. The statistical analysis of the ideality factor yielded an average value of 1.414 with a standard deviation of 0.270.

It is seen that the experimental effective potential barrier heights and ideality factors differ from contact to contact even though they were identically prepared in a single evaporation and on the same substrate. A plot of the effective potential barrier heights as a function of the respective ideality factors is shown in **Figure 19**.

The experimental effective potential barrier height decreases as the ideality factor increases. We see a linear relationship and the straight line drawn in the figure is the least-squares fit to the experimental data.

Five Pd/n-Ge contacts were experimentally examined at room temperature to obtain the reverse bias C^{-2}-V characteristics. The results are shown in **Figure 20**.

We see in **Figure 20** that each contact gives a straight line in the C^{-2}-V graphs. The value of the capacitance-voltage derived potential barrier height, $\Phi_{B(C-V)}$ can be obtained from **Figure 20** using,

$$\Phi_{B(C-V)} = V_D + E_F - \Delta\Phi_B \tag{1}$$

where E_F is the energy difference between the bulk Fermi level of Ge and the conduction band edge, V_D is the diffusion potential, and $\Delta\Phi_B$ is the image-force barrier lowering given by Eq. (16) in Section 1.1.4 of the previous chapter, where the maximum electric field E_m is calculated using Eq. (18) of the previous chapter.

The reverse bias C^{-2}-V characteristics were obtained for several samples and a histogram was produced to show the statistical distribution of the capacitance-voltage-derived potential barrier heights, and this is presented in **Figure 21**.
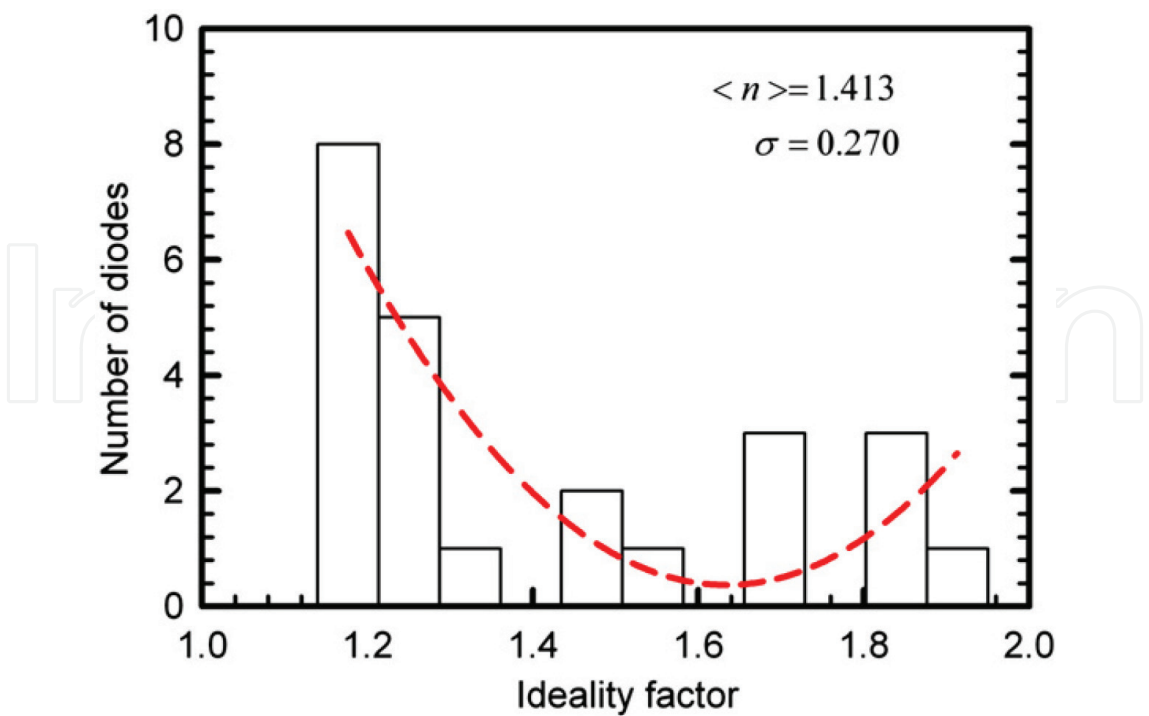
Figure 18. Statistical distribution of ideality factors from the forward bias I-V characteristics [13].
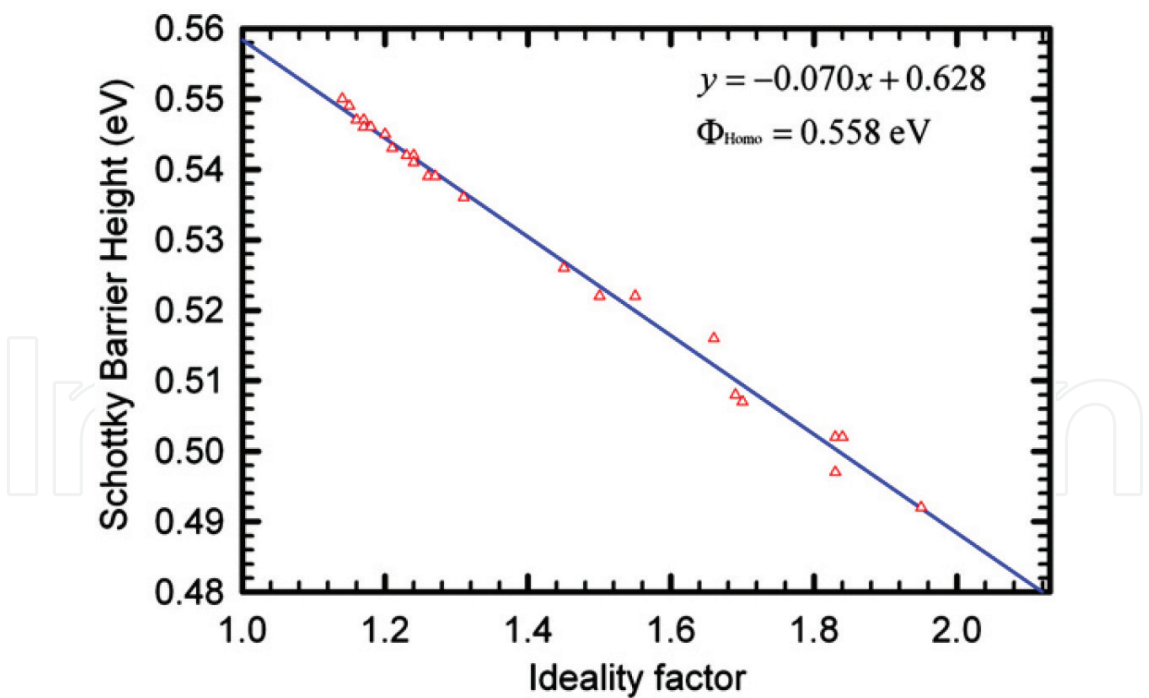

Figure 19. A linear plot of the Schottky potential barrier heights against the ideality factors [13].

The capacitance-voltage potential barrier heights for the Pd/n-Ge (111) Schottky structures varied from 0.427 to 0.509 eV. The statistical analysis yields a mean barrier height of 0.463 eV with a standard deviation of 0.023 eV. The difference between the mean Schottky potential barrier height obtained using the C^{-2}–V characteristics and that from the I-V characteristics
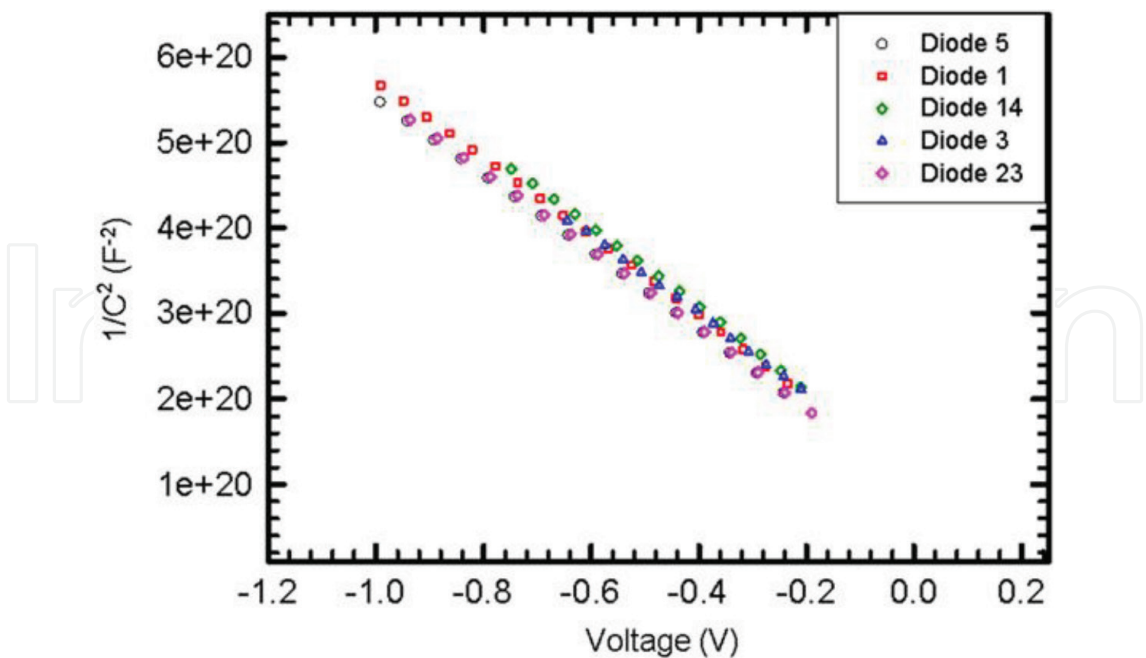
Figure 20. Schottky reverse bias C⁻²-V characteristics for five Pd/*n*-Ge samples [13].
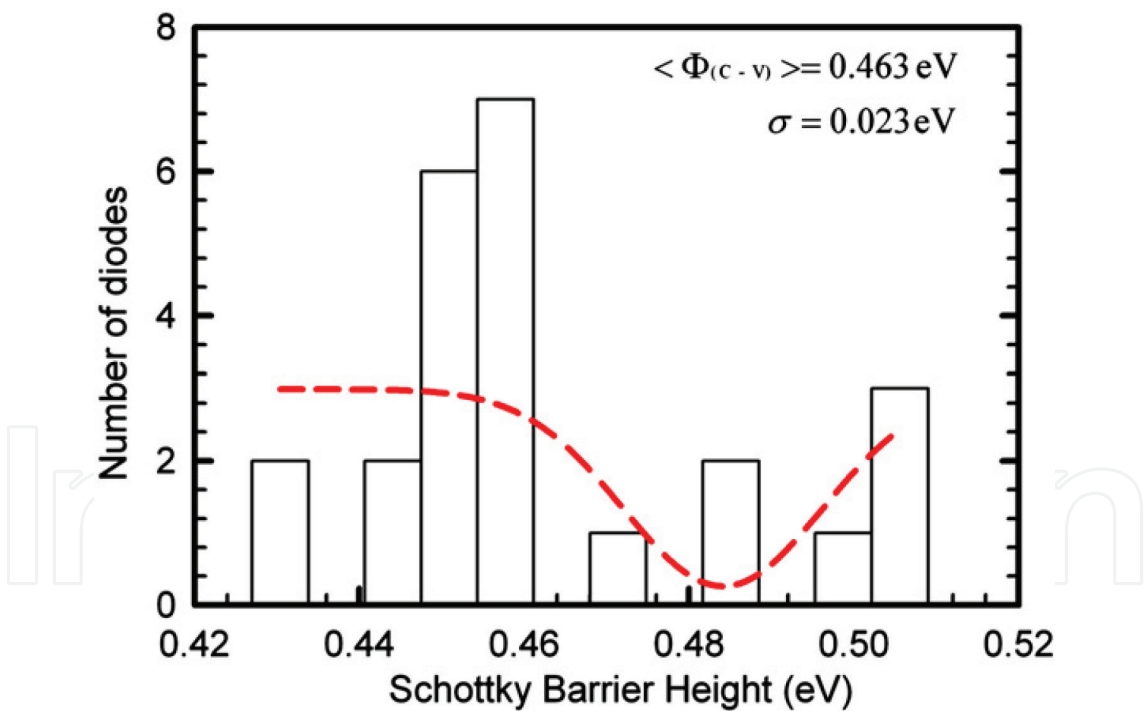
Figure 21. Schottky potential barrier height distribution derived from reverse bias C⁻²-V characteristics [13].

is 0.066 eV. Potential barrier heights obtained from the I-V and C⁻²-V characteristics are not always the same [14] because of the different nature of the two measurement techniques.

2.3.1. Interface dopant implantation

Descoins et al. [15] used Ge (001) substrates to form two types of Pd/Ge contacts. In the first type of samples the surface of the substrates were implanted with Se atoms at an energy of 130 keV

as explained in section 2.2 of the previous chapter. The samples were then vacuum annealed at a pressure of 4×10^{-5} Torr using a rapid thermal annealing (RTA) setup at 700°C for 30 min. This annealing was done to activate some diffusion of the Se dopant atoms further into the semiconductor surface, before metallization with Pd. A Pd film with a thickness of 20 nm was then deposited at room temperature onto the surface of the sample using magnetron sputtering at a base pressure of 10^{-8} Torr. The second type of samples was prepared in exactly the same way as the first type but with no Se implantation and activation. All the samples were then vacuum annealed at a pressure of 10^{-6} Torr to induce solid state reactions, resulting in the formation of the PdGe phase. X-ray diffraction (XRD) measurements were made in-situ. The heating ramp rate was 5°C per min steps and these steps were separated by 5 min-long XRD measurements at a constant temperature.

For the samples which were implanted with Se, the distribution of Se atoms in the surface region was determined at three stages of the sample preparation using secondary ion mass spectrometry (SIMS). The distribution was first obtained immediately after the Se implantation (as implanted). It was also obtained after the rapid thermal annealing at 700°C for 30 min, which was done to activate some diffusion of the Se dopant atoms. The third SIMS determination of the Se distribution was carried out after the annealing ramp which resulted in the formation and growth of the PdGe phase. All secondary ion mass spectrometry results are presented in **Figure 22**. The Se SIMS profile measured immediately after the Se implantation is represented by open triangles. The profile after the activation annealing was performed at 700°C for 30 min and is represented by the open squares.

The Se SIMS profile measured after the annealing ramp to form PdGe is represented by open circles in **Figure 22**. If we compare this profile to the one obtained after the activation annealing was performed at 700°C for 30 min (open squares), we see that Se atoms did not diffuse any further into the depth of the substrate during the annealing ramp. The Se profile immediately after the implantation corresponds to a Gaussian distribution with a maximum concentration
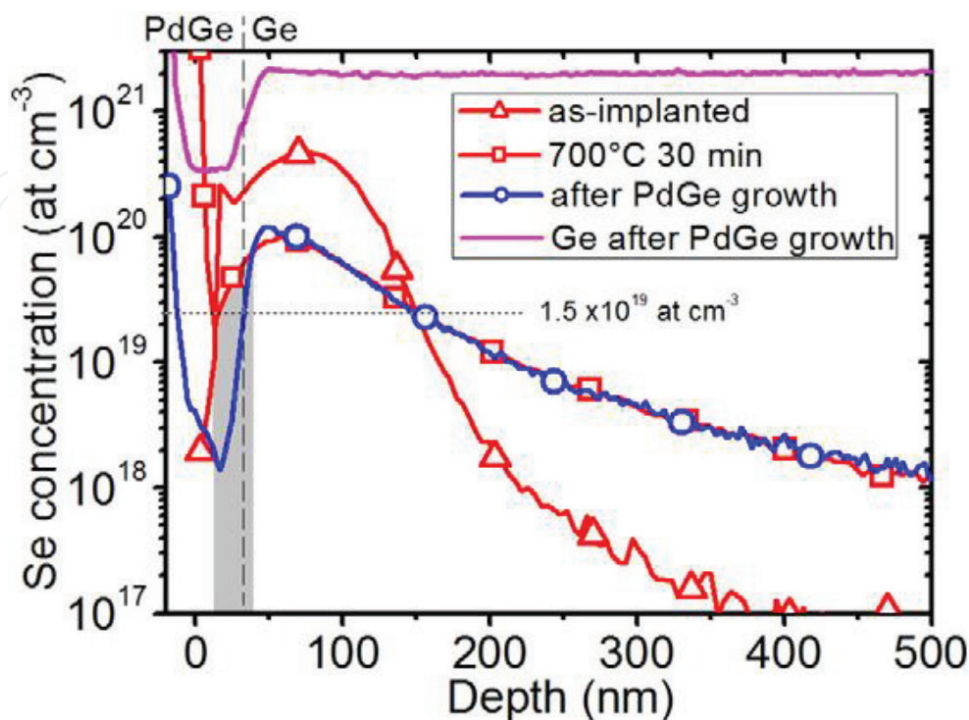

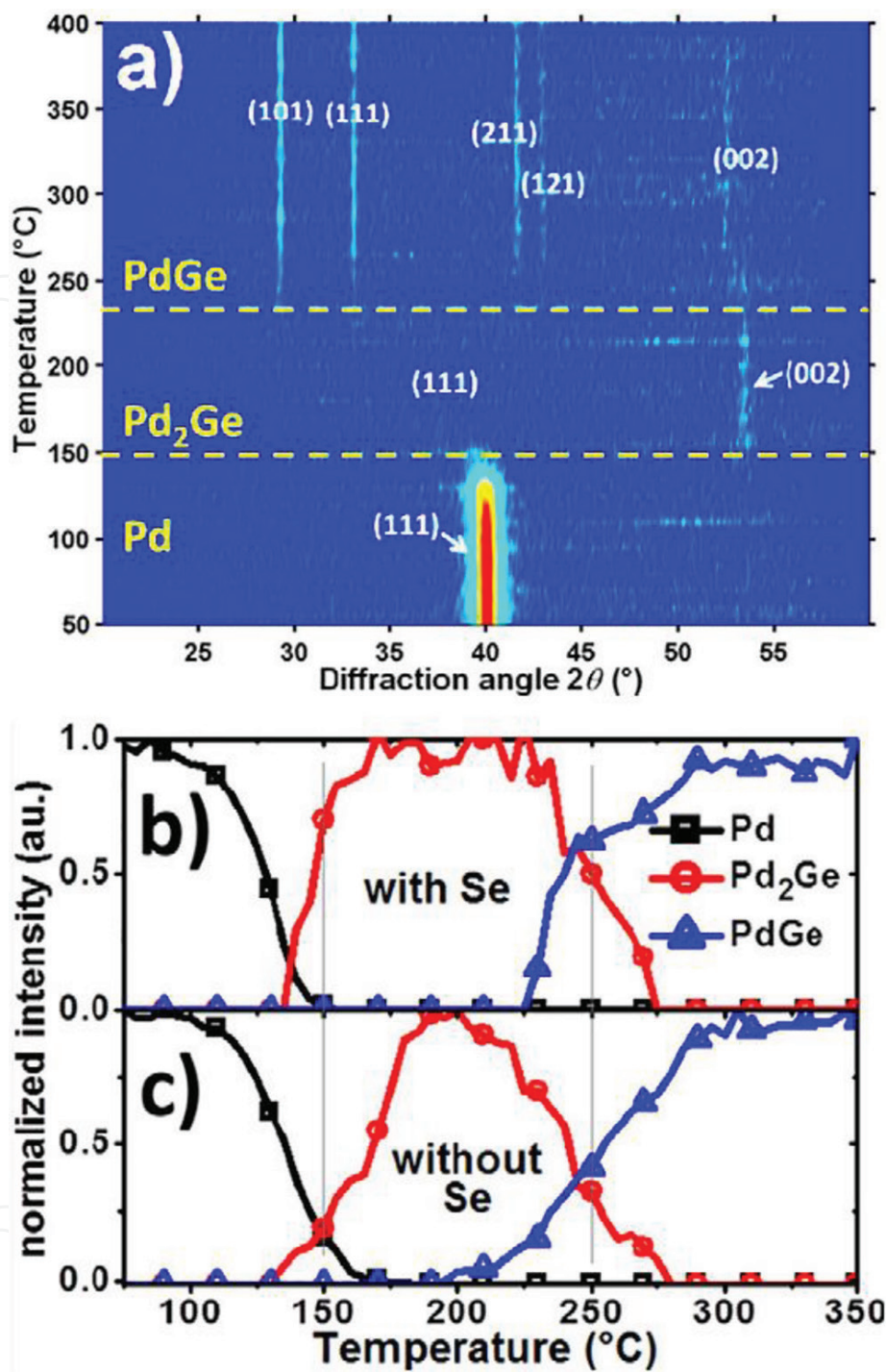**Figure 22.** Secondary ion mass spectrometry results [15].

Figure 23. (a) In-situ X-ray diffractogram obtained from an Se-doped sample. (b) Pd(111), Pd$_2$Ge(002) and PdGe(101) integrated and normalized XRD peak data extracted in-situ during the annealing of a sample with Se doping. (c) Integrated and normalized XRD peak data for a sample without Se doping [15].

of about 5×10^{20} atoms cm^{-3}, which is located at around 60 nm below the surface of the sample. As a result of the activation annealing, the Se atoms diffused further into the substrate decreasing the maximum Se concentration at a depth of 60 nm from 5×10^{20} to about 1×10^{20} at cm^{-3}.

Figure 23(a) shows the in-situ X-ray diffractogram obtained from an Se-doped sample. This diffractogram evolved during the in-situ XRD annealing process. Initially only a single Pd(111) diffraction peak is detected at a diffraction angle of $2\theta \approx 40°$. Upon annealing, the Pd_2Ge(111) and Pd_2Ge(002) peaks appeared at $2\theta \approx 37.5$ and $53.7°$, respectively. The intensity of the Pd(111) peak decreased during further annealing and that of the Pd_2Ge(111) and Pd_2Ge (002) peaks increased until the Pd(111) peak disappeared after which five new peaks corresponding to the PdGe(101), (111), (211), (121), and (002) planes appeared. The Pd_2Ge then starts to get consumed, giving way to PdGe growth. This evolution is displayed in **Figure 23(b)** for the sample with Se doping and in **Figure 23(c)** for the sample without Se doping. To get the results in **Figure 23(b)** and **(c)**, the XRD peak intensities corresponding to various phases were integrated and normalized. The normalized integrated intensities were then plotted against the temperatures of the ramp annealing. We see from **Figure 23(b)** and **(c)** that at the end of the experiment we have a layer of PdGe in contact with an Se-doped Ge substrate and another in contact with an Se-free Ge substrate. Sheet resistivity measurements were carried out on both, the samples with Se interface doping and those without Se doping. The resistivity of the PdGe film grown on the Se-free Ge substrate was found to be, $\rho_{sh} = 13 \pm 1 \ \mu\Omega$ cm and that on the Ge substrate with interface Se doping was, $\rho_{sh} = 6 \pm 0.8 \ \mu\Omega$ cm. This means that interface Se doping reduces the sheet resistivity by half which should result in a nearly ohmic contact because the sheet resistivity is closely related to the contact resistivity.

3. Summary and conclusion

Some of the novel interface control processes developed for the fabrication of NiGe and PdGe Schottky and ohmic contacts on *n*-type germanium have been reviewed.

NiGe grown using the cyclic stacking of Ni/Ge films on an *n*-Ge substrate showed a stable sheet resistivity in the annealing temperature range from 275 to around 500°C. This temperature range was much wider than the corresponding stable-sheet-resistance annealing temperature range obtained from NiGe grown under similar conditions but without the cyclic stacking. The Schottky potential barrier heights for the contacts with cyclically stacked NiGe exhibited stable values which were less than 0.54 eV, even after annealing at temperatures of up to 600°C. The ideality factors of these contacts were less than 1.2, even after annealing at temperatures of up to 500°C. NiGe contacts with the interface incorporation of phosphorus atoms and the insertion of a silicon film at the interface were explained. Ohmic characteristics have been observed for contacts with substantial P interface incorporation and those with minimal P interface incorporation coupled with the insertion of a 0.1 nm-thick Si film, which is essentially a monoatomic Si layer.

A linear relationship was observed between the potential barrier heights and corresponding ideality factors for Schottky contacts of Pd grown on Sb-doped Ge(111) with a doping density of about 2.5×10^{15} cm^{-3}. Current-voltage and capacitance-voltage characteristics were obtained at room temperature. The effective potential barrier heights obtained from these I-V characteristics varied from 0.492 to 0.550 eV, while the ideality factor varied from 1.140 to 1.950. The

barrier heights obtained from the reverse bias capacitance-voltage (C^{-2}-V) varied from 0.427 to 0.509 eV. A Gaussian distribution function was fitted over the experimental potential barrier height distributions, resulting in average values of 0.529 and 0.463 eV from I-V and C^{-2}-V characteristics, respectively.

The sheet resistivity of PdGe grown by Pd reactive diffusion on Ge substrates which had their surfaces implanted with Se atoms was two times lower than that for samples grown under the same conditions but without Se implantation. This result suggests that Se atoms at the Pd/*n*-Ge interface may be used to produce efficient PdGe contacts. The presence of the Se atoms does not modify either the phase-formation sequence or the phase growth kinetics during the Pd reactive diffusion with the Ge substrate, as seen in **Figure 23**.

The three interface control processes analyzed, namely the interface incorporation of P atoms, the thin film insertion of Si at the interface, and the implantation of Se atoms into the surface of the semiconductor substrate, have been demonstrated to be effective, and are therefore recommended for the improvement of Ni and Pd contacts in the next generation of *n*-type germanium-based nanoelectronic devices.

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