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Work Function Setting in High-k Metal Gate Devices

Elke Erben, Klaus Hempel and Dina Triyoso

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Abstract

As transistor size continues to shrink, SiO_2/polysilicon gate stack has been replaced by high-k/metal gate to enable further scaling. Two different integration approaches have been implemented in high-volume production: gate first and gate last; the latter is also known as replacement gate approach. In both integration schemes, getting the right work functions and threshold voltages for N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) devices is critical. A number of recent studies have shown that the threshold voltage of devices is highly dependent on not just the deposited material properties but also on subsequent device processing steps. This chapter contains a description on the different mechanisms of work function setting in gate last and gate first technologies, the sensitivities to different process conditions and special measurement techniques for gate stack analysis is shown.

Keywords: complementary metal-oxide-semiconductor, NMOS transistor, PMOS transistor, high-k metal gate, work function, gate first, gate last, replacement metal gate, low energy ion scattering, electron energy loss spectroscopy

1. Introduction

The basic principle of metal-oxide-semiconductor field-effect transistor (MOSFET) function has not been changed since the introduction of this transistor type ~40 years ago. The control of charges close to the silicon surface by an applied voltage to the gate electrode turns the transistor channel on and off. The required gate voltage to turn the transistor on (to form the inversion channel)—the threshold voltage Vt—is defined by the work functions of the transistor channel semiconductor and the gate electrode and by additional charges at the transistor channel-dielectric interface and distributed charges through the dielectric. The work function difference between channel material and gate electrode should be small to ensure a low threshold voltage (**Figure 1**). The Si/SiO$_2$-dielectric/polysilicon-electrode gate stack is optimized to
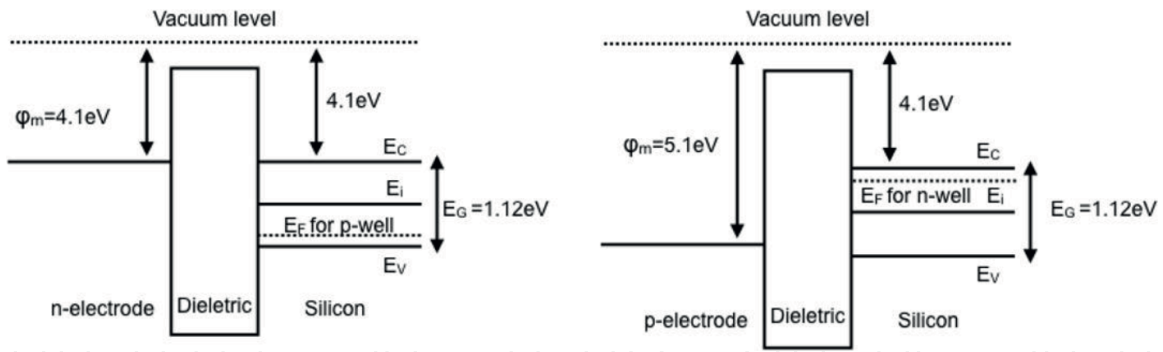
Figure 1. Energy diagrams for NMOS (left) and PMOS (right). φ_m is the work function of the gate electrode, E_C the conduction band, E_V the valence band, and E_F the Fermi level energy.

fulfill these requirements. Doping of the polysilicon can tune the work function for N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) transistors accordingly. In the early years of MOSFET technology, typical gate length was around several micrometers and the thickness of the dielectric between the silicon and the gate electrode was above 10 nm. Today's leading edge technologies have a gate length of below 20 nm, a shrink by a factor of 100 and almost in the range of gate oxide thickness from the early technologies. This scaling of the gate length also requires a significantly thinner gate dielectric for gate control and to mitigate short channel effects. The desired electrical thickness of the gate dielectric became less than 2 nm. The well-established SiO_2 dielectric became too leaky for this thickness range, since tunnel leakage became the dominating leakage path. Therefore, the SiO_2 with dielectric constant k = 3.9 had to be replaced by a dielectric material with higher dielectric constant, a so-called high-k material such as HfO_2 (k = 20). The introduction of this new material requires also a change in the material for the gate electrode. Direct contact of HfO_2 with polysilicon leads to oxygen and electron transfer through this interface. As a result, the Fermi level of p^+ polysilicon increases significantly and the Fermi level of n^+ polysilicon decreases, causing high threshold voltages. This effect is known as Fermi pinning [1]. The work function difference between n and p-gate electrodes becomes very small. To avoid this effect, the gate electrode on top of the high-k dielectric must be a metal electrode. Two different integration approaches for high-k metal gate have been developed and implemented in high-volume production: gate first and gate last; the latter is also known as replacement gate approach. In both integration schemes, getting the right threshold voltage for NMOS and PMOS devices is a challenge. In gate first technology, the complete gate stack is formed before gate patterning and has therefore to withstand the high thermal budget of all subsequent processes which are required for transistor formation, including dopant activation. This exposure to high temperature limits the material choice for the gate stack [2]. The work function of metals used in the gate stack is shifted toward mid-gap for temperatures above ~500°C. The required work functions for NMOS and PMOS have to be set by careful optimization of thermal treatments or anneals. The details of this approach are given in Section 2.1. For gate last approach, a polysilicon dummy gate is formed as in the classical SiO_2/polysilicon technology, and all process steps with high thermal budget will be performed with this dummy gate in place. The dummy gate will be removed after completion of all implant and high thermal budget processes and replaced by a metal gate electrode. The work function of this

gate stack will be defined by the used metals, their thickness values and deposition conditions. Details will be described in Section 2.2.

2. Metal gate technologies

2.1. Gate first technology

The metal gate for NMOS transistors requires a work function close to the conduction band of Si (~4.1 eV) and the PMOS transistor needs a metal gate with a work function close to Si valence band (~5 eV). There are known metals with the right work functions, TiN for PMOS and Al for NMOS [2]. But the high temperature processes required for several steps post gate patterning will shift the work functions of these metals toward mid-gap, causing unacceptably high threshold voltages. The reason for this work function shift is the diffusion of oxygen from the metal layer to the interface of the high-k dielectric and the metal electrode [3]. Therefore, another way has to be found to set the work function of a Si-high-k dielectric/metal gate stack. The interface between the transistor channel and the high-k dielectric plays a critical role for this purpose. The direct contact of Si to the high-k material decreases carrier mobility and creates defects impacting the electrical characteristics of the transistors, including reliability. A roughly 1 nm thick interfacial SiO_2 layer, grown by wet chemical oxidation, prevents these effects. The properties of this interfacial layer are not stable against several subsequent processes. A stabilization of the oxide interfacial layer by nitridation is required, leading finally to a SiON interfacial layer.

The effective work function of such a gate stack is defined by a dipole layer consisting of metal and oxygen atoms at the interface between the SiON interfacial layer and high-k dielectric [4]. To form this dipole layer, a thin capping metal layer has to be deposited on top of the high-k dielectric; TiN is used for this purpose. The atoms for NMOS- and PMOS-specific dipole formation are deposited by plasma enhanced vapor deposition (PVD) as very thin layers on top of this capping TiN and have to be driven into the high-k dielectric by high temperature anneal. Lanthanum (La) and Aluminum (Al) have been found to be suitable materials for dipole formation in NMOS and PMOS transistors, respectively [4]. The achievable threshold voltage depends on the number of metal atoms available for dipole formation at the interface between the SiON interfacial layer and high-k dielectric. La and Al have different saturation behavior of surface coverage through deposition. Therefore, La allows a wide range of Vt tuning. Al content, in contradiction, saturates quickly and therefore PMOS has a significantly smaller range of Vt tuning by the Al-based dipole formation. **Figure 2** shows the gate stack for NMOS and PMOS devices before the drive-in anneal. The dipole formation alone is not sufficient to achieve the PMOS band edge.

Replacing the Si in the transistor channel by SiGe lowers the achievable Vt significantly, due to the different energy band structure of SiGe versus Si, see **Figure 3**.

The valence band energy of SiGe is significantly higher compared to Si, the band gap is slightly smaller. The p-type field effect transistor (PFET) work function can then be tuned in addition
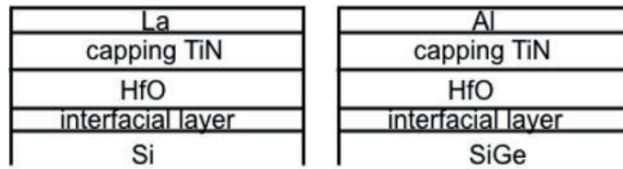
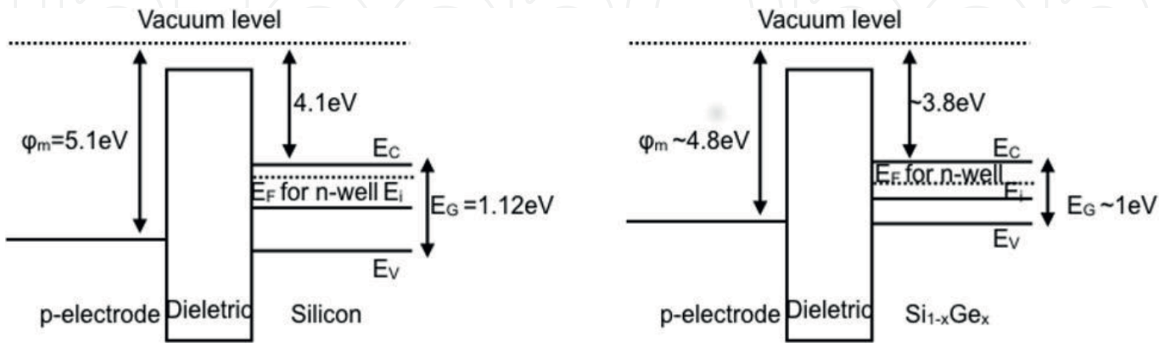**Figure 2.** Gate stack for NMOS (left) and PMOS (right) devices before the drive-in anneal.

Figure 3. Energy diagrams for PMOS on Si (left) and PMOS on SiGe with 25% Ge content (right). φ_m is the work function of the gate electrode, E_C the conduction band, E_V the valence band, and E_F the Fermi level energy.

by the Ge content of the SiGe channel [5]. Then, higher the Ge concentration, lower the Vt (~10 mV Vt shift by 1% change of Ge concentration).

The temperature range for the drive-in anneal must be chosen carefully, since interfacial regrowth may occur causing an increase of electrical interface thickness (CET). At the same time, oxygen scavenging will be observed, since the high temperature drive-in anneal is performed with a TiN layer on top of the stack [6]. Indirect scavenging will cause a thinning of SiON interface by N—O exchange in the interfacial layer and partially oxidation of TiN. This effect has a minor impact on CET reduction in comparison with other effects within complementary metal-oxide-semiconductor (CMOS) process but is also detrimental in terms of defect formation (oxygen vacancies) at the interface to the channel, leading to threshold variation and in worst case to reliability problems. Interfacial layer scavenging is observed for a couple of materials in gate first approach and happens either in a direct way by diffusing scavenging elements toward the HfO_2/SiON interface (like La and Al) or remote by isolating the scavenging elements from the interface (like TiN) [6]. Besides the temperature range and the scavenging element, the composition and deposition method of the interfacial layer contributes to the overall scavenging amount that could be achieved. The scavenging effect is basically a reduction of interface thickness by oxidation of metal dopants at the interface between high-k and interfacial layer and/or oxidation effects at the interface between HfO_2 and TiN top layer, see **Figure 4**.

After the drive-in anneal, the NMOS- and PMOS-specific capping layers have to be removed from the high-k dielectric and replaced by a common final metal electrode for both transistor flavors to avoid the Fermi pinning. A polysilicon layer is deposited on top of the metal gate electrode for a proper contact formation by silicidation. **Figure 5** shows the final gate stack after drive-in anneal and capping layer and polysilicon deposition.
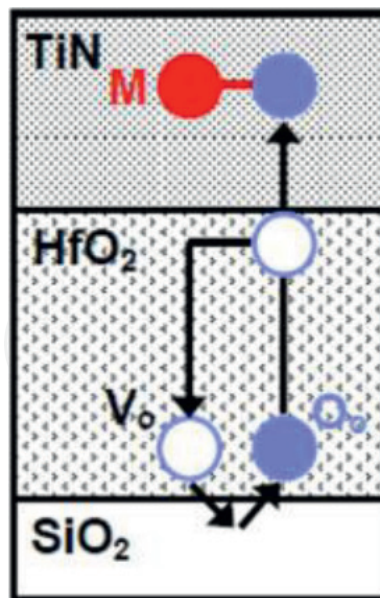
Figure 4. Mechanism of remote interfacial layer scavenging by high temperature anneal (T ≥ 850°C) with TiN on top of high-k/SiO stack. M, V0, and O0 represent the scavenging element, the oxygen vacancy in HfO_2, and the oxygen atom in the lattice position of HfO_2, respectively [6].
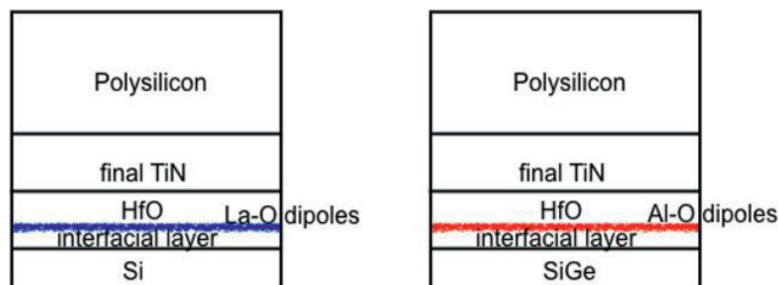

Figure 5. Final gate stack of NMOS transistor (left) and a PMOS transistor (right) with the corresponding dipole layers in place.

After formation of the gate stack, all following process steps are comparable to those in conventional SiO_2-polysilicon technology. Special care hast to be taken to avoid any oxygen ingress into the gate stack, since this will cause uncontrolled Vt shifts of the devices.

2.2. Gate last technology

In planar gate last technology, the high k metal gate stack is built after completion of all processes up to silicidation in the front end of line (FEOL) of the whole CMOS flow, including high-temperature processes. There have been two options developed, either the high-k gate stack is deposited prior to gate patterning and the metal gate stack is deposited after removal of the polysilicon gate or the complete high-k metal gate stack is deposited after removal of the polysilicon gate [7]. The mechanism of work function setting does not differ between these two options.

In addition to delivering the required work functions, the gate materials have to be compatible to the CMOS process flow, must not cause danger of uncontrolled metal contamination of wafers and tools or cause reliability problems. Aluminum with a work function of 4.1 eV is a suitable material for NMOS transistors. One possible material for PMOS transistors is TiN. The work function of TiN can be tuned close to 5 eV depending on the detailed composition of TiN, like the Ti to N ratio, the TiN thickness, and the deposition techniques.

The direct contact of the gate metals to the high-k dielectric or to a too thin capping layer on top of the dielectric may damage the dielectric and create leakage paths. One example of Al spiking through an insufficient protected gate dielectric is shown in **Figure 6**.

To avoid this, the high-k dielectric has to be protected against the gate metal, especially the Al for the NMOS, by a protection layer of certain thickness. A roughly 2 nm thick TiN layer on top of the high-k dielectric protects the high-k dielectric against damage due to metal gate deposition. CMOS technology sets an additional boundary condition to the processes of metal gate formation. Since there must be different gate materials for NMOS and PMOS transistors close to each other, a process sequence had to be developed allowing the deposition of the different gate metals without disturbing the gate stack of the complementary transistor. This could be realized by first depositing the metal gate for PMOS transistors on all devices, including NMOS, and then removing the PMOS metal gate (TiN) from the NMOS. To achieve this, the removal of the TiN has to be well controlled and selective to the TiN protection layer on top of the high-k dielectric. This can be realized by introducing a thin stopping layer on top of the protection TiN layer. TaN was found as a suitable material for this purpose. The removal of the TiN metal gate on the NMOS transistors stops on the TaN layer, and then the metal gate for the NMOS transistors is deposited. Once this has been completed, the gate electrodes of both NMOS and PMOS devices will be finalized with deposition of aluminum. As a result, the complete gate stack becomes quite complex, and it becomes difficult to ensure reproducible and reliable work functions. **Figure 7** shows the resulting gate stack for NMOS and PMOS transistors, respectively. The effective work function of both device flavors is defined rather by a multilayer gate stack then by a single metal with a clearly defined work function.

The thickness of the single metal layers is only a few nanometer each, so the gate stack is more a sequence of several interfaces than a stack of different bulk metal layers. A metal to metal interdiffusion of atoms from the single layers into neighboring layers takes place, resulting in an effective work function for the whole stack [8].
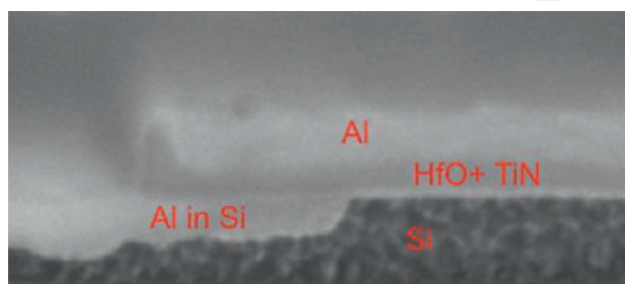

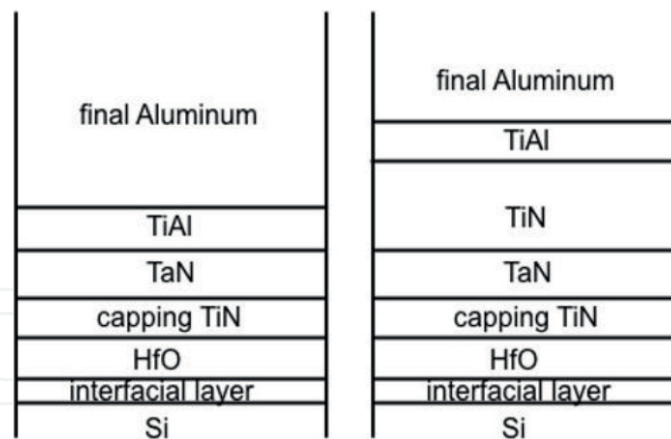**Figure 6.** SEM image of a transistor heavily affected by Al spiking.

Figure 7. Gate stack of NMOS transistor (left) and a PMOS transistor (right).

3. Analytical characterization of the gate stack

The effective work function of high-k metal gate transistors is defined by complex gate stacks in both gate first and gate last technologies. The analytical characterization of these gate stacks is challenging, but required for process development and optimization. Gate first technology requires a detailed quantitative mapping of the dipole forming metals close to the interfacial SiON-layer—high k dielectric interface. Since the deposition of these metals is realized on top of the TiN capping layer, a surface sensitive analytical technique must be applied for this task. The required spatial resolution is not high, since the deposition of the work function metals is done before gate patterning.

The characterization of the gate stack in gate last technology has to fulfill different requirements. Since the gate stack formation is done after gate patterning, it has to be applicable to real device structures, meaning it requires a very high spatial resolution combined with depth profiling for different elements through several metal layers down to the high-k dielectric.

3.1. LEIS for gate first technology

Low energy ion scattering (LEIS) is a unique tool in surface analysis, since it provides the atomic composition of the outer surface as well as a nondestructive ("static") in-depth profile (0–10 nm) for the heavier elements [9]. In LEIS, the surface of a solid is bombarded with noble gas ions such as 4He+ and 20Ne+ with energies between 1 and 10 keV. For a fixed scattering angle, the energy distribution of the backscattered ions is measured. The interaction of the ion with the surface can be considered as an elastic collision with a single surface atom at rest. For a given primary ion and energy, the energy Ef of the backscattered ion is determined by the mass of the (unknown) surface atom and the scattering angle. Conservation of energy and momentum results in a higher Ef for scattering by a heavier target atom. Using noble gas ions makes LEIS extremely surface sensitive because most of the ions that penetrate the outer monolayer are neutralized and therefore do not contribute to the scattered ion spectrum. In general, there are no matrix effects in LEIS; the ion yield for scattering by one atomic species

does not depend on the other atomic species in the surface. A LEIS analysis thus gives the atomic composition of the outer atomic layer of a surface. For atomic layer deposition (ALD) growth, the extreme surface sensitivity of LEIS allows to characterize the progress in the closure of the layer for every deposition cycle, precisely during the transient regime that is responsible for the thickness inhomogeneity of the final layer. **Figure 8** shows the different surface saturation behavior for sputtered La versus Al. The different substrates had been chosen since La signal was better detectable on Hf covered surface than on Si substrate. **Figure 9** illustrates the effect of surface treatment prior to ALD process. Surface coverage saturates already between 10 and 15 cycles in case of pretreated surface in comparison with >20 cycles for surface without pretreatment.
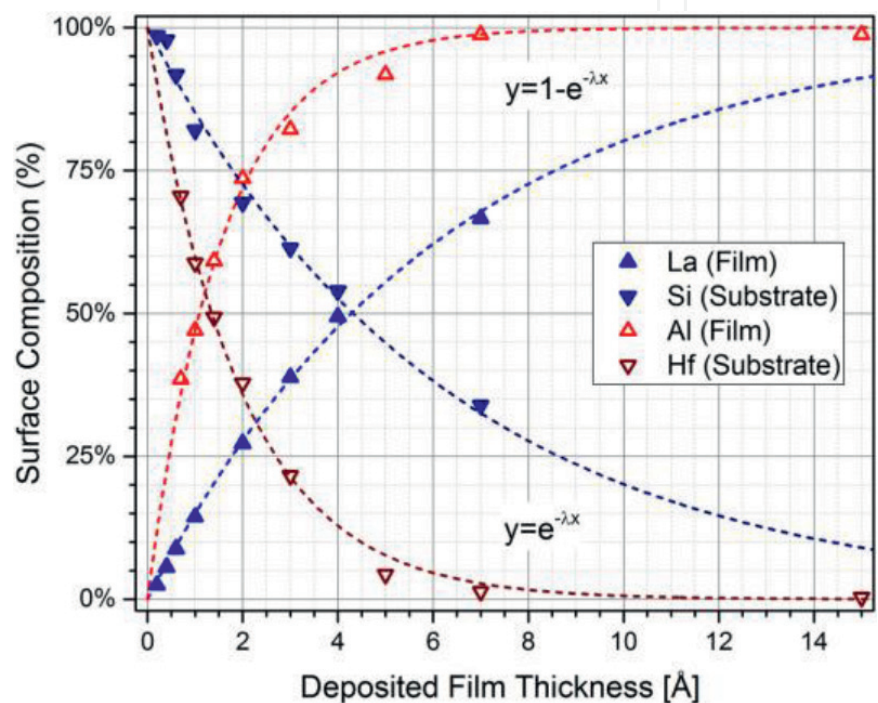

Figure 8. Surface coverage La versus Al deposited by PVD on pure Si substrate and on Si substrate covered by thin Hf layer for better solution of La signal [10].

3.2. EDX and EELS for gate last technology

The resulting work function and therefore threshold voltage are very sensitive to the details of the gate stack composition and deposition conditions. An analytical technique is required to investigate the impact of process details on the resulting threshold voltages. In order to accurately account for all of these impacts, there is a need to apply analytical methods which accurately measure material composition on real device structures, rather than on unpatterned wafers.

Energy-dispersive X-ray spectroscopy (EDX) is a well-established analytical method in conjunction with transmission electron microscopy (TEM) for the detection of metals used in the gate stack. TEM has the required spatial resolution to investigate the gate stack on real transistors. Electron energy loss spectroscopy (EELS) is a technique preferably used for the
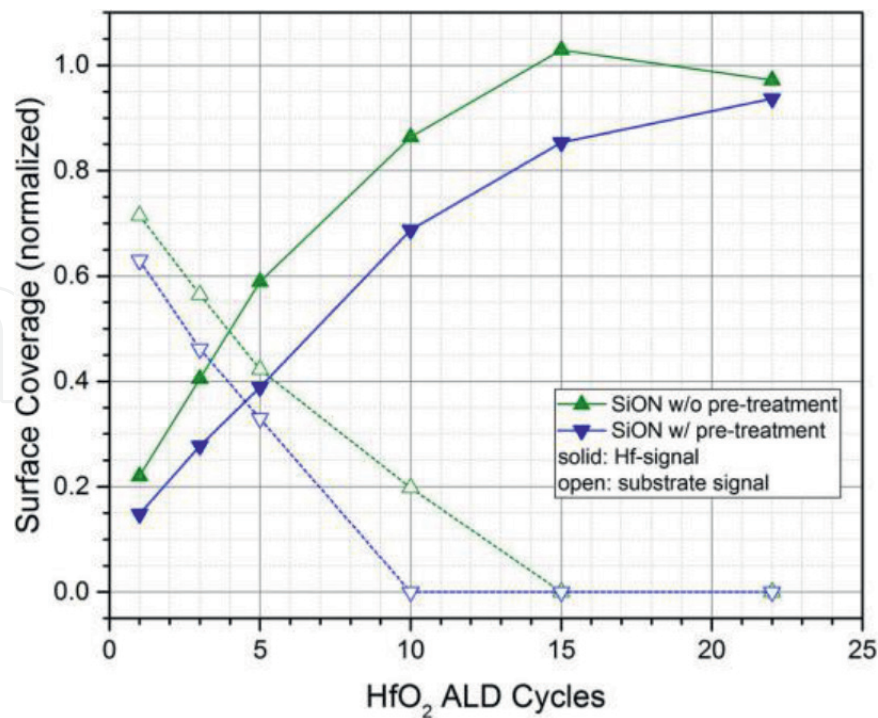
Figure 9. Surface coverage by HfO$_2$-ALD process in dependence on ALD cycle number and surface pretreatment [9].
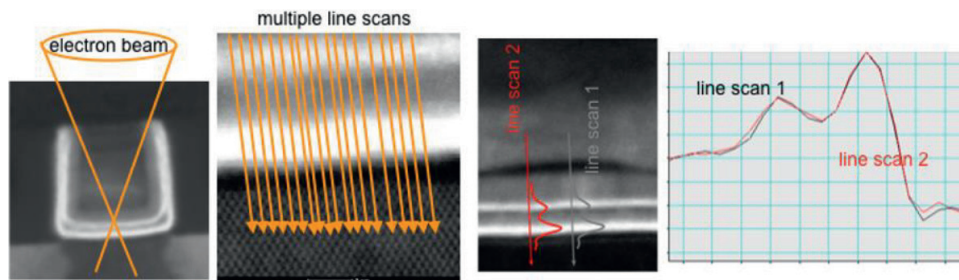

Figure 10. High-resolution EELS method with multiple line scans to improve SNR.

detection of lighter elements in the gate stack, like oxygen and nitrogen, which play also an important role in work function setting. An advanced high-resolution EELS method capable of accurate measurement of material composition on device structures can be applied for this task [11]. The standard EELS measurement has too low probe intensity for high enough signal-to-noise ratio (SNR). In order to improve the SNR, multiple line scans have to be done across the layers of the gate stack and then aligned to each other and integrated, see **Figure 10**.

The standard and high-resolution EELS profiles of a sample are shown in **Figure 11**. The gate stack is shown from right to left, bulk silicon, interfacial SiON, high-k dielectric, capping TiN layer, TaN stopping layer, TiN layer for PMOS. No details of the oxygen and nitrogen profiles in the lower part of the gate stack can be resolved. The high-resolution EELS spectrum of the same sample shows the profiles of both oxygen and nitrogen through the gate stack. A dip in the oxygen profile at the high-k dielectric-capping layer interface can now be resolved.
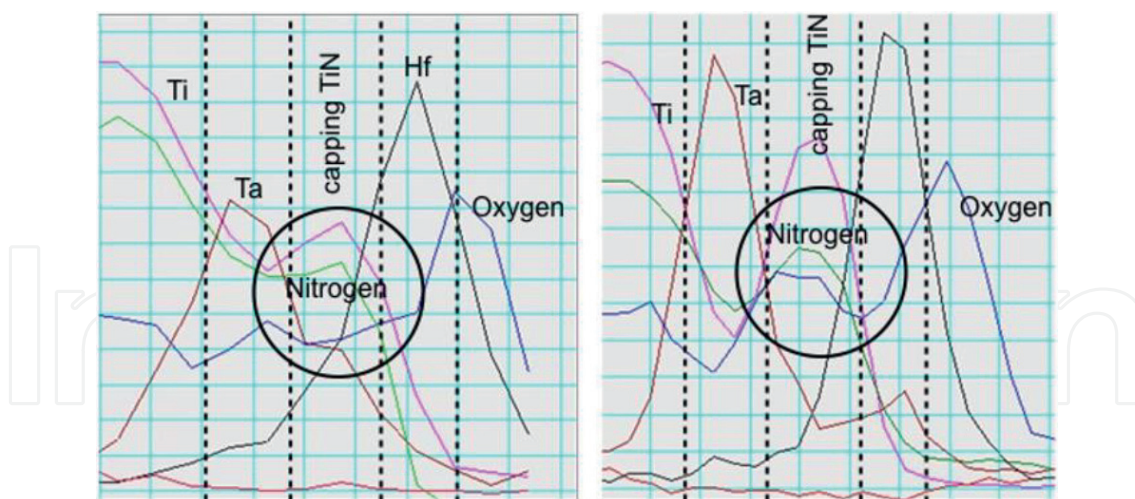
Figure 11. Standard resolution EELS spectrum (left), no details of the oxygen and nitrogen profiles in the lower part of the gate stack can be resolved. A dip in the oxygen profile at the interface capping TiN-HfO$_2$ can be resolved for a high-resolution EELS profile (right).

This technique can be used to understand the observed differences in threshold voltage between devices processed with slightly different formation of the gate stack.

3.2.1. N-type metal-oxide-semiconductor

The gate stack of NMOS transistors consists of interfacial oxide—high-k dielectric (HfO$_2$)—TiN—TaN—TiAl—final Al. The desired 4.1 eV work function from the Al has to be achieved for the whole stack of the gate electrode, even if the Al is not in direct contact with the HfO$_2$. Therefore, the TiN protection layer and the TaN stopping layer have to be thin enough not to screen the work function of the Al from the HfO$_2$. An interdiffusion of atoms occurs between the different metal layers resulting in the formation of the effective work function. This interdiffusion can be enhanced by thermal processes, like the reflow of the final aluminum with 400–480°C. If this interdiffusion is too strong or the TiN protection layer is not stable enough, aluminum atoms may penetrate the HfO$_2$ and cause leakage paths in the device, as shown in **Figure 6**. **Figure 12** shows the EDX and EELS profiles of two samples with different reflow temperatures for the final aluminum. A 50°C higher reflow temperature causes several orders of magnitude higher leakage current. One way to avoid this detrimental Al penetration is a thicker TaN layer on top of the capping TiN. However, if the thickness of the protection and stopping layers is too large, the effective work function of the gate electrode becomes too high, resulting in higher threshold voltage. This is also reflected in the combined EDX-EELS spectra shown in **Figure 13**. The optimum conditions require a tight balance between the thicknesses of the different metal layers, the deposition details and reflow temperatures.

3.2.2. P-type metal-oxide-semiconductor

The desired work function for PFETs is in the range of 5 eV. This requires a different gate stack composition as for the NFET, especially the impact of the final Al to the effective work function
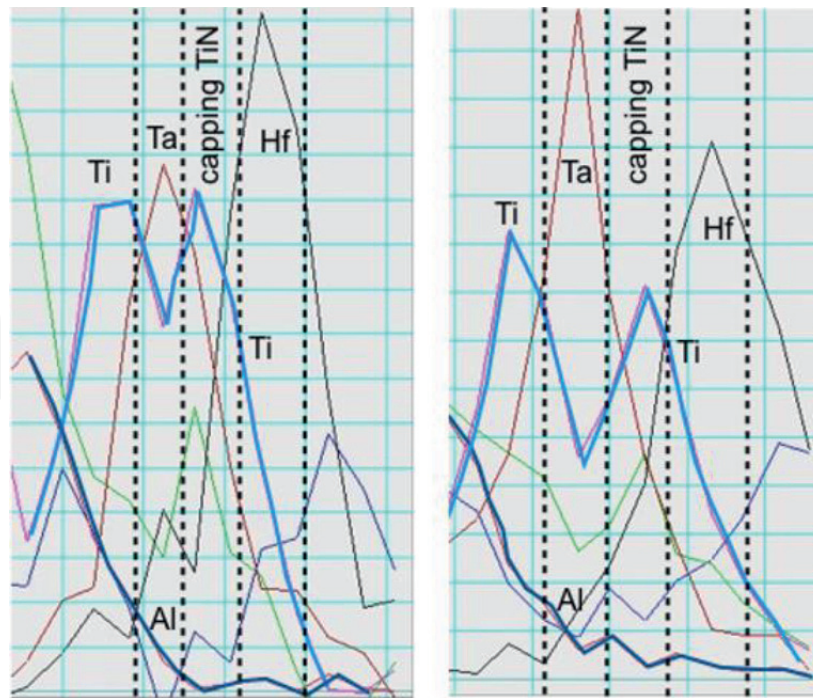
Figure 12. Combined EDX and EELS profiles of the different materials of the NMOS gate stack for a sample with lower reflow temperature (left) and higher reflow temperature (right). The Al tail in the region of capping TiN and HfO$_2$ layers is more pronounced for the sample with higher reflow temperature for the final Al.
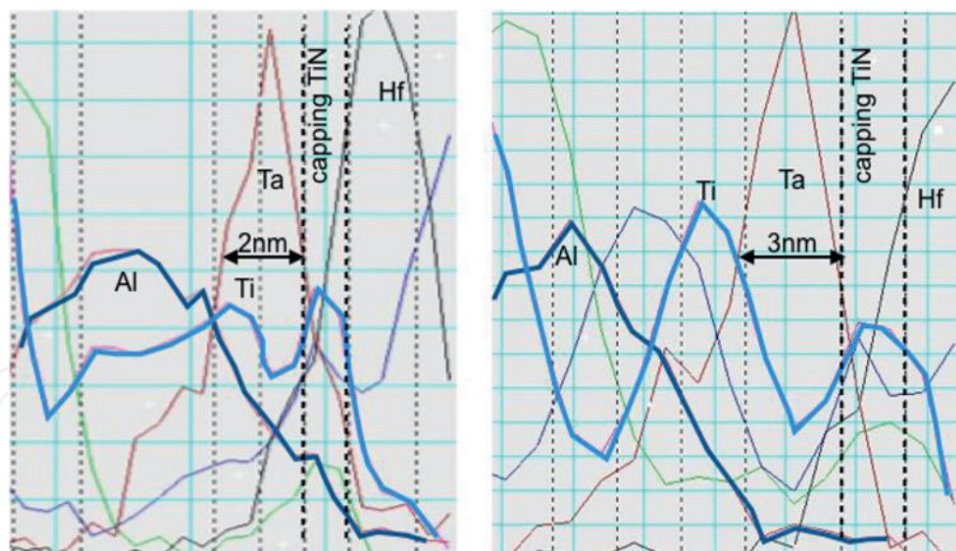

Figure 13. Combined EDX and EELS profiles of the different materials of the NMOS gate stack for a sample with low Vt (left) and 50 mV higher Vt (right). The thicker TaN layer and the lower Al content close to the HfO$_2$ can be seen.

must be screened from the lower part of the gate stack. TiN has been found as a suitable material for this purpose. The thickness of this second TiN in the gate stack must be larger than that of the capping TiN in order to keep the Al away from the high k dielectric. In addition to the composition of the metal electrode the resulting Vt for PMOS also depends
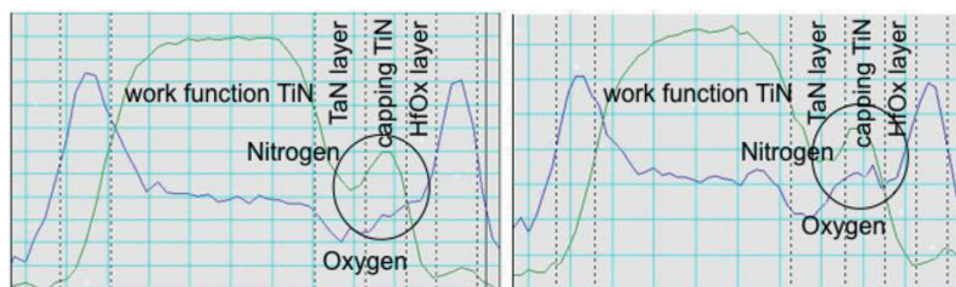
Figure 14. High-resolution EELS spectrum of a sample with high Vt (left), a low oxygen concentration in the capping layer with a strong gradient toward the high-k dielectric is detected. High-resolution EELS spectrum of a sample with low Vt (right). The dip of the oxygen concentration at the interface capping layer—high-k dielectric is well resolved.

strongly on the concentration of nitrogen and oxygen at the interface of high k dielectric and metal layer [12].

The responsible mechanism for the work function setting corresponds therefore more to the dipole engineering at the interfacial-high-k dielectric interface. The required PMOS Vt can only be achieved by having the correct concentration of nitrogen and oxygen at the high-k dielectric-capping layer interface. Again, as for the NFET, the dependency of the Vt from the gate stack composition can be checked by combined EDX/EELS spectra of the gate stack. High-resolution EELS spectra from two samples with different Vts are shown in **Figure 14**. There is reasonably a high oxygen level in the capping layer with a dip of the oxygen concentration at the interface cap layer—high-k dielectric for the transistor with reasonable low Vt. The EELS spectrum of a sample with high Vt shows a low oxygen concentration in the capping layer with a strong gradient toward the high-k dielectric.

4. Conclusion

As a consequence of the aggressive scaling of transistor dimensions, the engineers have developed two quite different approaches to address the integration of high-k gate dielectric into the very complex CMOS process flows. Gate first and gate last technologies use different mechanisms to set the work functions required to achieve the desired threshold voltage. Gate first technology is based on dipole formation at the interfacial layer-high-k dielectric interface, whereas gate last technology uses metal-metal interdiffusion within the metal gate electrode to tune the work function. Both technologies are capable to deliver high performance devices in high-volume production. To date, gate first technology is targeted more for low leakage, low-power applications and is applied, for example, in fully depleted SOI technology [13], whereas gate last is used in FINFET technology for high performance products [14]. The final gate stacks are quite complex for both approaches and involve a large number of process steps, which had to be optimized carefully to achieve the desired result. Advanced analytical techniques had to be adapted to meet the specific requirements for process characterization of gate first and gate last technologies.

Acknowledgements

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