Chapter 5

Status of SiC Products and Technology

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Additional information is available at the end of the chapter

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Abstract

The benefits of silicon carbide (SiC) devices for use in power electronics are driven by fundamental material benefits of high breakdown field and thermal conductivity, and over 25 years of sustained development in materials and devices has brought adoption to a tipping point. It takes the confluence of many separate developments to drive large-scale adoption, which we will examine in this chapter.

Keywords: silicon carbide, SiC, SiC substrates, SiC epitaxy, SiC applications, SiC packaging, SiC Schottky diode, SiC cascode, SiC MOSFET, supercascode, SiC reliability, SiC gate oxide

1. Introduction

Silicon carbide (SiC) has about a 10× higher critical field for breakdown and a 3.5× higher thermal conductivity than silicon (Si). The former characteristic allows unipolar devices to be built with 1/100 on-resistance of silicon devices for the same voltage rating, while the latter allows efficient removal of heat generated during power conversion. The system benefits of SiC for power electronic applications have been amply demonstrated, but the growth of SiC adoption especially for transistors to replace Si IGBTs and Si MOSFETs has, until 2017, been relatively slow [1–3]. Projections in the last 5–10 years showing a "hockey-stick" ramp in SiC shipments have not occurred. It has taken time for the material, technology, and products to mature, reliability concerns to be addressed, prices to drop sufficiently, and the driver and applications ecosystem to develop. Finally, with the migration to 6-inch wafers, SiC adoption is poised for rapid acceleration. We examine each of the major contributing factors,

highlighting the enormous progress across all fronts, as well as the work remaining to be done at this exciting time for SiC power electronics.

2. SiC market projections and driving applications

Figure 1 shows the projected SiC growth by the application area. The traditional markets in power supplies for SiC Schottky diodes and (photovoltaic) PV inverters are rapidly being supplemented by growth in (electric vehicle) EV on-board chargers and charging stations, and 2018 is expected to see growth of SiC transistors in power supplies, previously the domain of silicon super-junction (SJ) MOSFETs. Strong growth is also happening in the UPS systems driven by higher efficiency and in high-performance motor-drive segments. Moreover, strong market pull from automotive inverter companies developing SiC solutions, ramping 2020–2024, is expected to rapidly tip SiC device revenues past the $1 b revenue threshold. Given the favorable policies of governments in Asia and Europe toward EVs (**Figure 2**), the demand currently seen for SiC devices for chargers is expected to grow quickly as market penetration increases from the meager 1–2% to 10–15% in the next decade. Traditional applications will then open up to SiC as prices fall, driven by the growing economies of scale and increasing competition in the supply of SiC substrates, epitaxial material, and products. This will be tracked by the introduction of an ecosystem of high-performance passives, drivers, and sensors that simplify the extraction of the system benefits of this wide bandgap technology. It is expected that SiC will reach about 10% of the Si market by 2025. Over a longer time frame, 3300V–10KV class of products will get deployed in applications such as railway traction, MW motor drives for wind, ship, and industrial use, high-voltage DC power conversion, solid-state breakers, etc.

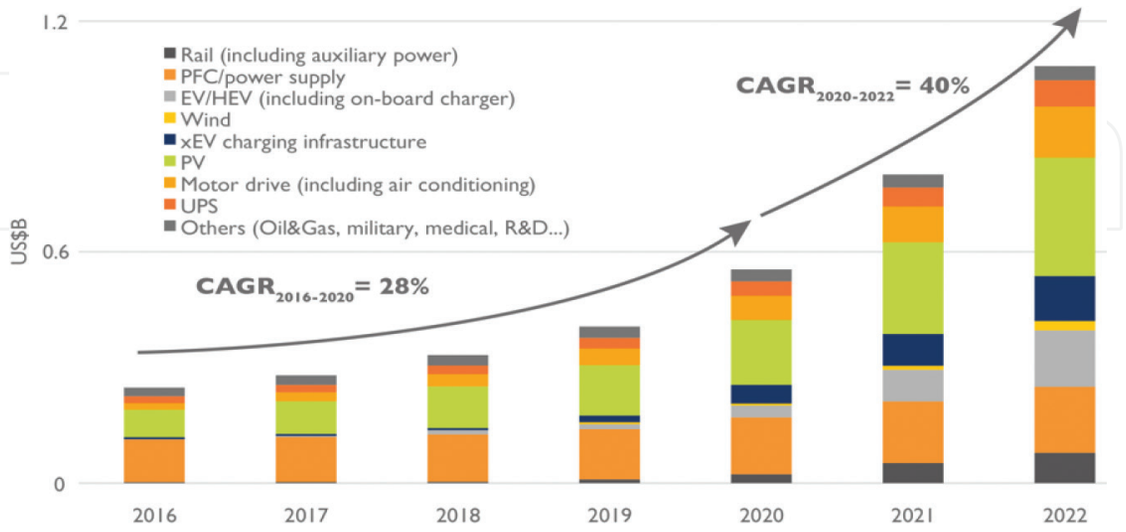

Figure 1. SiC device market projection. Source: Yole developpement 2016.

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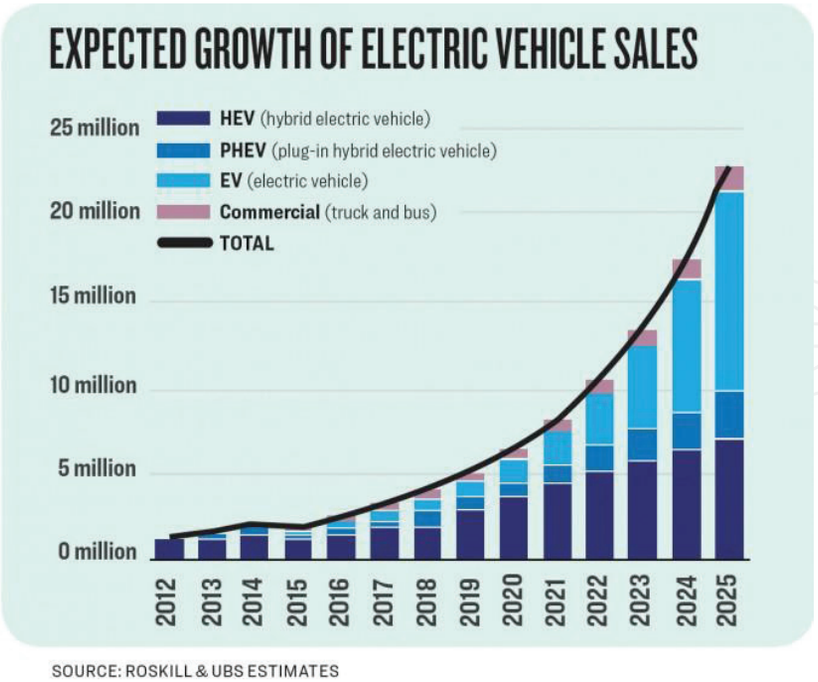

Figure 2. Expected growth of EV Sales.

3. SiC material and epitaxy progress

Figure 3 captures the rapid improvement in the density of micropipe defects in SiC 6-inch substrates. While 6-inch substrates dominate the cost of SiC products presently, the rapid capacity expansion by key suppliers in the USA, coupled with robust volume growth, is expected to bring cost parity with 4-inch mature SiC substrates by mid-2018. Beyond 2018, 6-in. SiC will drive cost reductions across all product types. Improvements in wafer shape, boule yields, and reduced defects are key to eventual device yields and lower costs. As with silicon technology, many quality improvements are possible only when the scale of the business allows large-scale manufacturing that brings clarity to underlying issues and drives equipment improvements and investments as manufacturers compete.

There has also been considerable progress in 6-in. epitaxy [4], along with the introduction of improved single-wafer tools and better metrology for defects. Post-epitaxy thickness uniformity ±8%, doping ±15%, and BPDs <0.1/cm^2 are available up to 1700 V. **Figure 4** shows the state-of-the-art 6-in. product yield on 200A, 650 V JBS diodes, a testament to the starting epi material quality married to Si foundry manufacturing discipline. **Figure 5** shows the rapid advancement in post-epitaxial wafer defect density.

Also significant is the introduction of the foundry model in SiC. Until SiC volumes grow to exceed 10–30 K wafers/month, the economics of a dedicated factory for wafer cost are not favorable, since the entire cost of running the fab must be amortized over a small

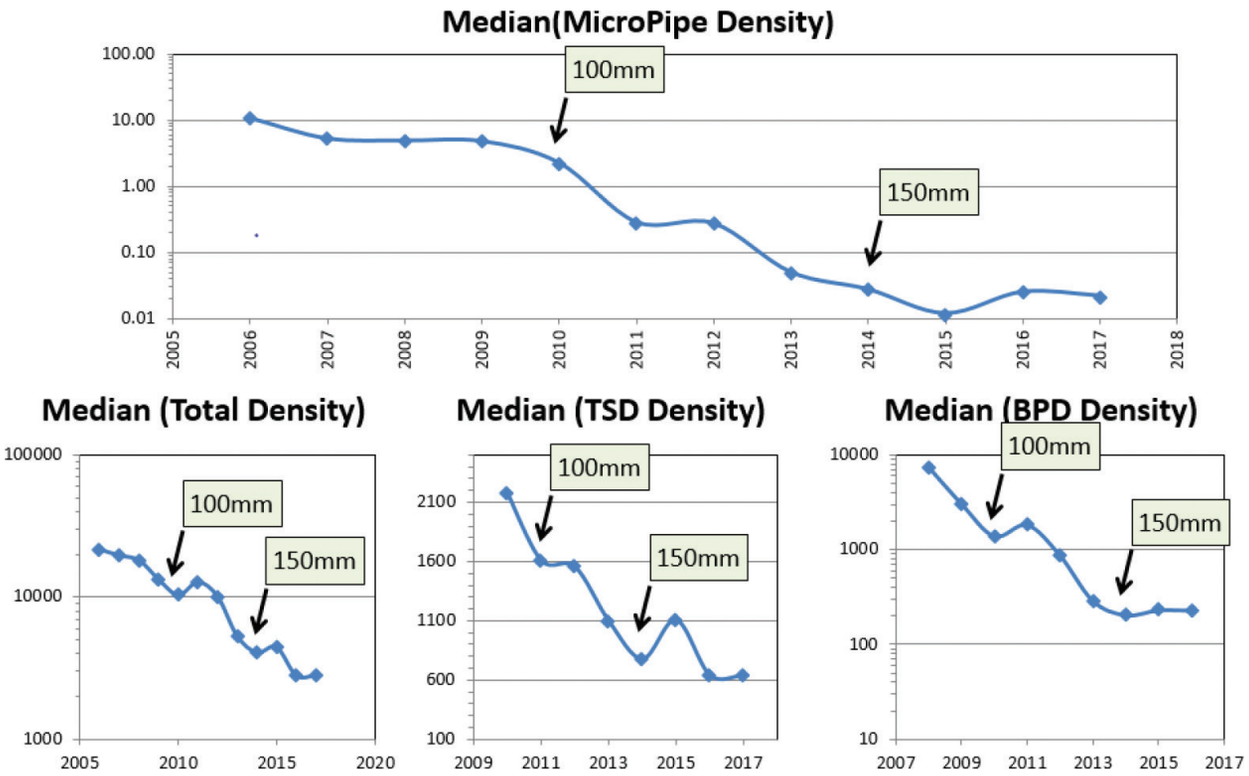

Figure 3. Improvement in SiC substrate quality over time. Courtesy: II-VI corporation.

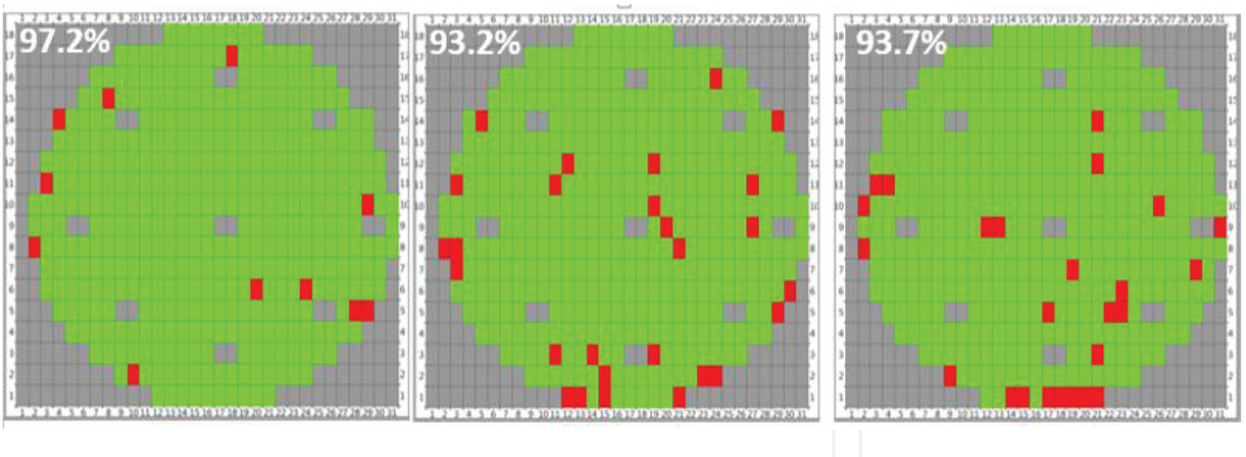

Figure 4. Yield on 6-inch 200A, 650 V JBS diodes. Courtesy: USCi 2017.

volume. Most large silicon manufacturers entering SiC try to leverage their silicon mass production lines. The transition to 6-in. makes this process easier, and an initial investment of $2–30 m is sufficient, since the majority of process steps can share equipment with silicon. The foundry model brings a high level of manufacturing expertise, low process cost from sharing the line with silicon, and the ability to aggregate SiC volume to further drive down prices.

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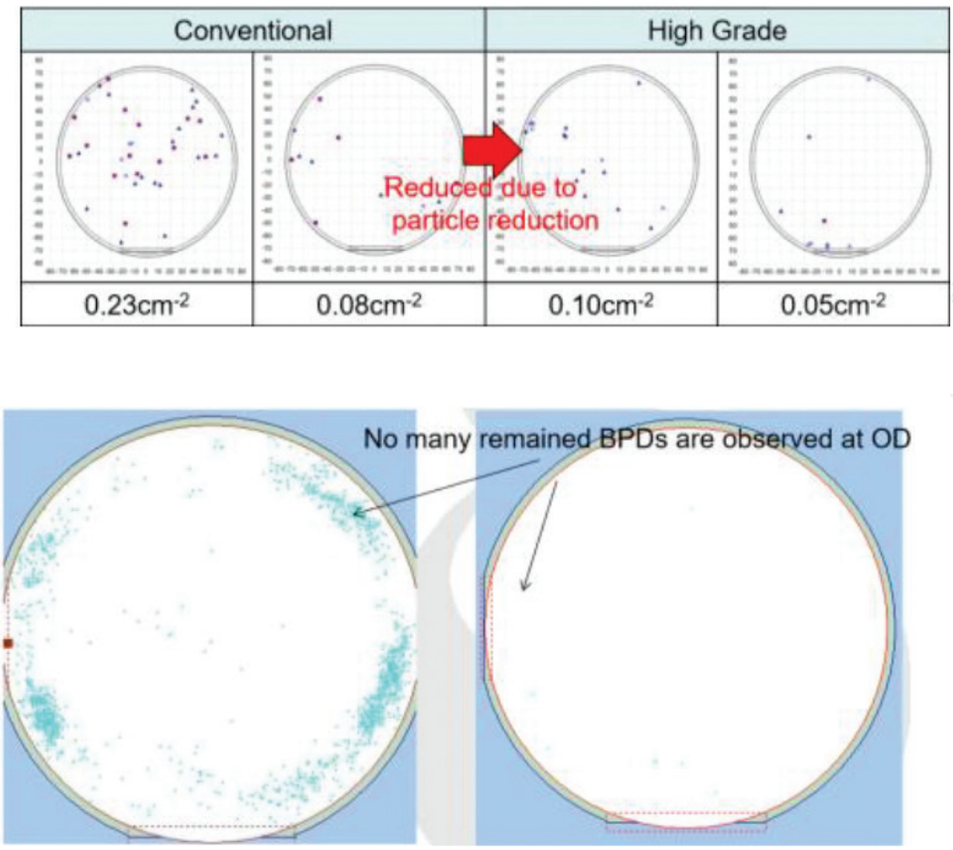

Figure 5. Rapid improvements in epitaxial layer defects. Courtesy: Showa Denko Corporation.

4. Device technology

Progress on device technology and products has been considerable in the last few years. The improvement in RdsA, reliability, chip current ratings, and improved knowledge on how to use the devices in new designs is now bearing fruit. Up to 100A, 1200 V, and 200A, 650 V single chip JBS diodes are now available, bringing SiC diode ratings to silicon soft-recovery diode levels. The improvements in Eon losses by 2× at 150°C through the use of these diodes lead to large loss reduction for hybrid SiC modules even at modest switching frequencies.

In the SiC transistor space, the main device structures in use are shown in **Figure 6**. Trench MOSFET offerings from Rohm and Infineon [5] compete with advanced planar technologies from Wolfspeed, Panasonic [6], Mitsubishi, ST, and GE. Evolution of trench technology is expected to continue the RdsA improvement of SiC MOSFETs, since mobility is improved along the a- and m-faces. Cascode technology from USCi based on trench JFETs provides the lowest RdsA technology SiC switch, configured as a normally-off MOSFET by cascode connection to a custom Si device, designed to present an IGBT/Si MOSFET interface to all users (**Figure 7**).

The use of advanced wafer thinning to reduce substrate resistance together with the dense trench JFET cell technology for SiC [7] has resulted in the introduction of 650 V cascode devices

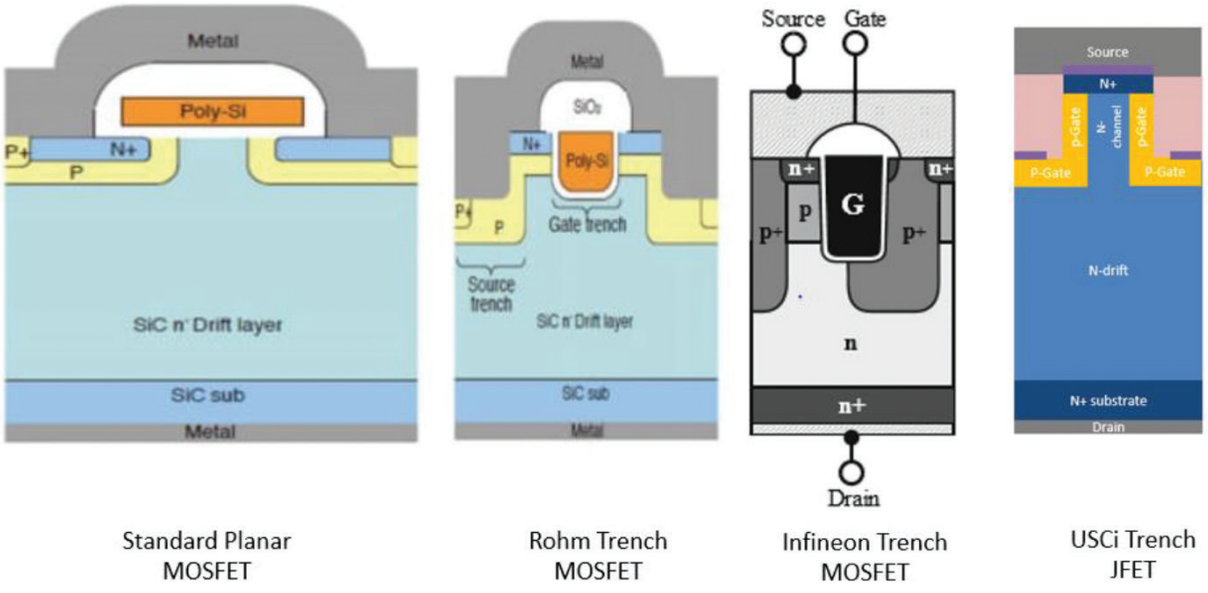

Figure 6. SiC transistor types aavilable in the 650–1200 V class 2016–2017.

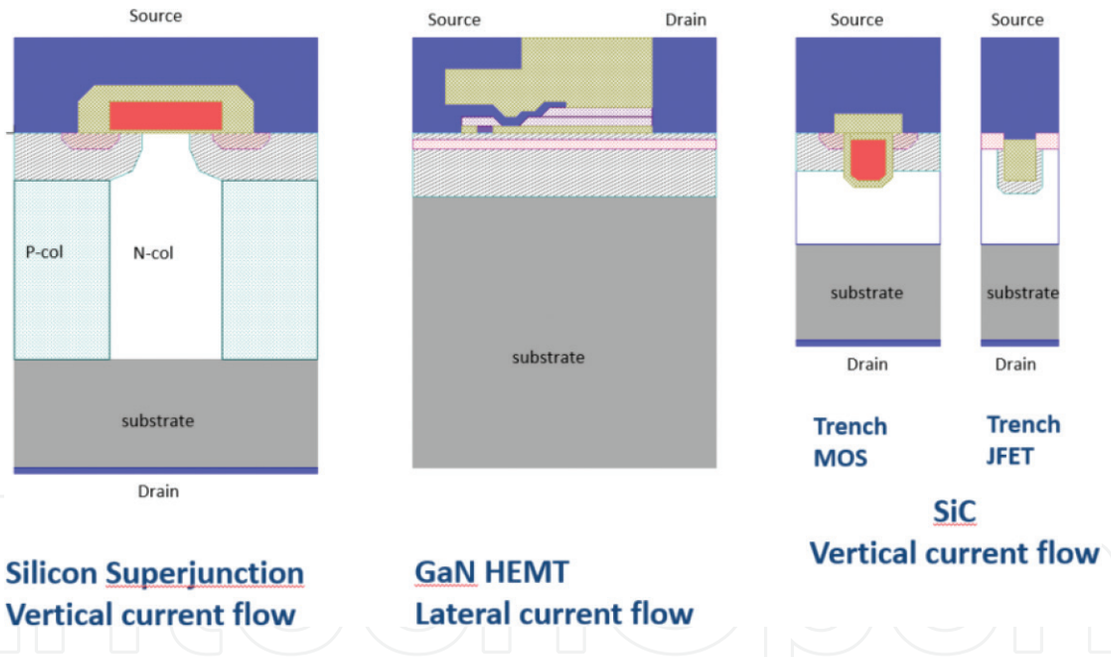

Figure 7. Comparison of transistor technology in the 650 V class 2016–2017.

from USCi that can complete very favorably with incumbent Si superjunction, GaN HEMT, and SiC MOS devices. **Table 1** shows the RdsA of commercially available 650 V devices, with SiC Cascodes providing >10× RdsA improvement over silicon devices, with obvious benefits in cost and lower capacitances. A key improvement with WBG devices is the improved body-diode with very low recovery losses that in turn allows the use of circuits such as totem-pole PFC to push efficiency to new heights. Thermal management for the smaller SiC chips is driving packaging technology enhancements, both in discrete devices and in power modules.

Development of 3300 V MOSFETs at 4 in. and 6 in. [8] indicates that commercial introduction from multiple suppliers may be expected in the next 1–2 years. The horizon for 6.5 kV- and

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Technology	SiC Cascode 650V-45mΩ (UJC6505K)	Commercial SiC MOSFET	Commercial GaN HEMT	Commercial Si Superjunction
R_{DSA}	0.75 mΩ-cm²	2-3 mΩ-cm²	3-7 mΩ-cm²	10 mΩ-cm²
Normalized Die Area	1	2.6X	4X	13X
E_{OSS}	7.5 μJ	32 μJ	12 μJ	14 μJ
Avalanche Capability	YES	YES	NO	YES
Short Circuit	YES	YES	NO	YES

Table 1. Comparative performance of advanced 650 V devices in 2016–2017.

10 kV-rated modules is longer, and the supercascode structure [9] is a very promising alternative, with large benefits in switching speed, diode recovery, and drive simplification as attractive cost points.

5. Reliability

Much has been reported in the last 3–4 years on the rapid improvements in the understanding of the MOS interface in SiC [10]. This has led to much reduced Vth shift in commercial products from leading manufacturers. In addition, the trench MOSFET structure allows the use of thicker gate oxides for better reliability margins, given the better mobility observed on the a- and m-faces of SiC. Progress has been made ensuring the reliability of SiC transistors and diodes to combined moisture and field-dependent degradations by the introduction of devices that can withstand 1000htrs of H3TRB stress at 80% of the rated $V_{DS(MAX)}$. A working group under JEDEC JC-70 is formalizing improved standards for SiC MOSFET testing and qualification, based on the deeper understanding of failure modes and interface physics. In addition, great strides have been made in understanding and mitigating BPD-dependent degradation mechanisms [11]. Most gate oxide issues are not a matter of concern in the cascode structure, since the SiC JFET device has no gate oxide and can therefore operate at higher bulk E-fields without degradation. Furthermore, the Si MOS used in the cascode has a high Vth and a thicker gate oxide, which leads to greater margin between operating and maximum ratings.

SiC MOSFETs and cascodes offer excellent avalanche ratings. SiC devices are also able to withstand repetitive avalanche events, and studies on cascodes have shown that 1E6 cycles at the rated datasheet EAS condition result in no-device degradation, since current flow is in the bulk SiC.

Figure 8 shows a UJC1206K cascode device tested for short-circuit withstand time at starting Tj = 25 and 200°C at Vds = 850 V. The datasheet conditions for SCWT are met for all operating gate voltages and even with Tj = 200°C since the SiC JFET limits the short-circuit current

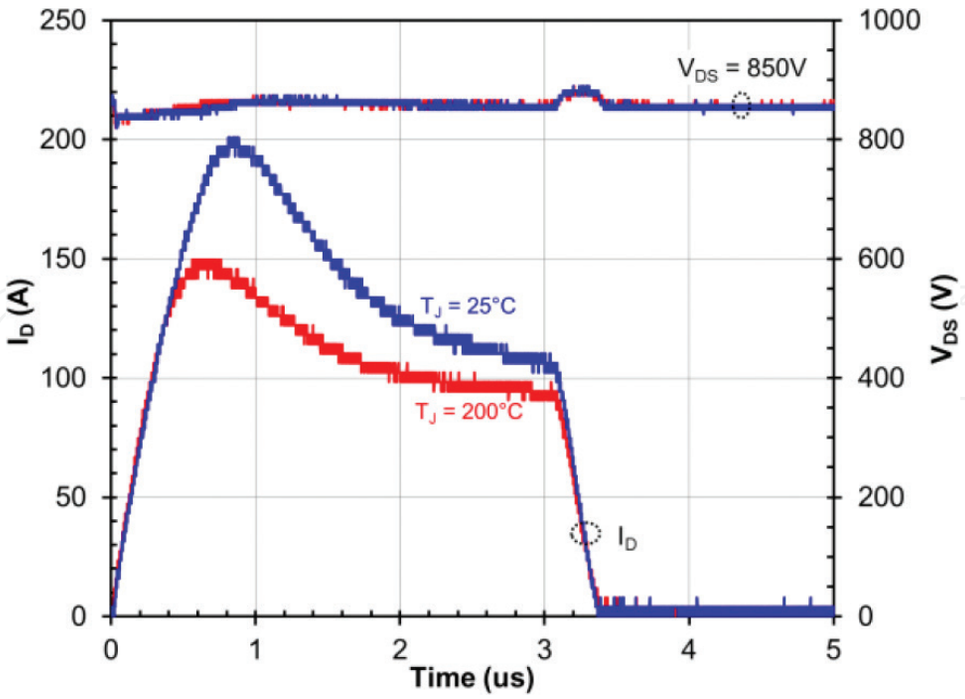

Figure 8. UJC1206K cascode device is capable of handling repetitive short circuits even with starting Tj=200°C. SiC devices will offer robustness exceeding Si IGBTs.

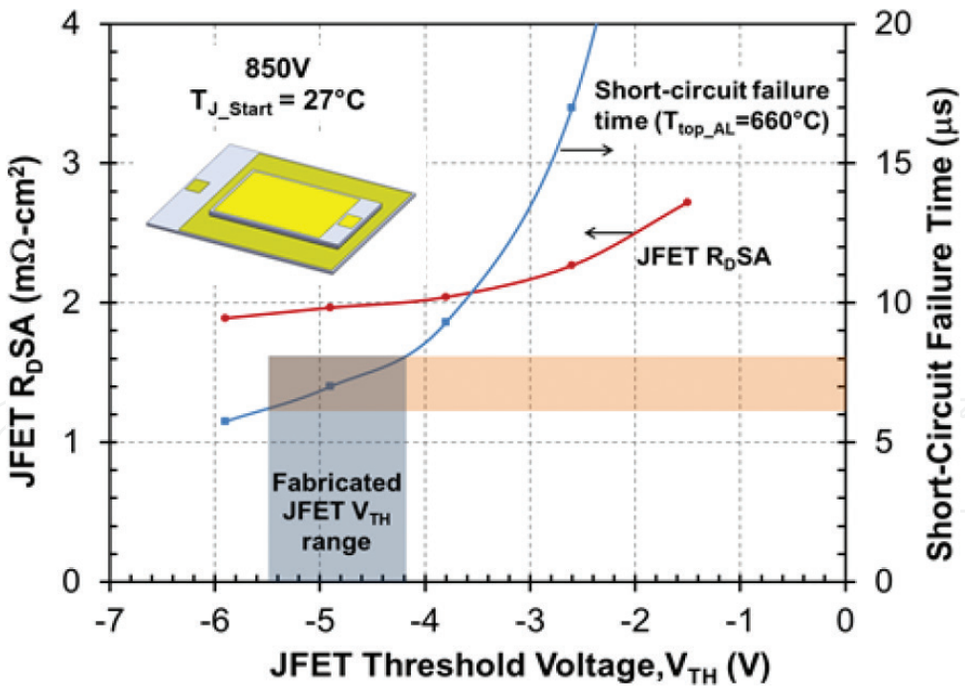

Figure 9. Short circuit time-RdsA trade-off for 1200V Stack cascode with Vbus = 850V. Courtesy USCi 2017.

within the cascode. A study of the 650/1200 V USCi cascodes undergoing 100 repetitions at the rated short-circuit conditions shows no degradation in any device characteristics, whereas SiC MOSFETs typical undergo Vth shifts after such exposure [12]. The trade-off in RdsA to get long

short-circuit withstand times in the cascode is favorable compared to SiC MOSFETs, since the reduction in peak current by tuning JFET Vth does not drastically increase RdsA. **Figure 9** shows that a short-circuit withstand time of 10 μs can be achieved with minimal change in JFET RdsA.

Recent studies of SiC devices have shown better immunity to terrestrial neutron radiation, which is a key problem for high-voltage IGBTs. Much work remains to be done, however, to improve the immunity of heavy ions that affect device operations in space. NASA has led the research into ultra-high temperature operation (500°C-long duration) of SiC JFET devices and ICs, in understanding the degradation mechanisms. At this time, these applications are niche but hold the potential to unlock entirely new businesses for SiC.

6. SiC gate drive

The last few years have also marked the rapid proliferation of gate drive solutions suitable for use for SiC power MOSFETs, with the extended voltage range and strong sink currents. Non-isolated drivers for use with signal isolators, or isolated drivers from multiple vendors, are available, with common mode transient immunity of 100–200 V/ns. However, many more options exist for the better developed ecosystem of Si MOSFET and IGBT drives, which can be used with SiC cascode devices, easing the transition to the use of WBG switches. **Figure 10** shows an important benefit of SiC cascode devices, which cannot only be dropped into Si IGBT/MOSFET circuits but also offer a larger margin between operating and maximum gate voltages, as is prevalent for incumbent silicon devices.

Figure 11 shows a schematic for the gate drive interfaced with a half-bridge connection of two SiC transistors. When the upper device is turned on, the voltage rises across the lower device once its body diode recovers. This fast dV/dt can induce a voltage spike at the gate, due to the Igd displacement current (proportional to C_{gd}.dV/dt), turning-on the lower device, creating a brief shoot-through condition where both transistors are on. This can be avoided by having a low Cgd/Ciss ratio, low internal Rg in the transistor, and a gate driver with a strong current sink or a Miller clamp. Similarly, if the gate driver power supply or the signal barrier allows capacitive coupling between the input and output, injected displacement currents during high dV/dt operations can cause misoperation of the signal processing electronics. Advanced solutions are now available to handle these issues from many analog IC companies (see **Table 2**).

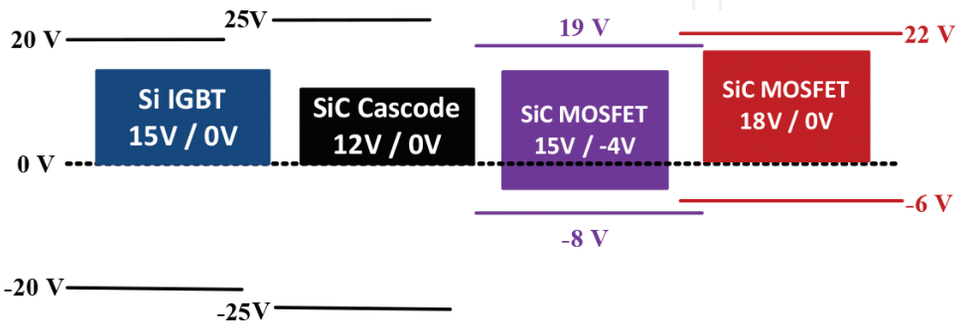

Figure 10. Operating and maximum gate voltages for Si IGBT, SiC cascode, and SiC MOSFET switches.

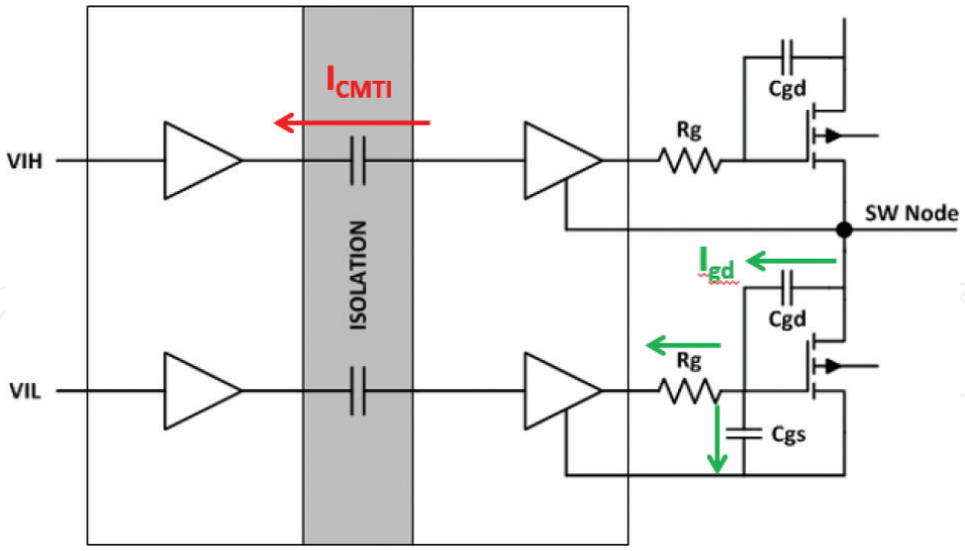

Figure 11. The key challenges of high dV/dt switching is to have gate drivers with strong current sink capability, dV/dt immunity and an isolation barrier with high common mode rejection.

Non isolated single drivers

Manufacturer	Part Num.	Vo range (V)	Source (A)	Sink (A)	Isolation
TI	UCC27531-Q1	10 to 35	2.5	5	No
Microchip	MIC4479YME-TR	4.5 to 32	2.5	2.5	No
IXYS	IXDN609SI	4.5 to 35	9	9	No
Infineon	IR4426SPBF	5 to 20	2.3	3.3	No

Isolated drivers

Manufacturer	Part Num.	Vo range (V)	Source / Sink (A)	Short Circuit Protection	Isolation (Vrms)	CMTI (kV/µs)
Analog Devices	ADuM4120-1	4.5-35	2.3 / 2.3	No	5000	150
Texas Instruments	ISO5852S	15-30	2.5 / 5	Yes	5700	100
Silicon Labs	SI8275	4.2-30	1.8 / 4	No	3000	200
Infineon	1EDI60N12AF	10 to 35	9.4 / 10	No	1200	100

Silicon Labs: SI8275 is a half bridge.

Table 2. A selection of gate drivers for SiC devices and key characteristics.

7. Packaging for SiC

It has been clear since the early days of SiC transistor technology that the high temperature and fast switching capability of SiC switches could not be exploited without the use of low-inductance packaging. However, the initial introduction of discrete devices has used traditional silicon through-hole packages like TO247-3L. Very recently, the range of discrete

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package offerings has been expanded to include the TO247-4L and D2PAK-7L, where the source Kelvin connection allows faster di/dt switching without excessive gate ringing. With the entry of 650 V SiC switches, in the near future, we can expect additional Si packages like the DFN8x8, TOLL, DPAK-3L, and D2PAK-3L to follow. As frequencies rise further, requiring switching at >200 V/ns, use of co-packaged half-bridge elements, as well as co-packaged drivers is planned to replace standard discretes.

Module packaging based on IPM technology is already offered by Mitsubishi, Fuji, and others. Automotive grade IPMs with built-in gate drives minimize losses for higher frequency switching and can serve the 8–25 kW space quite well for power supplies and on-board chargers, albeit at a cost premium.

The potential for hybrid modules has been thoroughly examined, but the expanding offerings of full SiC modules will likely see more growth. While few modules offer Tjmax >175°C today, considerable improvements have been made in inductance, to allow fast switching. **Figure 12**

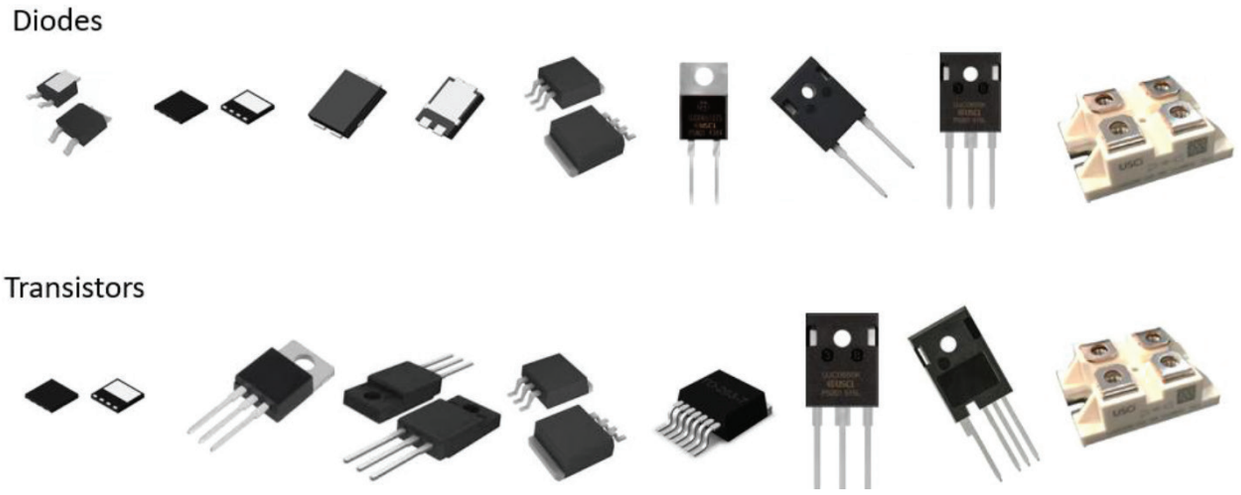

Figure 12. A wide-array of discrete surface mount and thorugh hole packages have become available for discrete SiC devices. For high-speed switching, packages that provide a separate source Kelvin connection are beneficial.

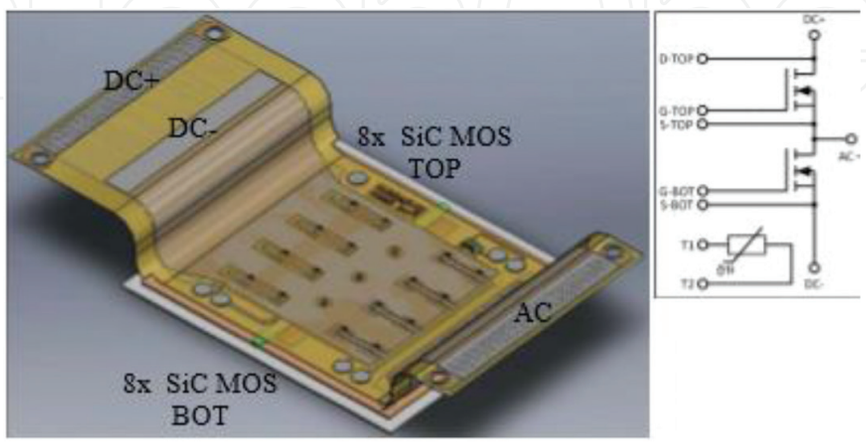

Figure 13. A 400, 1200V half-bridge module with 1.4nH power loop inductance presented by Semikron. Packaging of this type can allow the full use of the high frequency switching benefits of SiC at high power levels.

shows a recent Semikron development that cuts loop inductance to just 1.4 nH in a 400 A, 1200 V half-bridge [13], allowing very fast switching without excessive voltage overshoots and good current sharing. These packaging innovations are key to unlocking the system-level benefits of SiC (**Figures 13** and **14**).

In the automotive space, considerable effort has been expended on double-sided cooling. This technology is already used for Si IGBTs by many car manufacturers and is being actively developed for SiC as well [14]. While the CTE difference between Si and SiC is small, the much higher Young's modulus of SiC leads to higher stresses, requiring careful mechanical package development, especially for double sided cooling extended to 175–200°C temperature ratings.

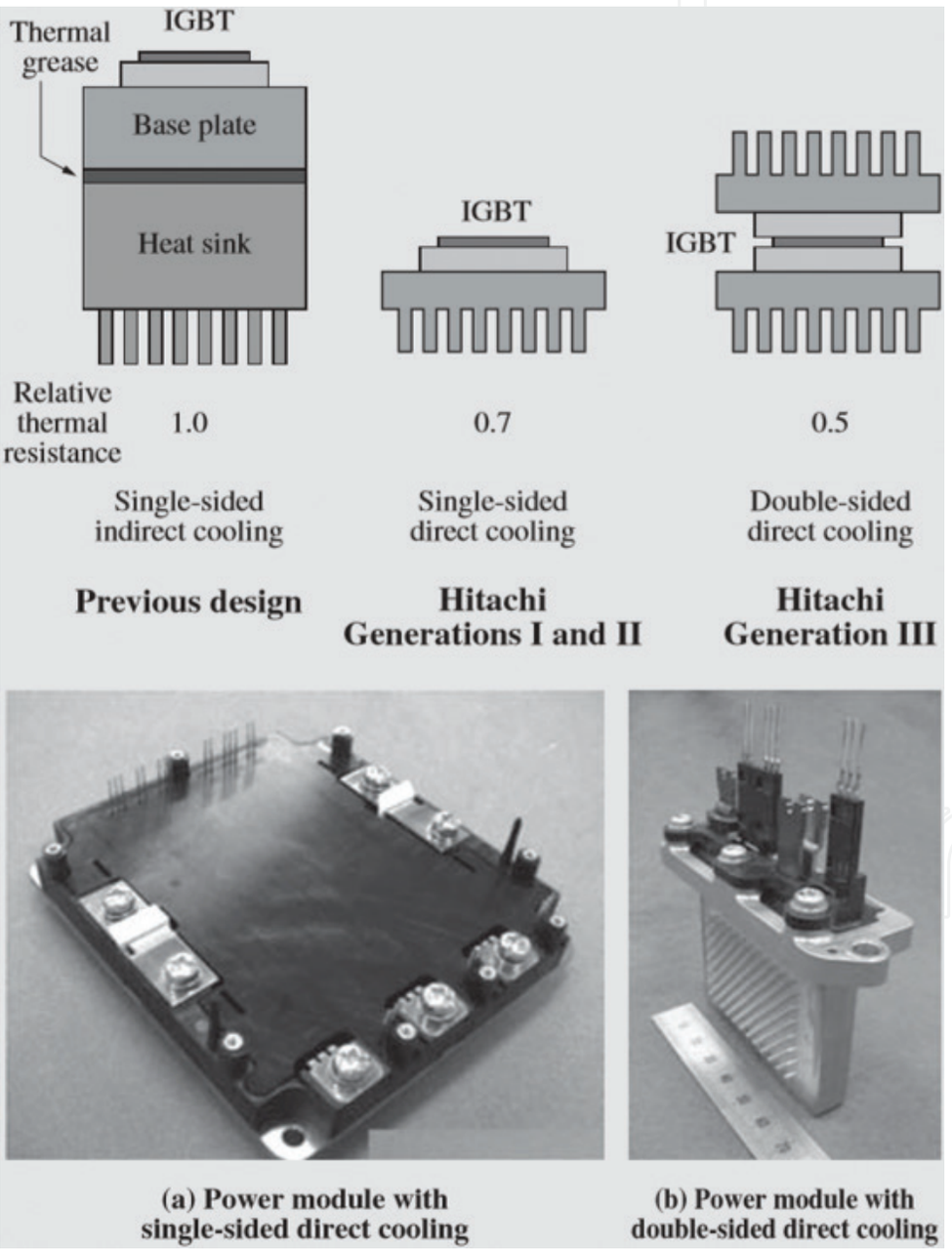

Figure 14. Double-sided cooling technologies developed for silicon IGBTs will be rapidly adapted to SiC MOSFETs.

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8. Application drivers

A roadmap of applications for SiC devices was compiled by the PowerAmerica Institute and described in terms of voltage class and whether they are near, medium, or long term, as shown in **Figure 15**. It can be seen that the near-term applications fall in the 650–1700 V range.

The benefits of SiC Schottky diodes in reducing CCM mode E_{ON} losses in PFC circuits that led to the widespread use of these devices in the last decade continue today. However, the drive to

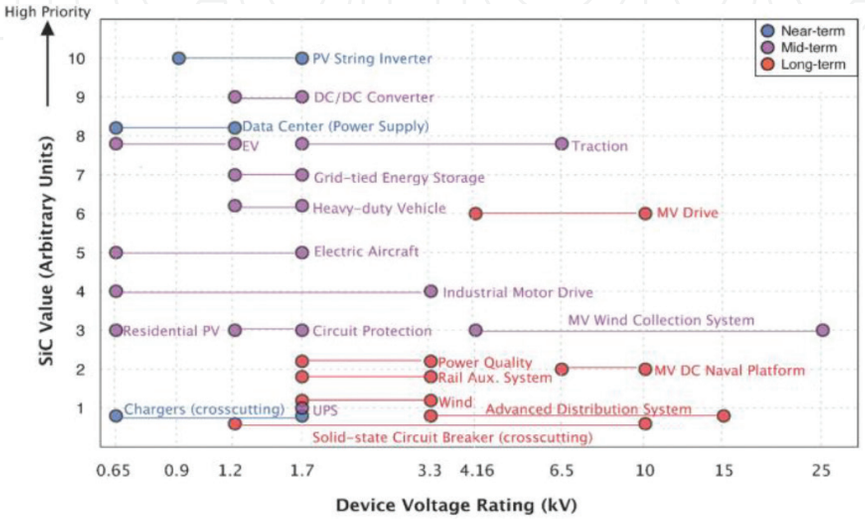

Figure 15. Applications roadmap for SiC devices by voltage rating. Courtesy: PowerAmerica.

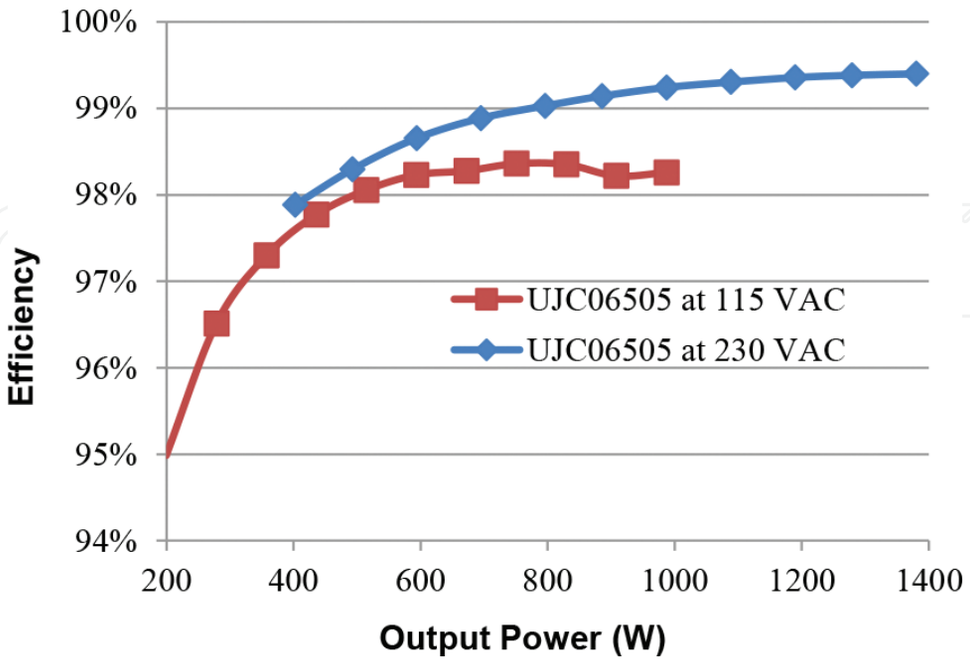

Figure 16. >99% Efficiency on Totem pole Demonstration board with UJC06505K.

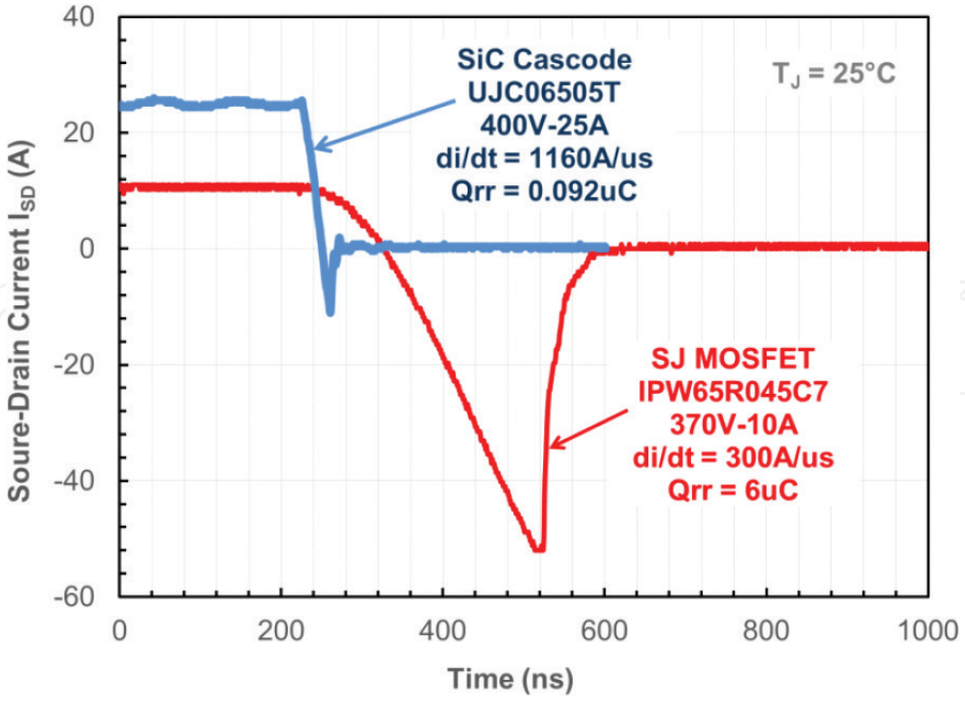

Figure 17. Excellent Qrr for UJC06505K enables hard switching. Low Qrr body diode behavior is a key benefit of SiC MOSFETs and GaN devices over silicon superjunction devices.

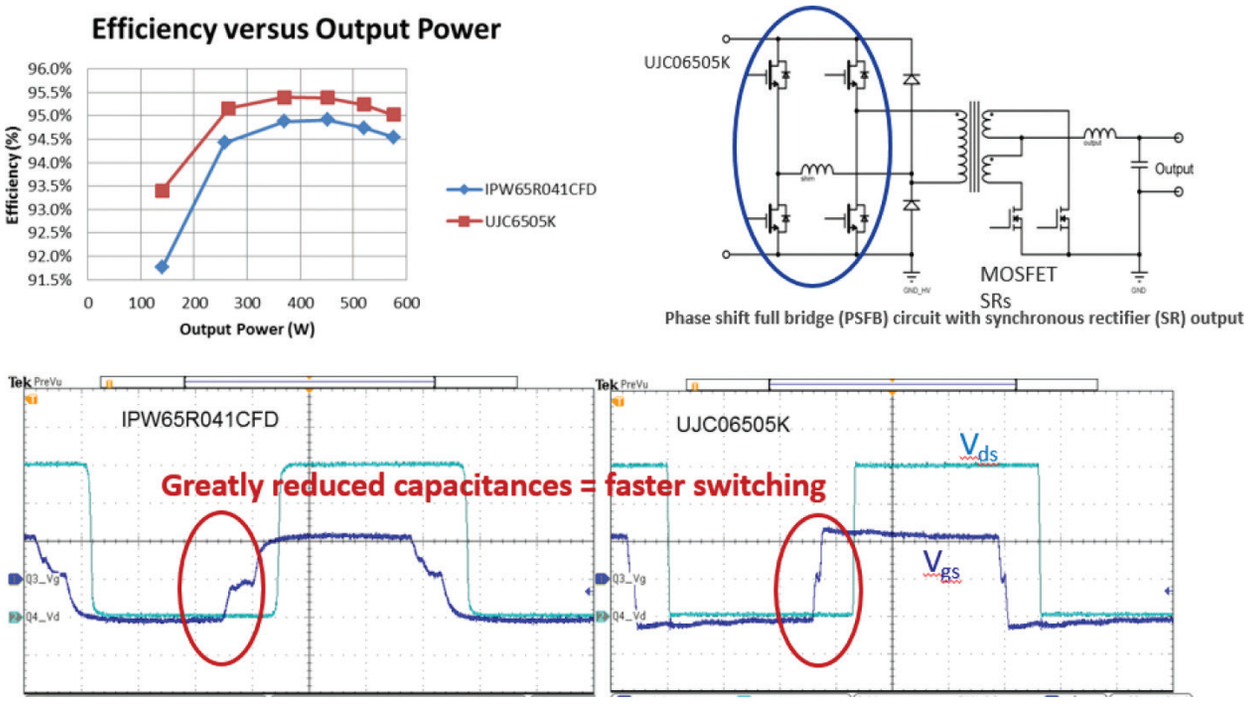

Figure 18. Phase shift full-bridge using SiC cascodes UJC06505K with low capacitances, driven by simple pulse-transformer gate drives at 75kHz. Efficiency benefits at standard operating frequencies are also enabled by SiC.

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Figure 19. A 200KW full-SiC converter presented by Fraunhofer. The converter achieves an impressive power density >100W/cm^3 switching at 200kHz, with an efficiency of 98.9%.

eliminate bridge losses [15] has led to the development of the Totem-pole PFC topology. To use this bridgeless circuit in CCM mode, the device required must feature very low-diode recovery losses in addition to basic fast switching capability. **Figure 16** shows the efficiency achieved in a Totem-Pole PFC, and **Figure 17** shows the excellent body diode recovery behavior that makes this possible. For this reason, 650 V SiC devices are likely to compete with GaN devices at >1.5 kW level of server/telecom supplies that require >99% PFC stage efficiency at high frequencies. This lack of diode recovery charge also makes the SiC-based switches useful in avoiding recovery-induced failures in PSFB and LLC applications when ZVS conditions are temporarily lost.

The rapid adoption of 1200 V SiC MOSFET and cascode devices in the charger market for forklifts and vehicle bidirectional on-board chargers can be easily understood based on the very high efficiency achieved with phase-shift full-bridge topology, that benefit from the low conduction and turn-off loss and from the low Coss and Qrr at light loads. **Figure 18** shows the PSFB efficiency and the waveforms resulting from the low capacitance of the SiC devices compared to incumbent superjunction devices. **Figure 19** shows an excellent demonstration of the power density improvements possible with SiC 1200 V switches for high-power conversion applications, needed on space constrained environments like EVs.

9. Conclusion and outlook

The long wait for SiC to reach a tipping point appears to be nearing its end. This is due to steady progress on every front needed to realize large-scale adoption, from the maturation of 6-in. SiC material and a deep understanding of SiC defects to improved, easy-to-use devices with a growing reliability track record. An ecosystem of excellent gate drivers makes design simpler, and improved discrete, IPM, and module packages have become available to allow

the exploitation of the faster switching capability of SiC. These benefits have allowed users to apply circuits previously not possible with Si devices, and this is fueling the growth in the power supply and on-board charger area. With the type of capability now demonstrated with commercial products, there is little doubt that expansion to the automotive inverter will further accelerate the ramp by the early 2020s.

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