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Band Gap Modulated Tunnel FET

Brinda Bhowmick and Rupam Goswami

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Abstract

This chapter presents bandgap-modulated tunnel field effect transistor (TFET) and discusses its simulation and modeling. A geometry of TFET, the heterojunction TFET, is considered, and different electrical parameters are discussed using Technology Computer Aided Design (TCAD) tool. The effect of the heterojunction on the characteristics is observed through the variations in the length and mole fraction of the pocket layer adjacent to the source. An analytical model is further presented for gate-drain underlap TFET using 2-D Poisson equation and Kane's interband tunneling model. The results are validated with the output from the TCAD tool.

Keywords: heterojunction TFET, TCAD, analytical model, subthreshold swing, tunneling

1. Introduction

Tunnel field effect transistor (TFET) is an asymmetrical gated p-i-n device. Unlike thermionic conduction in metal-oxide-semiconductor FETs (MOSFETs), its working principle is based on a band-to-band tunneling (BTBT) mechanism [1, 2]. This amendment results in a reduced sub-threshold swing (SS), low off-state leakage currents, and less short-channel effects. Recently, numerous structural and material designs of TFETs have been proposed with an objective to achieve improvement in subthreshold swing (SS) and off current. A few of them are bandgap-engineered TFETs [3], graphene nanoribbon TFETs [4], gate-engineered TFET [5], and strained silicon-germanium TFETs [6]. Double-gate TFET [7], dual-material gate TFET [8], hetero-gate dielectric TFET [9], and heterojunction TFETs [10] have also been investigated for improved electrical parameters of TFET. Generally, TFETs have a very low current as compared to ITRS requirement. In order to get a high ON current, a high-k gate dielectrics are preferred. High-k gate dielectrics causes improved capacitive coupling between the gate and the source-channel tunnel junction, resulting in an increased current in TFET. Moreover, to decline the effective oxide

thickness at the tunnel junction, high-k gate oxide is used so that the gate-tunneling current can be reduced. Actually, due to these reasons, the recent trend is to use high-k materials as a better replacement of the conventional SiO_2 (silicon dioxide). On the other hand, it causes a significant ambipolar current. The gate-drain underlap structure in association with heterojunction can be adopted to diminish ambipolar current [2]. A silicon-germanium (SiGe) layer is used at the tunnel junction so that bandgap and tunnel width can be modulated. Electrical parameters have been investigated for various Ge-mole fractions.

Technology Computer Aided Design (TCAD) simulation is a complex iterative mathematical process, and hence various analytical models have been proposed in order to develop a better understanding of the physics-based principles of TFETs and obtain results not constrained by computational time [11]. A number of analytical models based on Poisson equation have been proposed in the study for different geometries [12–14]. In this chapter, a mole fraction-dependent model has been proposed and validated.

This chapter is organized as follows: first, the heterojunction gate-drain underlap tunnel is discussed, and in the second section, the electrical parameters of the heterojunction gate-drain underlap tunnel FET (UL-HTFET) is investigated with the help of TCAD simulation. The third section discusses the physics-based compact model and the validation of the model with simulated results. In the last section, the effect of temperature on the electrical parameters is investigated.

2. Heterojunction gate-drain underlap tunnel FET

A 2-D structure of the proposed UL-HTFET is shown in **Figure 1**. Here, a p + source and n + drain with an intrinsic channel and a δp + $Si_{1-x}Ge_x$ layer at the source-channel tunnel junction are present. The δp + layer can be replaced by a δn + layer too.
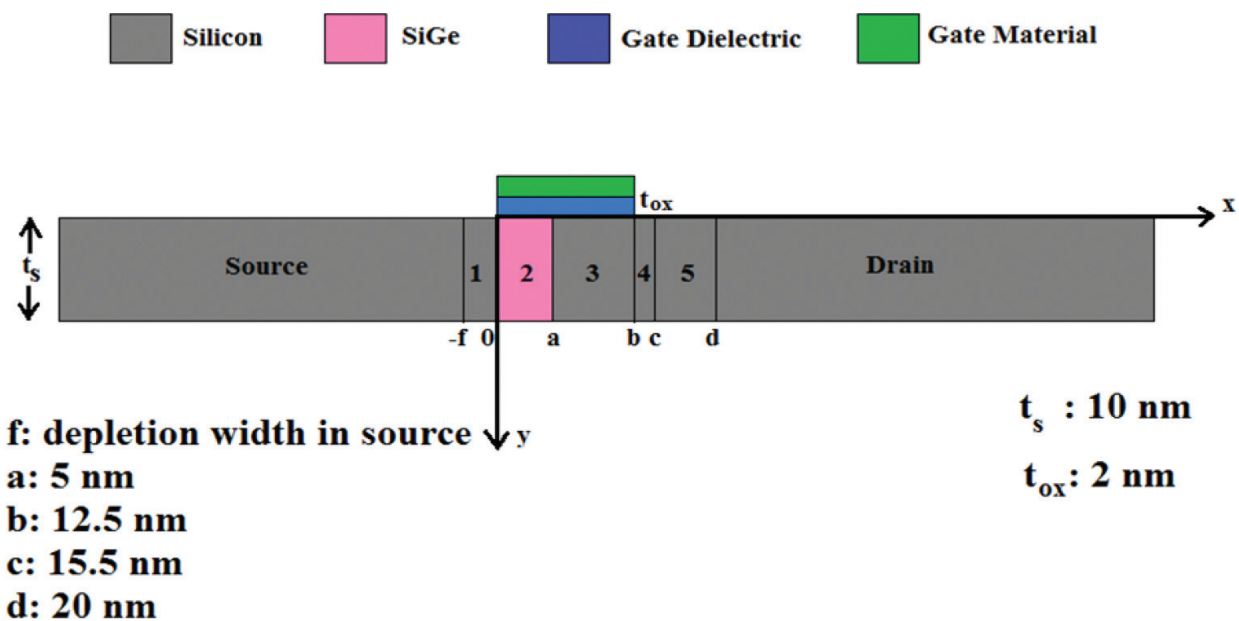

Figure 1. A 2-D geometry of the device (UL-HTFET).

The effect of germanium mole fraction on the UL-HTFET is investigated. Aluminum with work function (4.1 eV) is considered as the gate material. The proposed device spans across a total length of 100 nm with a length of the channel equal to 20 nm. The $\delta p + Si_{1-x}Ge_x$ layer extends from the source-channel junction up to 1 nm into the channel under the gate. The various doping concentrations are used such as source, 10^{21} cm^{-3}; drain, 5×10^{19} cm^{-3}; $\delta p +$ layer, 10^{18} cm^{-3}; and intrinsic region, 10^{16} cm^{-3}. In n-channel, the operation of TFET positive gate and drain voltages is applied with respect to the source. Here, voltage at the source is considered as the reference voltage.

The tunnel FET works on the principle of band-to-band tunneling. Here, SiGe layer is added at the channel near the source-channel junction to enhance the on-current.

3. Simulated results of UL-HTFET

Figure 2 shows the I_{ds}-V_{gs} characteristics of the Si/Ge heterojunction UL-HTFET at different lengths of L_p. When the HTFET is turned on, it shows very high on-current due to the effective bandgap narrowing at the interface of source-channel junction. The I_{ds}-V_{gs} curves are mainly dependent on n + −doped pocket length (L_p) as shown in **Figure 2**; as L_p gets longer, the effective area for tunneling width is extended for HTFET. However, the low off-state current in UL-HTFET (9.205×10^{-20} A/µm) when L_p is less than 2 nm, and this indicates that the ambipolar-tunneling effect at drain channel is suppressed. When L_p is 2 nm, as observed, the tunneling width becomes extremely thin to concede tunneling current at $V_{gs} = -0.5$ V. This tunneling current interrupts UL-HTFET device performance at off-state. The low I_{off} can be achieved at $L_p = 1$ and 2 nm, and I_{on} is greatly higher at $L_p = 4$ nm in TFET. Therefore, an optimum L_p can be located at 1 nm where high ion is achieved and the leakage is suppressed as shown in I_{ds}-V_{gs} characteristics.
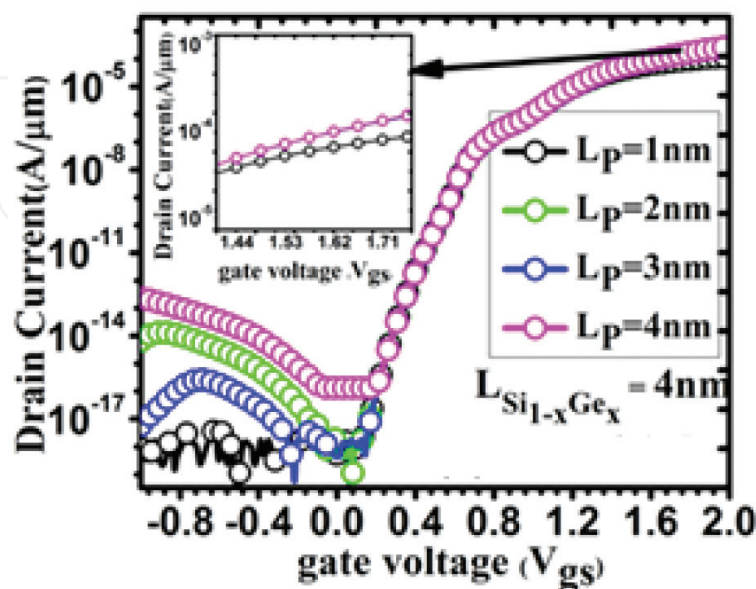

Figure 2. Transfer characteristics for varying L_p lengths at $V_{ds} = 0.7$ V.
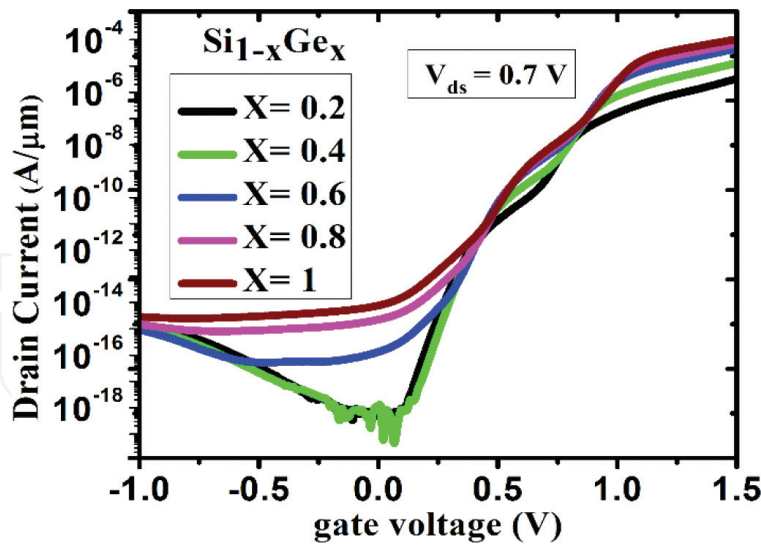
Figure 3. I_d-V_{gs} characteristics of UL-HTFET with varying Ge-mole fractions.

In **Figure 3**, the I_d-V_{gs} characteristics of the UL-HTFET is shown. The mole fraction of SiGe layer is varied. With germanium mole fraction of 0.4, the best I_{on}/I_{off} ratio has been achieved (10^{12}). For Ge-mole fractions below 0.5, the device exhibits a better ratio. As the mole fraction increases beyond 0.5, the properties of the n + layer align more with those of germanium than of silicon. With an increase in mole fraction greater than 0.4, the on-current increases but the increase in off-current is more. This is due to an effective band bending at the source-channel tunnel junction by which the tunnel width can be modulated. For a reduced tunnel width in ON state ($V_{gs} = 1$ V), more ON current is achieved. However, at OFF state, the current is due to thermionic emission as the tunnel current is insignificant.

The energy band diagram is plotted at different mole fractions at ON state ($V_{ds} = 0.7$ V, $V_{gs} = 1.2$ V) shown in **Figure 4**. It is observed that at 0.8-mole fraction of germanium, the ON current is more. With an increase in Ge-mole fraction, the tunnel width reduces and hence enhanced ON current is achieved. In the inset of **Figure 4**, the variation of valence band with mole fraction is shown. The conduction band variation is insignificant with mole fraction.

In **Figure 5**, the electric field is shown at different mole fractions. The peak electric field is observed around 20-nm length along the lateral direction. This is the source-channel tunnel junction. A high electric field at this location is due to the presence of a large tunnel barrier. With the increased mole fraction (at x = 1), a highest peak is observed, and hence tunneling probability will increase and be responsible for the increased current in ON state.

The ON/OFF current ratio and the subthreshold swing are shown in **Figure 6**. The best I_{ON}/I_{OFF} ratio is achieved for Ge-mole fraction of 0.3. In TFETs, an abrupt I_d-V_{gs} plot is obtained where the subthreshold swing varies with gate voltage. Therefore, two types of SS [15] are defined in TFETs: one is the average SS and the other is known as point SS. The average SS is defined mathematically as

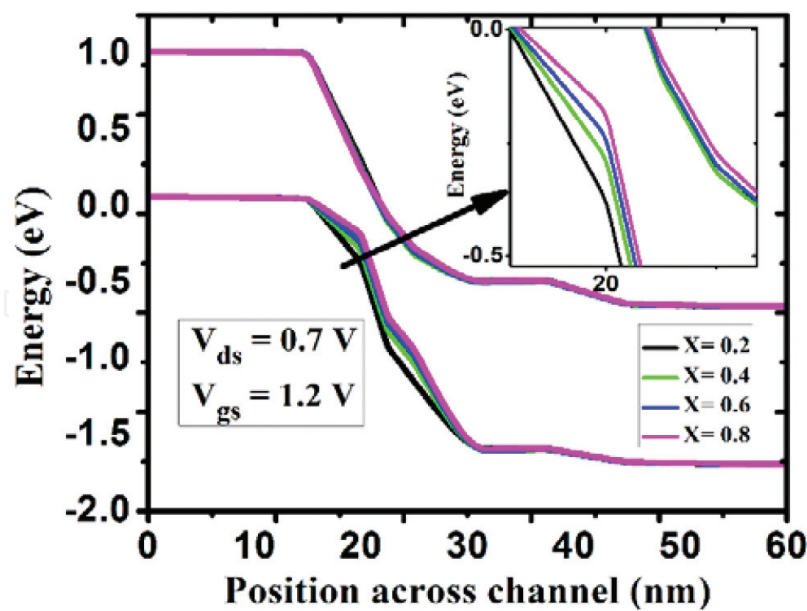$$SSav = (V_T - V_{OFF})/[\log(I_T) - \log(I_{OFF})] \tag{1}$$

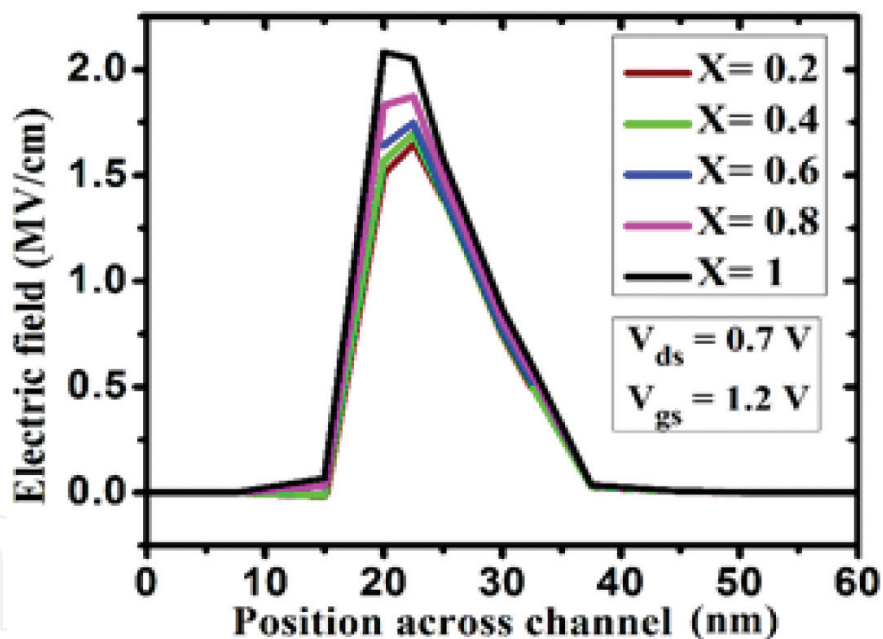**Figure 4.** Energy band diagram at ON state.

Figure 5. Electric field along the channel length in UL-HTFET.

where V_T is the threshold voltage and V_{OFF} is the value of gate voltage at which the drain current just begins to take off. I_T and I_{OFF} are the drain currents at the respective voltages. Point SS, on the other hand, is the minimum SS at any point on the I_d-V_{gs} plot. The plot of average SS for different Ge-mole fractions is shown in **Figure 6**. A remarkable average SS (37 mV/dec) is achieved at 0.2 Ge-mole fraction.
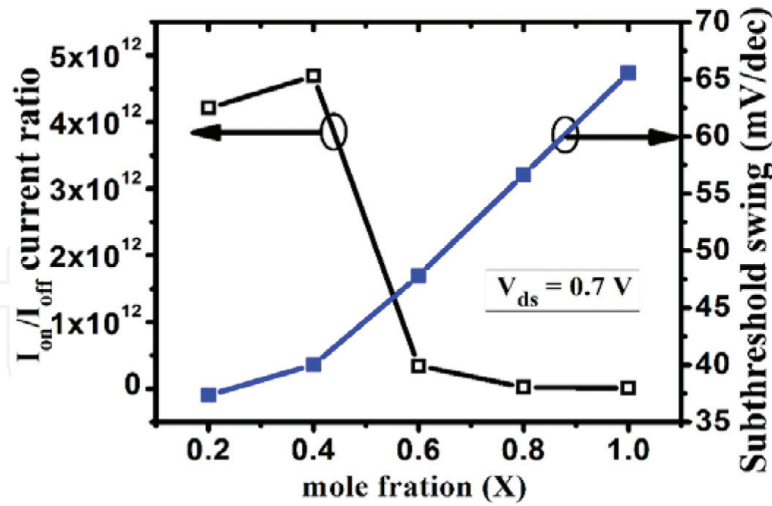
Figure 6. ON and OFF current ratios (I_{ON}/I_{OFF}) and subthreshold swing (SS) versus Ge-mole fraction.

4. Development of analytical model for UL-HTFET

4.1. 2-D Poisson equation-based model

In regions 1–4 of **Figure 1**, the 2-D Poisson's equation is considered and the 1-D Poisson's equation is solved on region 5 due to the absence of gate overlap. The following assumptions have been considered while modeling [12–16]:

1. No trap charges are considered.

2. There are no immobile charges in gate dielectric.

3. Gate leakage current is zero.

4. Source-channel and channel-drain depletion regions do not have any kind of mobile charges.

In regions I–IV, the 2-D Poisson's equation is given as follows:

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \frac{qN_i}{\varepsilon_i} \tag{2}$$

where the subscript $i = 1, 2, 3, 4$ corresponding to regions 1, 2, 3, or 4.

$\Psi_i(x,y)$, N_i, and ε_i are the two-dimensional potential, doping concentration, and permittivity of the semiconductor material, respectively, in the respective four regions.

The 2-D potential is approximated as parabolic along the depth of the device. So, the assumption for the 2-D potential is considered as

$$\Psi_i(x,y) = C_{0i}(x) + C_{1i}(x)y + C_{2i}(x)y^2 \tag{3}$$

where $C_{0i}(x)$, $C_{1i}(x)$, and $C_{2i}(x)$ are coefficients that are functions of mole fraction.

In each of the four regions, three vertical boundary conditions must be satisfied to confirm the continuity of potential and electric field at the gate insulator–semiconductor interface ($y = 0$) and at the lowermost part of the device ($y = t_s$)

$$\Psi_i(x, 0) = \Psi_{si}(x)$$

$$\frac{\partial \Psi_i(x, 0)}{\partial y} = \frac{\varepsilon_i}{\varepsilon_{ox} t_{ox}} \{\Psi_{si}(x) - v_i\}$$

$$\frac{\partial \Psi_i(x, t_s)}{\partial y} = 0 \tag{4}$$

where $\Psi_{si}(x)$ is the surface potential, ε_{ox} is the permittivity of gate dielectric, t_{ox} is the gate dielectric thickness, and $v_i = V_{GS} - V_{fbi}$. The gate voltages with respect to source and the flatband voltage are represented by V_{GS}, and V_{fbi}, respectively. The bandgap E_{Gi} is a function of Ge-mole fraction in $Si_{1-x}Ge_x$ expressed as a linear interpolation of the bandgaps of Si (~ 1.10 eV) and Ge (~ 0.66 eV):

$$E_{Gi} = 1.10 - 0.34x \tag{5}$$

Using the boundary conditions of Eq. (4), we obtain the coefficients of Eq. (3) as follows:

$$C_{0i} = \Psi_{si}(x)$$

$$C_{1i} = \frac{\varepsilon_i}{\varepsilon_{ox} t_{ox}} \{\Psi_{si}(x) - v_i\}$$

$$C_{2i} = \frac{\varepsilon_i}{2\varepsilon_{ox} t_{ox} t_s} \{v_i - \Psi_{si}(x)\} \tag{6}$$

Using the coefficients of Eq. (6) in the polynomial in Eq. (3), the 2-D Poisson's equation can be expressed as

$$\Psi_{si}'' - k_i^2 \Psi_{si} = k_i^2 \xi_i \tag{7}$$

with

$$k_i = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_i t_{ox} t_s}}$$

and $\xi_i = \frac{qN_i}{\varepsilon_i k_i^2} - v_i$.

Eq. (7) has a solution of the form:

$$\Psi_{si}(x) = A_i e^{+k_i x} + B_i e^{-k_i x} - \xi_i \tag{8}$$

The surface potentials for regions I–IV of the device are represented by Eq. (8). For region V, we apply 1-D Poisson's equation:

$$\frac{\partial^2 \Psi_5(x)}{\partial x^2} = \frac{qN_5}{\varepsilon_5} \tag{9}$$

to get

$$\Psi_5(x) = \Psi_{s5}(x) = \frac{qN_5}{\varepsilon_5}x^2 + C_1 x + C_2 \tag{10}$$

The coefficients A_1, B_1, A_2, B_2, A_3, B_3, A_4, B_4, C_1, and C_2 must satisfy the boundary conditions for the continuity of surface potential and electric field in the five regions:

$$\Psi_{s1}(-f) = -\left(\frac{kT}{q}\right)\ln\left(\frac{N_s}{n_{i1}}\right)$$

$$\Psi_{s1}(0) = \Psi_{s2}(0)$$

$$\frac{\partial \Psi_{s1}(0)}{\partial x} = \frac{\partial \Psi_{s2}(0)}{\partial x}$$

$$\Psi_{s2}(a) = \Psi_{s3}(a)$$

$$\frac{\partial \Psi_{s2}(a)}{\partial x} = \frac{\partial \Psi_{s3}(a)}{\partial x}$$

$$\Psi_{s3}(b) = \Psi_{s4}(b)$$

$$\frac{\partial \Psi_{s3}(b)}{\partial x} = \frac{\partial \Psi_{s4}(b)}{\partial x}$$

$$\Psi_{s4}(c) = \Psi_{s5}(c)$$

$$\frac{\partial \Psi_{s4}(c)}{\partial x} = \frac{\partial \Psi_{s5}(c)}{\partial x}$$

$$\Psi_{s5}(d) = V_{DS} + \left(\frac{kT}{q}\right)\ln\left(\frac{N_d}{n_{i2}}\right) \tag{11}$$

where V_{DS} is the drain voltage with respect to source, and n_{i1} and n_{i2} are the intrinsic concentrations of the Si$_{1-x}$Ge$_x$ layer and silicon, respectively. Here, a, b, c, d, and -f are the various positions along the channel at which the boundary conditions are applied. Their

values are mentioned in the inset of **Figure 1**. The width of the depletion region in the source is expressed as

$$f = \sqrt{\frac{2\varepsilon_1|\xi_1 - \Psi_{ss}|}{q|N_1|}} \tag{12}$$

where

$$\Psi_{ss} = -\frac{kT}{q}\ln\left(\frac{N_s}{n_{i2}}\right)$$

Using Eqs. (8) and (10), the lateral electric field for the five regions is given as

$$E_{xi} = -k_i\left(P_i e^{k_i x} - Q_i e^{-k_i x}\right)$$

for i = 1, 2, 3, 4 corresponding to regions I, II, III, or IV.

and

$$E_{x5} = -\left(\frac{qN_5 x}{\varepsilon_5} + C_1\right) \tag{13}$$

The vertical electric fields for the different regions are expressed using Eqs. (3) and Eq. (10) as

$$E_{yi} = -(a_{1i} + 2a_{2i}y) \tag{14}$$

for i = 1, 2, 3, 4 corresponding to regions I, II, III, or IV.

and

$$E_{y5} = 0 \tag{15}$$

The drain current is calculated by integrating the band-to-band generation rate G_{BTBT} over the volume of the device

$$I_d = q\int G_{BTBT}dV \tag{16}$$

where

$$G_{BTBT} = A\frac{|E|^2}{\sqrt{E_{Gi}}}\exp\left(-B\frac{E_{Gi}^{1.5}}{|E|}\right) \tag{17}$$
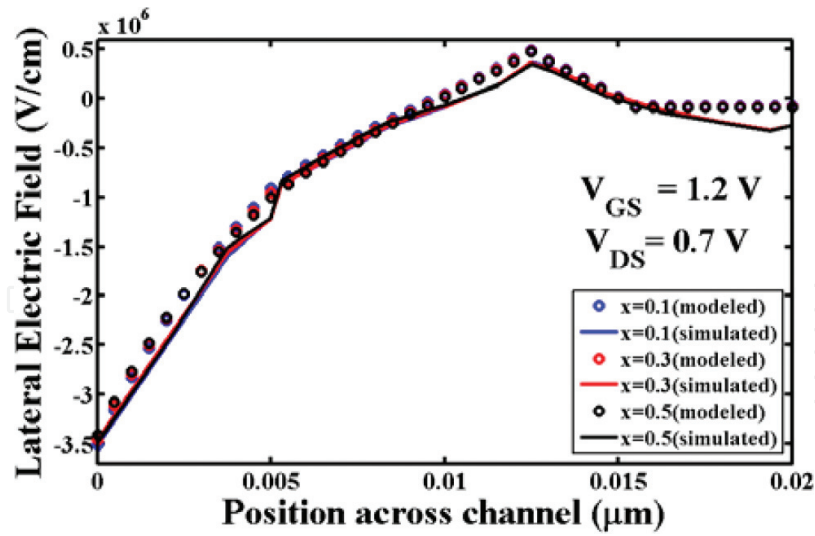
where $E = \sqrt{E_x^2 + E_y^2}$

Figure 7. Variation of lateral electric field at the surface in the channel for different Ge-mole fractions.

4.2. Validation of the analytical model

The developed analytical models are validated with simulation data from TCAD. **Figure 7** shows the plot of lateral electric field at the surface of the UL-HTFET in the channel region for different Ge-mole fractions of the silicon-germanium layer, at $V_{GS} = 1.2\ V$ and $V_{DS} = 0.7\ V$. It has been seen that the modeled values match with the simulated values of lateral electric field except that a small mismatch in the field is observed at the position in the channel where the gate-channel overlap terminates.
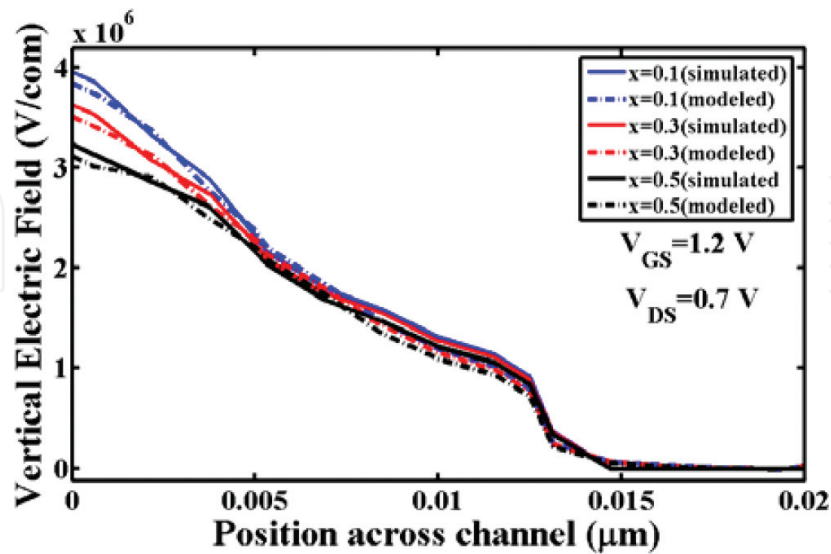

Figure 8. Variation of vertical electric field at the surface in the channel for different Ge-mole fractions.
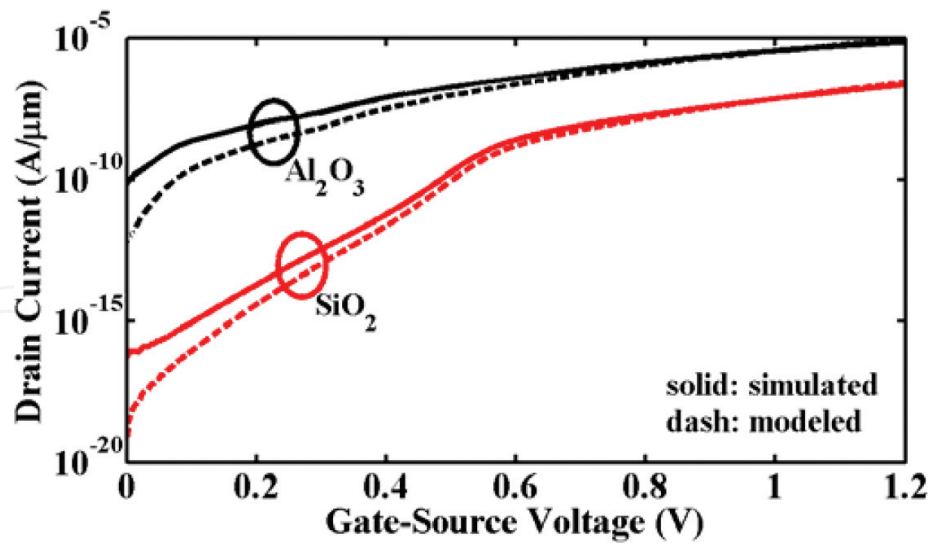
Figure 9. I_D-V_{gs} characteristics at Ge-mole fraction equal to 0.5, gate voltage equal to 1.2 V, and drain voltage equal to 0.7 V.

A plot of vertical electric field at the surface of the device versus horizontal position in the channel region is shown in **Figure 8** for different values of Ge-mole fractions at a fixed drain voltage of 0.7 V and a gate voltage of 1.2 V. For all the cases, it has been observed that the modeled results closely approach the simulated results. The simulated vertical electric field is slightly different as compared to the modeled ones near the junction of silicon-germanium-silicon in the channel region; however, at other positions in the channel, there is a close match between the modeled and the simulated values of vertical electric field.

The variation of drain current with gate voltage has been computed and portrayed in **Figure 9**. There is a close match between the model and the simulated data.

5. Dependence of threshold voltage on temperature

An algorithm for the extraction of threshold voltage in heterojunction TFET is presented in **Figure 10** [17]. The algorithm uses the analytical model of Section 4 to plot multiple curves of surface potential versus position for different gate voltages and fixed drain voltage. The advantage of this algorithm is that the procedure is completely computational, and the threshold voltage can be determined without deriving the transfer characteristics. Moreover, the method can be extended to fit different threshold voltage extraction methods by changing the fitting parameter [17].

The model takes into account the dependence of temperature. The method involves geometrical constructions on a plot of surface potential versus position and using mathematical parameters to define a variable *range_point*.
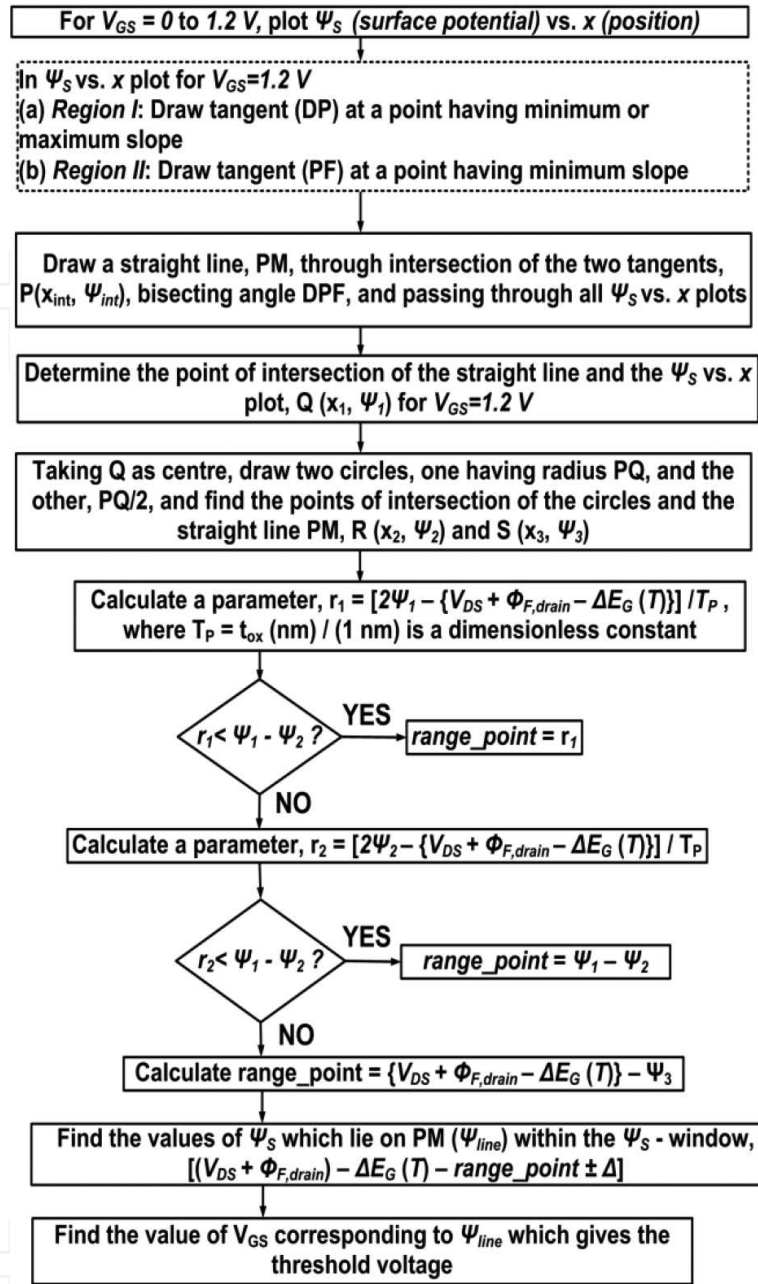
For V_{GS} = 0 to 1.2 V, plot Ψ_S (surface potential) vs. x (position)

In Ψ_S vs. x plot for V_{GS}=1.2 V
(a) Region I: Draw tangent (DP) at a point having minimum or maximum slope
(b) Region II: Draw tangent (PF) at a point having minimum slope

Draw a straight line, PM, through intersection of the two tangents, P(x_{int}, Ψ_{int}), bisecting angle DPF, and passing through all Ψ_S vs. x plots

Determine the point of intersection of the straight line and the Ψ_S vs. x plot, Q (x_1, Ψ_1) for V_{GS}=1.2 V

Taking Q as centre, draw two circles, one having radius PQ, and the other, PQ/2, and find the points of intersection of the circles and the straight line PM, R (x_2, Ψ_2) and S (x_3, Ψ_3)

Calculate a parameter, $r_1 = [2\Psi_1 - \{V_{DS} + \Phi_{F,drain} - \Delta E_G (T)\}] / T_P$, where $T_P = t_{ox}$ (nm) / (1 nm) is a dimensionless constant

$r_1 < \Psi_1 - \Psi_2$?   YES   →   range_point = r_1

NO

Calculate a parameter, $r_2 = [2\Psi_2 - \{V_{DS} + \Phi_{F,drain} - \Delta E_G (T)\}] / T_P$

$r_2 < \Psi_1 - \Psi_2$?   YES   →   range_point = $\Psi_1 - \Psi_2$

NO

Calculate range_point = $\{V_{DS} + \Phi_{F,drain} - \Delta E_G (T)\} - \Psi_3$

Find the values of Ψ_S which lie on PM (Ψ_{line}) within the Ψ_S - window, $[(V_{DS} + \Phi_{F,drain}) - \Delta E_G (T) - range\_point \pm \Delta]$

Find the value of V_{GS} corresponding to Ψ_{line} which gives the threshold voltage

Figure 10. Algorithm for the extraction of threshold voltage in heterojunction and homojunction TFETs [17].

A plot of threshold voltage versus temperature is shown in **Figure 11**. The plot shows that for high-*k* gate dielectric TFET, the threshold voltage rises with an increase in temperature, whereas for low-*k* dielectric, the threshold voltage remains almost constant. The simulated values of threshold voltage have been derived using linear extrapolation method of determining threshold voltage. The method involves the construction of a tangent at the point on the
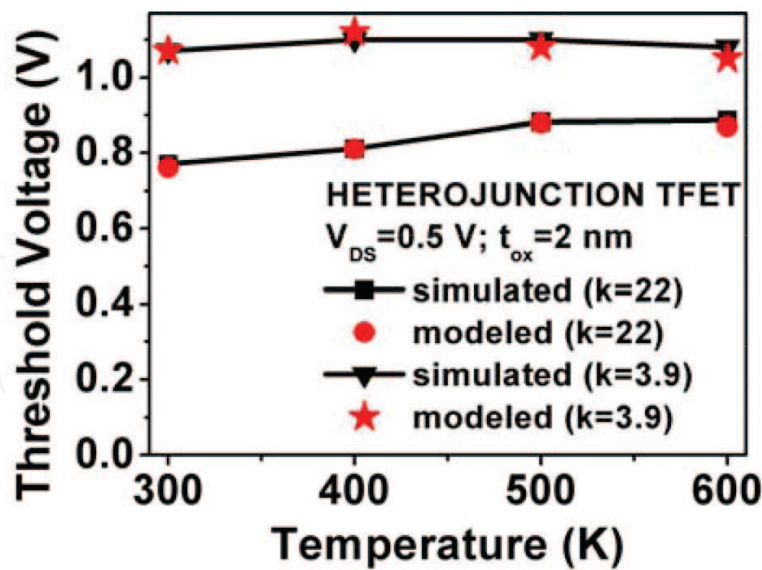
Figure 11. A plot of threshold voltage versus temperature for dielectric constants, 3.9 and 22.

transfer characteristics where the transconductance is maximum. The value at which the tangent intersects the gate voltage axis is taken to be the threshold voltage.

6. Conclusion

This chapter has presented a comprehensive evaluation of a bandgap-modulated UL-HTFET. The simulation analyses have examined the different electrical parameters and their dependence on the pocket length, mole fraction of the SiGe layer, and gate voltage. An impressive on-off current ratio of $>10^{12}$ and a subthreshold swing less than 60 mV/dec are observed. An analytical model based on 2-D Poisson equation has been developed for the gate-drain underlap heterojunction TFET. The modeled values of surface potential, electric field, and drain current satisfy the results of the simulation. Furthermore, a temperature-dependent algorithm has been discussed to extract threshold voltage in heterojunction TFETs, and a validation has been presented for the plot of threshold voltage at different temperatures.

Acknowledgements

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