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Adaptive Control Methodology for High-performance Low-power VLSI Design

Se-Joong Lee
Texas Instruments Inc.
U.S.A.

1. Introduction

Very Large Scale Integrated chip design consists of several steps including modeling characteristics of transistors, profiling circuit level behaviors, abstracting into gate level parameters, synthesizing logic based on timing constraints, and so on. The common concept that runs through all these sequence of design flow is modeling. Traditional VLSI design highly replies on the modeling process, and the percentage that a design chip is successful, or say yield, is determined by how much the modeling is done accurately and precisely. In order to increase the yield, designers put margins while they design. A designer assumes worst cases in design parameters like transistor speed, supply voltage, temperature, and operation frequency. Even though sufficient margin on those design parameters leads higher chance of success in chip design, the margins imply overhead on the other hand. The overhead costs additional power consumption, which should be conquered in this low-power era.

Another cause of such over-design is variable workload in a system. Most of traditional VLSI systems are designed to support the maximum possible workload and the system becomes to have headroom in terms of performance when the workload is not that high.

Modern VLSI designs deploy the concept of adaptive control schemes to manage the costs caused by the over-designs. A chip embeds transistor speed meter, and temperature sensors to monitor actual environment that the chip is operating in, and adjusts the margins to be minimal in order to minimize the additional cost. According to the workload offered to the system, the system controls its supply voltage dynamically thus the system keeps its performance just as enough. In this chapter, we introduce the design cases that use adaptive control schemes to manage the overhead while reducing power consumption.

One another factor causing over-design is uncertainty, which is emerged in recent VLSI design area. Huge complexity of system-on-chips and ever shrinking transistor size has brought the uncertainty issue in modern VLSI design. One example is clock synchronization issue. As the clock frequency goes beyond Giga-hertz, the chip area is no longer bounded within a single clock cycle, thus, clock synchronization in a chip became extremely challenging, and even impossible to achieve. The terminology, Network-on-Chip has begun to widely spread in the VLSI design field as a chip becomes a set of systems interconnected through a network. In such a big system, transmitting and receiving data signals involves timing uncertainty because it is no longer a synchronous system. Such uncertainty incurs timing overhead in the signal transactions and requires additional circuitry resources. In this chapter, we also introduce design examples utilizing adaptive control schemes to address the issues in Network-on-chip design.

2. Adaptive Control on Design Margins

As hand-held devices became the ones driving the electronic market, demand on low-power consumption became very aggressive. And, the chip designers are requested to devise low-power schemes in entire design flow from architecture-level to process-level. While innovating the designs for such low-power constraint, one trend was featured: Minimizing the design margins. The design margins are re-considered as a source of power reduction. In this Section, some examples of design margins are introduced and efforts to minimize them with adaptive control schemes are addressed.

2.1 Process Variation

The very first agenda placed in VLSI chip design flow is modeling of transistor characteristics. Based on measurements on actual transistors implemented on Silicon, electrical behavior of transistors is modeled as a function of voltages supplied to the devices, temperature in which the device is running, etc. Based on the modeling, a VLSI chip designer can simulate system behavior using computer-assisted tools.

The issue in this process is that the transistors have different characteristics whenever they are implemented on Silicon. Due to many practical reasons, transistors are not implemented identically per implementation. To come up with the phenomena, transistor characteristics are modeled with Gaussian distribution curve, rather than a fixed parameter. Based on statistics obtained from extensive measurements, designers use transistor models representing very worst case scenario thus the fabricated chips are operational unless they belong to even worse cases. In other words, designers put margins to their designs to make it operational for any condition of chip fabrication[1]. And, such margins are overhead in terms of performance and power of the chip.

If the chip fabrication process is well under control, the distribution of the transistor characteristics will be narrow enough to neglect such margin overhead. However, as the process technology scales down its minimum feature size lower than tens of nanometers, just small errors in transistor etching or doping on Silicon introduces larger deviation of its characteristics than ever (Figure 1) [1,15]. This implies that designers should put more percentage margins to their designs due to the increased uncertainty of the chip fabrication process.

[1] Even though the author uses the term, 'any', to emphasize the importance of design margin, there is no perfect process, therefore, there will be non-zero failure probability.

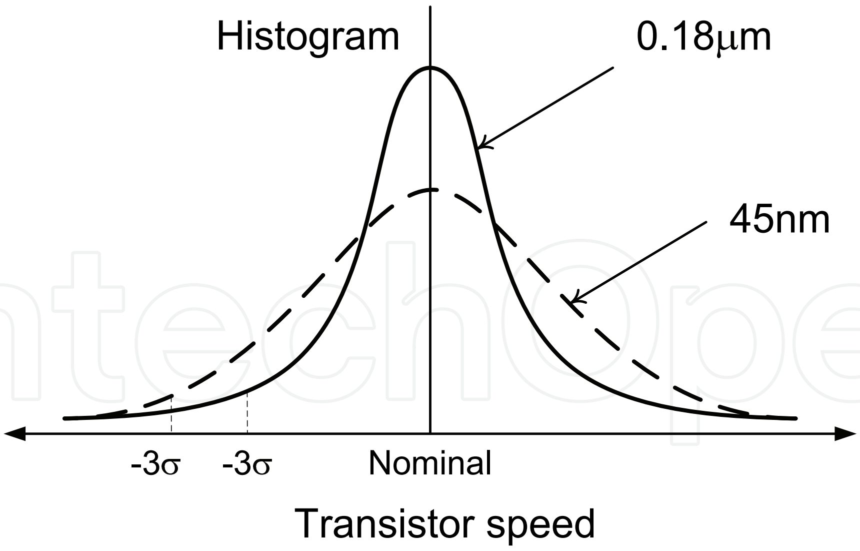

Figure 1. Distribution of transistor characteristics for different feature sizes

Putting voltage margins is trade-off between stability/productivity and power-consumption. As the pressure for low-power consumption gets so strong in hand-held device market, such margins are re-considered as headroom for power reduction. In Figure 1, the additional voltage margin is required by only the chips that belong to the low three sigma profile. If we can measure the quality of transistors of a chip, so that determine the proper supply voltage for that specific chip, it is possible to reduce the power consumption of most of the chips having good and even typical quality transistors.

The *SmartReflex* technology from *Texas Instruments* [2] is one practical example exploiting this type of technology. The Adaptive Voltage Scaling (AVS) scheme, used in the *SmartReflex* technology suite, implements a monitoring circuit in the chip, so that the circuit measures on-chip transistors' speed and temperature during run-time, and determines the quality of them. If the chip has higher quality than the chip designer assumed to be, the chip either commands the external power IC to reduce the supply voltage or decrease the internal supply voltage if embedded. In other words, the chip changes its supply voltage adaptively according to the demand of the chip itself.

The fundamental reason that this type of adaptive voltage control is successful is that the transistor quality is measurable by practical means, so that, the design margin is no longer simply insurance for safe operation, but, it is a controllable parameter. In addition to such known, or we can say measurable, distribution of the process parameters, designers consider another type of margin, which is there to protect the designs from unknown uncertainties either we haven't recognized yet or we weren't able to model properly even if we recognized. And, such unknown parameters will be discovered to turn them into useful headroom for further enhancement in the future.

2.2 Dynamic Voltage Frequency Scaling

Power consumption of VLSI digital systems is represented by Equation (1).

$$P = \alpha \cdot f \cdot V^2 \text{, where } \alpha = \text{coefficient, } f = \text{clock frequency, V=supply voltage} \quad (1)$$

As the equation tells explicitly, reducing the supply voltage is the most effective way to save the power. The supply voltage limits the maximum clock frequency achievable. The clock frequency, *f*, determines the performance of the system. Higher clock frequency implies faster operation, so that, executes more workload within given time. Except some high-end VLSI systems, the supply voltage is a static value which is fixed during entire operation of the chip. Therefore, the supply voltage is set to support the maximum clock frequency.

Even though a system's workload is less than the maximum for which the supply voltage is determined, the chip operates just as fast as possible and goes back to idle mode when it completes, until next task is called. However, this is not an optimal solution from the energy perspective. If we can scale down the supply voltage, thus, the operating clock frequency, we can reduce the total energy consumption while completing the task just on time. The technology scaling the supply voltage and frequency according to the workload is called Dynamic Voltage Frequency Scaling (DVFS). The underlying concept of the DVFS is turning the system performance margin into useful energy so that reduce the overall energy and power consumption [3,4,5].

One of most challenging issue in this adaptive voltage control is estimating the future workload to change the supply voltage prior to arrival of the workload. The supply voltage cannot be changed frequently due to many practical limitations: Once the voltage is changed it should be kept for a while, i.e. a few msec which corresponds to 1 million cycles when it comes to 1GHz clock. Therefore, the change of supply voltage must guarantee that it is enough to support the workload of next, let's say 1 million cycles.

The prediction of future workload is one of open research area. Current system information like CPU utilization, Bus and Memory activity, OS scheduling, and protocol states, can be used to statistically predict the future workload. And, more accurate estimation will result in better power saving with less performance hit problems. If the system is not running hard-deadline tasks, the system is allowed to catch up any residue workload during next time frame, if its current workload estimation was incorrect so the performance setting was not enough to complete the current workload on time. Even if such catch up mechanism is allowed, it may cause sluggishness in user experience, which must be minimized.

2.3 Range of Operational Condition

Another design margin existing in chip design flow occurs due to environmental conditions. Some major parameters considered as the environmental conditions of a chip are supply voltage and temperatures. The speed of a circuit is a linear function of supply voltage, and leakage current of the circuit is an exponential function of temperature. Chip designers want their chips are operational in wider conditions. For example, they want their chips are operational for 0°C to 125°C, rather than 30°C to 50°C, because wider temperature range implies larger market and more reliable operation in unknown situations.

However, satisfying wider specification brings additional overhead in terms of power and area of the chip. One good example can be found in Dynamic Random Access Memory (DRAM) design. The DRAM is developed to store very large amount of digital information. A main physical mechanism in DRAM operations is charging electrons into a capacitor, which is a write operation, and detecting the charge, which is a read operation. And, the DRAM designer wants the electrons in the capacitor remain thus they can be detected later whenever needed. However, the charges leak out from the capacitor slowly, which is called leakage current. Eventually, most of the charges are gone so the capacitor does not have enough charges to be detected. In other words, the information stored in the DRAM capacitor is volatile, therefore, the charges need to be detected within certain limited time, and re-charged in order to extend the life time of information. This operation is called, *refresh*. The refresh operation of a DRAM is one of major factor consuming power when the system is idle. For example, when a lap-top computer is in standby-mode, the main CPU can sleep to reduce the power consumption, but, the DRAM should perform refresh operation regularly in order to retain the data stored in. Therefore, the DRAM designers want their DRAMs get refreshed as less frequently as possible. The refresh frequency is determined based on the leakage current, and it increases exponentially according to the temperature. If the temperature of the DRAM is high, the leakage current is also high; therefore, refresh must be done more frequently. Therefore, if the temperature specification of the DRAM is 30°C ~ 100°C, which looks typical, the DRAM designer determines the refresh frequency based on the highest temperature, say 100°C.

For advanced power management, some designers had started to embed a temperature sensor circuitry to monitor the temperature and determine decent refresh frequency based on the temperature [6,7]. Figure 2 shows an example block diagram of this type of DRAM architecture. Around the DRAM cells which are the source of leakage current drawing, temperature sensor circuits are placed, and the adaptive refresh controller monitors the highest temperature. Based on pre-programmed temperature-to-refresh conversion curve, the adaptive refresh controller commands the refresh circuit with minimum frequency necessary.

This adaptive refresh frequency control is very useful for extending the standby time of our lap-top computers, because, the lap-top computers are not that literally hot during standby mode, and the DRAM will adaptively set the refresh frequency low, and decrease the power consumption while retaining the data properly.

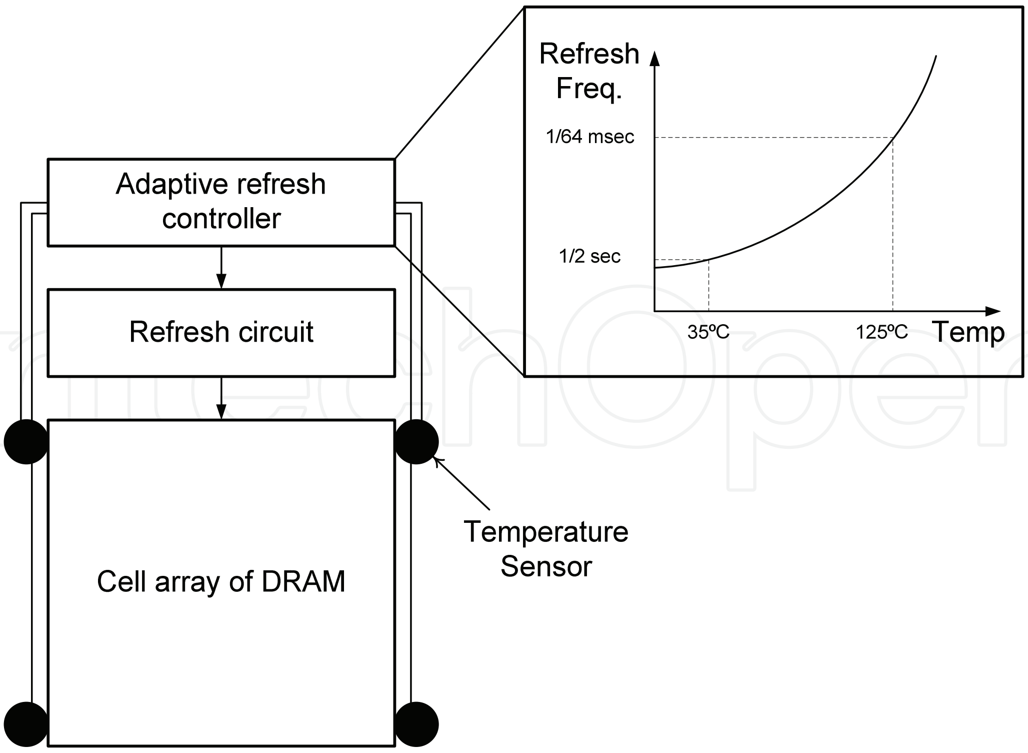

Figure 2. An example of DRAM block diagram with adaptive refresh scheme

3. Adaptive Technologies in Network-on-Chips

A modern VLSI chip is no longer a simple functional unit, but, it consists of tens of processing elements, constituting a system in the chip, and we call it as a System-on-Chip or SoC. As the number of processing elements in an SoC increases, the interconnection gets longer and more complex. It is intuitive that the complexity of an interconnect system for the number of N processing elements is N^2, which implies that the interconnect complexity will dominate the SoC design as the N increases. The Network-on-Chip, which is a new concept representing the most complex SoC in which the interconnect system is even considered as a network [8,9,10,11].

Such an on-chip network consists of sophisticated circuitry to comply with complex data transaction pattern in the VLSI system. This Section introduces some adaptive control schemes making the on-chip network more flexible, stable, and power-efficient.

3.1 Adaptive Topology Configuration

On-chip network topology has impacts on chip performance, power, and area of the network, and choosing optimal topology depends on the traffic pattern traversing through the network [14]. For example, Mesh topology shown in Figure 3-(a) is a widely used network architecture for parallel computing systems, because of its beauty of symmetric shape, unique link length, and scalability with low cost. However, the Mesh topology suffers from long latency for long-distance packet transmission. In Figure 3-(a), a packet from the left-top switch takes 7 intermediate switches to arrive at the right-bottom one. Each switch is a packet-switching switch, and a packet-switching operation requires a series of pipeline activities like packet header parsing, arbitration, and routing. As a result, each packet switch takes at least a couple of clock cycles to transfer a packet from an input port to an output port, thus, passing through several packet switches takes tens of cycles. Due to the high latency issue for long-distance packet transmission, it is known that Mesh network is useful for traffics with high locality. Figure 3-(b) shows another topology, Star, which has different characteristics against Mesh. A Star network shows the minimum packet latency[2], because the switch hop count between two nodes is 1. In case of Tree-topology, the number of switch hops is given by logarithmic function of the distance of the two nodes, whereas that of Mesh network is linear function of the distance.

[2] The Star network may have longer interconnect wires, which will contribute additional propagation delay thus increases the end-to-end packet latency. The author, however, points out that the propagation delay is not yet considerable compared to the packet switch's pipeline latency in a few Gigahertz clock frequency era.

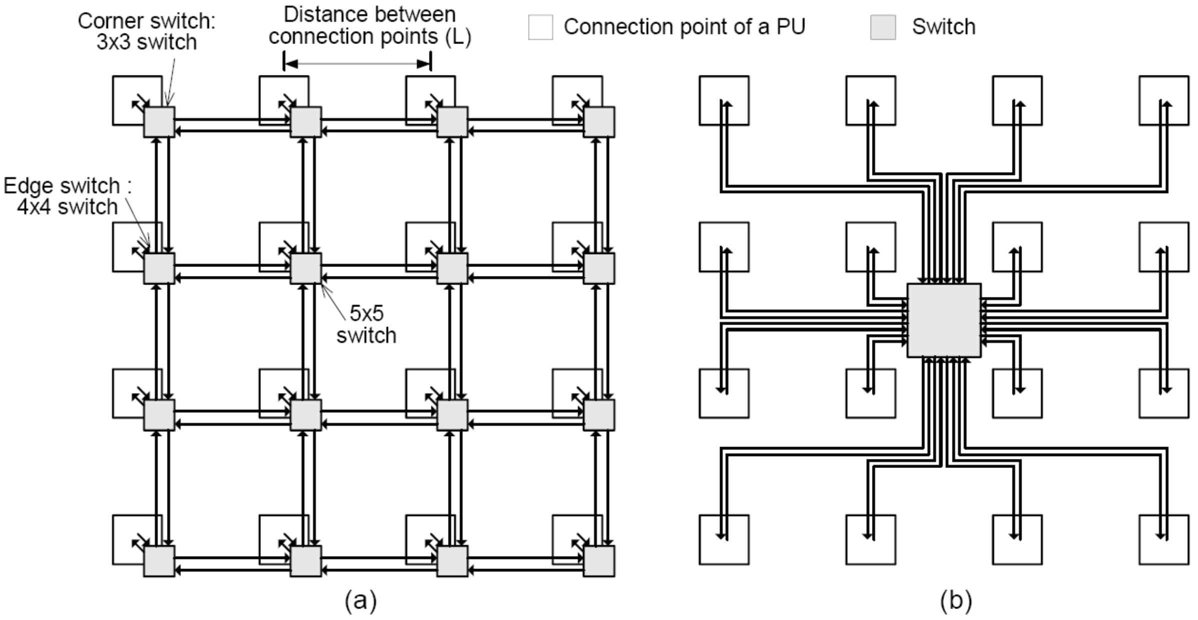
Corner switch: 3x3 switch
Distance between connection points (L)
□ Connection point of a PU
▨ Switch
Edge switch : 4x4 switch
5x5 switch
(a)
(b)

Figure 3. (a) Mesh and (b) Start topology configurations

The issue of choosing a best topology for a VLSI chip design is that the optimal topology is determined by traffic pattern and the traffic pattern is either 1. diversified per situations or 2. not determined until the system is actually used. Therefore, a configurable topology which changes *adaptively* according to the situations or system usage is definitely demanded.

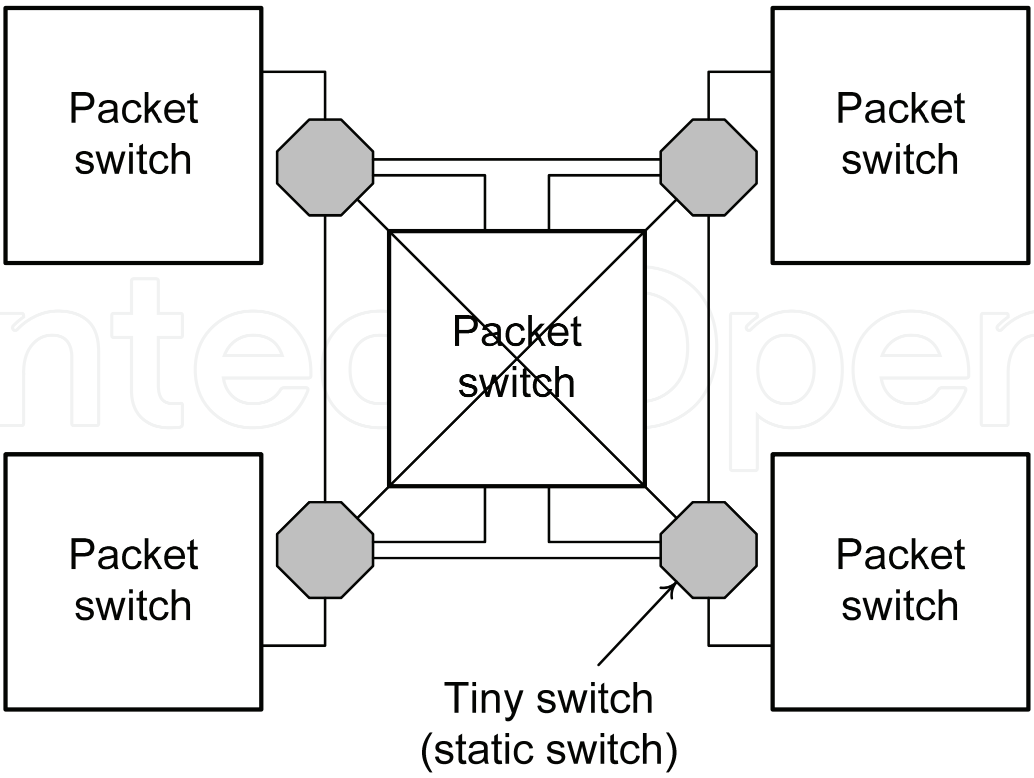

Figure 4. Configurable network topology with tiny switches

One interesting evolution found in the VLSI chip [12] is the adaptive topology configuration. Figure 4 illustrates the overall block diagram of the architecture. Using tiny switches consisting of simple switch transistors and wires, the way the main packet network switches are connected is changed according to the control signals. The tiny switch is not a packet switch, therefore, it does not incur cycle-level latency. Instead, it takes propagation delay time for signals passing through the tiny switches.

In order to utilize the adaptive topology configuration scheme, an efficient mechanism detecting the system situation is required. A traffic monitoring unit can be deployed to inspect the average packet delivery distance, and feedbacks the information to a central network controller. The network controller changes the network topology based on the traffic information in order to tune the network performance or reduce power consumption. This type of research will be continued in Network-on-Chip area.

3.2 Adaptive Voltage Scaling in Interconnect

In spite of ever shrinking chip size as the process technology scales down the minimum feature size aggressively, the relative chip size that the interconnect experiences gets increasing as the integration level of the chip does. And, it is well-known that the portion that the power-consumption of the interconnect occupies in total power consumption of a VLSI chip is considerable. And, among the power-consuming sources in the interconnect architecture, link wire, which is physical conductive and capacitive connection to propagate electrical signal, is one of major current drawer. Therefore, energy minimization in link wires is highly demanded.

As described in Section 2.2, the DVFS technology can be applied to a processing element having diversified workload profile, so that, the supply voltage is adaptively changed to let the processing element consume decent energy which is just enough to perform the processing within a given time constraint. This concept can be applied to the interconnect wires, too.

Figure 5 explains the correlation between the supply voltage and bandwidth of a wire. The bandwidth implies how many peak-to-peak switching digital signal symbols can propagate within a unit time. For a given capacitance of the wire, higher supply voltage results in higher bandwidth, thus, the wire can transfer the digital signal more frequently.

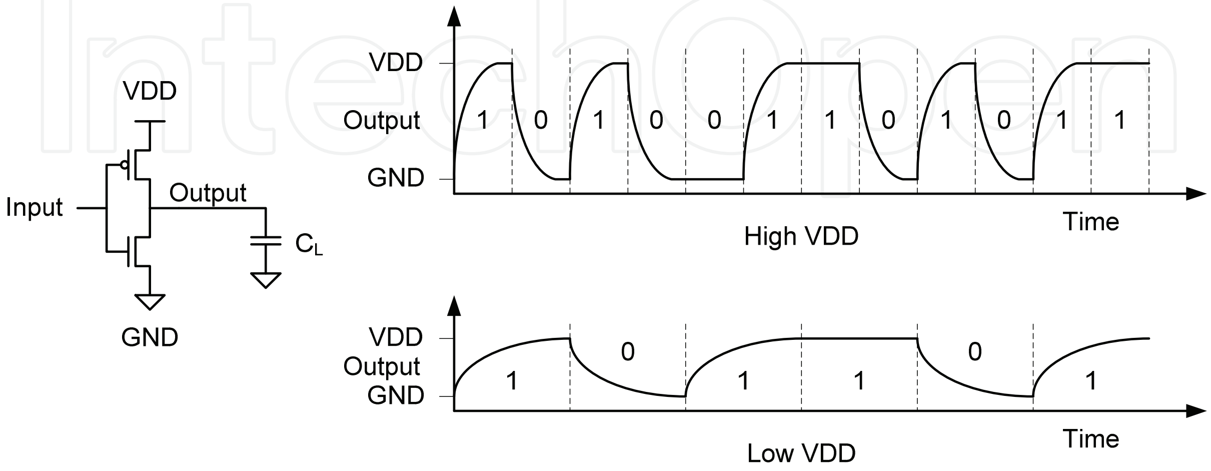

Figure 5. The correlation between the supply voltage and link bandwidth

The maximum bandwidth of a wire required in a VLSI system is determined by maximum data transfer rate that the designer intended to have. However, as same as the motivation of DVFS in the processing elements, the data rate required is time-varying according to the system state. Therefore, if we can detect the requirement, we can adjust the supply voltage of the wire to support just enough bandwidth required.

Figure 6 illustrates an example of adaptive supply voltage control in link wires used in Network-on-Chip [13]. The queue is a FIFO buffer storing data to be transferred. If the backlog of the queue exceeds a certain threshold, the adaptive supply voltage controller decides that the transmitter unit is demanding higher data transfer rate than the one currently supported by the link. Therefore, the controller chooses to use higher supply voltage. In case of the other way around, the controller selects lower supply voltage.

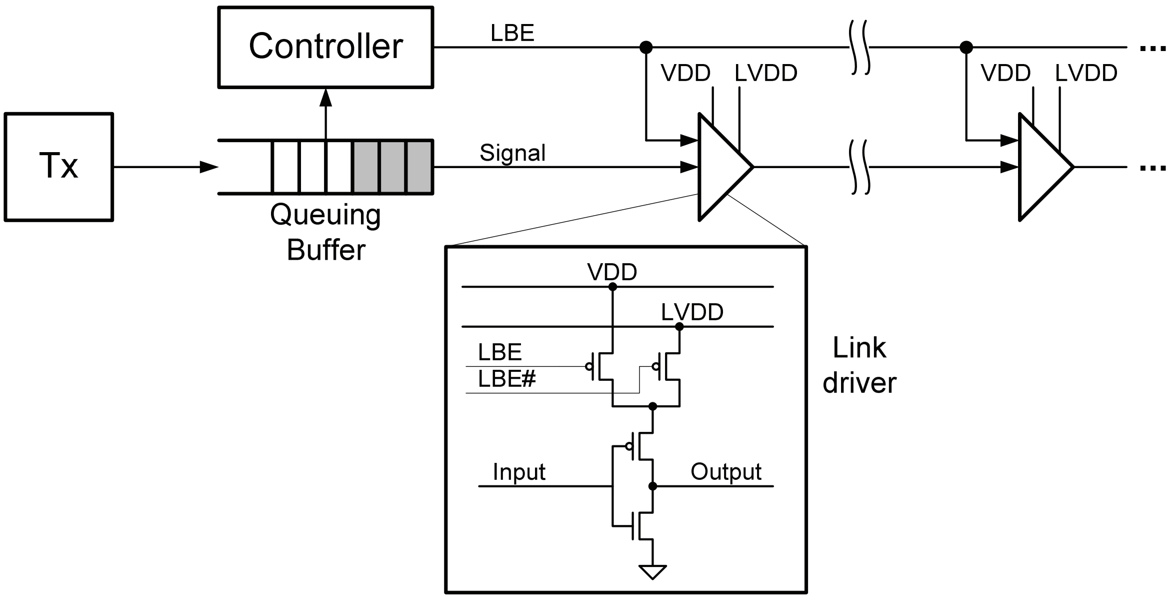

Figure 6. Adaptive bandwidth adjustment circuit

How promptly the wire’s bandwidth can be changed, or the response time of the voltage scaling command, is an important parameter determining overall behavior of this adaptive control scheme. The change of bandwidth is the same operation as the change of supply voltage. And, the time required for scaling the supply voltage differs design by design. Many design solutions for voltage scaling in interconnect wires are feasible, and, one of cost-effective solutions adopted in [13] is illustrated in Figure 6. The two different voltage supply lines, VDD and low VDD, are placed along with the interconnect wires, the driver circuits are connected to both of the supplies, and the control signal selects one of the two supplies. In other words, the number of available voltage levels is two. We can say this is selective voltage scheme rather than voltage scaling. The parameter determining the time for voltage change is the propagation delay time of the control signal from the transmitter to the receiver, and the actuation time required by the power switch. The actuation of the power swtich and the propagation of the control signal occur in parallel, and, the propagation delay is typically much higher than the switch enable time, so that the response time of the voltage change control is dominated by the propagation time of the control signal.

The control signal is placed along with the link wire together, therefore, the propagation delay is substantial when it comes to global interconnect. And, the power consumption of global interconnect is the issue of interest due to its large capacitive load, therefore, the long propagation delay is not evitable. The long propagation time, or the response time, determines the performance of the adaptive control. As the response time is shorter, the link bandwidth can be controlled more closely to follow the actual performance requirement, thus, optimize energy-consumption.

In order to overcome the long propagation delay problem, we can use more aggressive circuit technique called wave-pipelining. Underlying idea of wave-pipelining in general circuit implementation is to utilize propagation delay to split two sequential signal symbols. Figure 7 depicts how this mechanism is used to hide the propagation delay time. Once the control signal is considered to be propagated enough length, the controller circuit treats the link as if its bandwidth change has been completed. Even though this assumption is not valid yet and only a part of the link has been changed, we know that the signals from the transmitter will take the same path and experience similar propagation delay, therefore, the link bandwidth at a certain link point will be updated prior to the signal's arrival to the point. As long as we confirm that the control signal propagates at the higher or same speed compared to the data signal, this wave-pipelining scheme works properly while minimizing the response time in the adaptive control loop.

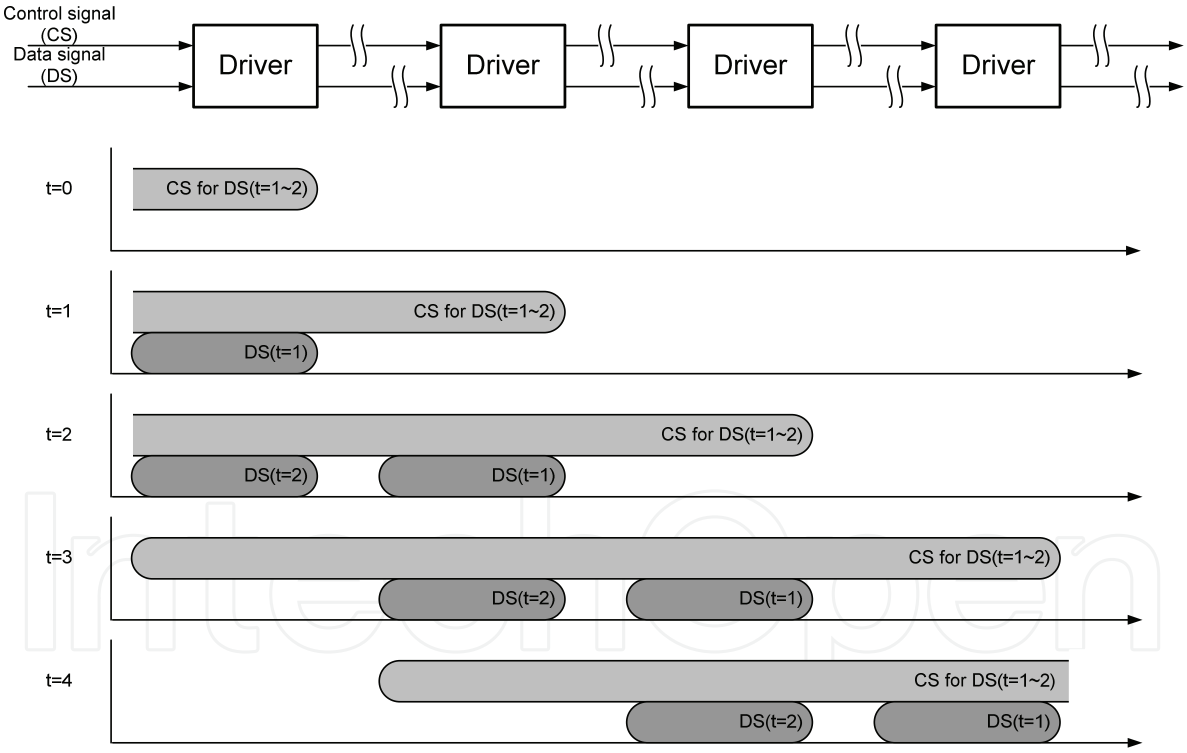

Figure 7. Wave-pipelining scheme for the control signal

3.3 Adaptive Fetching Point Control

One of on-chip network (OCN) roles in an SoC design is to lessen the burden of global synchronization using mesochronous communication in which network blocks share the same clock but the phase difference is not compensated. In general, mesochronous communication implies clock phase difference between clock domains is unknown. Due to such uncertainty in clock phase, clock synchronization circuit typically deploys multiple stages of flip-flops incurring synchronization latency and power consumption.

In a hard-wired chip, however, the phase difference is bounded to *unknown but deterministic* difference. This implies that adaptive adjustment of synchronization clock with an architecture of simple pipeline synchronizer is enough to resolve the phase difference.

According to the circumstance in which a chip is working, the deterministic phase difference can vary. Below, three situations are listed, in which the phase difference between two communicating blocks can vary:

- Packet route variation (physical distance variation)
- Supply voltage variation (electrical distance variation)
- Network clock frequency variation (reference timing variation)

If the dynamic topology adaptation scheme described in Section 3.1 is applied, a switch receives packets not only from a certain neighborhood switch but also from somewhere else. This means that the physical distance between two communicating blocks can change. Supply voltage control is used as a mean of power management as described in the previous Section. In case of supply voltage variation, electrical distances[3] between blocks vary, so that phase difference is changed. The network clock frequency variation also changes clock phase difference. The clock frequency variation is useful technique to manage overall power consumption based on network bandwidth requirement: For example, the OCN [9] controls network frequency with 4 steps for low-power application. When the clock frequency is changed, reference timing is changed, which shifts phase.

Due to the reasons stated above, the phase difference can be varied. In other words, if we have information about clock frequency, supply voltage, and network configuration, we can estimate phase variation. Since the combinations of the phase-varying factors are limited to several cases, the phase difference can be thought *unknown but quantized*.

To deal with the quantized phase differences, a programmable delay is used as shown in Figure 8. A variable delay (VD) is connected with a simple pipeline synchronizer, and the VD is controlled according to the network circumstance. The appropriate VD setting for a certain circumstance is obtained through calibration process. Once the adaptive clock-phase selection unit gathered the appropriate settings for every combination of the system states, it adaptively controls the delay time of the VD, therefore, it avoids hazardous situations in synchronization.

Measured waveforms of the adaptive clock-phase selection mechanism are shown in Figure 9. The initial problem is that the EN signal may be not synchronized with the clock so that the rising edge of the EN could be very close to the "rising edge minus setup time margin". In Figure 9-(a), the mode C represents such a system situation that the rising edge of the EN signal is very close to the clock timing. When the system state, mode C, is detected, the controller expects that fetching the EN signal is very unstable so that the EN would be fetched at the next clock cycle as shown in Figure 9-(a). This phenomenon is captured more clearly in Figure 10. The EN signal should be fetched at the clock rising edge T_A. However, the signal is fetched at the timing T_B with some finite probability. Such an unstable behavior may produce synchronization failure or meta-stable state, which is undesirable phenomenon in signal transmission.

[3] The propagation delay time between nodes.

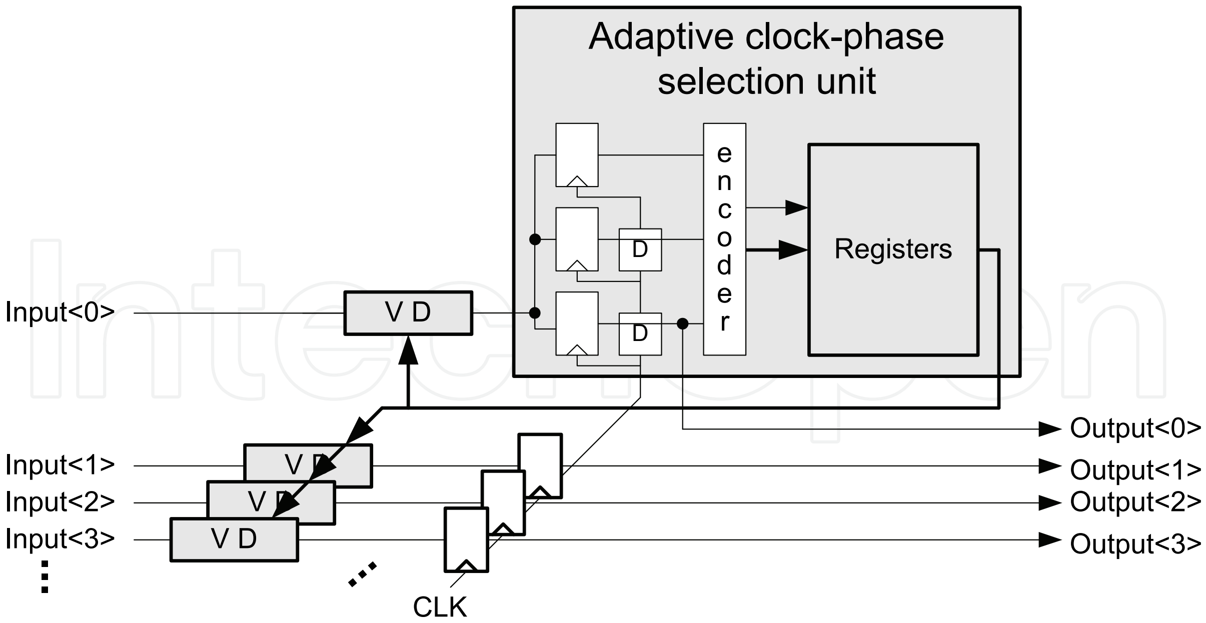

Figure 8. Adaptive clock-phase selection with variable delay circuit

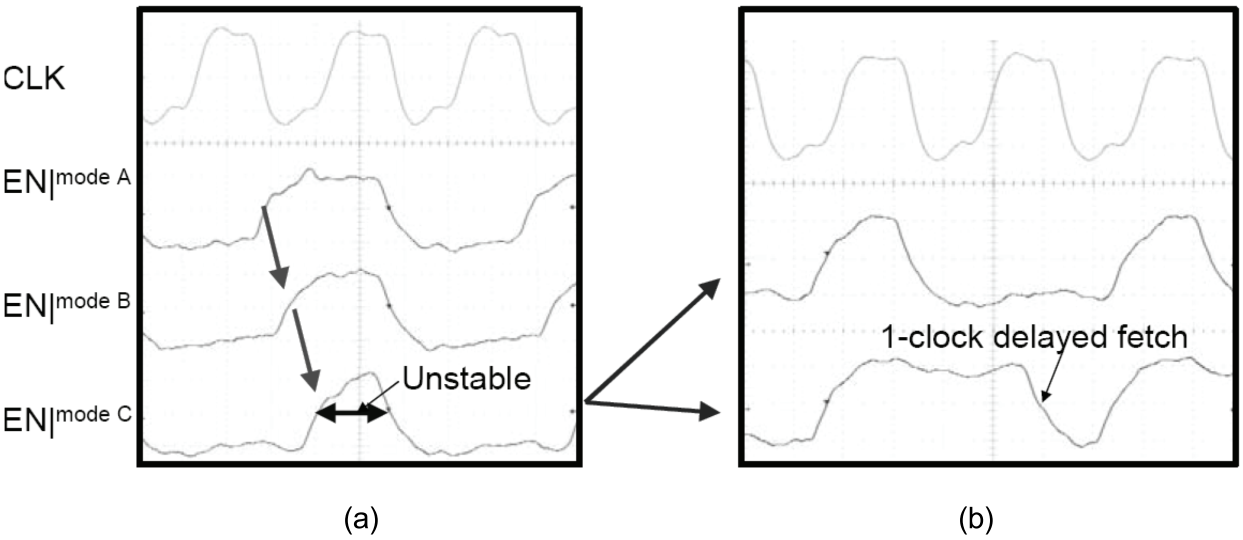

Figure 9. Uncertainty in non-synchronized global interconnect

Figure 11 shows the measured waveform when the adaptive clock-phase delay synchronization is enabled. When the mode C is detected, delay time applied to the EN signal is reduced so that the fetching timing is effectively delayed compared to normal operation, which ensures sufficient timing margin to fetch the EN signal. As a result, the deassertion of the EN signal is delayed as shown in the figure.

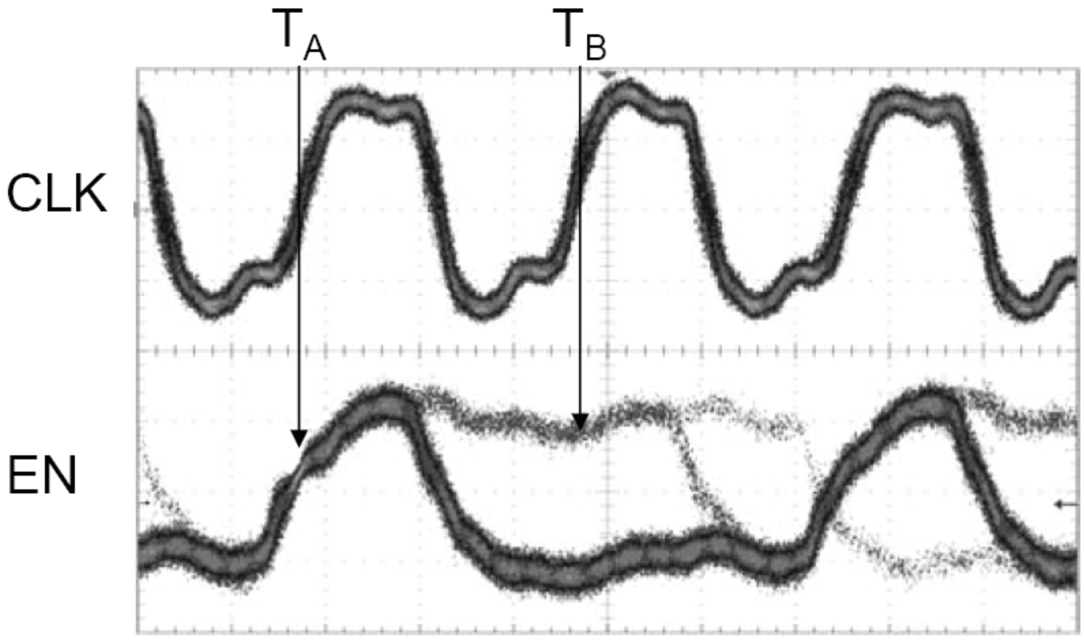

Figure 10. Accumulative display of synchronized EN signal with finite probability of delayed synchronization

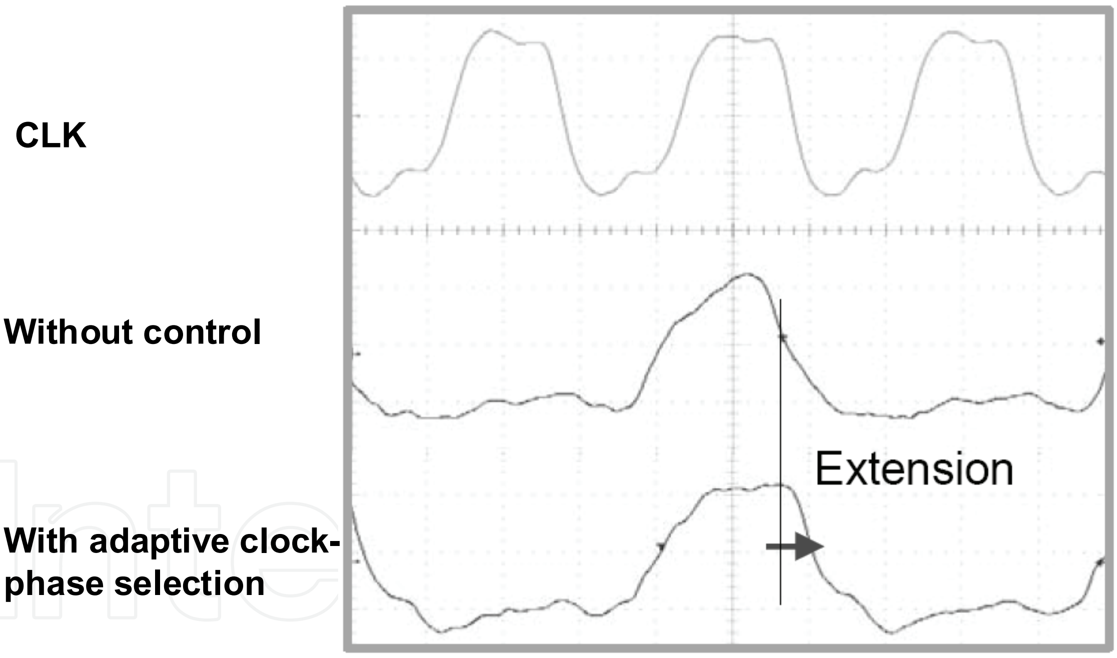

Figure 11. Stable synchronization when adaptive clock-phase shifting is applied

4. Summary

In this Chapter, we surveyed various topics in VLSI technology in adaptive control perspective: The design margins in process and circuit level are considered to be headroom for power savings, and adaptive control schemes are used to figure out the margins automatically and to make adjustment without harming the system operation. The margin is also found in system performance, and dynamic voltage frequency scaling can be thought as an adaptive control based on estimated workload. An adaptive control is also used to optimize the circuit operation for time-varying circumstances. This type of scheme enables the chip to operate always in optimal condition for wide range of operation conditions. We found the application of adaptive controls in the most advanced SoC architecture called Network-on-Chips. To comply with such a high-performance aspect of the modern VLSI systems as well as low-power requirement, the NoC utilized adaptive schemes in topology selection and link bandwidth control. And, adaptive clock-phase shifting was a solution to address uncertainty in such a large scale designs.

There is no doubt that the VLSI designer will seek adaptive control schemes more and more, as the VLSI system grows with higher complexity and wider application spectrum.

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