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System and Component Failure from Electrical Overstress and Electrostatic Discharge

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Abstract

Electrical overstress (EOS) and electrostatic discharge (ESD) have been an issue in devices, circuit and systems for electronics for many decades, as early as the 1970s, and continued to be an issue to today. In this chapter, the issue of EOS and ESD will be discussed. The sources of both EOS and ESD failure history will be discussed. EOS and ESD physical models, failure mechanisms, testing methods and solutions will be shown. The chapter will close with discussion on how to provide both EOS and ESD robust devices, circuits, and systems, design practices, and procedures, as well as EOS and ESD factory control programs. EOS sources also occur from design characteristics of devices, circuits, and systems.

Keywords: electrical overstress, electrostatic discharge, latchup, system failure, component failure

1. Introduction

Electrostatic discharge (ESD) and Electrical overstress (EOS) have been an issue with the coming of the electrical age, when electricity and electrical product were first introduced into the mainstream of society [1–5]. With the scaling of semiconductor components, electrostatic discharge (ESD) has been a growing issue [2]. With the introduction of electrical power systems, the telephone, and electronics, inventions such as circuit breakers, and fuses became the first type of electrical over-stress protection concepts to avoid over-load of electronic systems [1, 16–25]. Electrostatic discharge (ESD) and electrical overstress (EOS) will be discussed in the following sections.

In electronic design, a plethora of electrical events can occur. **Figure 1** illustrates the type of topics including ESD, EOS, latchup as well as electromagnetic interference (EMI), and electro-magnetic compatibility (EMC).

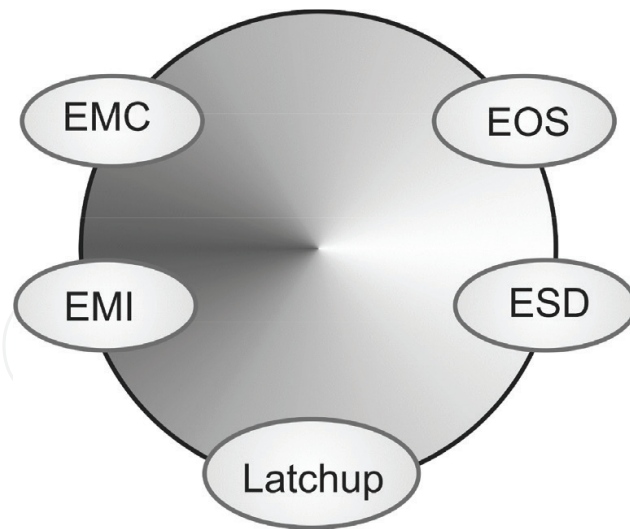


Figure 1. ESD, EOS, Latchup, EMI and EMC.

2. Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is a common form of component level failure from manufacturing, shipping, and handling. Today, the ESD models and performed for qualification and shipping of semiconductor components are as follows [4]:

- Human Body Model (HBM).
- Charged Device Model (CDM).

Additional models that are still performed, but not used for qualification of components include [4]:

- Machine Model (MM).
- Transmission Line Pulse (TLP).
- Very-Fast Transmission Line Pulse (VF-TLP).
- Latchup.
- Transient Latchup.

2.1. Human body model (HBM)

ESD pulse models have been established to quantify the interaction of semiconductor chips and human beings. An important model is the human body model (HBM). Today, HBM is the most widely established standard for the reliability and quality in the semiconductor industry [2–4, 6]. The HBM test is integrated into the qualification and release process of the quality and reliability teams for components in corporations, and foundries [6].

The human body model is regarded as an electrostatic discharge (ESD) event, not an electrical overstress (EOS) event [1–11]. HBM represents the interaction the electrical discharge from a human being and component. The model assumes that the human being is the initial condition.

The human body model (HBM) became of interest in early days in the mining industry in the 1950s. In the Bureau of Mines, investigation reports discussed the issue of electrostatic in the mining industry. A first publication was published by P.G. Guest, V.W. Sikora, and B.L. Lewis as the *Bureau of Mines, Report of Investigation 4833*, U.S. Department of Interior, January 1952 [7]. A second article of interest was published by D. Bulgin, referred as D. Bulgin. Static Electrofication. *British Journal of Applied Physics*, Supplemental 2, 1953 [8].

An early investigator of issues with the human body model standard was T. M. Madzy and L.A. Price II of IBM in 1979 discussed a test system titled “Module Electrostatic Discharge Simulator” [4]. In this article, it was discussed that the ESD simulator was used within IBM since 1974. In 1980, H. Calvin, H. Hyatt, H. Mellberg, and D. Pellinen proposed values for the resistance and capacitance for the human ESD event for the finger tip and field enhanced discharges in “Measurement of Fast Transients and Application to Human ESD,” published in the 1980 Proceedings of the EOS/ESD Symposium [4, 10–11]. The proposed resistance for the finger tip was averaged 1920 Ω , and capacitance of 110 pF, whereas the field enhanced discharge was a resistance of 550 Ω , and 120 pF. In 1981, H. Hyatt, H. Calvin, and H. Mellberg investigated the human ESD event, published in the 1981 Proceedings of the EOS/ESD Symposium, titled “A closer look at the human ESD event” [4, 10–11].

HBM failure mechanisms are associated with permanent damage on the peripheral circuitry of a semiconductor chip [3]. Additionally, HBM failures can occur power rails and ESD power clamps between the power rails. HBM failures can occur in both passive and active semiconductor devices. The failure signature is typically isolated to a single device, or a few elements. ESD circuits are designed to be “tuned” to be responsive to specific pulse widths; this is an issue for EOS events since they are not “tuned” for EOS events. For example, the RC-triggered ESD power clamp is tuned to the HBM pulse, not EOS events.

HBM ESD failures are also distinct from EOS events [1, 4]. HBM events will not typically cause failures in the package, printed circuit board (PCB), or single component devices mounted on a printed circuit board.

Human body model (HBM) failures can occur in diode and MOSFET structures. Integrated circuit diode structures fail at the contact interface, silicon surface, or junction region. Human body model failure occurs in a metal oxide semiconductor field effect transistor (MOSFET) structure. Integrated circuit MOSFET structures failure occurs from MOSFET source-to-drain, or at the MOSFET gate. From HBM failures, typically, the failure is MOSFET source-to-drain failures [2, 3].

An example of an ESD protection network is known as a dual-diode network [3]. The dual-diode ESD network is a commonly used network for complimentary metal oxide semiconductor (CMOS) technology. A first p-n diode element is formed in an n-well region where the p-anode is the p-diffusion implant of the p-channel MOSFET device and the n-cathode is the n-well region connected to the power supply V_{DD} . This is sometimes referred to as the “up diode.” A second p-n diode element is formed in an p-well or p-substrate region

where the n-cathode is the n-diffusion implant of the n-channel MOSFET device, or the n+/n-well implant and the p-anode is the p-well region or p-substrate region connected to the power supply V_{SS} . This is sometimes referred to as the “down diode.” This circuit provides a “forward bias” ESD protection solution for positive and negative ESD pulse events to the two power rails V_{DD} and V_{SS} . An advantage of the dual-diode ESD network is that it is easily to migrate from technology generation to technology generation. In shallow trench isolation (STI) technology, this structure is scalable. A second advantage is that it has a low turn-on voltage of 0.7 V. A third advantage is that it can be designed with low capacitance, making it suitable for CMOS, advanced CMOS, and RF technologies. A fourth advantage is that it does not contain MOSFET gate dielectric failure mechanisms.

An example of a signal pin ESD network consisting of a grounded gate n-channel MOSFET device [3]. The grounded gate NMOS (also referred to as GGNMOS) ESD network is a commonly used network for complimentary metal oxide semiconductor (CMOS) technology. Typically, it is a n-channel MOSFET whose MOSFET drain is connected to the signal pin, and whose MOSFET source and gate are connected to the ground power rail. This circuit remains “off” in normal operation. When the signal pin exceeds the MOSFET snapback voltage, this circuit discharges to the V_{SS} power rail. When the signal pin is below the ground potential, the MOSFET drain forward biases to the p-well or p-substrate region. An advantage of the GGNMOS ESD network is that it is a natural scalable solution. As the technology scales, the MOSFET snapback voltage reduces, leading to an earlier turn-on of the MOSFET.

2.2. Charged device model (CDM)

The charged device model is an electrostatic discharge (ESD) test method that is part of the qualification of semiconductor components [4]. The charged device model (CDM) standard is supported by ESD Association as ANSI/ESD ESD-STM5.3.1-1999 [12]. Presently, there are four CDM test standard (ESDA S5.3.1, JEDEC JESD22-C101, AEC-Q100-011 Rev. C, and JEITA ED-4701-300). Each require different test platform, testing, waveform, and calibration requirements [4]. The charged device model (CDM) event is associated with the charging of the semiconductor component substrate and package. The charging of the package occurs through direct contact charging, or field-induced charging process (e.g. the field-induced charge device model (FICDM)).

There is presently an effort to align the CDM standards between the ESD Association and the JEDEC organization, by establishing a joint ESDA/JEDEC standard. The ESDA/JEDEC joint standard (JS-002 2014) will replace existing CDM ESD standards JESD22-C101 and ANSI/ESD S5.3.1. The new joint standard will preserve test systems in the field, and improve the waveform measurement process.

The charged device model (CDM) pulse is regarded as the fastest event of all the ESD events [4, 12–15]. Note that the CDM pulse waveform is influenced by the test platform and measurement metrology. The test platform is influenced by the field plate, field plate dielectric thickness and material type, and the probe assembly (e.g. test head, and ground plane). The metrology is influenced by the oscilloscope and verification module specifications.

First, the event is oscillatory. The CDM current pulse rise time is on the order of 250 ps, and with peak currents in the range of 10 A. The energy spectrum of the CDM pulse event extends to 5 GHz frequency. The CDM pulse waveform has a fast current pulse. The time scale of the CDM event is significantly lower than the thermal diffusion time; hence CDM events are in the “adiabatic regime” of a Wunsch-Bell power-to-failure curve [4].

In the calibration and verification procedure, the JEDEC standard requires a 1 GHz oscilloscope, whereas the ESDA standard requires 3 GHz [13]. Both standards today are bandwidth limited signal since the CDM waveform is faster than 1 GHz. These oscilloscopes were chosen based on availability at the time. It is well known that the energy spectrum of the CDM pulse waveform can extend into the 5 GHz frequency.

CDM event damage occurs in the semiconductor chip through the substrate. It can also occur through the power supply. Charge is stored on the package, and the substrate; then the power supply rapidly discharges through the grounded pin. The CDM failure mechanism can be small "pin-hole" in a MOSFET gate structure; this can occur in receiver networks, as well as metal interconnects.

The current path for charged device model (CDM) in components is significantly different from other electrostatic discharge (ESD) events. In the case of the charged device model (CDM), the package and/or chip substrate is charged through a power or ground rail. The component itself is charged slowly to a desired voltage state. As a result, the current flows from the component itself to the grounded pin during ESD testing. This is significantly from other ESD tests that ground a reference, and then apply an ESD event to a signal or power pin. As a result, the current path that a CDM event follows is from inside the component to pin that is grounded during test.

To avoid CDM failures of the MOSFET gate structure, an additional charged device model (CDM) ESD network is used [3]. The ESD network comprises of a first stage dual-diode network placed adjacent or in proximity of the signal pad. A second set of diodes (e.g. second stage network) are placed adjacent to the receiver circuit. A resistor is placed between the first and second stage. Three paths are possible for the CDM current from a charged ground rail (e.g. p-substrate) to the grounded receiver pin. For a positive charging of the substrate, the current flows from the substrate to any possible path that will reach the grounded signal pad node. A first path is through the n-channel MOSFET receiver circuit gate and to the second stage ESD diode. A second path is through the substrate to the second stage diode network. A third path is through the substrate to the first stage ESD network.

In the case of the first stage ESD protection circuit is far from the signal pad, the substrate resistance can be significant. For the third path, the total resistance from the grounded location to the grounded signal path is the sum of the substrate resistance and the ESD diode series resistance. In the case that the receiver network is adjacent to the second stage ESD network, the current will prefer to follow the second path instead of first path. When the impedance of the n-channel MOSFET receiver (e.g. Path A) is higher than resistance through the second path, the receiver gate structure can avoid rupturing of the MOSFET gate dielectric. To insure that the current flows through the second path through the second stage CDM ESD network, the circuit must be physically close to the receiver, and a low series resistance diode element.

3. Electrical overstress (EOS)

Electrical overstress (EOS) has been an issue in devices, circuit and systems for electronics for many decades, as early as the 1970s, and continues to be an issue today [1]. EOS failures are occurring at the device manufacturer, supplier, assembly and the field. In the electronic

industry, many products and applications are returned from the field due to “EOS” failure. To make progress in addressing the electrical overstress (EOS) issue, it is important to provide a framework for evaluation and analysis of EOS phenomena.

Electrical overstress (EOS) sources exist from natural phenomena, and power distribution [1, 14–25]. Switches, cables, and other power electronics that can be a source of electrical overstress. EOS sources exist in devices, circuits and systems. In the following sections, these issues will be discussed [1].

3.1. EOS design issues

Many of the electrical overstress (EOS) issues can occur from the design of the semiconductor component, the system and its integration. Examples of EOS source design issues are as follows [1]:

- Semiconductor process - application mismatch.
- Printed circuit board (PCB) inductance.
- Printed circuit board (PCB) resistance.
- Latchup sensitivity [5].
- Safe operating area (SOA) power rating violation.
- Safe operating area (SOA) voltage rating violation.
- Safe operating area (SOA) current rating violation.
- Transient safe operating area - di/dt and dv/dt .

Figure 2 illustrates the safe operating area (SOA) of a semiconductor device. There is a current limit, and a voltage limit on the borders of the SOA. At the corner of the SOA, the limitation is a thermal limit, and a second breakdown limit. Thermal limit has to do with the thermal limit of a device. The second breakdown limit has to do with second breakdown or thermal breakdown limit.

Testing and test simulation of devices, components and systems are an important part of the evaluation to electrical overstress (EOS) [4]. EOS test simulation is valuable part of understand EOS failures. EOS testing provides [1, 4]:

- Root cause analysis.
- Replication of failure signature.
- Technology EOS hardness evaluation.
- Technology benchmarking.
- Component reliability qualification.
- System qualification.

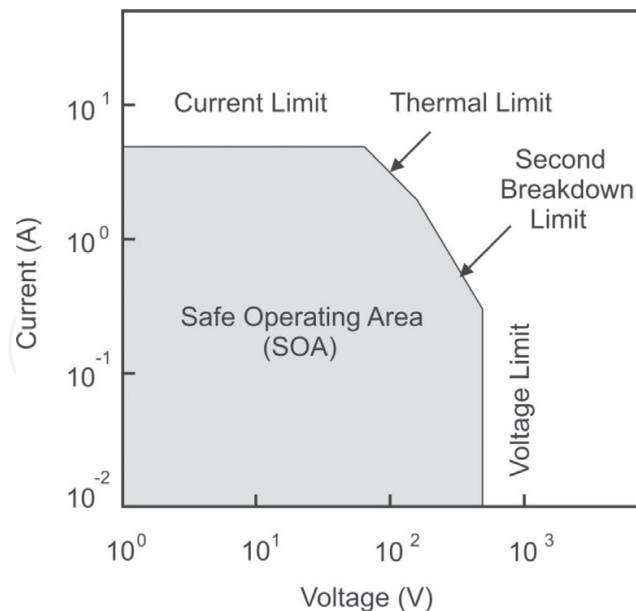


Figure 2. Safe operating area (SOA).

Field returns occur in all electronic components independent of the technology generation and period of time of evaluation. One of the key difficulties in the semiconductor industry is the ability to track, record and maintain a database of these field failures.

EOS events do not have a characteristic time response. EOS events are typically slower, and distinguishable from ESD events by having longer characteristic times. The time constant for EOS events range from sub-microseconds to seconds.

Electrical over-voltage (EOV), electric over-current (EOC), and electrical over-power (EOP) can lead to failure mechanisms; these can lead to melted packages, blown single component capacitors and resistors, ruptured packages, blown bond wires, cracked dielectrics, fused and melted metal layers, and molten silicon.

The failure analysis process can comprise of the following steps:

- Information gathering.
- Failure verification.
- Failure site identification and localization.
- Root cause determination.
- Feedback of root cause.
- Corrective action.
- Documentation reports.

3.2. EOS failure mechanisms

Visual external or internal inspection can be applied to evaluate EOS failure mechanisms. Visual damage signatures can include the following:

- Package lead damage.
- Foreign material.
- Cracks.
- Package discoloration.
- Corrosion.

Visual damage can also be evaluated from internal inspection. For internal inspection, the following visual damage signatures are:

- Melted metallurgy.
- Cracked inter-level dielectrics.
- Molten silicon.

There are certain categories of failures that electrostatic discharge (ESD) does not typically cause, and EOS events do cause. Failures that typically are caused by EOS phenomena but not ESD are as follows [1]:

- Printed circuit board (PCB) damage.
- Package molding damage.
- Package pin damage.
- Wire bond damage.

Today, electrical overstress (EOS) is still an issue in today's electronic systems. To address electrical overstress in systems, electrical overstress (EOS) protection device are added to printed circuit boards (PCB), cards, and systems. The integration of EOS protection devices into systems.

3.3. EOS protection devices

Electrical overstress (EOS) protection devices are supported by a large variety of technologies. Although material and operation may differ between the EOS protection devices, their electrical characteristics can be classified into a few fundamental groups [16–25].

EOS protection networks can be identified as a voltage suppression device, or as a current-limiting device. The voltage suppression device limits the voltage observed on the signal pins or power rails of a component, preventing electrical over-voltage (EOV). The current-limiting device prevents a high current from reaching sensitive nodes, avoiding electrical over-current (EOC) [1].

Voltage suppression devices can also be sub-divided into two major classifications [1]. Voltage suppression devices can be segmented into devices that remain with a positive differential resistance, and those that undergo a negative resistance region. For positive differential resistance,

these devices can be referred to as “voltage clamp” devices where dI/dV remains positive for all states; for the second group, there exists a region where dI/dV is negative. The first group can be classified as “voltage clamp devices” whereas the second group can be referred to as an “S-type I-V characteristic device”, or as a “snapback device.” In the classification of voltage suppression devices, the second classification can be associated with the directionality; a voltage suppression device can be “uni-directional” or “bidirectional.”

The choice of electrical overstress (EOS) device to use in an application is dependent on the electrical characteristics, cost, and size. The electrical characteristics that are of interest are the breakdown voltage, and the forward conduction [1].

The types of voltage suppression devices used electrical overstress (EOS) are Transient Voltage Suppression (TVS) Diodes [22], Thyristor devices, Varistor devices [21], Polymer Voltage Suppression (PVS) devices, and Gas Discharge Tube (GDT) devices [23].

Current-limiting devices can be used in a series configuration for electrical overstress (EOS) protection. EOS current-limiting devices can be as follows [16–24]:

- Resistors.
- Resetting fuses.
- Non-resetting fuses.
- eFUSE.
- Positive temperature coefficient (PTC) devices.
- Circuit breakers.

The choice of the current-limiting EOS protection device is a function of the cost, size, rated current, time response, I^2t value, rated voltage, voltage drops, and application requirements.

Diodes are uni-directional type EOS structure, but can be utilized in a forward or reverse breakdown mode of operation for a voltage limiting EOS solution [1]. Schottky diodes are also commonly used uni-directional electrical overstress (EOS) protection device [1]. Schottky diodes have a forward conduction state, and reverse blocking state. Schottky diodes have a lower forward turn-on (e.g. 0.35 V) compared to standard silicon p-n junction (e.g. 0.7 V). For electrical overstress, Schottky diodes are mounted on printed circuit board (PCB) by soldering in the leads through vias, or surface mount. Schottky diodes are not as commonly used within components to provide electrostatic discharge (ESD) protection due to lack of availability. Schottky diodes are uni-directional type EOS structure, but can be utilized in a forward or reverse breakdown mode of operation for a voltage limiting EOS solution. Zener diodes are also used as a uni-directional electrical overstress (EOS) protection device [1].

Zener diodes are used for electrostatic discharge (ESD) protection for high voltage and power applications. Zener diodes are not used for ESD protection for low voltage CMOS applications. For electrical overstress (EOS) single component Zener diodes are mounted on printed circuit board (PCB) through vias, or surface mount. Zener diodes are uni-directional type EOS

structure, but can be utilized primarily in reverse breakdown mode of operation for a voltage limiting EOS solution.

Zener diodes are used uni-directional electrical overstress (EOS) protection device. Zener diodes are typically used as a voltage clamping EOS protection device, and typically used in the breakdown state. Schottky and Zener diodes can both be integrated into a given application.

An EOS protection device used for high voltages is the varistor. A varistor is also known as a voltage dependent resistor (VDR). The varistor element behaves like a diode, forming a non-linear current-voltage (I-V characteristic).

Another EOS protection device is the metal oxide varistor (MOV) device; this is the most common varistor composition [1, 21]. Zinc oxide, combined with other metal oxides are integrated between two metal electrodes. Metal oxide varistors can also include bismuth, cobalt, and manganese. The operation of the MOV device is based on conduction through ZnO grains; current flows “diode-like” through the grain structures creating a low current flow at low voltages. At higher voltages, the current flow is dominated by a combination of thermionic emissions and tunneling. This diode-like behavior forms the diode-like characteristic provides the high resistance/low voltage state, and the low resistance/high voltage state. An advantage of the MOV structure is it has a high trigger voltage, making it suitable for EOS protection in power electronics (e.g. 120–700 V applications) [1, 21]. The disadvantage of these elements is that it has high capacitance, high on-resistance, high trigger voltage, and variability of the device response (e.g. on-resistance and clamping voltage) in the MOV device characteristics. Key device parameters of varistor are the energy rating, operating voltage, response time, maximum current and breakdown voltages.

Gas discharge tubes (GDT) devices can be used to avoid electrical overstress (EOS) in systems [1, 23]. Gas discharge tubes (GDT) are bidirectional, allowing for protection for both positive and negative EOS events. GDT elements are suitable from surge protection. GDT devices have high trigger voltages (unless used as a first stage followed by other low voltage secondary EOS solutions) [1].

Gas-filled tubes (GDT) utilize electrical discharge in gases. An applied voltage initiates the device by ionizing the electrical gas, followed by electrical glow discharge, and an electrical arc. With creation of an electrical arc, the GDT device becomes a low resistance shunt for EOS protection. These gas-filled tubes can contain hydrogen, deuterium, and noble gases (e.g. helium, neon, argon, krypton, and xenon). GDT devices can vary their electrical characteristics by choices of the gas type, pressure, electrode design, and spacings.

GDT devices undergo three states: (1) electrical breakdown, (2) glow discharge, and (3) electrical arc [1, 23]. The electrical breakdown is a high voltage low current state prior to triggering of the GDT device. A glow discharge region forms a second state which incorporates a low current high voltage state. Lastly, after full ionization of the gas, a low voltage high current state occurs with a low “on-resistance.”

GDT devices have high trigger voltages suitable for LDMOS power electronic applications to HV LDMOS (e.g. 120 V), and UHV LDMOS applications (e.g. 600–700 V) [1, 23]. These devices are used in a number of high voltage switch devices, such as ignitrons, krytrons, and thyratrons.

One of the disadvantages of the GDT devices is the slow turn-on times typically in the micro-seconds. An example of some of the electrical characteristics can exhibit d.c. breakdown from 75 to 600 V, with a single surge response of 40 kA in 10–20 s, or multiple surges of magnitude of 20 kA.

The electrical circuit breaker is used in industrial, commercial, and residential electrical systems for high currents. Electrical circuit breakers have issues of physical size, weight, cost, and time response. Circuit breakers can be used to protect household appliances, and large scale switchgear high voltage circuits. The circuit breaker is an electrical switch designed for the purpose of electrical over-current events, short circuits, or fault detection. Circuit breakers are typically “tripped” by the high current event, and can be manually reset. The concept of the circuit breaker was invented by Charles Grafton Page, in 1836 [17].

A class of circuit breakers is the thermal-magnetic circuit breaker [1]. Thermal-magnetic circuit breakers are used to avoid “short-circuit” currents. Thermal-magnetic circuit breakers are sensitive to temperature. Thermal-magnetic circuit breakers contain a bi-metal switch and an electromagnet. The bi-metal switch provides over-current protection. During current over-load, the bi-metal switch heats up, leading to bending of the element. The electromagnet responds to short-circuit currents [1].

Power controllers are used for low power and low voltage applications; power controllers typically are low voltage high efficiency products that can carry amperes of current per channel. Buck-converters use over-current protection logic and networks; over-current functions protect the switching converter from an output short by monitoring current flow in the application. Hence, in power applications, it is possible to integrate electrical over-voltage (EOV) and electrical over-current (EOC) within a component design. Many analog and power applications also contain thermal protection networks as well to avoid thermal runaway and EOS damage.

4. Challenges in the future

Future challenges exist in improve reliability and safety in components and systems due to electrostatic discharge (ESD) and electrical overstress (EOS). Challenges include the following:

- Achieving EOS and ESD standards protection levels in future technology generations.
- Maintaining chip and system level performance objectives without lowering of ESD and EOS protection levels.
- Electronic system failure from CMOS latchup in scaled future technology.
- Electronic system failure from overheating in handheld and portable devices.

5. Conclusions

In conclusion, ESD and EOS failures occur in devices, components and systems in electronics in the past, and in the future with the introduction of both single component to VLSI technology.

Significant advancements have been made in the understanding of failure mechanisms, as well as solutions to address them have been applied in semiconductor electronics.

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