We are IntechOpen,
the world's leading publisher of
Open Access books
Built by scientists, for scientists

6,900
Open access books available

185,000
International authors and editors

200M
Downloads

154
Countries delivered to

Our authors are among the

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS
BOOK CITATION INDEX
INDEXED

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

Sequential Selective Harmonic Elimination and Outphasing Amplitude Control for the Modular Multilevel Converters Operating with the Fundamental Frequency

Alexey Tyshko

Additional information is available at the end of the chapter

Abstract

With the growing use of DC voltage for power transmission (HVDC) and DC links for efficient AC motor drives, the R&D efforts are directed to the increase of DC/AC converter's efficiency and reliability. Commonly used DC/AC converters, based on the carrier-frequency pulse-width modulation (PWM) to form a sinusoidal output voltage with a low level of higher harmonics, have switching time and switching loss issues. The use of multimodule multilevel converters (MMC), operating with the fundamental switching frequency and phase-shift control to form the ladder-style output voltage, reduces switching losses to minimum while keeping the low level of higher harmonics in the output voltage. The discussed sequential harmonic elimination method for MMC, using identical power modules operating with 50% duty cycle and fundamental frequency, is based on the combination of the multiple fixed phase shifts to form a ladder-style sinusoidal voltage with low total harmonic distortion (THD) and symmetrical variable phase shifts to control the output voltage amplitude. The principles of the sequential selective harmonic elimination for MMC topology and amplitude control are described with two examples. The first example is the industrial-frequency DC/AC converter complying with THD requirements of IEEE 519 2014 standard without the output filter. The second example is a high-frequency converter, used as a transmitter, loaded with the resonant antenna, where the evaluation criteria are decreasing of the transmitter losses and increasing of the reliability or life expectancy at elevated temperature.

Keywords: amplitude control, selective harmonic elimination, staircase modulation, Chireix-Doherty amplitude modulation, DC/AC converter, high temperature, multimodule multilevel converter (MMC), multivector control, outphasing, phase-shift modulation, reliability, life expectancy

1. Introduction

The conversion of DC voltage into sinusoidal AC voltage at power levels from kilowatts to megawatts with low power losses and low higher harmonics in the output voltage is a common task for modern power engineering. Multimodule multilevel converter is the best approach to generate the high-power sinusoidal voltage from HVDC bus for electrical grid consumers, propulsion electrical motor drives, etc. High-efficiency switch-mode modules, used to synthesize sinusoidal output voltage, may operate at the fundamental frequency of the sine voltage, required for the load, or at higher frequencies (the carrier frequency) using the pulse-width modulation to reduce higher harmonics of the fundamental frequency. In the last case, the output filters, required for reducing total harmonic distortion (THD) of the output voltage to the acceptable level, are significantly smaller [1–20].

The biggest problem with the phase-shift pulse-width modulation, providing the highest quality of the output sinusoidal voltage with minimum switching losses, is its control methodology, which requires complicated calculation of the necessary phase shifts in real time [8, 21, 22].

In this paper a simple method of the sequential selective harmonic elimination and amplitude control is discussed. It is based on the combination of the fixed precalculated phase shifts/ delays for harmonic elimination and variable phase shift for amplitude control. Application of this method is illustrated using two examples—the industrial-frequency DC/AC converter and the high-frequency converter used as a transmitter for the nuclear magnetic resonance (NMR) oil/gas well logging tool, operating in harsh conditions. LTspice was used for simulation in time and frequency domains. A simple expression is provided for the resulting THD vs. the number of eliminated harmonics to comply with industrial grid voltage of THD standards without the output filter. For the NMR transmitter, decreasing of conductive losses due to the harmonic elimination reduces operating temperature and increases the reliability. Improvement of the life expectancy is calculated according to the Arrhenius equation for three transmitter cases with the same number of switches but with different harmonic contents.

2. Full-bridge module operation and spectrum of the output voltage

The building block or module for multimodule multilevel converter (MMC) is a full-bridge DC/AC converter utilizing maximum voltage and current ratings of the power switches S1–S4 (**Figure 1**), powered from bus V_0, producing rectangular voltage pulses with 50% duty cycle
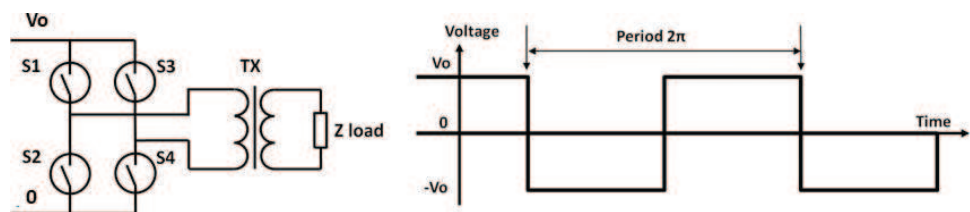

Figure 1. Full-bridge stage and output voltage waveform.

for maximum output power. The bridge load Z is connected directly to the bridge outputs or via the output transformer TX. For the industrial frequency 50 Hz–60 Hz and other low-frequency high-power applications, fully controlled thyristors are the best choice, while for the frequency range over few kilohertz, IGBTs are the preferred ones. Operation in the frequency range over 100 kHz requires fast-switching power MOSFETs. To simplify analysis of the following circuits, the switches are assumed to be ideal and have zero-switching time and zero internal losses.

The Fourier analysis provides the expression for the full-bridge symmetrical 50% duty cycle output voltage $V_{out(t)}$ (**Figure 1**) as the sum of only odd harmonics V_n (n = 1, 3, 5, 7, etc.):

$$V_{out(t)} = \frac{4\,V_0}{\pi} \sum_{n=1} \frac{\cos n\omega t}{n} \tag{1}$$

where n is the harmonic number (only odd harmonics 1, 3, 5, etc.), ω is the angular frequency, V_0 is the full-bridge inverter DC bus voltage and t is time.

Each harmonic n has its amplitude V_n decreasing with the harmonic number n:

$$V_n = \frac{4\,V_0}{\pi n} \tag{2}$$

Spectrum of the bridge output voltage with amplitude of 1 V and frequency of 1 kHz is shown on **Figure 2**. The vertical axis represents the RMS values of each harmonic starting with the first one equal to 0.9Vrms (or 1.273 V peak value). Horizontal axis is frequency.

Converter output current $I_{out(t)}$ is a combination of the fundamental harmonic and higher harmonics, each of them being a product of the harmonic voltage $V_{n(t)}$ and load admittance Y_n for this harmonic:

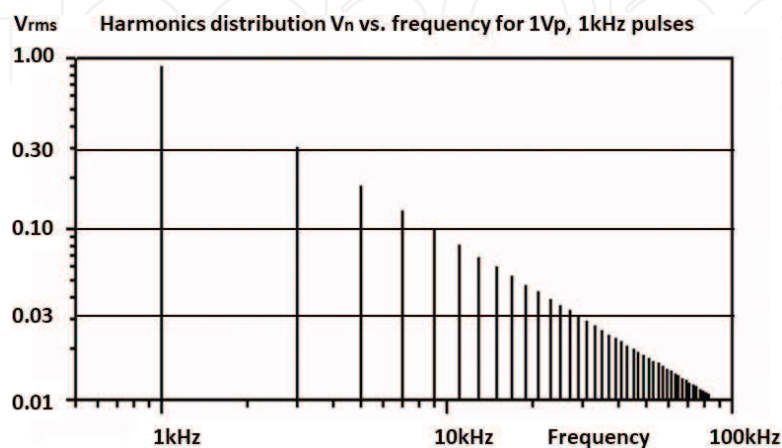$$I_{out(t)} = \sum_{n=1}^{\infty} V_{n(t)}\, Y_n \tag{3}$$

Figure 2. Spectrum of the 1 kHz 50% duty cycle signal.

Several load types such as resistive, inductive, capacitive and resonant ones have different current vs. frequency characteristics as shown in **Figure 3**, which is obtained in LTspice environment under 1 V sinusoidal test signal.

Only resistive load current replicates the spectrum of the input voltage. Inductive load decreases high-frequency current components, but capacitive and resonant loads significantly increase relative values of the high-frequency current harmonics compared to the spectrum of the applied voltage. Voltage harmonics and resulting currents affect both load and voltage sources (converter) in different ways. Excessive current harmonics increase power losses and create electrical noise (EMI) affecting electronic equipment.

Maximum voltage harmonic content for the industrial AC lines is regulated by IEEE 519 2014 standard [23, 24]. Limits for total harmonic distortion (THD) and maximum amplitude of the highest harmonic are provided in **Table 1**.

THD and individual harmonic maximum values are different for different line voltages. The power distributor should keep total harmonic distortion (THD) for voltages <1 kV under 8% and individual harmonic value less than 5% of the fundamental one at the point of consumer connection (PCC). In the process of conversion of HVDC bus voltage into lower-level AC, the switch-mode converters create higher harmonics as unwanted byproduct. For full-bridge DC/AC converter output voltage spectrum (**Figure 2**) of THD is 0.483 or 48.3% [25]. To comply with THD limits, the simple DC/AC converters include the output filters reducing higher harmonics to the acceptable level. Those filters introduce additional losses and have significant size, weight and cost especially if the filter has to remove harmonics starting with the third one,
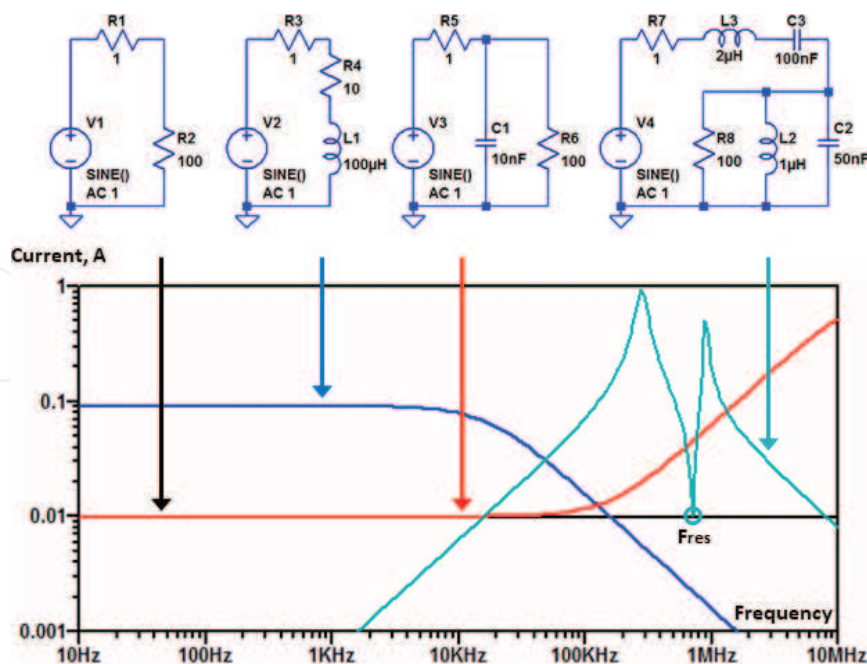

Figure 3. Load current vs. frequency for different loads.

Bus voltage (V) at PCC	Individual harmonic (%)	Total harmonic distortion (THD) (%)
V ≤ 1.0 kV	5.0	8.0
1 kV < V ≤ 69 kV	3.0	5.0
69 kV < V ≤ 161 kV	1.5	2.5
161 kV < V	1.0	1.5

High-voltage systems can have up to 2% THD where the cause is an HVDC terminal where effects will have attenuated at the point in the network where future users may be connected.

Table 1. Voltage distortion limits.

which is 150 Hz and 180 Hz for the EU and USA, respectively. Eliminating the most powerful higher harmonics from the output voltage in the process of DC to AC conversion and reducing the highest-frequency harmonic leftovers with a simple output filters are the most efficient ways to comply with THD standard.

For the high-frequency converters operating as transmitter with the resonant loads at elevated temperature, the output current's higher harmonics cause additional heating, which results in the reliability problems. In this case the effectiveness of the harmonic elimination is reducing the power component temperature and increasing the converter life expectancy.

3. Multimodule converters and synthesis of the quasi-sinusoidal output voltage

Multimodule multilevel converters (**Figure 4**) have their outputs connected in series to produce the so-called modified sinusoidal voltage or ladder-style voltage (**Figure 5**). DC inputs may be connected in parallel with the transformer combining the output voltages or in series for HVDC
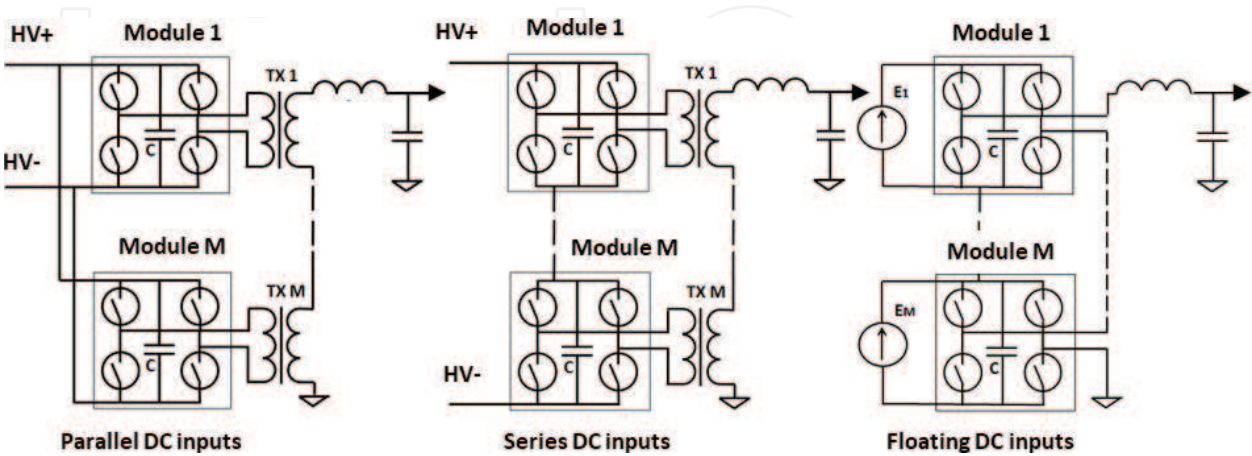

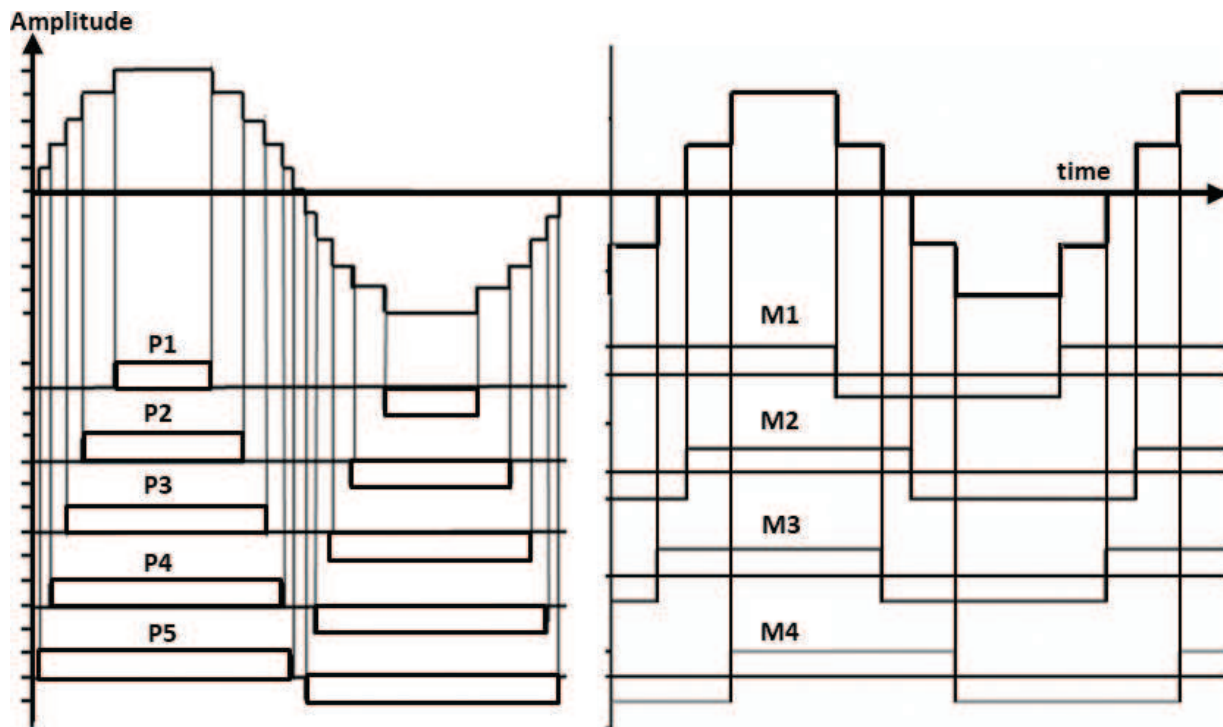**Figure 4.** Multimodule converters with different DC line feeds.

Figure 5. Forming ladder-style voltage using PWM (left) and phase shift only (right).

converters or be floating, for example, powered from the photovoltaic batteries, depending upon the application. Each module operates with high efficiency producing rectangular pulses with controlled timing. The control algorithm for timing calculations is a subject of this analysis.

Commonly used control algorithms are based on the pulse-width modulated signals to control multiple modules. The module output voltages are added in series to form the ladder-style voltage with optimized width of each pulse to eliminate harmonics and to regulate output voltage as shown in **Figure 5** (left). The discussed method was developed to operate the identical modules, producing 50% duty cycle pulses with the fundamental frequency and equal amplitude, combining their outputs in series and controlled by the phase shift only (**Figure 5**, right).

Equal ON and OFF time operation of all power switches has the following advantages:

a) Equal conductive losses

b) Guaranteed time to reset snubbers (if used to reduce switching losses)

c) Guaranteed time to build up the lagging current for soft switching (if needed)

d) Guaranteed time to recharge gate drivers (if needed)

4. Harmonic elimination based on the phase shift

Minimal configuration of the DC/AC multimodule converter includes two basic full-bridge modules with the output voltages connected in series. Their DC inputs may be connected in

parallel to the same bus V_0 or in series (this is used for HVDC lines to share input DC voltage according to the module maximum voltage rating).

To simplify analysis two identical modules are connected to the same DC bus, and their outputs are connected in series using two ideal output transformers TX1 and TX2 with transformer ratio 1:1 (**Figure 6**). The output voltages have identical amplitude and 50% duty cycle, and their relative position in time domain (delay or phase shift) is defined by the controller (not shown).

The relative phase shift (relative to the fundamental harmonic) equal to $\pi/3$ or 1/6 of the module operation period is shown in **Figure 7**. For the third harmonic, the relative phase shift is π, and combined output signal has the third harmonics subtracted or eliminated. All other odd harmonics like 9th, 15th, 21st, 27th, etc., which are multiples of three, are eliminated too.

Two identical periodic signals being combined with the phase shift Φ have eliminated harmonics n satisfying the following requirement:

$$\Phi = \frac{\pi}{n} \tag{4}$$

Two module output voltages shifted $\pi/3$ and combined output without 3rd, 9th, etc. harmonics are shown in **Figure 8**. When two signals with eliminated 3rd harmonic are added with phase shift $\pi/5$, their combined voltage has eliminated the 5th harmonic and also 15th, 25th, etc. To eliminate the fifth and seventh harmonics, this process should be repeated as shown in **Figure 9** where control signals to a set of eight modules are getting additional delay starting from sync pulse. This process may be continued to eliminate enough harmonics to comply with THD requirements or other special conditions [26–31].

Total delays (or phase shift) α_m per module m of a set of modules M (**Figure 9**) may be calculated as scalar product of matrix C formed by assigned to each module m binary numbers (c = m-1) of the modules and set Φ of harmonic canceling delays $\phi = \pi/n$:
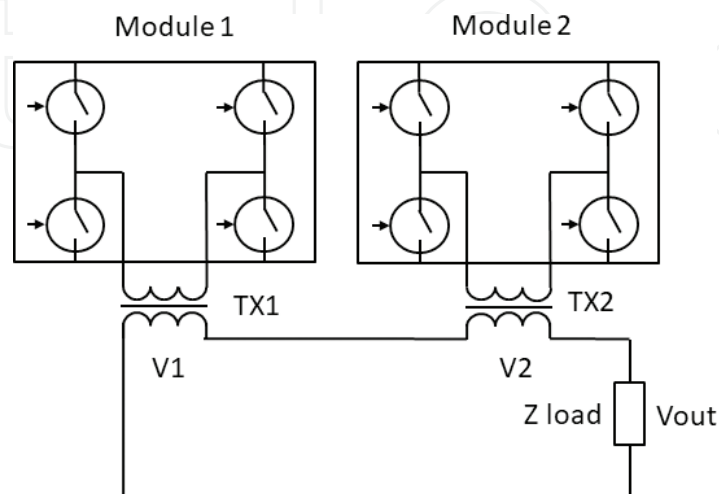
$$\alpha_m = [c_m] \cdot [\varphi] \tag{5}$$

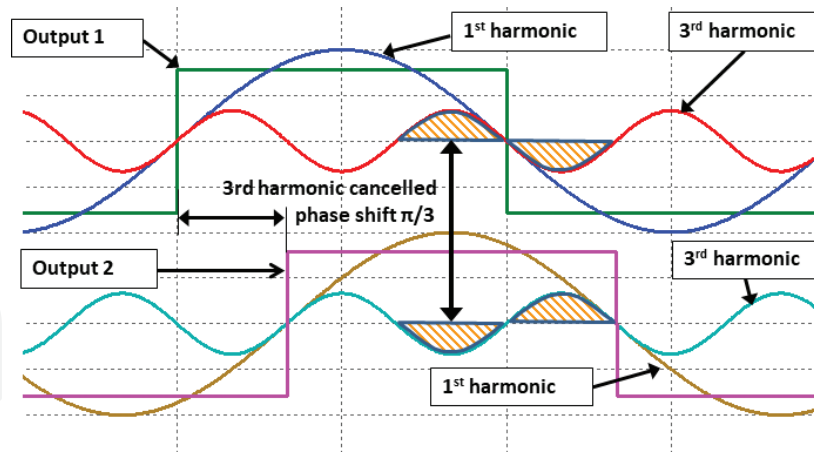**Figure 6.** Two module converter.

Figure 7. Third harmonic canceling.

Examples of delay/phase-shift calculation for the eight modules of MMC are provided in **Table 2**.

Number M of modules, needed for eliminating K harmonics

$$M = 2^K \tag{6}$$

To find THD dependence on the sequential selective harmonic elimination using phase shift, seven harmonic elimination circuitries with different numbers of modules, marked A to G, were simulated. Example of circuitry topology marked as A, B, C and D, reference A full-spectrum single module and with eliminated third (B-2 modules), third and fifth (C-4 modules) and third, fifth and seventh (D-8 modules) harmonics are provided in **Figure 10**. More complicated circuits (E-16 modules, F-32 modules and G-64 modules) were also simulated.

THD for each simulated case (A to G) was calculated based on the RMS value of the simulated output ladder-style voltage V_{out} and RMS value of the fundamental harmonic V_1 [25]:

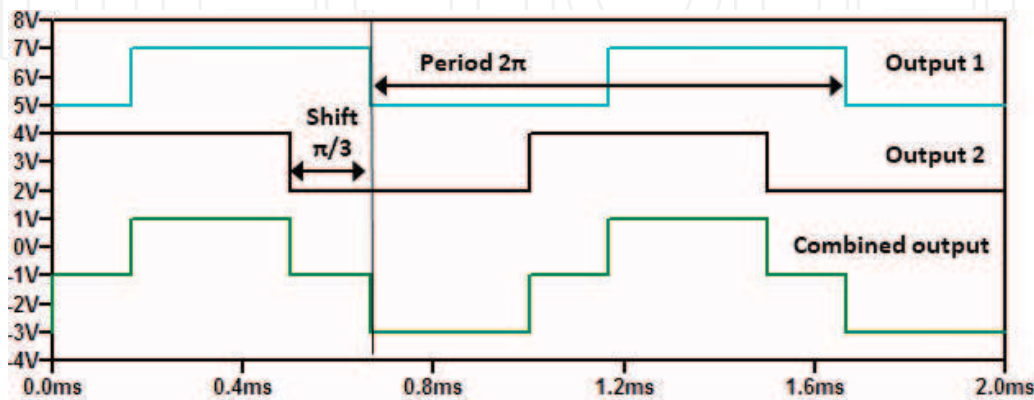$$THD = \frac{\sqrt{V_{out}^2 - V_1^2}}{V_1} \tag{7}$$

Figure 8. Forming ladder voltage with two modules with canceled the third harmonic.
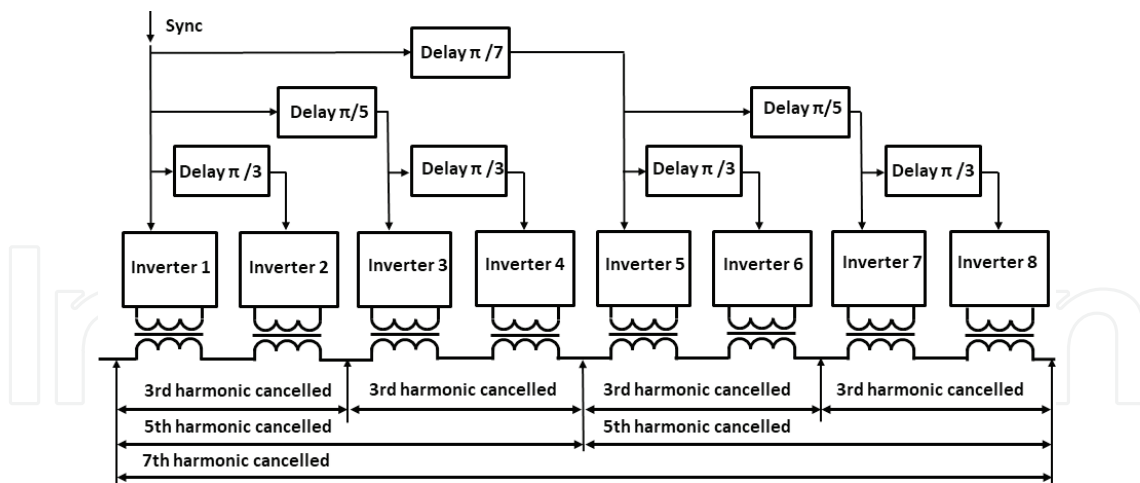
Figure 9. Topology for canceling the third, fifth and seventh harmonics.

The drawback of any kind of modulation is decreasing of the resulting fundamental harmonic V_1. **Table 3** provides not only THD and maximum value of the biggest voltage harmonic left after multiple harmonic eliminations but also a change of the fundamental harmonic compared to expected value in case of all phase shifts, which were zero, and combined output voltage replicates 50% duty cycle output voltage of the single module multiplied by the number of modules.

THD value vs. the number of eliminated harmonics starting from the third from Cases A to G is presented in **Figure 11**. The relative amplitude of the fundamental harmonic $V_{1,k}$ after the first k higher harmonics are eliminated is calculated as

$$V_{1,k} = \frac{4 V_0}{\pi} \prod_{n=3}^{k} Sin\left\{ \frac{\pi}{2}\left(1 - \frac{1}{n}\right) \right\}$$

(8)

Module number (m)	Module's assigned binary code ($c_m = m-1$)	nth harmonic phase shift in module ($\varphi_n = \pi/n$)			Total module phase shift ($\alpha_m = c_m \cdot \Phi$)	Total module phase shift (α_m)
		n = 7	n = 5	n = 3		
1	0 0 0	0	0	0	0	0
2	0 0 1	0	0	φ_3	φ_3	$\pi/3$
3	0 1 0	0	φ_5	0	φ_5	$\pi/5$
4	0 1 1	0	φ_5	φ_3	$\varphi_5 + \varphi_3$	$\pi/5 + \pi/3$
5	1 0 0	φ_7	0	0	φ_7	$\pi/7$
6	1 0 1	φ_7	0	φ_3	$\varphi_7 + \varphi_3$	$\pi/7 + \pi/3$
7	1 1 0	φ_7	φ_5	0	$\varphi_7 + \varphi_5$	$\pi/7 + \pi/5$
8	1 1 1	φ_7	φ_5	φ_3	$\varphi_7 + \varphi_5 + \varphi_3$	$\pi/7 + \pi/5 + \pi/3$

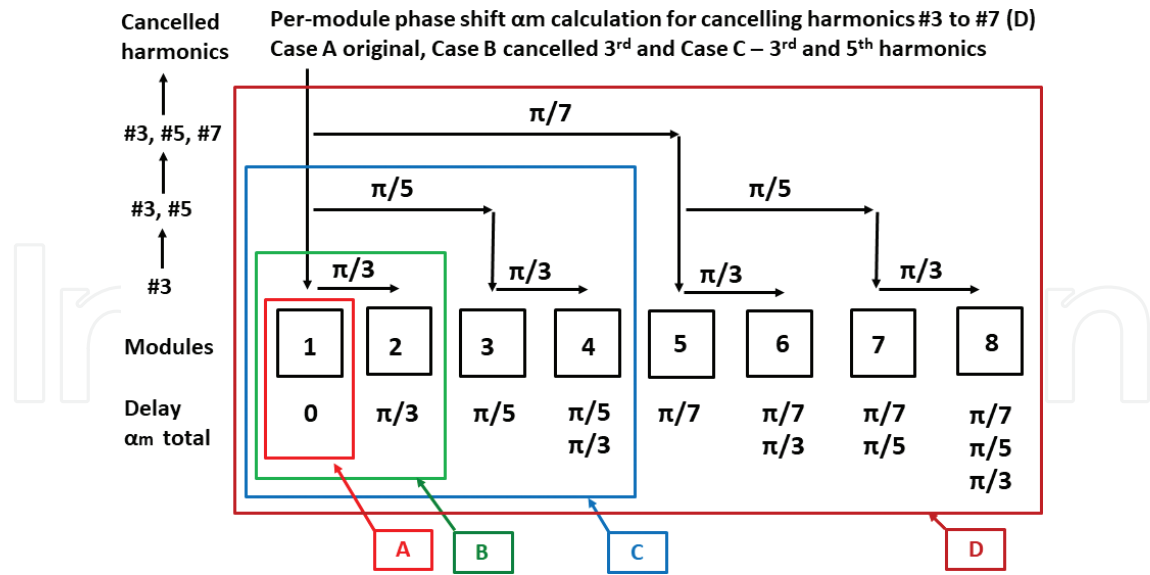**Table 2.** Phase shift per module calculation.

Figure 10. Harmonic elimination topology and phase-shift control.

Multimodule converter with eliminated the first four harmonics (Case E, 16 modules) complies with IEEE 519 2014 [23] requirements for voltage <1 kV, with five eliminated harmonics (Case F) for 1 kV to 69 kV and with six eliminated harmonics (Case G) from 69 kV to 161 kV without using any output power line filters. Eq. (9) may be useful for approximate calculation of THD of the MMC output voltage after canceling the first k harmonics using this method:

$$THD_k \approx 0.5 * e^{-0.5k} \tag{9}$$

Configuration	A	B	C	D	E	F	G
Number of modules	1	2	4	8	16	32	64
Harmonics canceled +	0	3	5	7	11	13	17
Phase shift per next module set	0	$\pi/3$	$\pi/5$	$\pi/7$	$\pi/11$	$\pi/13$	$\pi/17$
Relative change of the first harmonic	1.0000	0.8660	0.9511	0.9749	0.9898	0.9927	0.9957
Combined output value (Vrms)	1.0000	0.8165	0.7528	0.7278	0.7167	0.7108	0.7076
First harmonic k value V_1 (Vrms)	0.9003	0.7798	0.7415	0.7229	0.7156	0.7103	0.7074
THD	0.4834	0.3103	0.1752	0.1166	0.0575	0.0360	0.0238
Max higher harmonic number	3	5	7	11	17	29	29
Max harmonic value (Vrms)	0.3001	0.1559	0.0658	0.0526	0.0160	0.0127	0.0113
Max harmonic relative to the first harmonic	0.3333	0.1999	0.0887	0.0728	0.0224	0.0179	0.0160

Table 3. Simulation results for voltage THD and maximum high harmonic left.
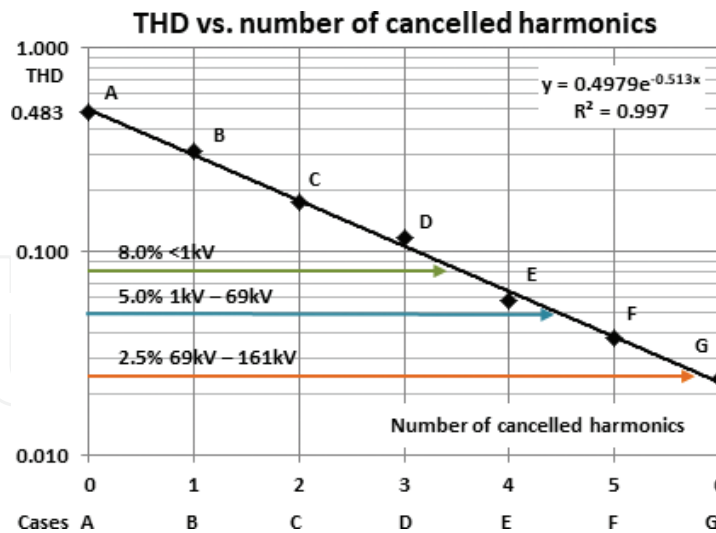
Figure 11. Voltage THD vs. the number of canceled harmonics starting with the third one.
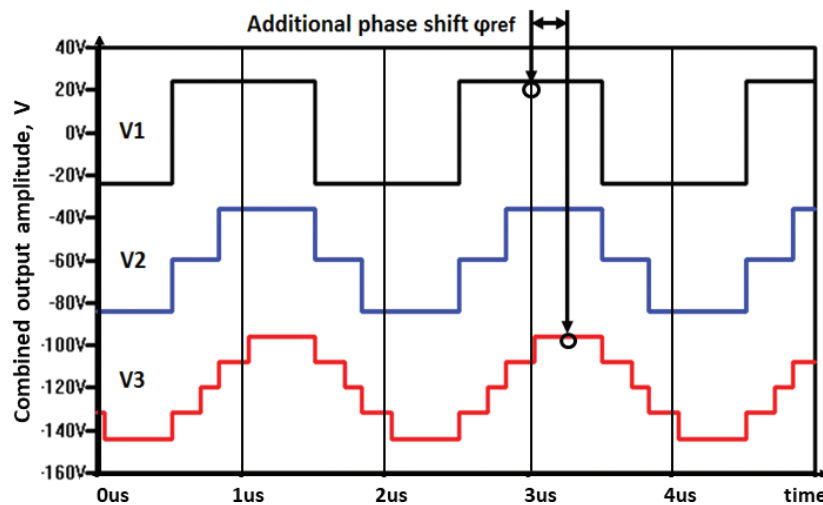

Figure 12. Buildup of the output voltage additional phase shift (case C vs. case a).

Due to the buildup of the module output voltage phase shifts, the resulting quasi-sinusoidal voltage fundamental harmonic is shifted to φ_{ref} as shown in **Figure 12** which should be taken into consideration and if necessary added to the carrier signal.

The additional phase-shift value φ_{ref} is calculated for MMC with M modules as

$$\varphi_{ref} = \frac{1}{2}\sum_{m}^{M}\alpha_m \tag{10}$$

5. Amplitude control

MMC with fixed phase shifts produces low THD sinusoidal output voltage with the amplitude proportion to the DC bus voltage. To regulate the output voltage amplitude from zero to maxi-

mum without affecting the harmonic elimination results, two identical voltages V1 and V2 have to be combined with the variable symmetrical phase shift [32, 33] (**Figure 13**).

The variable phase-shift symmetry maintains stable phase of the resulting output voltage at the load during the amplitude regulation. This method (also known as outphasing) was originally developed for AM transmitters and assumed two sinusoidal combining voltages, now widely used for high-efficiency communication transmitters [34]. The amplitude of the combined output voltage *Vc* depends upon the phase shift φ as shown on phasor diagram (**Figure 13**):

$$V_c = 2\,V_0\,Sin\varphi \tag{11}$$

For the high-power applications, the switch-mode converters are used instead of the sine generators (**Figure 14**) where two sets of power modules Mod A and Mod B are controlled from two multiple outputs of fixed delay modules A and B. Delay modules may be shift registers or digital delay lines (for RF transmitters). Inputs of delay lines controlling leading vector A and lagging vector B are connected to the outputs of symmetrical phase-shift modulator with amplitude control voltage and sinusoidal carrier voltage inputs. The shown output transformers are the simplest way to combine output voltages and to form regulated output. For power conversion with the strict requirements to the harmonic content of the regulated sinusoidal voltage at the output, each of two DC/AC converters shall comply with those requirements, and the number of modules is chosen based in **Figure 11** data.

Sinusoidal carrier voltage (not triangular or sawtooth voltage) provides linear modulation characteristic for the resulting fundamental harmonic, which allows direct control of the RF output pulses restored at the resonant antenna without the real-time negative feedback. In some cases the correction of the total system gain depending on the DC bus voltage may be done between RF pulses [29].
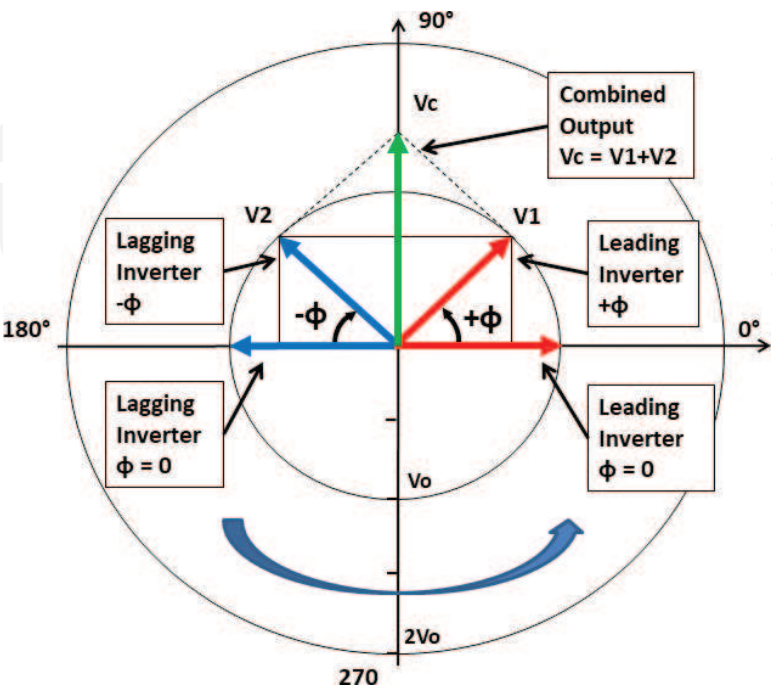

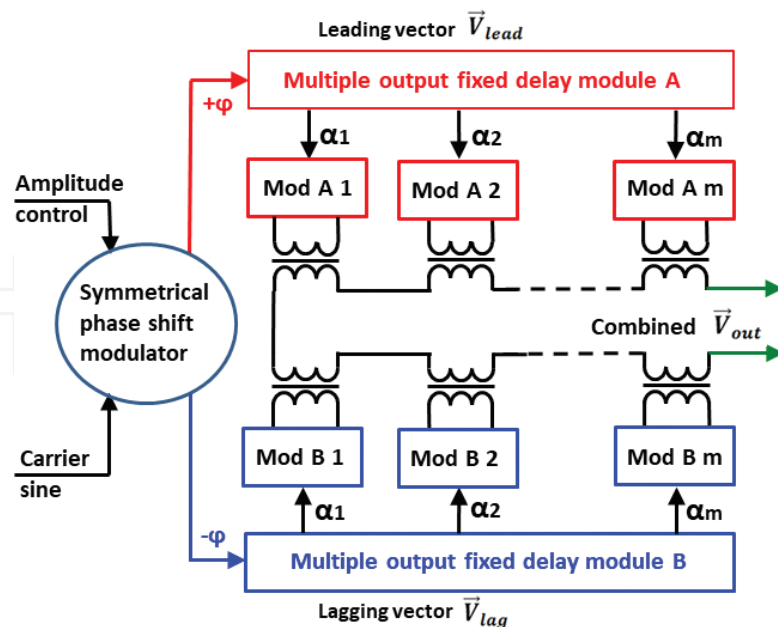**Figure 13.** Outphasing modulation phasor diagram for the fundamental harmonic.

Figure 14. DC/AC multimodule multilevel converter with outphasing amplitude control.

6. RF transmitter current harmonics and life expectancy

The simplified schematic of the two module switch-mode outphasing transmitters is shown in **Figure 15** [35]. Two full-bridge converters, named leading and lagging, have their output voltages combined using their output transformers TX1 and TX2. The load is a resonant antenna consisting of the antenna inductor La, parallel-tuned capacitor Ca and resistor Ra representing antenna losses and defying antenna Q. The load impedance has its maximum at the operating frequency of the parallel resonance equal to Ra. For the higher harmonics of the output voltage, antenna impedance is capacitive and drops at higher frequency. Higher harmonics of the transmitter output current are limited by the output filters Lf and Cf. This filter is tuned to the series resonance at the operating frequency to introduce minimum output filter voltage drop which is proportional to the output current.
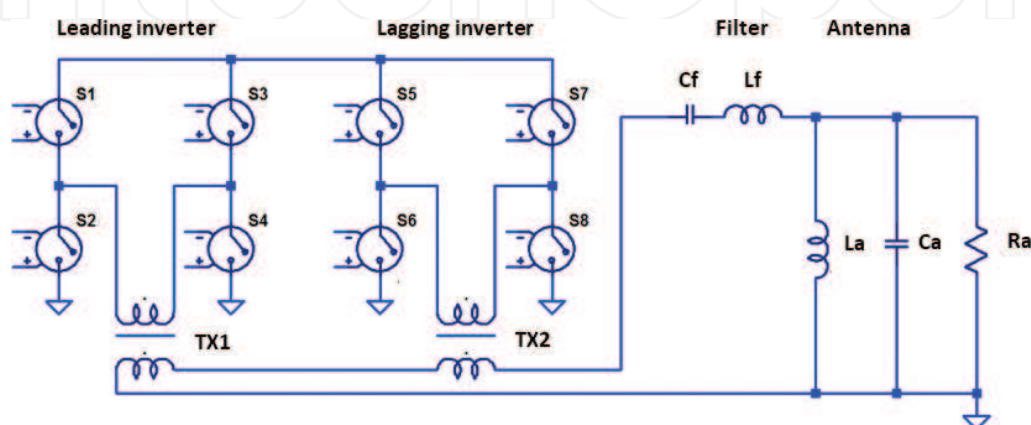

Figure 15. Switch-mode outphasing transmitter.

The transferring function transmitter output voltage to the antenna voltage is shown in **Figure 16**. The "saddle characteristic" has two poles reflecting two resonances at lower and higher frequencies than the operating frequency. The amplitude of those peaks depends upon the antenna and filter losses as shown for Q = 10 and Q = 100. The box at the operational frequency 0.5 MHz sets the acceptable system bandwidth which is necessary for correct restoring of the envelope of RF pulses used in NMR tools for the proton excitation. For RF pulses with Hann envelope with duration of 25us minimum bandwidth to correctly recover amplified antenna pulses, the bandwidth of the system output filter plus antenna should be 40 kHz minimum; with reliable margin for wide temperature range, it should be 80 kHz with flatness 5% or 0.5db (**Figure 17**).

Increase of the system bandwidth benefits the metrological parameters of the tool and accuracy in the replication of the shortest RF pulses, used for the hydrogen nuclei excitation, and makes possible to use the same filter for more than one frequency without the filter capacitor switched. But there is another drawback: the higher-frequency resonance (the right pole) amplifies higher harmonics of the output current due to the drop of the filter/antenna input impedance (**Figure 18**). The biggest harmonic in the 50% duty cycle module output voltage is the third harmonic, and the third harmonic of the output current may significantly exceed the amplitude of the fundamental harmonic. The smaller is output filter inductance the higher are values of the unwanted higher harmonics in the output current and the higher are conductive losses resulting in the component temperature rise. The output filter design is a compromise between the bandwidth and accuracy vs. losses and reliability. Higher harmonic elimination removes the cause of the excessive output current and significantly reduces power losses for the same number of switches [28].

To assess the advantage of the discussed harmonic elimination method, three 500 kHz transmitters operating identical loads (2uH, 52 nF output filter and 1uH, 100 nF, 90ohm, Q 30 antenna) and using the same number of power MOSFET switches (32 total) but different topologies and control signals corresponding to Case A, Case B and Case C configurations (**Figure 10**) were simulated for the standard for NMR pulse train with 25us and 50us Hann envelope, 1000Vmax and 20% duty cycle (**Figure 19**) [29].
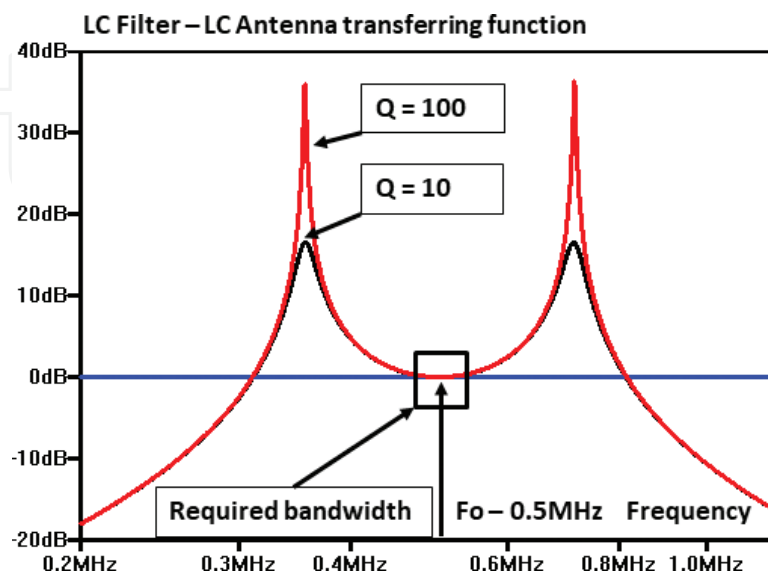

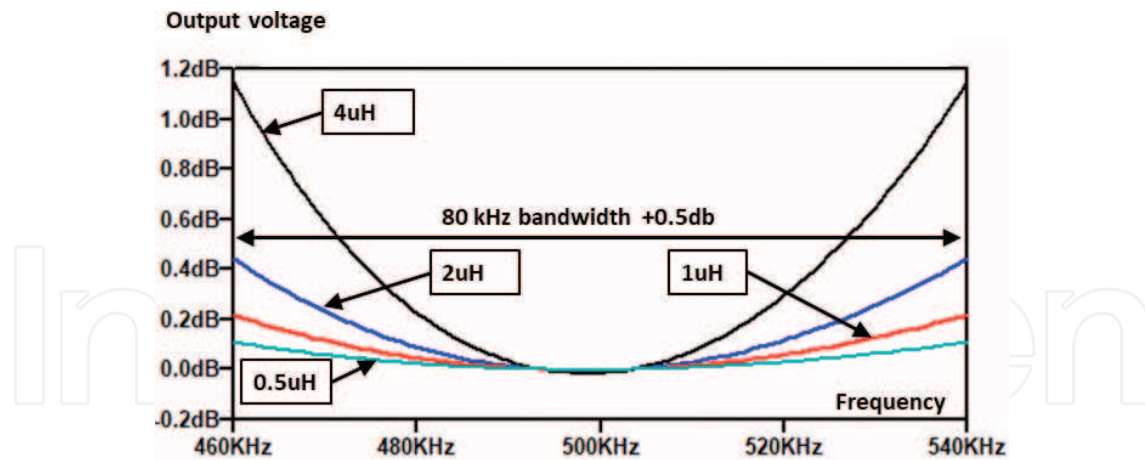**Figure 16.** Transferring function filter plus antenna.

Figure 17. Bandwidth vs. filter inductance.

Standard NMR excitation pulse sequence consists of the multiple identical pulses with the equal period and the first pulse with half duration and the same amplitude Vp =1000 V as shown on **Figure 19**.

The harmonics of the transmitter output current depend upon the voltage harmonics in the transmitter output signal. **Figure 20** shows the values of the first seven most important harmonics of the output current for transmitters based on the simplest two module Case A configurations [35], four module-enhanced transmitter Case B with eliminated the 3rd harmonic [30] and eight module transmitter Case C with eliminated the 3rd and 5th harmonics. Proper waveforms of the leading or lagging voltages marked as A, B and C are provided in **Figure 12**. Elimination of higher harmonics decreases the total output RMS current I_{out} per switch and resulting conductive power dissipation P_s:

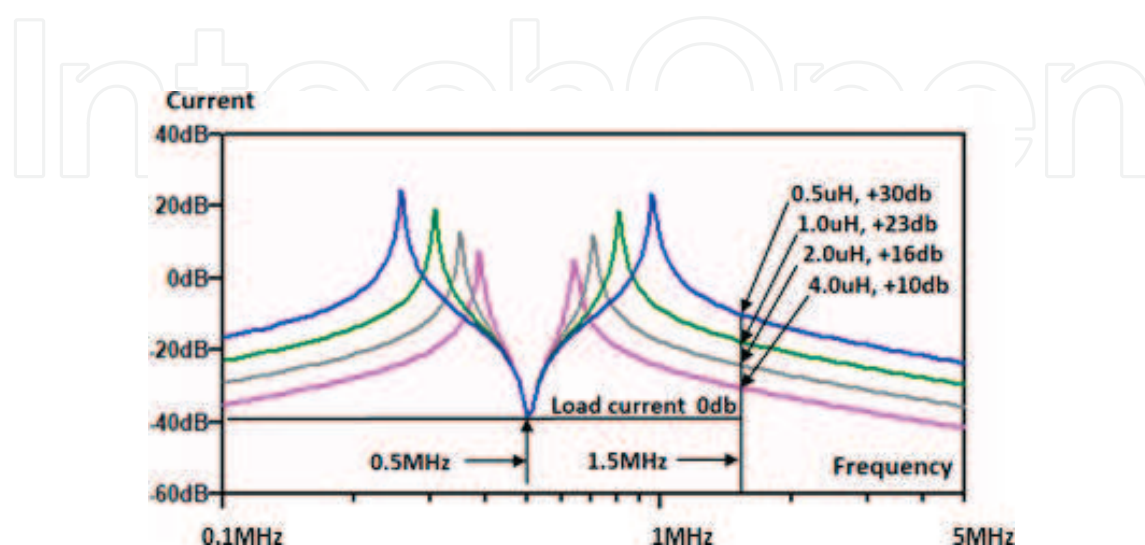$$P_s = P_{sw} + I_{out}^2 * R_{dson} \tag{12}$$

Figure 18. Transmitter output current of the third harmonic compared to the first one vs. filter inductance.
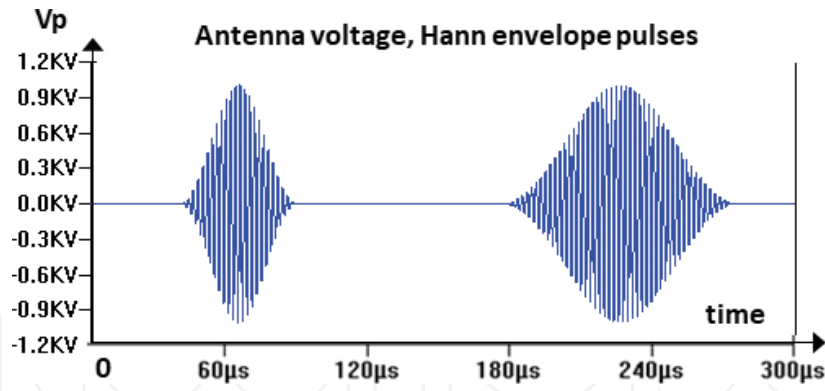
Figure 19. Antenna voltage (Vp(t)) and RF pulses with Hann envelope.

where P_s is the power switch total power dissipation, P_{sw} is the power of switching losses, I_{out} is the RMS value of switch current and R_{dson} is the switch resistance drain to source, which for silicon MOSFET is the function of the temperature and current [36].

Additional temperature rise ΔT_j of the switch die over the ambient temperature T_A depends on the thermal resistance R_{th} from the switch die to the ambient temperature T_A and current I_{out}:

$$T_j = T_A + \Delta T = T_A + R_{th} * \left(P_{sw} + I_{out}^2\right) \tag{13}$$

The die temperature T_j affects the switch life expectancy t_v according to the Arrhenius law:

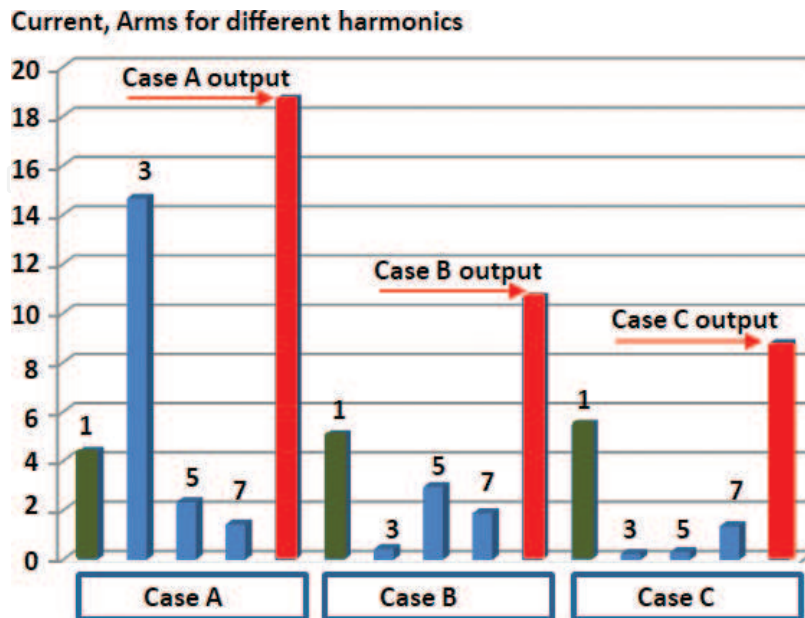$$t_v = C * e^{\frac{E_A}{kT_j}} \tag{14}$$

Figure 20. Higher harmonic (blue) elimination decreases total output current (red).
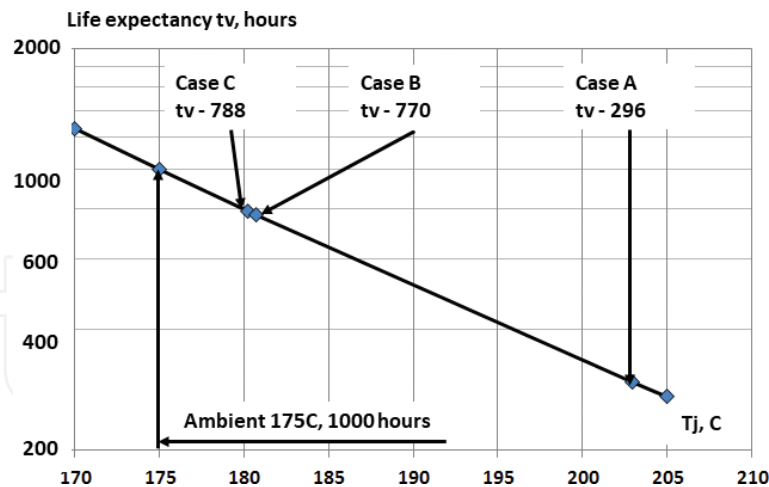
Figure 21. Life expectancy tv vs. transmitter topology.

where t_v is the switch life expectancy in time units, years or hours; T is the absolute temperature; E_A is the apparent activation energy in general depending on T, recommended value 0.8 eV [37]; C is a constant and k is the Boltzmann constant [38].

Additional temperature rise ΔT_j decreases life expectancy at T_j by the accelerator factor (AF) compared to the life expectancy at T_A:

$$AF = \frac{t_{v(T_j)}}{t_{v(T_A)}} = e^{\frac{E_A}{k}\left(\frac{1}{T_j} - \frac{1}{T_A}\right)} \tag{15}$$

Implementation of the sequential harmonic elimination decreases output current and related temperature rise, which results into the improvement of the transmitter reliability in terms of the life expectancy. The life expectancy (shown in **Figure 21**) changes from 1000 h at 175°C, taken as a reference point, down to 296 h for Case A, to 770 h for Case B and to 788 h for Case C. All transmitters use 32 power MOSFET switches; the difference is in the topology, control method and number of the additional RF output transformers, which easily fit the pressure housing and do not generate significant amount of heat.

Switching from classic transmitter topology Case A to Case B increases life expectancy 2.6 times, from Case A to Case C—2.66 times. It is clear that Case B transmitter is the best solution in terms of reliability improvement vs. extra cost and complexity. The benefits include not only increases of the life expectancy but also increases of tool accuracy, improving EMI conditions in the confined space of the power train placed in the high-pressure housing due to the spread in time switch operation [29].

7. Conclusion

The sequential harmonic elimination provides a simple method of removing higher harmonics from the output voltage of the multimodule multilevel converters operating with the fundamental switching frequency and using identical modules, generating 50% duty cycle output

voltages. A simple algorithm for the control circuitries used to eliminate harmonics and regulate output voltage from zero to maximum maintaining stable phase is discussed. A simple expression for THD of the output voltage vs. the number of eliminated harmonics, derived from simulation results, is provided for design evaluation against IEEE 519 standard requirements. The application of this method to the NMR transmitters operating in the high-temperature environment eliminates the most dangerous output current harmonics and shows more than twice the gain in the life expectancy. This method was validated for NMR downhole logging equipment, and two patents were granted.

Author details

Alexey Tyshko

Address all correspondence to: alex.tyshko@gmail.com

Baker Hughes, a GE Company, Global Research Center, Oklahoma City, OK, USA

References

[1] Patel HS, Hoft RG. Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I harmonic elimination. IEEE Transactions on Industry Applications. 9, May 1973;**IA**:310-317. DOI: 10.1109/TIA.1973.349908

[2] Baker, R, Bannister L. Electric power converter. Patent US 3,867,643 A USA. 1974. https://www.google.com/patents/US3867643

[3] Bhagwat P, Stefanovic V. Generalized structure of a multilevel PWM converter. IEEE Transactions on Industry Applications. 1983;**19**(6):1067-1069. DOI: 10.1109/TIA.1983.4504335

[4] Carrara G, Gardella S, Marchesoni M, Salutari R, Scuitto G. A new multilevel PWM method: A theoretical analysis. IEEE Transactions on Power Electronics. July 1992;**7**:497-505. DOI: 10.1109/63.145137

[5] Menzies RW, Zhuang Y. Advanced static compensation using a multilevel GTO thyristor inverter. IEEE Transactions on Power Delivery. April 1995;**10**(2):732-738. DOI: 10.1109/61.400858

[6] Cengelci E, Enjeti P, Singh C, Blaabjerg F, Pederson J. New medium voltage PWM inverter topologies for adjustible speed AC motor drive systems. Proceedings IEEE APEC' 98. 1998;**2**:565-571. DOI: 10.1109/APEC.1998.653955

[7] Lai J-S, Peng F. Multilevel converters: A new breed of power converters. IEEE Transactions on Industry Applications. May/June 1996;**32**(3):509-517. DOI: 10.1109/28.502161

[8] Li L, Czarkowski D, Liu Y, Pillay P. Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters. IEEE Transactions on Industry Applications. Jan/Feb 2000;**36**(1):160-170. DOI: 10.1109/28.821811

[9] Rodriguez J, Lai J-S, Peng FZ. Multilevel inverters: A survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics. August 2002;**49**(4):724-738. DOI: 10.1109/TIE.2002.801052

[10] Tolbert L, Peng F, Habetler T. Multilevel converters for large electric drives. IEEE Transactions on Industrial Applications. Jan/Feb 1999;**35**:36-44. DOI: 10.1109/28.740843

[11] Du Z, Tolbert L, Chiasson J. Harmonic Elimination for Multilevel Converter with Programmed PWM Method. IEEE IAS; 2004. pp. 2210-2215. DOI: 10.1109/IAS.2004.1348783

[12] Rodrigues J, Bernet S, Wu B, Pontt J, Kouro S. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. IEEE Transactions on Industrial Electronics. December 2007;**54**:2930-2945. DOI: 10.1109/TIE.2007.907044

[13] Rodriuez P, Bellar MD, Munoz-Aguilar RS, Busgues-Monge S, Blaabjerg F. Multilevel-Clamped Multilevel Converters (MLC). 3, s.l. IEEE. 2012;**27**:1055-1060. DOI: 10.1109/TPEL.2011.2172224

[14] Dahidah M, Agelidis V. Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula. IEEE Transactions on Power Electronics. 2008;**23**(4):1620-1630. DOI: 10.1109/TPEL.2008.925179

[15] Dahidah M, Konstantinou G, Agelidis VA. Review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications. IEEE Transactions on Power Electronics. 2014;**99**:1-16. DOI: 10.1109/TPEL.2014.2355226

[16] Darus R, Konstantinou G, Pou J, Ceballos S, Agelidis V. Comparison of Phase-Shifted and Level-Shifted PWM in the Modular Multilevel Converter. In: IEEE International Power Electronics Conference (IPEC–ECCE Asia) 2014. Hiroshima, Japan: IEEE; 2014. DOI: 10.1109/IPEC.2014.6870039

[17] Gnanasambandam K, Rathor AK, Edpuganti A, Srinivasan D, Rodriguez J. Current-Fed Multilevel Converters: An Overview of Circuit Topologies, Modulation Techniques, and Applications. IEEE Transactions on Power Electronics. 2017;**32**:3382-3402. DOI: 10.1109/TPEL.2016.2585576

[18] Ilves K, Antonopoulos A, Norrga S, Nee HP. A new modulation method for the modular multilevel converter allowing fundamental switching frequency. Proc. IEEE ICPE (ECCE Asia). June 2011:991-998. DOI: 10.1109/ICPE.2011.5944672

[19] Ilves K, Harnefors L, Norrga S, Nee H-P. Analysis and operation of modular multilevel converters with phase-shifted carrier PWM. IEEE Transactions on Power Electronics. Jan 2015;**30**(1):268-296. DOI: 10.1109/TPEL.2014.2321049

[20] Konstantinou G, Pulikanti S, Agelidis V. Harmonic Elimination Control of a Five-Level DC-AC Cascaded H-Bridge Hybrid Inverter. s.l. 2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems, 2010. 2010. DOI: 10.1109/PEDG.2010.5545762

[21] Li B, Yang R, Xu D, Wang G, Wang W, Xu D. Analysis of the phase-shifted carrier modulation for modular multilevel converters. IEEE Transactions on Power Electronics. Jan 2015;**30**(1):297-310. DOI: 10.1109/TPEL.2014.2299802

[22] Chiasson JN, Tolbert LM, Mckenzie KJ, Du Z. Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials and resultants. IEEE Transactions on Control Systems Technology. 2005:216-223. DOI: 10.1109/CDC.2003.1271691

[23] IEEE Standard 519-2014. IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, New York. https://edisciplinas.usp.br/pluginfile.php/2587631/mod_resource/content/2/IEE%20Std%20519-2014.pdf

[24] Capua CD, Romeo E. A smart THD meter performing an original uncertainty evaluation procedure. IEEE Transactions on Instrumentation and Measurement. Aug. 2007;**56**(4):1257-1264. DOI: 10.1109/TIM.2007.899895

[25] Blagouchine I, Moreau E. Analytic method for the computation of the total harmonic distortion by the Cauchy method of residues. IEEE Transactions on Communications. 2011;**59**(9):2478-2491. DOI: 10.1109/TCOMM.2011.061511.100749

[26] Tyshko A. Multi-Vector Outphasing DC to AC Converter and method. US Patent 9680396, granted June 13, 2017. https://www.google.com/patents/US9680396

[27] Tyshko A. Multi-Vector Outphasing Provides High Power, Low Harmonics. IEEE Digital Library ELNANO-2014. Kiev, Ukraine: IEEE, 2014. Electronics and Nanotechnology (ELNANO), 2014 IEEE 34th International Conference. pp. 416-420. DOI: 10.1109/ELNANO.2014.6873437

[28] Tyshko A. Excitation of the Resonant Loads with the Multi-Vector Synthesized Sinusoidal Voltage Decreases Conduction Losses and Improves Reliability. Vol. 19. Kiev, Ukraine: Electronics and Communications, Power Electronics Section; 2014. pp. 37-42 ISSN 1811-4512

[29] Tyshko A, Balevicius S, Padmanaban S. An increase of a down-hole nuclear magnetic resonance Tool's reliability and accuracy by the cancellation of a multi-module DC/AC Converter's Output's higher harmonics. IEEE Access. 2016;**4**:7912-7920. DOI: 10.1109/ACCESS.2016.2624498

[30] Tyshko A. Enhanced Transmitter and Method for a Nuclear Magnetic Resonance Logging Tool. Patent US 9,405,035. Jan 10, 2012. Patent granted Aug 2, 2016; https://www.google.com/patents/US9405035

[31] Tyshko A. DC to AC 3 Phase Modular Multilevel Conversion Using Chireix Outphasing Method. Kiev, Ukraine: IEEE, 2015. Electronics and Nanotechnology (ELNANO), 2015 IEEE 35th International Conference. pp. 539-542. DOI: 10.1109/ELNANO.2015.7146946

[32] Chireix H. High power outphasing modulation. Proceedings of IRE. 1935;**23**:11

[33] Doherty WH. A new high efficiency power amplifier for modulated waves. Proceedings of IRE. 1936;**24**:9

[34] Perreault DJ. A new power combining and Outphasing modulation system for high efficiency power amplification. IEEE Transactions on Circuits and Systems. Aug 2011;**58**(8):1713-1726 http://dx.doi.org/10.1109/TCSI.2011.2106230

[35] Dent, Paul Wilkinson. Hybrid Chireix/Doherty amplifiers and methods. Patent US 6,133,788 USA, Apr 2, 1998. https://www.google.com/patents/US6133788

[36] Tyshko A. Analyze MOSFET parameter shifts near maximum operating temperature. Electronic Design. March 2014;**17**:62-65 EDN (ISSN 0012-7515)

[37] Bayle F, Metta A. Temperature acceleration models in reliability predictions, Justification and Improvements. In: Proc. Reliability and Maintainability Symp. San Jose, CA, USA. Jan. 2010. pp. 1-7 http://www.reliasoft.com/pubs/2010_RAMS_temperature_acceleration_models.pdf

[38] Calixto E. Gas and Oil Reliability Engineering: Modeling and Analysis. Oxford, UK: Gulf Professional Publishing; 2012 ISBN: 9780128054277