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Operational Amplifier Design in CMOS at Low-Voltage for Sensor Input Front-End Circuits in VLSI Devices

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Additional information is available at the end of the chapter

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Abstract

Today, digital circuit cores provide the main circuit implementation approach for integrated circuit (IC) functions in very-large-scale integration (VLSI) circuits and systems. Typical functions include sensor signal input, data storage, digital signal processing (DSP) operations, system control and communications. Despite the fact that a large portion of the circuitry may be developed and implemented using digital logic techniques, there is still a need for high performance analogue circuits such as amplifiers and filters that provide signal conditioning functionality prior to sampling into the digital domain using an analogue-to-digital converter (ADC) for analogue sensor signals. The demands on the design require a multitude of requirements to be taken into account. In this chapter, the design of the operational amplifier (op-amp) is discussed as an important circuit within the front-end circuitry of a mixed-signal IC. The discussion will focus on the design of the op-amp using different compensation schemes incorporating negative Miller compensation and designed to operate at lower power supply voltage levels. A design case study is included which utilises the g_m/I_D ratio design approach to determine the transistor sizes. The simulation approach is focussed on the open-loop frequency response performance of the op-amp.

Keywords: op-amp, design, stability, g_m/I_D , Miller compensation, negative Miller compensation

1. Introduction

In this chapter, the focus of the discussion is on the design of the op-amp, which will act as an integral part of the on-chip analogue signal conditioning circuitry for the front-end section of a

mixed-signal IC. The performance requirements and design issues for circuit operation on a single-rail power supply and operating at 3.3 V or lower will be considered. The op-amp architecture will be discussed, and the focus will be on the design of the compensation circuitry that will be required for amplifier stability purposes. In particular, the use of Miller and negative Miller compensation techniques, and the effects of different compensation techniques on amplifier operation, will be identified. The discussion will be supported using suitable simulation study results. The chapter will initially consider the analogue circuit requirements before discussing op-amp design and compensation techniques. The concepts introduced and analysed will be accompanied by analogue circuit simulation results using Cadence Spectre simulator and the circuit design will be implemented using a 0.35 μm n-well complementary metal oxide semiconductor (CMOS) fabrication process. In order to provide a better understanding, the discussion will include the use of MATLAB for mathematical modelling the frequency response of the op-amp in open loop.

2. Analogue front end circuits in mixed-signal IC designs

Today, electronic systems are embedded in everyday items such as smart phones, mobile computing, biomedical monitoring (bioinstrumentation) systems, entertainment systems and environmental monitoring systems. In many cases, these systems are based on capturing sensor signals, processing and converting them to a suitable digital representation, undertaking digital signal processing (DSP) operations, storing values in local memory, interfacing to a user and finally providing wired or wireless communications to another electronic system. The basic idea is shown in **Figure 1**. The sensors can provide either analogue outputs (such as voltage, current, frequency and impedance) or digital outputs (logic 0 and 1 levels with associated voltage values). In general, the sensor output signals would require signal conditioning in order to create signal values that are in a suitable form to be captured by a digital processing module. This digital processing module would provide the necessary functions in hardware only or as a mixture of

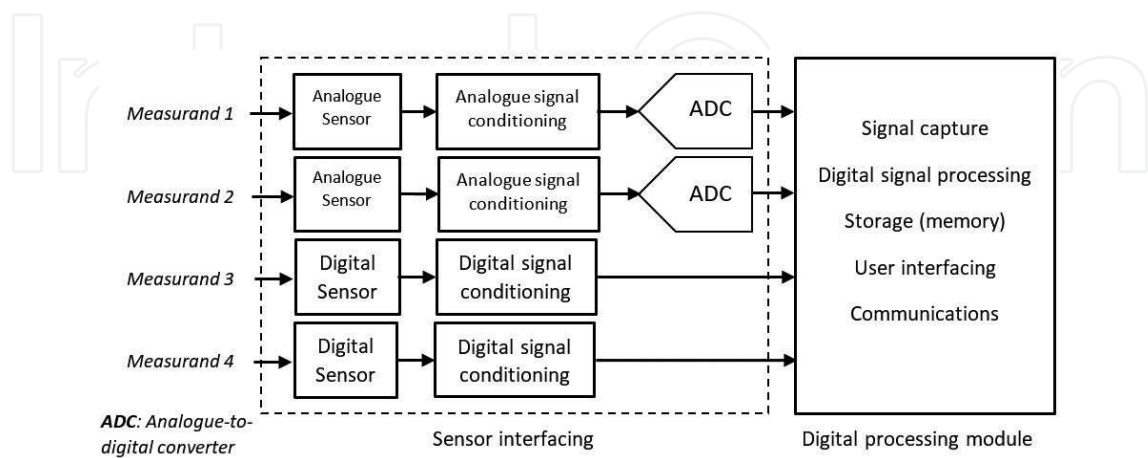


Figure 1. Sensor signal sampling and digital signal processing.

hardware and software operations. The choice of the electronics in the digital processing module in many cases is based on using either software programmable devices such as the microcontroller (μC), microprocessor (μP) and digital signal processor (DSP), or hardware configurable devices such as the field programmable gate array ($FPGA$) and complex programmable logic device ($CPLD$). However, the alternative that involves the design of a custom integrated circuit would be based on application specific integrated circuit ($ASIC$) design techniques. Designing such $ASICs$ would enable a custom design to be created and higher levels of integration that result in physically smaller electronics and the integration of digital, analogue and mixed-signal circuits within a single packaged device. Considering the analogue sensor part of the system, the signal output from the sensor would normally need to be modified (conditioned) in order to provide signal levels that can be sampled by the digital signal-processing module via a suitable ADC, which converts the analogue signal to a digital representation.

Such signal conditioning operations include signal amplification, DC level shifting and anti-aliasing filtering (low-pass filtering to remove any high frequency signal components that would be aliased to lower frequencies). In general, these signal conditioning circuits are based on the use of the op-amp with negative feedback using external resistors and capacitors. However, the operating conditions of the op-amp such as the power supply voltage level would need to be taken into account when either selecting an existing op-amp to use or when designing the op-amp itself. The performance of the op-amp in these types of signal conditioning circuits would be a key factor in what performance could be achieved with the circuits used. In the past, the power supply voltage would not have been a major factor in determining the op-amp performance. The power supply voltage would have been at levels that enabled the op-amp circuitry to operate without encountering power supply voltage limitation issues. With the move towards lower power supply voltage levels at, and below 3.3 V operation, and moving towards 1 V system operation, the power supply conditions must now be accounted for. The op-amp circuit architectures along with circuit design approaches must be reconsidered in order to enable these op-amps to be designed with appropriate characteristics for low-voltage operation.

3. Conventional op-amp design approach

3.1. Introduction

The op-amp is a high-gain DC differential amplifier that is the core building block for many analogue circuits. In general, it consists of two or more amplification stages using transistors, integrated capacitors and in some designs, integrated resistors. **Figure 2** identifies the basic symbol for the voltage input/voltage output op-amp, which has two inputs (the inverting ($IN-$) and non-inverting ($IN+$) inputs), a DC power supply ($V+$ and $V-$) and either one output (a single-ended output (a)) or two outputs (a differential output (b)). The op-amp is designed to have certain characteristics that include a high open-loop differential gain (A_{OL}), a high gain-bandwidth product, a high input resistance, a low output resistance, a low output offset voltage, a high dynamic range (minimum to maximum signal range) and a high common-mode rejection ratio ($CMRR$) [1]. The op-amps shown in **Figure 2** identify the circuits in open loop without any

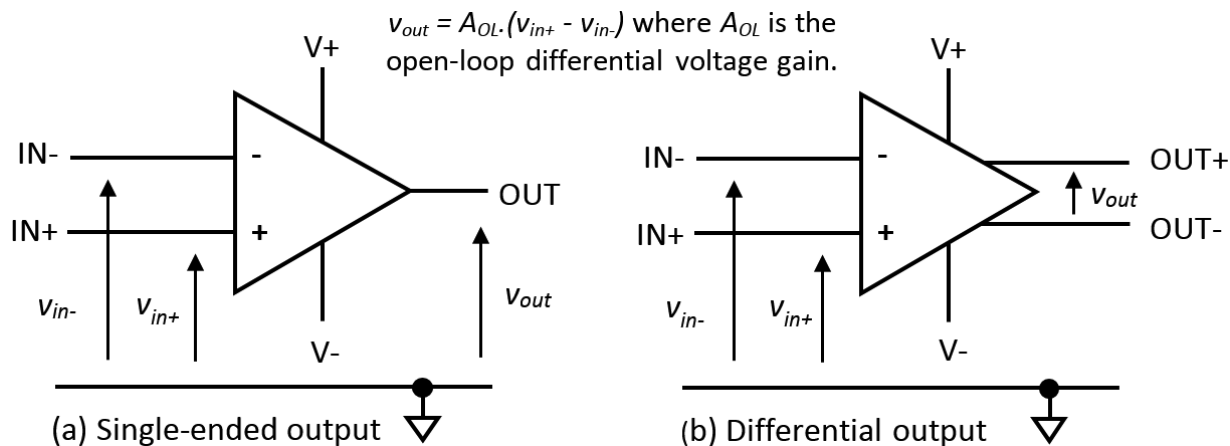


Figure 2. Single-ended output and differential output op-amps.

external feedback components from the output signal back to the input signal. The op-amp, therefore, would have a set of open-loop characteristics. In general, the op-amp would be designed to operate in closed loop where feedback components, primarily resistors and capacitors are used to provide either negative (linear operations) or positive (non-linear operations) feedback.

In the discussion within this chapter, CMOS fabrication process is considered as it is the most widely used fabrication process to realise VLSI ICs. The work presented here will focus on CMOS op-amp circuit design considerations, particularly the AC (frequency) response and stability. The standard topology for the single-ended output two-stage op-amp is considered, and the behaviour of an example case study design will be presented.

3.2. Metal oxide semiconductor field effect transistor

The metal oxide semiconductor field effect transistor (MOSFET) is the most widely used semiconductor device. It is a non-linear device that has four terminals: the drain, source, gate and bulk (or body, substrate). Two forms of MOSFET can be created: the n-channel (nMOS) and p-channel (pMOS) [2]. With these transistors, a voltage between the gate and the source (v_{gs}) controls the flow of drain current (i_d). To design circuits using these devices, it is necessary to know their current-voltage (IV) characteristics. In conventional circuit design, the transistor is usually modelled using two discrete models to mathematically describe the IV characteristics: a large-signal and a small-signal model. Each model would be used for different design and analysis purposes.

3.3. Large-signal model

A curve that describes the large-signal IV characteristic is shown in **Figure 3**. The operation of the transistor is modelled using three different regions according to the values of the gate-source voltage (v_{GS}) and the drain-source voltage (v_{DS}). This models the MOSFET drain current (i_D) against v_{DS} with different values of v_{GS} .

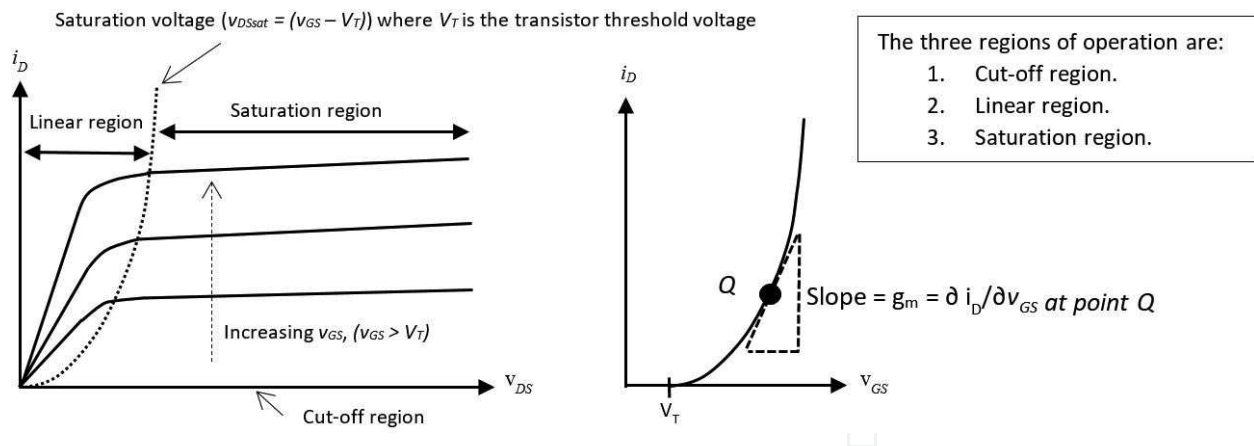


Figure 3. Large-signal IV characteristic of the MOSFET.

The three defined regions of operation are *cut-off*, *linear* and *saturation* where:

Cut-off region: Cut-off is a region in which the transistor will be OFF, and there will be no current flow from the drain to the source (i_D (cut-off) = 0). The gate-source voltage is less than the transistor threshold voltage (V_T) in this region.

Linear or ohmic or non-saturation region: In this region, the gate-source voltage is larger than, or equal to, V_T and the drain-source voltage larger than zero but less than the saturation (pinch-off) voltage ($v_{DSsat} = (v_{GS} - V_T)$). A channel is created between the drain and source terminals, and there is current flow from drain to source. The drain current will increase linearly with increasing drain-source voltage.

Saturation region: In this region, the gate-source voltage is larger or equal to, the transistor threshold voltage, and drain-source voltage has reached or exceeds, v_{DSsat} . This occurs when the channel charge becomes pinched off at the drain-channel interface, and the transistor operation is now in the saturation region. In the simplest (first order) transistor model, increases in v_{DS} do not cause an increase in i_D and so i_D becomes independent of v_{DS} . However, a more representative model includes an i_D dependence on the value of v_{DS} . Moreover, the transistor operation depends on the gate overdrive voltage ($v_{eff} = (v_{GS} - V_T)$) with the drain-source channel in strong inversion.

3.4. Small-signal model

Although the transistor is a non-linear device, for circuit analysis purposes when developing linear circuits, a linear model for the transistor operating in the saturation region at a specified DC operating (bias) point is initially created. This then describes the behaviour of the transistor to small-signal changes around the bias point, and the small-signal model is then used to determine AC gain values. The signal changes are considered to be small so enabling the approximation that the transistor operation is linear around this DC operating point to be valid. Moreover, defining the small-signal behaviour of the transistor as a transfer function, the transconductance (g_m), and output conductance (g_o) is required model parameters. The small-signal equivalent circuit model for the MOSFET is shown in Figure 4.

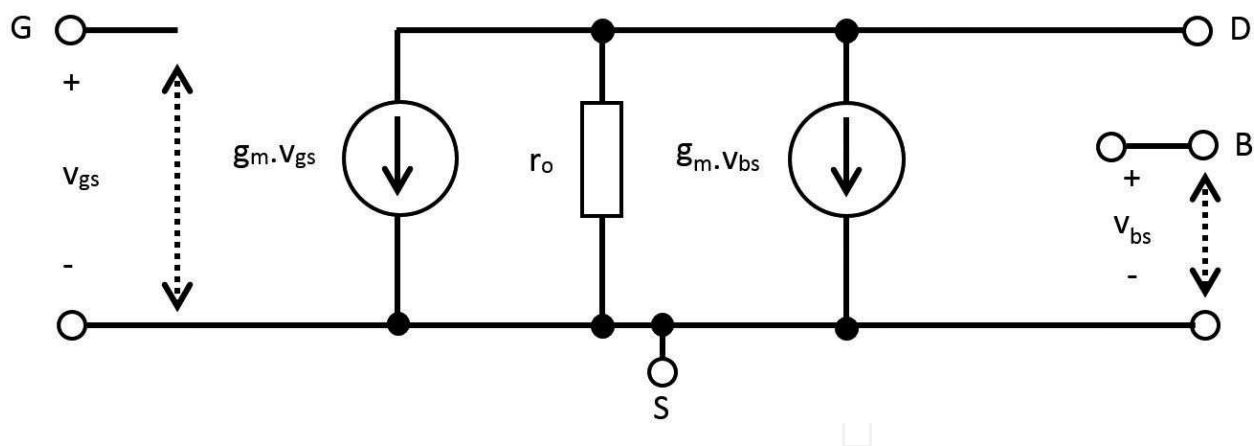


Figure 4. MOSFET small-signal equivalent circuit model.

However, if the signal level is increased, the transistor operation becomes non-linear and will represent by the large-signal model. The conventional analogue design method for the op-amp considers the use of the transistor operating in the saturation region and the drain-source channel to be in strong inversion. This requires the circuit voltage levels (and hence the power supply voltage) to be of suitably high levels to ensure that the transistor remains in saturation and strong inversion for linear circuit operation. Analogue CMOS integrated circuit design needs to use a suitable technology to determine MOSFET dimensions and create the required circuit performance. However, today, when developing circuit designs based on using MOSFETs at low-power and low-voltage, the small-signal and large-signal models are no longer suitable to define transistor operation.

3.5. Example two-stage CMOS op-amp design

The op-amp circuit can be based on different architectures, and each architecture provides advantages in operation when compared to other architectures. In the design considered in this chapter, the two-stage CMOS operational amplifier is used with a simplified architecture as shown in **Figure 5**. Two amplification stages are used, the first stage providing high voltage gain and the second stage providing additional voltage gain and a large output signal swing. In addition, each stage uses negative feedback frequency compensation to improve stability and bandwidth. Negative Miller compensation is applied around the first stage using two identical capacitors (C_{NM}), and Miller compensation is applied around the second stage using two identical capacitors (C_M). The circuit schematic of the selected op-amp architecture is shown in **Figure 6**. Note how the signals between the first stage and the second stage are connected and how the actual circuit connections differ from the simplified architecture (**Figure 5**). The first stage consists of a transconductance stage with differential input transistors $PM1$ and $PM2$ followed by folded cascode (FC) stage. The mirror connected transistors $NM5$ and $NM6$ in the folded cascode sum the input transistors differential current. The current sources $PM8$ and $PM9$ on the upper side must provide a current larger than the bias current for each input transistor.

The second stage is a class AB amplifier, and the single-ended output comes from transistors $PM17$ and $NM14$. The second stage is primarily used to provide a large output voltage swing

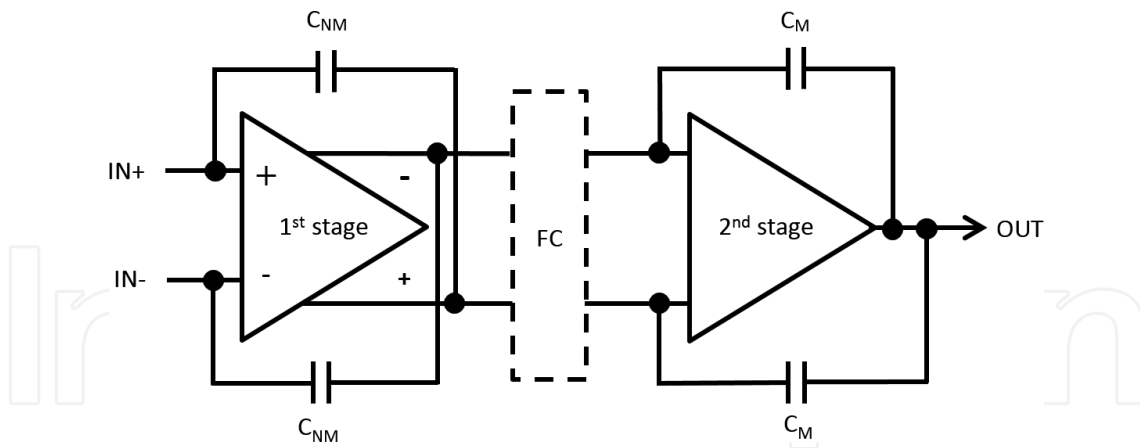


Figure 5. Two-stage op-amp case study design simplified architecture.

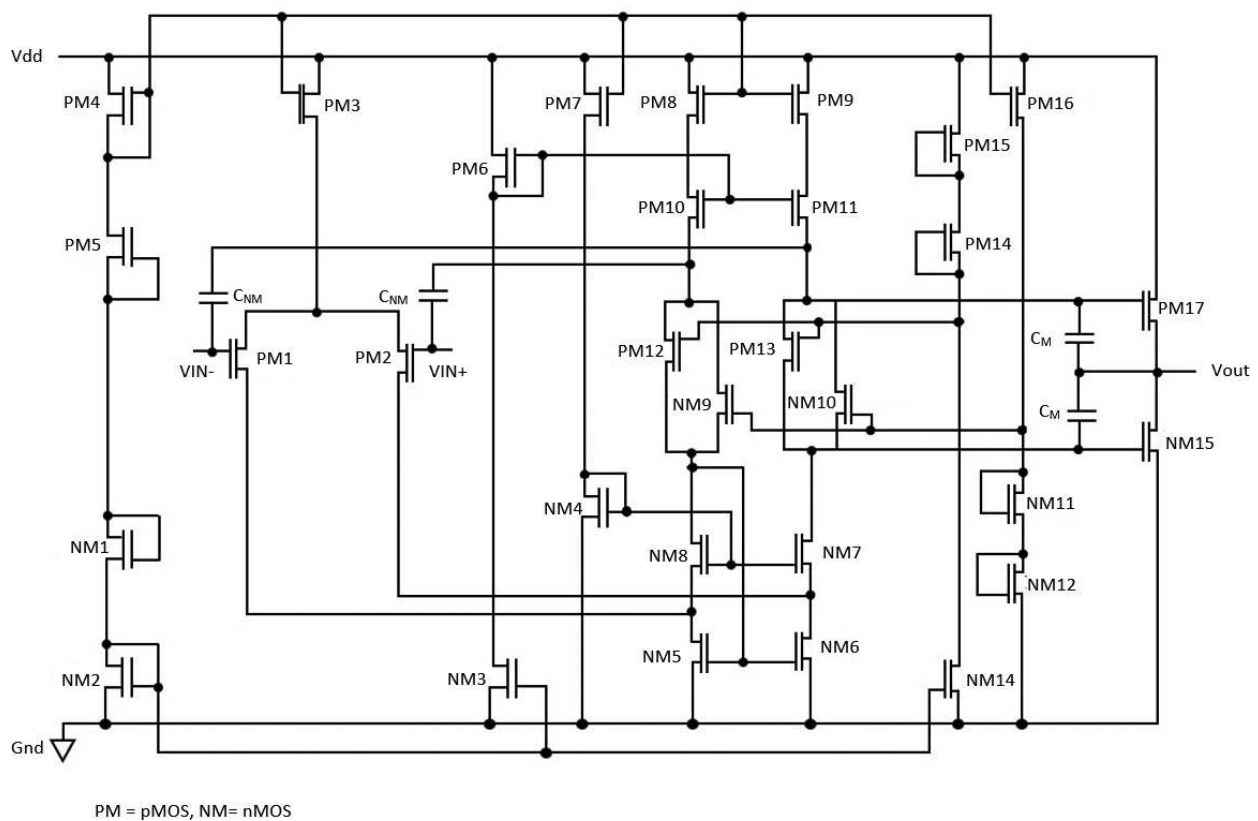


Figure 6. Two-stage op-amp design case study design schematic.

(rail-to-rail output) with high DC voltage gain. *NM10* and *PM13* perform the feed-forward class-AB control. These transistors are biased by two in-phase signal currents using the two cascode transistors *NM8* and *PM11*. The gate voltages for these two transistors are kept at a constant value using the stacked diode-connected transistors (*PM14*, *PM15* and *NM11*, *NM12*). The floating current source (*PM12* and *PM13*) has the same structure as the feed-forward

class-AB control. The compensation circuitry is split into two parts. Miller compensation around the second stage provides op-amp stability. The op-amp has two Miller capacitors around the class-AB amplifier. Negative Miller compensation around the first stage is provided the extended the bandwidth (increases the unity gain frequency) and also uses two capacitors.

4. Op-amp stability and compensation techniques

4.1. Introduction

The reason for considering stability in a circuit design is to ensure that the circuit remains stable under the required operating conditions. Instability occurs when the op-amp is configured with negative feedback, and under certain conditions, the negative feedback becomes positive. In the unstable case, the circuit output then oscillates. Stability under any input condition is referred to as unconditionally stable, or absolutely stable [3]. However, if a system is not unconditionally stable, a margin of stability must be built-in to ensure stable operation under the required operating conditions. To achieve stable op-amp operation in closed-loop, the designer can add a capacitance between specific nodes within the op-amp that deliberately reduces the open-loop gain magnitude at higher signal frequencies. This technique, referred to as *compensation*, is implemented by typically bypassing one of the internal op-amp gain stages with a high-pass filter. In the simplest sense, a capacitor is connected between the output and input nodes of a gain stage. The purpose is to decrease the gain magnitude to less than unity at frequencies where instability could occur. A single compensation capacitor implementation is widely used in two-stage op-amp designs. However, there are several other techniques used for the op-amp compensation. Improvements to the op-amp performance using the single capacitor compensation approach include the inclusion of a series resistor, buffer or buffer and series resistor. Other techniques, for example, use multiple feedback capacitors connected to different stages within the circuit. These techniques can be used with the two-stage op-amp. Additional techniques require the inclusion of more than two gain stages and, with decreases in integrated circuit process geometries, op-amps with more than two gain stages have become more common to achieve a sufficiently high open-loop gain. There are two common assumptions in the design of compensation topologies. First, the gain magnitude of the stage is larger than one. Second, the compensation and output load capacitance values are larger than the combined output transistor capacitances for each stage. In addition to the DC gain of the op-amp, there are four parameters of particular interest pertaining to its frequency response. These are the unity-gain bandwidth (UGB), gain-bandwidth product (GBWP), phase margin (PM) and gain margin (GM). UGB specifies the frequency at which the op-amp open-loop differential gain magnitude ($|A_{OL}|$) is unity (i.e. 0 dB). GBWP defines the gain-bandwidth product of the op-amp gain magnitude and frequency (f):

$$GBWP = |A_{OL}| * f \quad (1)$$

A potential problem, however, of using a multiple-stage op-amp is for unstable circuit behaviour resulting in an oscillatory output signal due to the capacitances within the op-amp circuit and signal feedback paths that exist. The transistor capacitances and parasitic effects due to

layout, along with external components, will contribute to the potential for instability when the op-amp is used in a closed-loop configuration, for example, when the op-amp is used in a unity gain buffer configuration. One common way to predict the closed-loop stability of an amplifier is by determining the PM of the open-loop gain response. The PM must be greater than 0° to prevent negative feedback becoming positive feedback thus creating signal oscillation rather than signal amplification. To determine PM at the unity gain frequency, the difference between the amount of signal phase shift and 180° is determined:

$$PM = (180^\circ - |\theta|) \text{ at the unity gain frequency} \quad (2)$$

where θ is the phase shift of the output signal in degrees (referenced to 0°) when the gain magnitude is unity (0 dB). It is commonly considered that an op-amp in open-loop will require a phase margin of 45° or higher. The GM (in dB) is the difference between the gain magnitude at 180° phase shift and the unity gain magnitude (i.e. 0 dB):

$$GM = (0 \text{ dB} - \text{Gain magnitude (in dB)}) \text{ at } 180^\circ \text{ phase shift} \quad (3)$$

Given the complexity of the input-output relationship of the op-amp, it is common to model the op-amp input-output behaviour in terms of a transfer function for analysis purposes. Typically, a Laplace transfer function is created to model the frequency response and the response is viewed using a Bode plot. The transfer function provides a form for determining important system response characteristics (without solving the complete set of differential equations) in the form:

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1} s^{(m-1)} + \dots + a_2 s + \dots + a_0}{b_n s^n + b_{n-1} s^{(n-1)} + \dots + b_2 s + \dots + b_0} \quad (4)$$

The roots of the numerator $N(s)$ (z_x) are called the zeros of the transfer function, and the roots of the denominator $D(s)$ (p_y) are called as the poles of the transfer function. s is a complex frequency. It is often suitable to factor the polynomials in the numerator and denominator so that the transfer function then becomes:

$$H(s) = \frac{Z(s)}{P(s)} = K \cdot \frac{(s - z_1) \cdot (s - z_2) \dots (s - z_m)}{(s - p_1) (s - p_2) \dots (s - p_n)} \quad (5)$$

This form of equation directly identifies the system poles and zeros. Using the transfer function characteristics, the Bode plot is a particularly useful tool to visualise the frequency response for analysis purposes. However, with the complexity of the networks formed by the circuit (i.e. the connection of the transistors) and the compensation structures, any system transfer functions that can be derived from the frequency response of the actual circuit to mathematically model the op-amp behaviour rapidly becomes complex. The result is a transfer function with multiple poles and zeros to consider with a complexity that cannot be easily investigated using hand calculations. Hand calculations usually utilise a simplified transfer function, using a form with the most dominant two or three poles, and a full analysis would require the use of a suitable analogue circuit simulator (typically SPICE based) and

mathematical modelling tools such as MATLAB. However, deriving simplified transfer function models of the complex circuit can result in loss of detail with some of the critical frequency response parameters. Assumptions are therefore required to simplify the transfer functions without losing important information and any results must be treated with caution, particularly as the relevance of the results obtained must be determined.

4.2. Miller compensation

Miller compensation is achieved by using a capacitor (C_M) between the input and output nodes [4] of the second inverting stage of the two-stage op amp as shown in **Figure 7a**. The dominant (lower frequency) pole in the circuit transfer function is shifted to a lower frequency due to the Miller effect, and the non-dominant (higher frequency) pole is shifted to a higher frequency. The capacitor does not influence the DC response of the amplifier but retains a high gain at mid-band frequencies and reduces the high frequency gain. In this way, the two poles are split and this stabilises the amplifier, but this results in a reduction in signal bandwidth. In addition, the right-hand plane (RHP) zero causes a negative phase shift. The zero comes from the direct feedthrough of the input to the output through the Miller capacitor. If A is the voltage gain of the amplifier, and C_M is a feedback capacitance across the amplifier, Miller theory identifies that C_M effectively shows as a capacitance from the input and output nodes to ground as shown in **Figure 7b**. For a two-stage CMOS op-amp design, considering it to be modelled as a transfer function with two poles only, Miller compensation is used for pole splitting. To establish the frequency dependent gain of this circuit, the small-signal equivalent circuit, as shown in **Figure 8**, can also be created.

The Bode plot for the equivalent circuit in **Figure 8** is shown in **Figure 9** and can be used to identify the positions of the poles and zeros in the transfer function. The first pole ($f_{1'}$) is shifted to a lower frequency (f_1) and the second pole ($f_{2'}$) is shifted to a higher frequency (f_2), although creating the zero (f_z). In addition, the phase is shifted to a higher frequency.

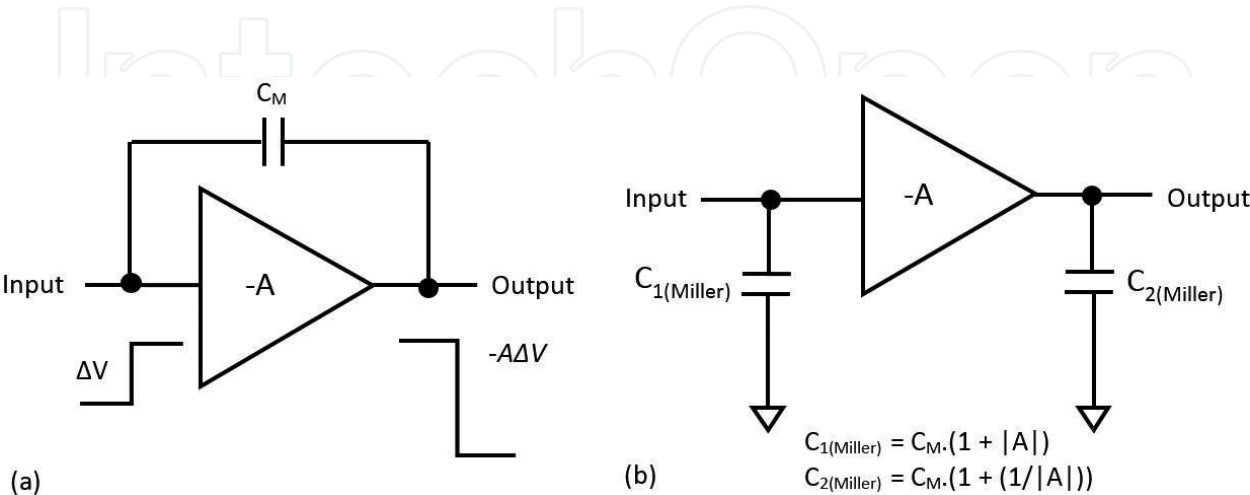


Figure 7. Inverting amplifier with (a) Miller capacitance and (b) equivalent model.

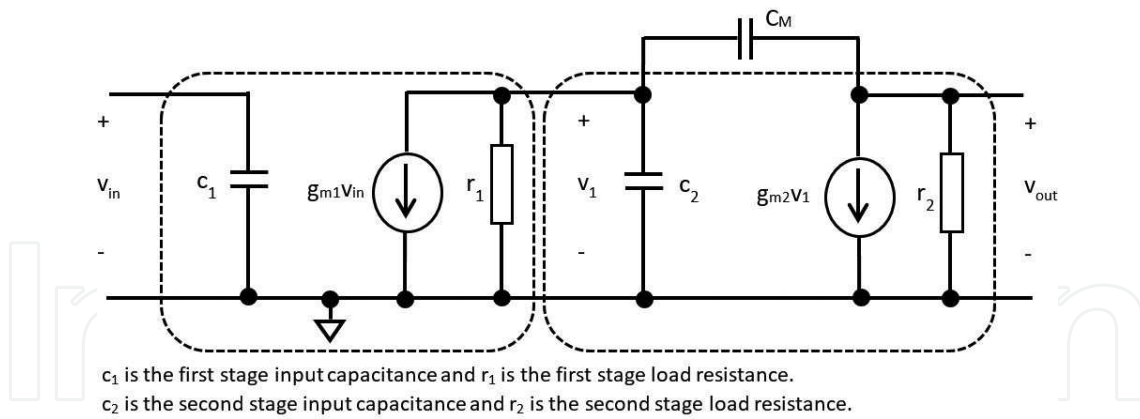


Figure 8. Small-signal equivalent circuit for a two-stage CMOS op-amp including Miller compensation.

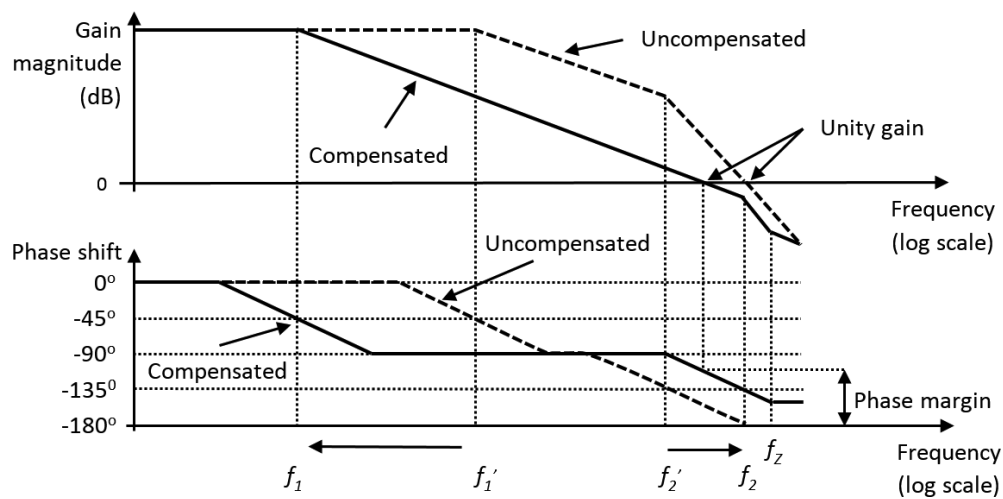


Figure 9. Bode plot showing the pole movement in frequency due to the Miller capacitor.

4.3. Negative Miller compensation

The effect of circuit capacitances, in particular, considering the transistor capacitances, must be considered at higher frequencies as they can cause undesirable phase shifts at higher frequencies that would not be present at lower frequencies. For example, transistor input capacitances can cause problems in circuit operation at higher frequencies and are difficult to eliminate, resulting in reduced op-amp performance. However, as improvement in the fabrication processes leads to reduced transistor geometries, a decrease in transistor capacitance values can be obtained. Negative Miller compensation can, however, be used to improve the frequency response of an op-amp [5]. The idea is shown in **Figure 10**. Negative Miller compensation is based on Miller effect, which defines the effect of the feedback capacitance C_{NM} on the input capacitance C_I . In **Figure 10**, a capacitance (C_{NM}) is connected between the output and input nodes of a non-inverting amplifier. This creates the effect of a negative capacitance. Negative capacitance provides a method for reducing the effects of the transistor input capacitances by the partial cancellation of these capacitances.

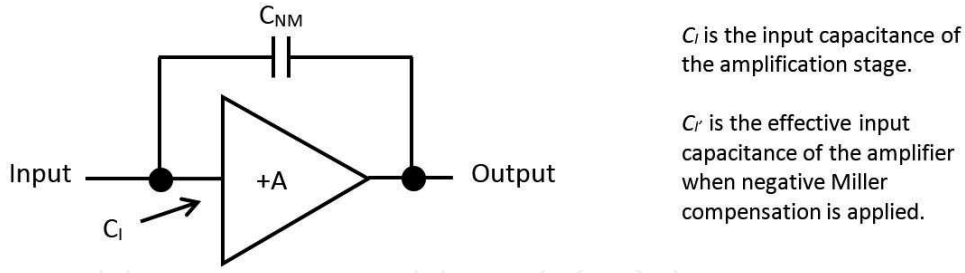


Figure 10. Concept for negative Miller compensation.

The amplifier has a gain magnitude greater than unity. The equivalent input capacitance (C_I') is given by:

$$C_I' = C_I + (1 - |A|)C_{NM} \quad (6)$$

The value of C_I' can be controlled by varying C_{NM} and if C_{NM} is large, there will be a net negative capacitance, or an equivalent inductive effect, over a narrow frequency band [6]. Within the op-amp, a gain stage is usually created using an inverting amplifier with a single-ended output. However, with a single-ended output amplifier, in order to incorporate negative Miller compensation then two cascaded gain stages would need to be used. One gain stage would be a non-inverting amplifier, and the feedback capacitor connection is then possible. The second would be an inverting amplifier to provide the overall inverting amplifier arrangement. For a fully differential gain stage, the negative Miller technique can be applied directly. A negative capacitance property can be utilised to improve bandwidth and phase margin. The negative capacitance design moves the non-dominant pole to a higher frequency whilst keeping the location of the dominant pole approximately the same.

5. g_m/I_D ratio design approach

5.1. Introduction

When designing a CMOS op-amp using available transistor models, there can be a substantial difference between the hand calculation results using simple first-order models and simulation results using more complex models (typically BSIM3 transistor simulation models are available for a fabrication process). This would be due to both the complexities of the models used and the accuracy of the models taking into account the boundaries of operation at which the models are designed to operate in. The transistors are, however, operating in the saturation region and in the conventional op-amp design approach, the transistors are considered to also operate in strong inversion where the gate-source voltage is high as discussed in Section 3. At low-voltage operation that is appropriate also for low-power designs, the transistor gate-source voltage is lower and the transistor may be operating in moderate or weak inversion. The transconductance-DC drain current ratio (g_m/I_D) design approach provides separate analytical formulas for strong, moderate and weak inversion, so as to provide simple formulas that are useable in all channel inversion conditions. The approach is particularly suitable for

analogue design in CMOS technologies. It considers the relationship between the ratio of the transconductance g_m over DC drain current I_D . In addition, the normalised drain current is also a basic design parameter. The g_m/I_D characteristic provides a useful way to describe the MOSFET operation and provides a straightforward way to estimate transistor dimensions and support circuit design at low-voltage operation. The g_m/I_D ratio is expressed as follows:

$$\frac{g_m}{I_D} = \frac{\partial I_D / \partial V_{gs}}{I_D} = \frac{\partial \log(I_D)}{\partial V_{gs}} \quad (7)$$

Figure 11 identifies two key graphs used. **Figure 11a** on the left shows the g_m/I_D versus V_{GS} characteristic, and **Figure 11b** on the right shows the g_m/I_D versus I_D characteristic. The greater the slope of the curve, the greater the g_m/I_D ratio. This condition occurs when the transistor is operating in weak inversion. As the slope of the curve reduces, the transistor moves into strong inversion. Between weak and strong inversion, moderate inversion occurs. It is to be noted, however, that the region of the moderate inversion is not clearly defined. Weak and moderate inversion are more satisfactory for low-power designs [7]. Moreover, the overdrive voltage (v_{eff}) is low, which is suitable for low supply voltage operation. **Figure 12a** on the left shows the relationship between the g_m/I_D with normalised current $I_D \cdot (W/L)$, and **Figure 12b** on the right shows the transistor transit frequency (f_T) versus g_m/I_D . These curves act as aids to design and hence determining the transistor dimensions. In addition, its analytical form covers all transistor channel inversion conditions, from weak through moderate to strong inversion. The g_m/I_D ratio design approach allows the designer to evaluate design trade-offs for different circuit design operation scenarios.

5.2. MOSFET circuit design from weak to strong inversion

As previously identified, the g_m/I_D ratio is a MOSFET characteristic directly related to all channel inversion conditions [8] of the transistor when the transistor is operating in saturation.

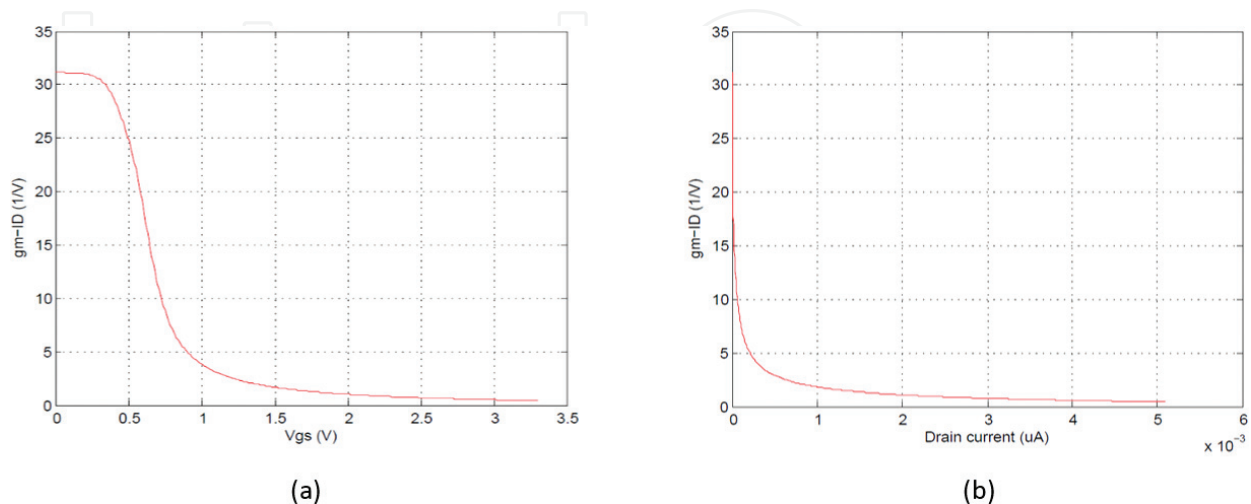


Figure 11. The g_m/I_D ratio of the MOSFET versus: (a) gate-source voltage (V_{GS}) and (b) drain current (I_D).

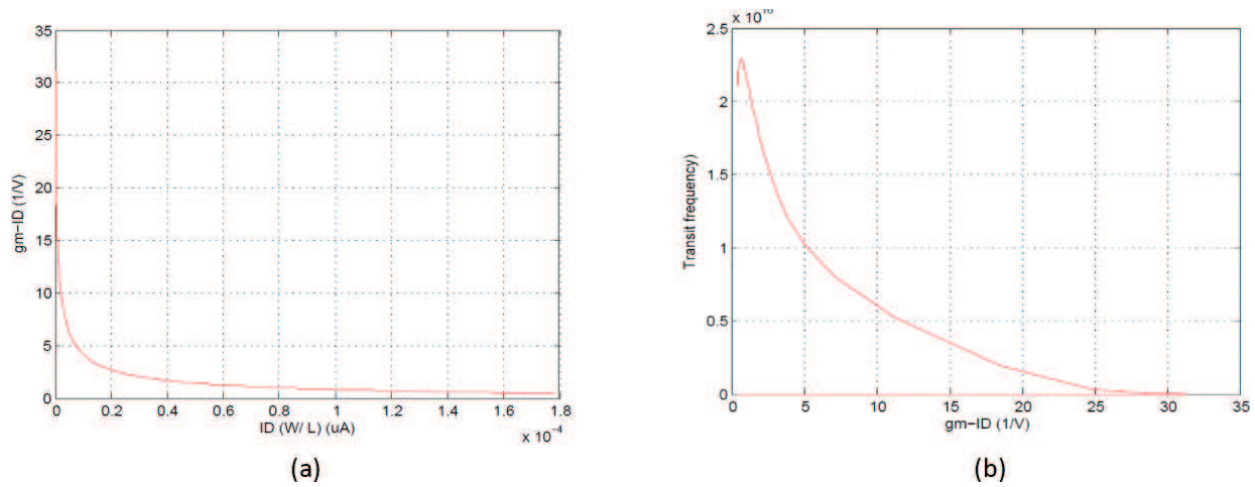


Figure 12. MOSFET characteristics: (a) g_m/I_D ratio versus normalised current ($I_D(W/L)$) and (b) transit frequency (f_T) versus g_m/I_D ratio.

5.2.1. Strong inversion

When v_{GS} is higher than the threshold voltage V_T , the inversion channel is strongly created, and the drift current is dominant. The classical quadratic i_D - v_{GS} MOSFET equation is based on this condition. The value for g_m in strong inversion is independent of MOSFET sizing and process parameters, and it depends only on the DC bias conditions, I_D and v_{eff} . Similarly, g_m/I_D depends only on v_{eff} and the transistor has a small g_m/I_D , a high gate-source voltage, a high drain current, a high f_T , low noise and small dimensions (width and length).

5.2.2. Moderate inversion

The transition between weak inversion and strong inversion is called moderate inversion. Moderate inversion is important for modern analogue CMOS circuit design where designs are created to operate the MOSFET in this condition. Moderate inversion presents a higher g_m/I_D ratio and a lower gate-source voltage in relation to strong inversion combined with smaller gate area and capacitance, and a higher bandwidth compared to weak inversion.

5.2.3. Weak inversion

In weak inversion, the drain current can be determined using an exponential expression. The transistor has a large g_m/I_D , a low gate-source voltage, a low drain current, a low f_T , high noise and large dimensions (width and length).

Each channel inversion condition has different performance characteristics and a circuit design would then be optimised to account for these characteristics. Given that a design can be created by either using the conventional design approach or the g_m/I_D ratio design approach, **Table 1** provides a summary comparison between the approaches.

g_m/I_D design approach	Conventional design approach using V_T , KP and λ
Is valid in all channel operating conditions (weak, moderate and strong) of the MOSFET.	Is valid only in strong inversion of the MOSFET.
Not necessary to create the condition $V_{GS} > V_T$.	Valid only if $V_{GS} > V_T$.
There are different curves for g_m/I_D depending on the inversion region.	Uses the I_D versus V_{GS} and I_D versus V_{DS} curves.
Used for circuits operating on lower power supply voltage levels.	Used for circuits operating on higher power supply voltage levels.
A simplified technique suitable for new evolving fabrication process technologies.	Not suitable for new evolving fabrication process technologies.
A fast design technique as the equations that model the electrical behaviour of circuits can be signified by g_m/I_D .	Not appropriate as a fast design technique. It does not have compact electrical models capable of simple current and voltage relationships.
In this design approach, V_{GS} should be kept as small as possible and transistor gate-source capacitance should be small as possible.	If $(V_{GS} - V_T)$ is small, a large geometry device is required and thus large transistor gate-source capacitance.
The g_m/I_D ratio is used directly as a central design variable to determine circuit performance.	The g_m/I_D ratio is not directly used to determine the performance of the circuit.
Links the variables such as g_m , f_T , I_D and V_{eff} to specifications such as bandwidth and power.	Parameters such as μC_{ox} , V_T and $v_{DS(sat)}$ are considered as poorly defined parameters.
Uses charts and simple equations.	Depends on complex equations and sometimes based on assumptions such as ignoring the effect of channel length modulation (λ).
The g_m/I_D ratio associates small-signal and a large-signal ($g_m \rightarrow I_D$) parameters.	Small- and a large-signal models are not associated.

Table 1. Differences between the g_m/I_D ratio design approach and the conventional design approach.

6. Case study op-amp design

6.1. Introduction

The op-amp is an important differential amplifier circuit that has formed the basis of many analogue and mixed-signal IC designs. In this design case study, a two-stage op-amp has been designed and internally compensated by using negative Miller capacitance in the first stage and Miller capacitance in the second stage as shown in **Figure 5**. The idea behind this approach was to develop circuit stability using Miller compensation and increase the bandwidth using negative Miller compensation. The op-amp was designed using the g_m/I_D ratio design approach in order to consider low-voltage operation and is based on the architecture shown in **Figure 5**, with the circuit as shown in **Figure 6**. When operated on a 3.3 V power supply voltage, the MOSFETs operate in moderate inversion to optimise DC gain, unity gain frequency, PM and GM. The op-amp operation was simulated using Cadence Spectre simulator, the MOSFET models were based on a 0.35 μm CMOS fabrication process, and the AC performance both without and with an output load capacitance was assessed in simulation. A differential input voltage was applied to the op-amp in open loop and a single-ended output voltage monitored.

6.2. Op-amp simulation and results

The op-amp simulation study was performed with two conditions: first, no output load capacitance and second, with a variable output load capacitance. An AC analysis was performed on the op-amp design using typical transistor models with the transistors biased for a 3.3 V single-rail power supply voltage operation.

6.2.1. Study 1: without output load capacitance

In this study, the simulation approach and results obtained concentrated on the frequency response by using the op-amp with different internal compensation techniques and no output load capacitance. First, no internal compensation was incorporated and then compensation using Miller, negative Miller and a combination of Miller and negative Miller arrangements were considered. **Table 2** shows the results of the simulation study that are shown in Bode plot format in **Figure 13**.

For the op-amp with no compensation and negative Miller compensation only, the GM was a positive number (based on the simulator output value), and hence, the op-amp would be unstable in closed loop. In addition, with these two scenarios, the PM was negative (simulator output value) and this also indicated that the op-amp would be unstable in closed-loop. The results show that the gain magnitude and phase shift are controllable with the different

C_{NM} and $C_M = 0.31$ pF	No compensation	Negative Miller only	Miller only	Miller and negative Miller
DC gain (dB)	82.5	82.5	82.5	82.5
Phase margin (degrees)	-65.19	-52.56	57.47	63.03
Unity gain frequency (MHz)	1073	1177	177.33	205.54
Gain margin (dB)	14.27	11.08	-10.61	-9.93

Table 2. Open-loop op-amp performance with different compensation techniques.

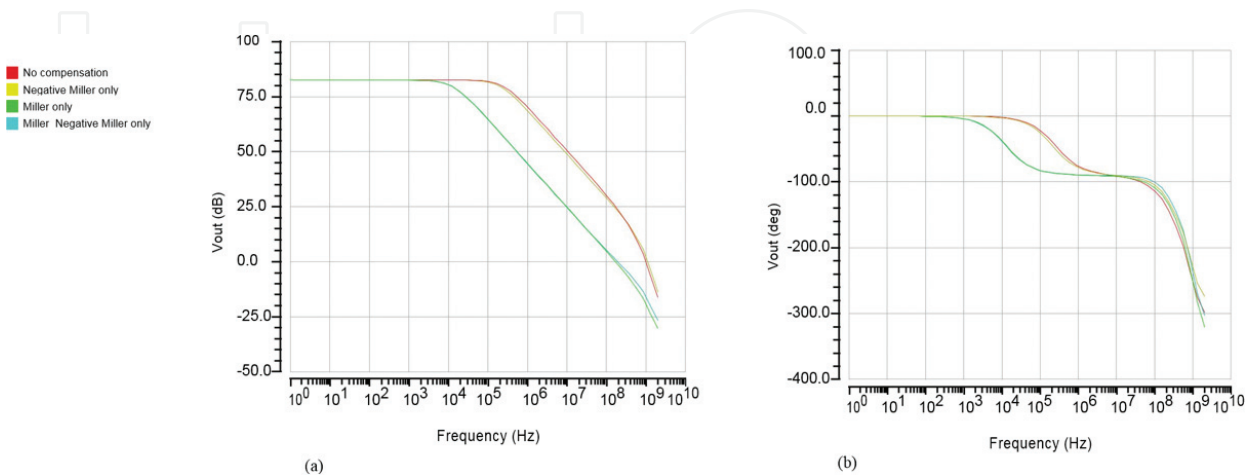


Figure 13. Bode plot of the open-loop op-amp performance with different compensation techniques: (a) gain and (b) phase (Spectre simulation on the transistor circuit model).

compensation techniques and that the choice of compensation technique would determine whether the op-amp is stable or not in closed loop.

6.2.2. Study 2: with output load capacitance

In this study, the simulation approach and results obtained concentrated on the frequency response by using the op-amp with different internal compensation techniques and an output load capacitance with values of 0.1, 0.5 and 1.0 pF. **Table 3** shows the results of the simulation study that are shown in Bode plot format in **Figure 14**.

6.3. Transfer function analysis

An additional form of analysis undertaken with this design was to consider the transfer function for the op-amp input-output relationship. The transfer function is a useful form for evaluating the op-amp frequency response. For a typical op-amp, then the transfer function would contain a large number of poles and zeros. This form would be too complex for initial design development, and so it is common to approximate the transfer function to a simple form that contains typically only two or three poles. These can be estimated from the small-signal equivalent circuit. In addition, once the op-amp design has been created, it is possible to extract the poles and zeros using the circuit simulator and to minimise the initial transfer function of the circuit model having large number of poles and zeros into a simpler transfer

Characteristic	No output load capacitance	0.1 pF	0.5 pF	1.0 pF
DC gain (dB)	82.5	82.5	82.5	82.5
Phase margin (degree)	63.03	61.39	55.99	50.96
Unity gain frequency (MHz)	205.54	203.83	195.54	183.38
Gain margin (dB)	−9.93	−9.80	−9.44	−9.23

Table 3. Open-loop op-amp performance with different output load capacitance values (with combined Miller and negative Miller compensation).

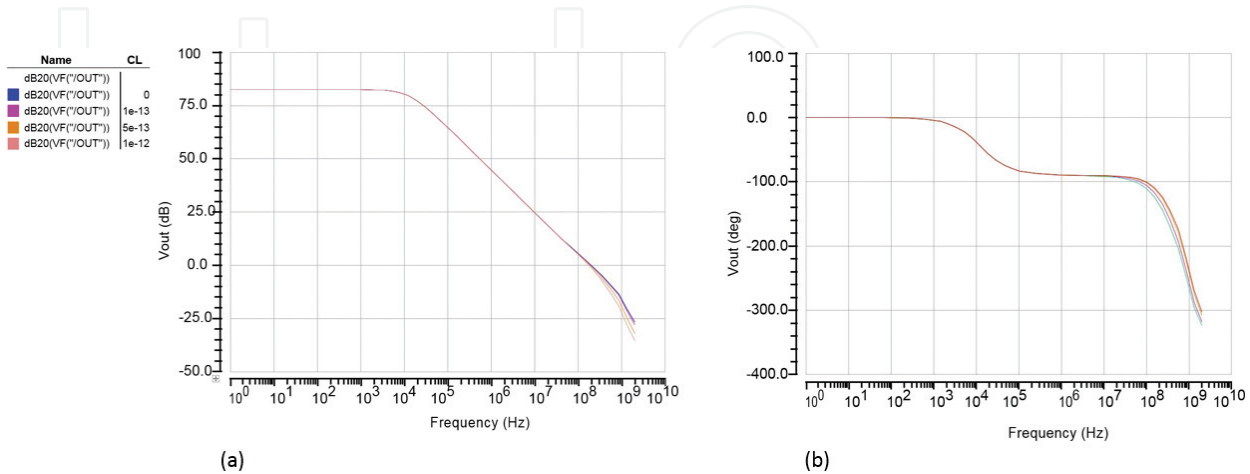


Figure 14. Frequency response of the open-loop op-amp design with different load capacitances: (a) gain and (b) phase (Spectre simulation on the transistor circuit model).

function having a reduced number of poles and zeros. The process for investigating the circuit operation and simplifying the transfer function considered was to:

1. Extract the poles and zeros from the circuit model using Cadence Spectre simulator.
2. Transfer the pole and zero values to MATLAB and create the transfer function.
3. Use MATLAB to reduce the number of poles and zeros in the transfer function and simulate the transfer function behaviour to ensure that the reduced transfer function Bode plot and key characteristics are comparable to the original transfer function.
4. Translate the new transfer function to high-level Verilog-A model and compare the Verilog-A model to the original analogue circuit simulation results and the MATLAB simulation study results.

From the analysis of the open-loop op-amp pole and zero locations as extracted from the circuit, the initial transfer function consisted of 23 poles and 23 zeros. Although it would be expected that the number of poles should be greater than the number of zeros in the transfer function for a strictly proper system, the original 23 pole and zero transfer function extracted is used in the following discussion, and hence, the results are used with a certain level of caution. These were the raw results obtained from the pole-zero analysis in Spectre. It should be noted that the transfer function has the same number of poles and zeros and hence would be referred to as a biproper system. When the transfer function is biproper, it is not reflective of a realisable system at high frequencies as it would have a finite gain at the higher signal frequencies. A strictly proper system where the gain reduces to zero at higher frequencies, as would be expected in a real op-amp, the number of poles must be greater than the number of zeros. This effect can be seen when simulating the transfer function for this design at the higher signal frequencies that would not actually be encountered. To simplify this transfer function from original number of poles and zeros, MATLAB was used to reduce the transfer function to one with just three poles and zeros. **Table 4** shows the resulting performance of the different simulation models, noting that the response of the three models would be valid only up to a certain frequency as the

Number of poles/zeros	Performance	Spectre	MATLAB	Verilog-A
23/23 (MATLAB and Verilog-A transfer function models only)	Gain margin (dB)	9.938	9.95	9.938
	Unity gain frequency (MHz)	205.5	198	205.5
	Phase margin (degrees)	63	63	63
	DC gain (dB)	82.47	82.5	82.47
3/3 (MATLAB and Verilog-A transfer function models only)	Gain margin (dB)	–	10.7	10.64
	Unity gain frequency (MHz)	–	192	200.8
	Phase margin (degrees)	–	54.4	54.61
	DC gain (dB)	–	83.9	83.88

Table 4. Simulated op-amp performance comparison (Spectre (transistor level model), MATLAB (transfer function) and Verilog-A (transfer function)).

transfer functions model a biproper system with a finite high frequency gain rather than a realistic strictly proper transfer function.

7. Op-amp design and operation at lower power supply voltages

Designing and operating analogue circuits at low power supply voltages are challenging tasks. In the past, the circuits typically encountered were designed to operate at higher voltage levels, and so circuit performance limitations due to a limited voltage range was not an issue for many designs. Today, the operation of electronic circuits with low-voltage power supplies is now a requirement for use in electronic systems where size, weight, and power consumption are especially important. For example, in battery-operated portable equipment, a reduction in the battery requirements such as size, weight and energy capacity can provide cost reduction benefits in equipment production, purchase and use as well as making the equipment more portable. The move towards low-voltage operation can be considered from three different perspectives:

1. The increasing use of battery-operated portable systems requires low-power dissipation in order to prolong circuit operation time with a battery energy source.
2. Reduced feature sizes in modern VLSI fabrication processes results in larger electric fields that, unless the power supply voltages are reduced, result in reliability problems.
3. Reduced feature sizes in modern VLSI fabrication processes results in a higher density of the electronics that increases the power dissipation per unit area. The low-voltage operation can be used to reduce the power dissipation per unit area.

As device geometries in CMOS are reduced, the benefits include reduced size, higher operating speeds and reduced power consumption (due to the ability to operate the designs on lower power supply voltage levels), which are mostly exploited in the digital parts of a design. However, this move comes at a cost of introducing device characteristics not seen with larger device geometries. Reducing the power supply voltage has been exploited effectively in digital circuits, but analogue circuits exploiting reduced geometry and voltage operation need to account for a range of circuit performance limiting issues not a concern in digital. In analogue circuits, reducing device geometries and power supply voltage levels have an enormous impact on the analogue circuit capability. For example, as the device geometries become smaller and circuit densities increase, currents in the circuit may need to be reduced in order to prevent excessive temperature increments due to the power consumption per unit area. In addition, reliability problems would exist at higher voltage levels (voltage levels which were commonly used in the past, such as 5 V, but now would be too high for reliable circuit operation) due to excessively high electric fields that would exist. Process variations as CMOS technology move to the lower (deep) sub-micron levels and their effects on low geometry devices, such as transistor width and length dimensions, means that analogue circuit performance can vary widely between devices of the same type and this is accompanied in reduced device geometries by an increase in transistor leakage currents. Whilst the geometries reduce, the transistor threshold voltage (V_T) is, however, remaining relatively constant, and as the power supply voltage is reduced, this causes as

reduction in the available voltage range for circuit operation (a reduction in the $(V_{DD} - V_T)$ value). Analogue circuits would typically require the creation of bias currents for circuits such as current mirrors which are created using transistors. The need to account for the transistor to be operating in either the weak, moderate or strong inversion regions of operation and the resulting transistor performance differences due to the region of operation would need to be accounted for. The use of fully differential structures is considered given their superior performance with circuit parameters such as $CMRR$ and $PSRR$ (power-supply rejection-ratio), lower signal distortion and wider signal swing range. Finally, the need to maximise dynamic signal range which often requires a rail-to-rail output voltage range and for op-amps operated in unity-gain configuration, the input stage should also have a rail-to-rail common mode input voltage range [9].

8. Conclusions

The op-amp is an integral part of the on-chip analogue signal conditioning circuitry for the front-end section of mixed-signal ICs. In this chapter, the design of the two-stage op-amp was considered, which was designed using a $0.35\ \mu\text{m}$ CMOS fabrication process and working on a single rail 3.3 V power supply. Considerations were given to low-voltage design (operating at and below 3.3 V) by using the g_m/I_D ratio design approach and the use of both Miller and negative Miller compensation as an internal compensation scheme for op-amp stability and signal bandwidth reasons. The discussion was accompanied by an op-amp case study design and simulation study results that focused on AC performance.

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