Chapter 2

A Reduced Switch Asymmetric Multilevel Inverter Topology Using Unipolar Pulse Width Modulation Strategies for Photovoltaic Application

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Additional information is available at the end of the chapter

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Abstract

A new design of multilevel inverter configuration is proposed for reducing the component count and improving the quality of waveform in a photovoltaic system. The proposed configuration operates at the binary asymmetric condition for generating the large amount output voltage level with small amount harmonic distortion. Unipolar trapezoidal reference with triangular carriers is used for generating the desired switching pulses to generate the required output voltage level. The proposed configuration requires eight unipolar switches for generating the 31-level output voltage level with total harmonic distortion of 3.18% without using any filters. The value of %total harmonic distortion (THD) satisfies the IEEE 519 harmonic standard. Separate DC sources of proposed configuration are replaced by the array of photovoltaic panels for testing the configuration with the renewable energy source. The proposed configuration is tested with an experimental setup for proving the operation of it. Selected simulation and experimental results are shown for the verification of proposed configuration ability.

Keywords: multilevel inverter, pulse width modulation, trapezoidal waveform, reduced switch inverter

1. Introduction

The theory of multilevel inverter has been discussed over 30 years ago. The multilevel inverter (MLI) has many advantages when compared to conventional two-level inverter such as withstanding high voltage capability, lower harmonic distortion, lower switching losses, lower switching stress, and producing high quality of output voltage with better electromagnetic compatibility [1]. Due to that numerous advantages, the adoption of multilevel inverter has been tremendously expanded in the area of medium or high power and medium or high voltage application [2]. Generally, diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and cascaded H-bridge multilevel (CHBMLI) are three remarkable traditional MLI topologies [3]. The drawback of conventional MLIs is the total number of components. The count of components is directly proportional to the number of levels. The balancing of voltage across DC bus capacitor in FCMLI and DCMLI is the difficult task. Also, the presence of clamping diodes and clamping capacitors in DCMLI and FCMLI, respectively, makes the circuit complex, costly and large size [4]. To overwhelm those drawbacks, numerous topologies for multilevel inverter have been introduced recently.

Reduced switch multilevel inverter configurations have their own advantages and disadvantages. In Refs. [5–20], the configurations require bidirectional switches for achieving the desired output voltage level. Utilizing of bidirectional switches increases, the total count of switches in those configurations, because the combination of two unipolar switches makes one bidirectional switch using the concept of emitter coupled to both switches. In Refs. [21–25], the transformers have utilized for generating the required output voltage level. The usage of a transformer in that configuration makes the system bulky, costly, less life span and requires more maintenance. The transformer is connected to the secondary side in series to achieve the required output voltage level. In Refs. [8, 10, 12, 14], configuration utilizes more diode and capacitors for generating the required output voltage level. The balancing of capacitor voltage is more important to achieve the particular level of the output voltage waveform.

In this chapter, the reduced switch configuration is proposed without any bidirectional switches and transformer. Therefore, the proposed configuration size and cost are considerably low. It requires only eight switches for generating the 31-level output voltage level with total harmonic distortion of 3.18%. Multicarrier unipolar trapezoidal reference with triangular carrier pulse width modulation technique is utilized for generating the switching pulses for the proposed configuration. The proposed configuration has a minimum number of conducting switches for generating per voltage level. Also, this configuration requires minimum power loss (switching loss + conduction loss) for a different number of levels when compared to other MLIs. Also, the proposed configuration is tested with the photovoltaic system for checking the ability of it.

The remaining section of this chapter is as follows: Section 2 describes the operation of proposed multilevel inverter configuration with an asymmetric condition. Section 3 describes with the multicarrier unipolar trapezoidal pulse width modulation with three different carriers such as phase disposition, alternative phase opposition and disposition and variable frequency. Section 4 describes with proposed multilevel inverter configuration integrated with the photovoltaic system. Section 5 describes with results and discussion of the proposed multilevel inverter. Section 6 ends with conclusion of this chapter.

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2. Proposed multilevel inverter configurations

The proposed multilevel inverter configuration is the combination of power semiconductor switches and bypass diodes. **Figure 1a** shows the basic structure for the proposed MLI configuration. The bypass diode is connected in parallel with the combination of power semiconductor switch and DC voltage source. The basic structure has two different modes of operation. When the switch T_1 is turned on, the V_{dc1} voltage appears across the diode D1. Therefore, the value of output voltage is $2V_{dc}$ ($V_{dc1} + V_{dc2}$). When the switch T_1 is turned off, the bypass diode conducts to generate the V_{dc} output voltage. The higher number of levels can generate the cascading connection of proposed basic structure. Symmetric and asymmetric are the two different conditions of multilevel inverter for generating the output voltage level. Generally, symmetric multilevel inverter produces the minimum count of output voltage level when compared to an asymmetric multilevel inverter. **Figure 1b** shows the proposed multilevel inverter configuration

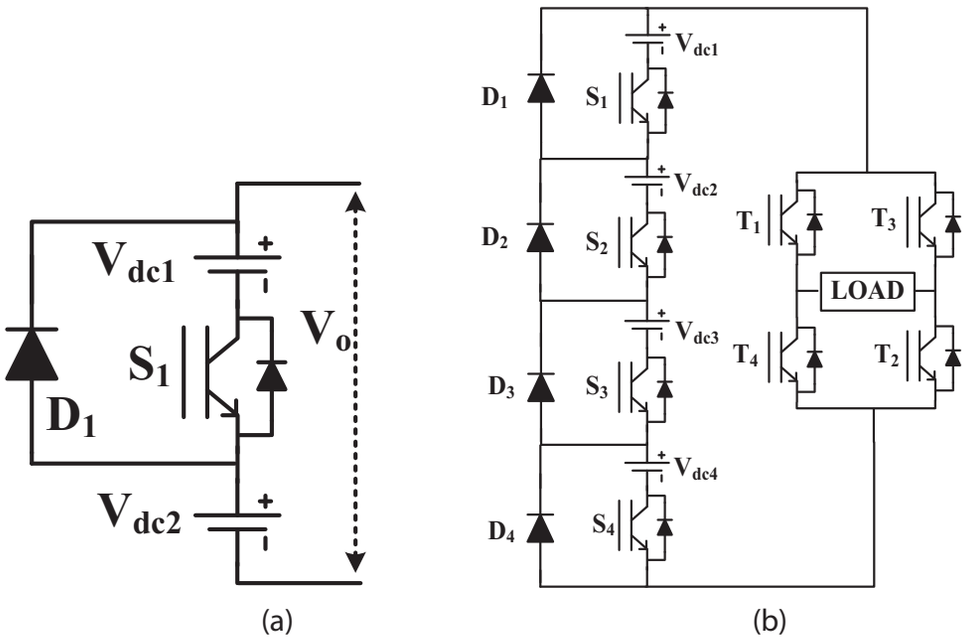

Figure 1. Proposed configuration. (a) Basic structure. (b) Proposed multilevel inverter configuration.

Parameters	Generalized formulas
Value of DC sources	2^n where $n = 0, 1, 2\ldots$
Ratio of DC sources	1: 2: 4: 8
Number of switches	$k + 4$
Number of DC source	k
Number of diodes	$k + 4$
Number of driver circuit	$k + 4$
Number of level	$2^{k+1} - 1$

Table 1. Generalized formula for the different parameters in proposed multilevel inverter.

for generating the 31-level output voltage. The DC sources are assumed as an asymmetric condition in which binary sequence is adopted. The ratio of binary sequence is 1:2:4:8. The configuration is the combination of single phase H-Bridge inverter and reduced switch configuration. The reduced switch configuration contains the set of single DC source, switch and bypass diode is connected in series. **Table 1** shows the generalized formula for the proposed multilevel inverter configuration. **Table 2** shows the switching table for the proposed topology for generating the 31-level output voltage in both positive and negative polarity.

Modes	Conducting switches and diodes	Output voltage	Modes	Conducting switches and diodes	Output Voltage
1	$S_1, D_2, D_3, D_4, T_1, T_2$	V_{dc}	1	$S_1, D_2, D_3, D_4, T_3, T_4$	$-V_{dc}$
2	$S_2, D_1, D_3, D_4, T_1, T_2$	$2V_{dc}$	2	$S_2, D_1, D_3, D_4, T_3, T_4$	$-2V_{dc}$
3	$S_1, S_2, D_3, D_4, T_1, T_2$	$3V_{dc}$	3	$S_1, S_2, D_3, D_4, T_3, T_4$	$-3V_{dc}$
4	$S_3, D_1, D_2, D_4, T_1, T_2$	$4V_{dc}$	4	$S_3, D_1, D_2, D_4, T_3, T_4$	$-4V_{dc}$
5	$S_1, S_3, D_2, D_4, T_1, T_2$	$5V_{dc}$	5	$S_1, S_3, D_2, D_4, T_3, T_4$	$-5V_{dc}$
6	$S_2, S_3, D_1, D_4, T_1, T_2$	$6V_{dc}$	6	$S_2, S_3, D_1, D_4, T_3, T_4$	$-6V_{dc}$
7	$S_1, S_2, S_3, D_4, T_1, T_2$	$7V_{dc}$	7	$S_1, S_2, S_3, D_4, T_3, T_4$	$-7V_{dc}$
8	$S_4, D_1, D_2, D_3, T_1, T_2$	$8V_{dc}$	8	$S_4, D_1, D_2, D_3, T_3, T_4$	$-8V_{dc}$
9	$S_1, S_4, D_2, D_3, T_1, T_2$	$9V_{dc}$	9	$S_1, S_4, D_2, D_3, T_3, T_4$	$-9V_{dc}$
10	$S_2, S_4, D_1, D_3, T_1, T_2$	$10V_{dc}$	10	$S_2, S_4, D_1, D_3, T_3, T_4$	$-10V_{dc}$
11	$S_1, S_2, S_4, D_3, T_1, T_2$	$11V_{dc}$	11	$S_1, S_2, S_4, D_3, T_3, T_4$	$-11V_{dc}$
12	$S_3, S_4, D_1, D_2, T_1, T_2$	$12V_{dc}$	12	$S_3, S_4, D_1, D_2, T_3, T_4$	$-12V_{dc}$
13	$S_1, S_3, S_4, D_2, T_1, T_2$	$13V_{dc}$	13	$S_1, S_3, S_4, D_2, T_3, T_4$	$-13V_{dc}$
14	$S_2, S_3, S_4, D_1, T_1, T_2$	$14V_{dc}$	14	$S_2, S_3, S_4, D_1, T_3, T_4$	$-14V_{dc}$
15	$S_1, S_2, S_3, S_4, T_1, T_2$	$15V_{dc}$	15	$S_1, S_2, S_3, S_4, T_3, T_4$	$-15V_{dc}$

Table 2. Switching table for generating 31-level output voltage in proposed configuration.

3. Switching techniques

The pulse width modulation is the most important and effective switching technique for controlling the multilevel inverter output voltage. Based on PWM technique, the output voltage can be easily converted to sinusoidal waveform by utilizing the less size of passive filters. Generally, sinusoidal pulse width modulation technique (SPWM) is utilized for generating the switching pulses to achieve the desired output voltage waveform [26–29]. In this chapter, the proposed configuration switches are triggered by using the trapezoidal reference with triangular carriers. Trapezoidal pulse width modulation technique is one of the types of advanced pulse width modulation technique. This technique provides better performance output voltage when compared with sinusoidal pulse width modulation technique which is the main advantage [28]. The combination of two slopes and one horizontal line makes the trapezoidal reference waveform. Generally, the waveform can be attained by the triangular reference waveform by limiting the magnitude or peak value of the waveform.

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The angle of horizontal line of the waveform is as follows:

$$2\varnothing = (1 - \sigma)\pi \tag{1}$$

where σ is called the triangular factor. If the triangular factor is $\sigma = 1$, the waveform shape will become triangular waveform. The shape of trapezoidal waveform is purely depending on the location of slope angle (α). **Figure 2** shows the different angle of slope for the trapezoidal waveform. The harmonic content and waveform quality will differ based on the different locations of the slope angle (α). The mathematical formula for calculating the harmonic amplitude for different slope of different order is given by

$$A_n = \frac{4}{\pi}\int_0^{\pi/2} F(\theta)\,\sin n\theta\, d\theta \tag{2}$$

where

$$F(\theta) = \begin{cases} 1/\alpha & 0^\circ < \theta < \alpha \\ 1 & \alpha < \theta < 90^\circ \end{cases} \tag{3}$$

So, the Eq. (8) can be written as follows

$$A_n = \frac{4}{2\pi}\left[\left[\frac{-\theta k\cos(n\theta)}{n}\right]\right]_0^{\alpha} + \frac{1}{n}\int_0^{\alpha} k\cos(n\theta)\, d\theta + \frac{4}{\pi}\int_0^{\pi/2} \sin(n\theta)\, d\theta \tag{4}$$

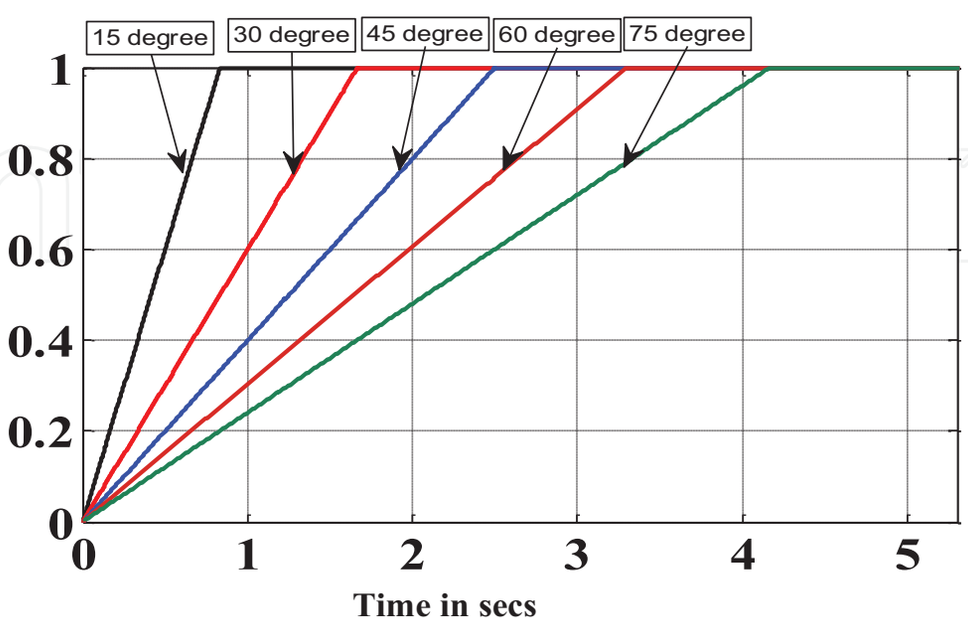

Figure 2. Different angle of slope in trapezoidal reference.

The above equation can be simplified and rewritten as follows

$$A_n = \frac{4}{n^2\pi} \times \frac{\sin(n\alpha)}{\alpha} \tag{5}$$

Figure 3 shows the harmonic content of different harmonic order for different slope angle. From that **Figure 3**, it is evident that the harmonic order value increases when the slope angle near to zero degree. If the slope angle moves towards to 90 degree, the harmonic order value decreases. In this paper, the slope of the trapezoidal reference waveform is considered as 60°. Also, in this paper, unipolar reference is considered for generating the switching pulses. In unipolar, the carriers count is reduced half of the value when compared to bipolar PWM technique, which is the main advantage of unipolar PWM method [26]. The proposed topology is tested with phase disposition (PD) carrier arrangement. Phase disposition defines that the utilization of 15 carriers is each in phase with same amplitude and frequency. The representation of unipolar trapezoidal reference with phase disposition carriers is shown in **Figure 4**.

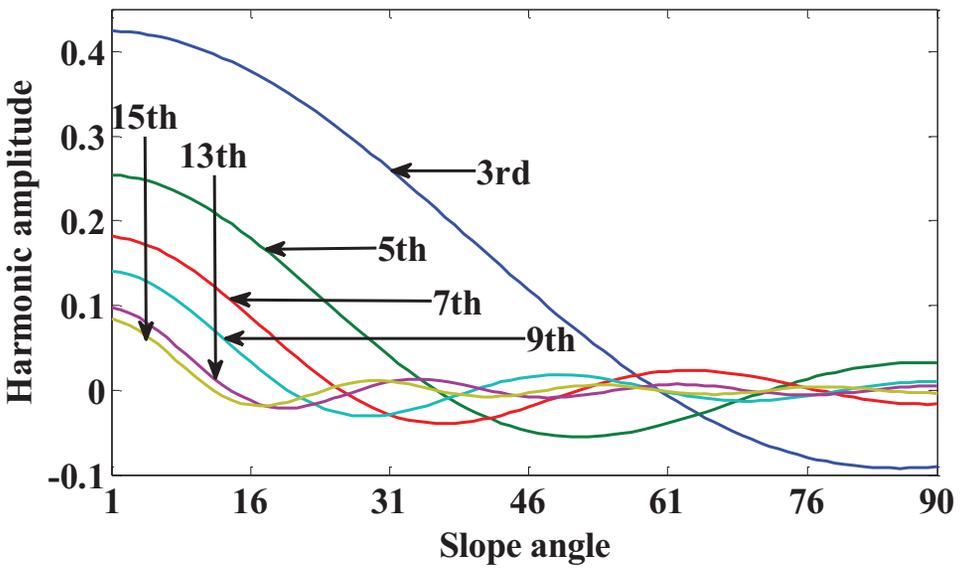

Figure 3. Harmonic content for different individual order in different slope angle of trapezoidal reference.

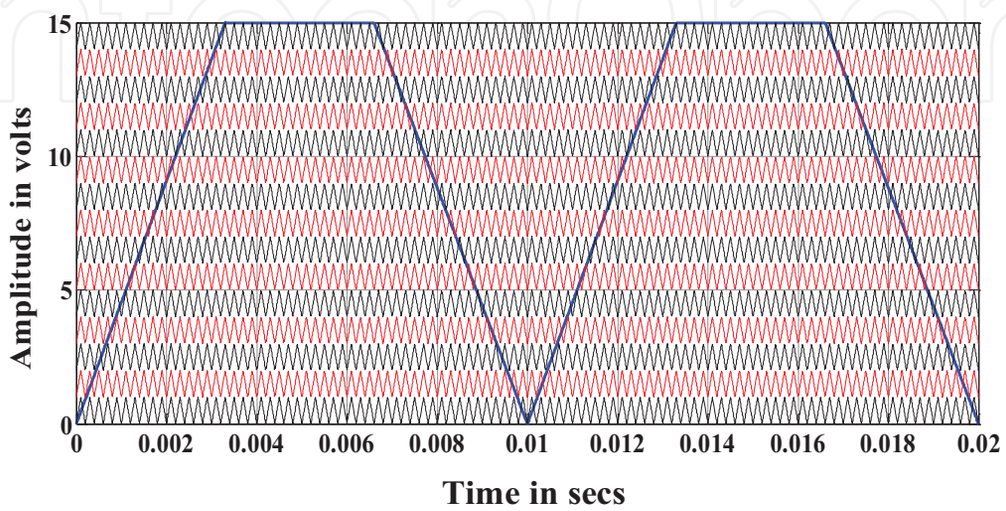

Figure 4. Unipolar trapezoidal reference with PD carrier arrangement.

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4. Proposed MLI integrated with photovoltaic system

The proposed multilevel inverter requires four separate DC sources for generating the 31-level output voltage. So, the separate DC sources are replaced by the photovoltaic panel or array of photovoltaic panel depends on the input value of proposed multilevel inverter configuration. In this work, 80 W photovoltaic panel is considered. **Figure 5** shows that the proposed multilevel

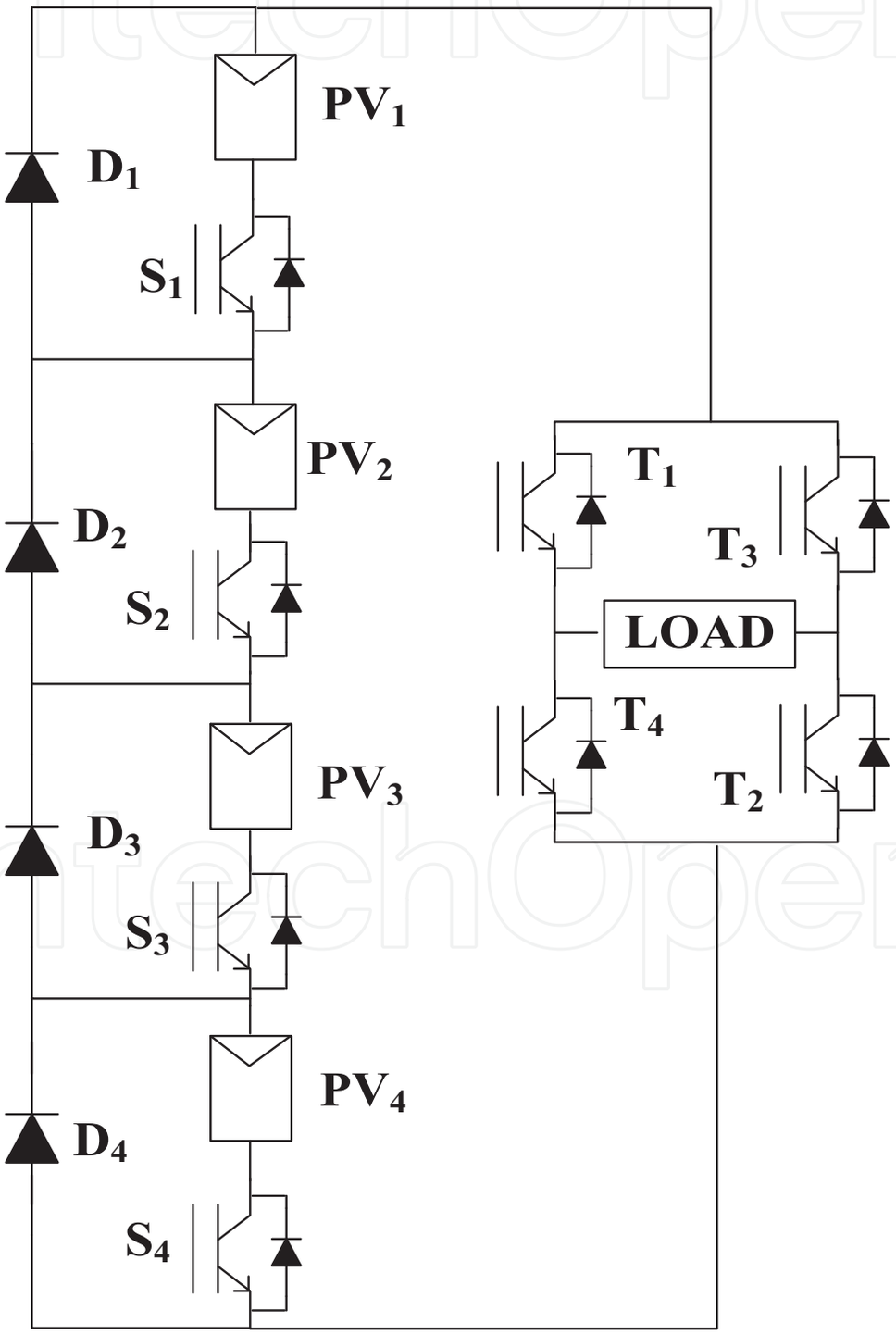

Figure 5. Proposed configuration integrated with photovoltaic system.

inverter is integrated with the photovoltaic system. For a conventional type, the integration of MLI with photovoltaic system requires separate solar panel with separate boost converter with MPPT technique for achieving the required output voltage level. Therefore, the system becomes complexity, and an initial cost of the system is too high. To overcome this drawback, this chapter proposed that the array of PV panels is connected in the series manner to achieve the required output voltage. The array of PV panels is directly connected to the proposed MLI for replacing the each DC source of it. In future, the same study is further extended with the high gain multi-output converters with appropriate MPPT techniques for reducing the count of PV array panels. The first DC source of proposed MLI is replaced by a single photovoltaic panel. The second DC source of proposed MLI is replaced by the series connection of two 80 W photovoltaic panel. The third and fourth DC sources are placed by the series connection of four panels and eight panels, respectively. **Figure 6** shows the single diode model equivalent circuit for the photovoltaic cell. **Figures 7** and **8** show the I-V and P-V characteristics of the PV model. The generalized formula for photovoltaic panel is modeled as follows [30, 31]

$$I = I_{PV} - I_o\left[exp\left(\frac{V + R_s I}{aV_t}\right) - 1\right] - \frac{V + R_s I}{R_p}\ ;\ V_t = \frac{V_s kT}{q} \tag{6}$$

$$I_{PV} = (I_{PV,n} + K_I \Delta_t)\frac{G}{G_n} \tag{7}$$

$$I_o = \frac{I_{sc,n} + K_I \Delta_t}{exp[(V_{oc,n} + K_V \Delta_t)/aV_t] - 1} \tag{8}$$

where k, a, T and q denote Boltzmann constant ($1.3806503 \times 10^{-23}$ J/K), diode ideality constant, absolute temperature (K), and electron charge ($1.60217646 \times 10^{-19}$ C), respectively. I_{PV} and I_o denote photovoltaic current and saturation current of array, respectively. $I_{PV,n}$ represents

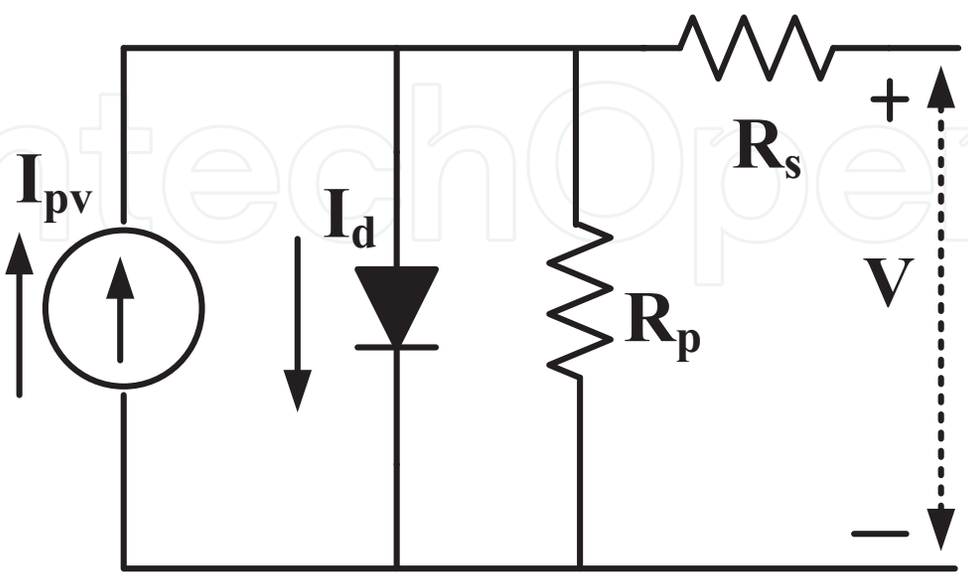

Figure 6. Single diode model equivalent circuit.

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nominal PV current, and R_s and R_p denote equivalent series and parallel resistance of solar cell respectively. V_t denotes thermal voltage. N_s and N_p denote solar cells connected in series and solar cells connected in parallel, respectively. $V_{oc,n}$ and $I_{sc,n}$ indicate open circuit voltage and nominal short circuit current, respectively; K_V and K_I represent the short circuit voltage/temperature co-efficient and short circuit current/temperature co-efficient, respectively; T_n indicates nominal temperature (K); G and G_n represent irradiation (W/m^2) on the device surface and nominal irradiation and Δ_t indicates $T - T_n$, difference between actual and normal temperature. **Table 3** shows the parameters value for the 80 W photovoltaic panel.

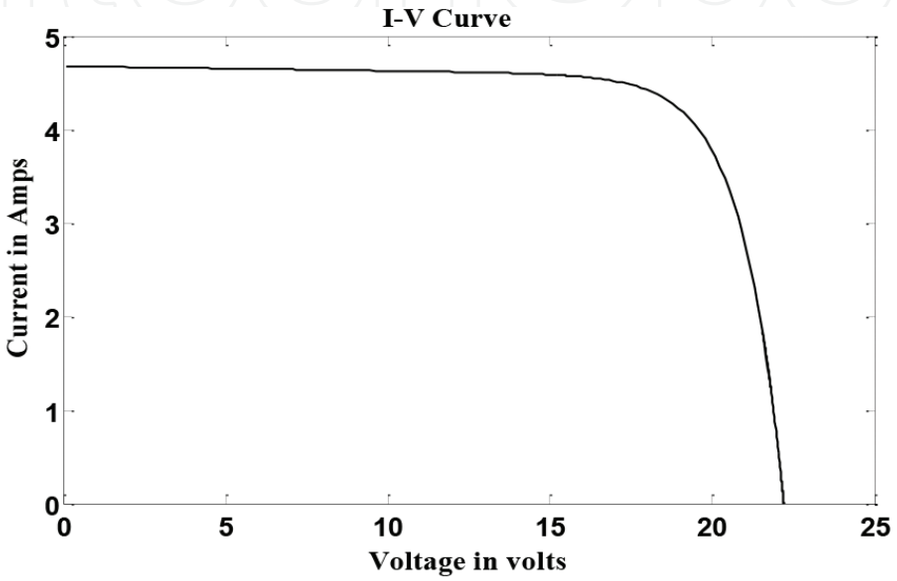

Figure 7. I-V characteristics of photovoltaic panel.

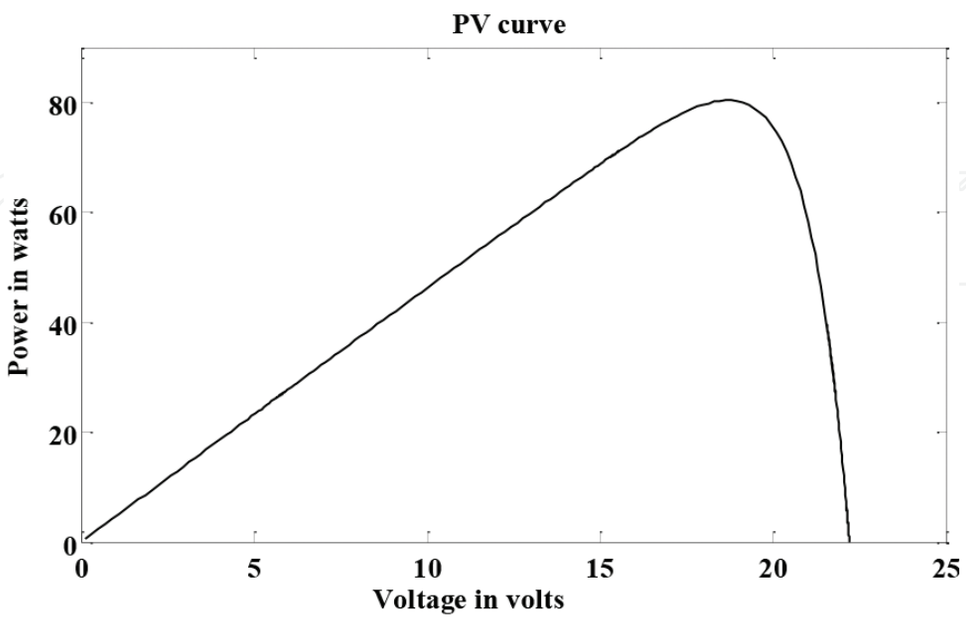

Figure 8. P-V characteristics of photovoltaic panel.

Parameters	Values
Short circuit current (I_{sc})	4.71 A
Open circuit voltage (V_{oc})	22.24 V
Maximum power point voltage (V_{mp})	18.33 V
Maximum power point current (I_{mp})	4.37 A
Maximum power (P_{mp})	80 W
Capacitors (C_1–C_4)	1500 μF

Table 3. Different parameters value for photovoltaic panel.

5. Result and discussion

The conventional CHBMLI and proposed MLI configuration are tested with MATLAB/SIMULINK for generating the 9-level and 31-level output voltage with trapezoidal pulse width modulation technique for the same number of DC source. Here, the conventional CHBMLI consists of four single H-bridge multilevel inverters which are connected in series. The conventional CHBMLI and proposed MLI configuration are tested with laboratory-based experimental set up for generating the desired output voltage using dSpace 1104 real-time controller. The unipolar PWM trapezoidal reference with triangular carriers is utilized for generating the switching pulses of the proposed multilevel inverter configuration switches in simulation and experimental step-up. Insulated Gate Bipolar Transistor (IGBT-FGA25N120) is utilized as switching devices and TLP250 as the IGBT driver for proposed topology. The main reason for selecting this PWM strategy is to produce better harmonic profile as well as to radically reduce the utilization of carrier count. **Figures 9** and **10** show the simulation 9-level output voltage, output current and their harmonics plot for output voltage, respectively, for conventional CHBMLI. **Figures 11** and **12** show the experimental result of 9-level output voltage and output current and their harmonics plot for the conventional CHBMLI. The conventional CHBMLI is

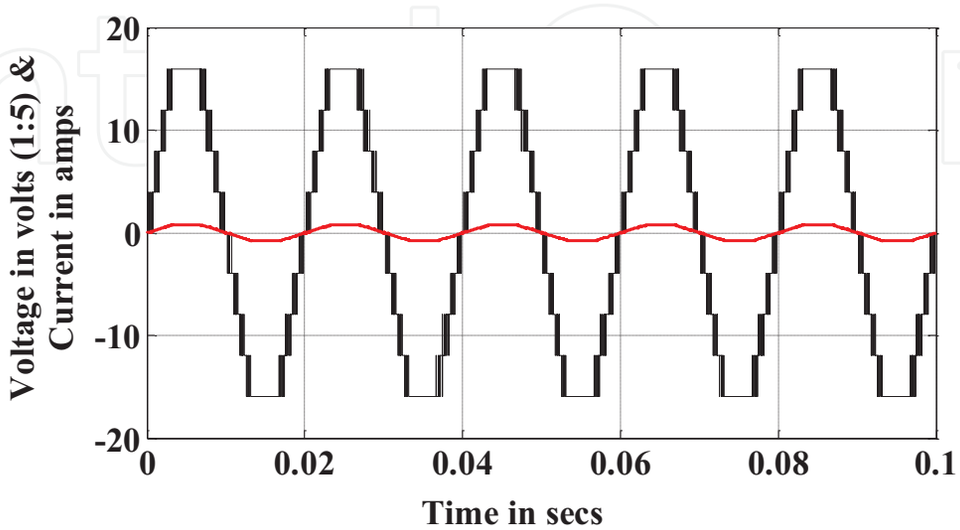

Figure 9. Simulation results for output voltage and current in conventional CHBMLI.

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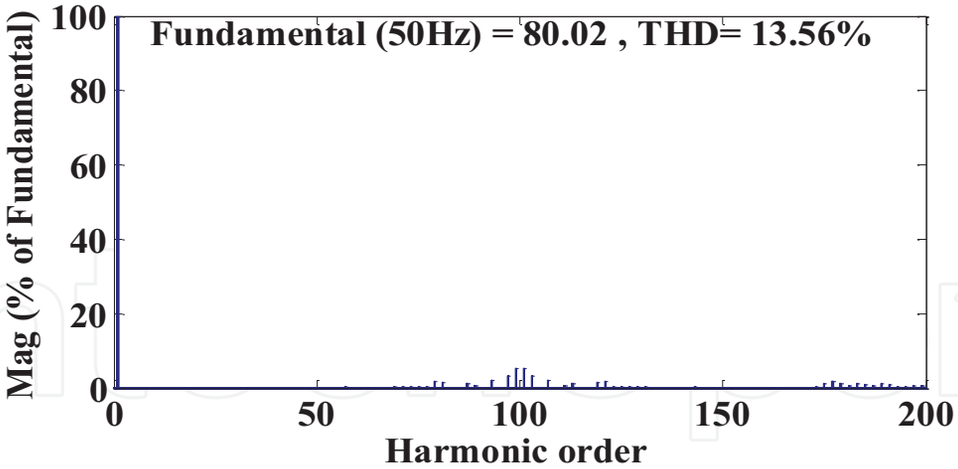


Figure 10. Harmonics plot for output voltage in conventional CHBMLI.

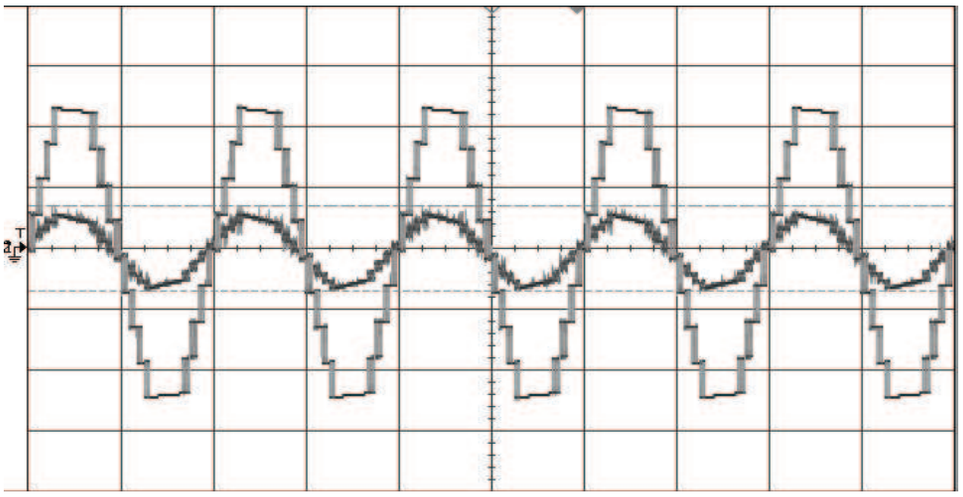
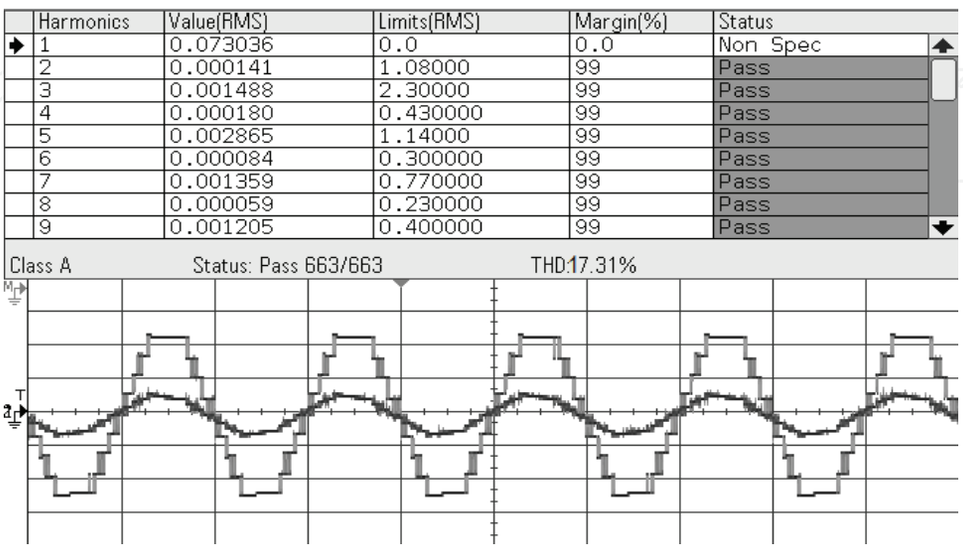


Figure 11. Experimental results for output voltage and current in conventional CHBMLI (CH1: 30 V/div, CH2: 5 A/div).



Harmonics	Value(RMS)	Limits(RMS)	Margin(%)	Status
1	0.073036	0.0	0.0	Non Spec
2	0.000141	1.08000	99	Pass
3	0.001488	2.30000	99	Pass
4	0.000180	0.430000	99	Pass
5	0.002865	1.14000	99	Pass
6	0.000084	0.300000	99	Pass
7	0.001359	0.770000	99	Pass
8	0.000059	0.230000	99	Pass
9	0.001205	0.400000	99	Pass

Figure 12. Experimental Harmonics plot for output voltage in conventional CHBMLI.

tested with the photovoltaic panels by replacing the separate DC sources. **Figures 13** and **14** show the output voltage and output current and their harmonics plot for the CHBMLI with photovoltaic systems. **Figures 15** and **16** show the simulation output voltage, output current and their harmonics plot for trapezoidal reference with PD carriers. **Figures 17** and **18** show the experimental result of output voltage and output current and their harmonics plot for the proposed topology. Also, this configuration is tested with the photovoltaic panels by replacing the separate DC sources. **Figures 19** and **20** show the output voltage and output current and their harmonics plot for the proposed configuration with photovoltaic systems. The power loss is the addition of switching losses and conduction losses. The switching losses and conduction losses can be calculated using the following formulas [18–19]

$$L_{sw} = \sum_{k=1}^{N_{sw}} \left(\sum_{i=1}^{N_{on,k}} E_{on,k,i} + \sum_{i=1}^{N_{off,k}} E_{off,k,i} \right) \tag{9}$$

$$L_c(t) = \sum_{k=1}^{N_{sw}} (L_{c,sw,k}(t) + L_{c,d,k}(t)) \tag{10}$$

Figure 21 shows that the total power loss versus a different number of levels for the proposed configuration. Also, the proposed configuration is tested with different modulation indices. **Table 4** shows the comparison table for proposed configuration with conventional MLIs in terms of many factors. From that **Table 4**, it is clearly understood that the proposed configuration requires lesser component count for generating the desired output voltage level. Also, the minimum count of conducting switches is required for generating each voltage level when compared to conventional MLIs. **Figure 22** shows the efficiency graph for the proposed configuration for different modulation indices. Therefore, the proposed configuration provides better results in terms of number of levels, efficiency and switching

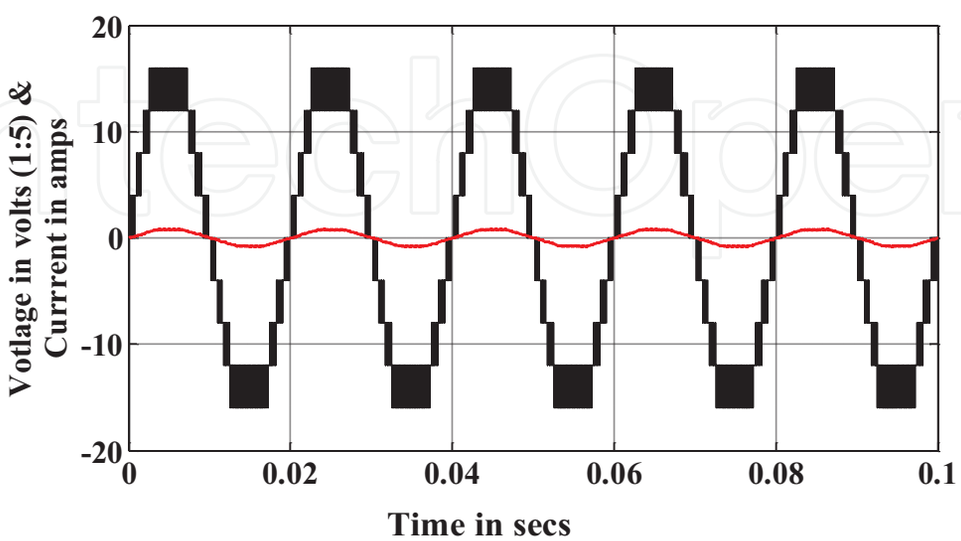


Figure 13. Output voltage and current for conventional CHBMLI integrated with PV.

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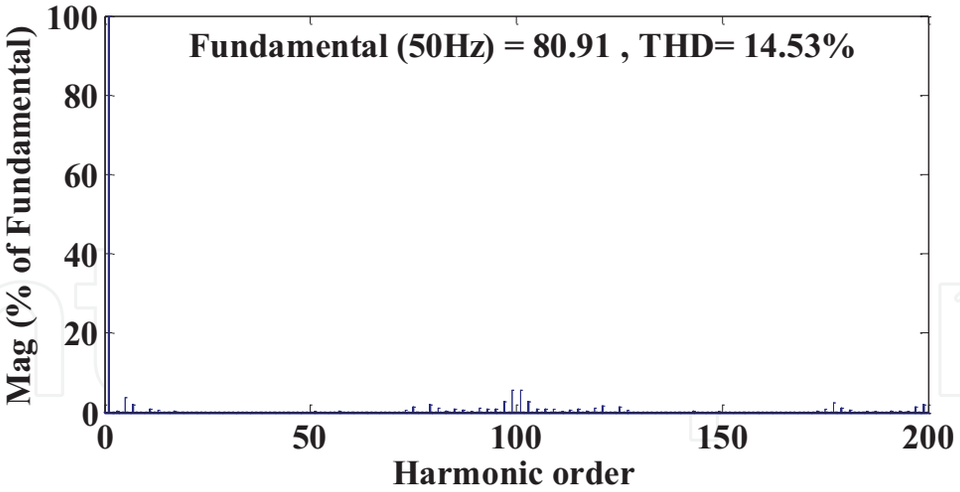


Figure 14. Harmonics plot for output voltage in conventional CHBMLI integrated with PV.

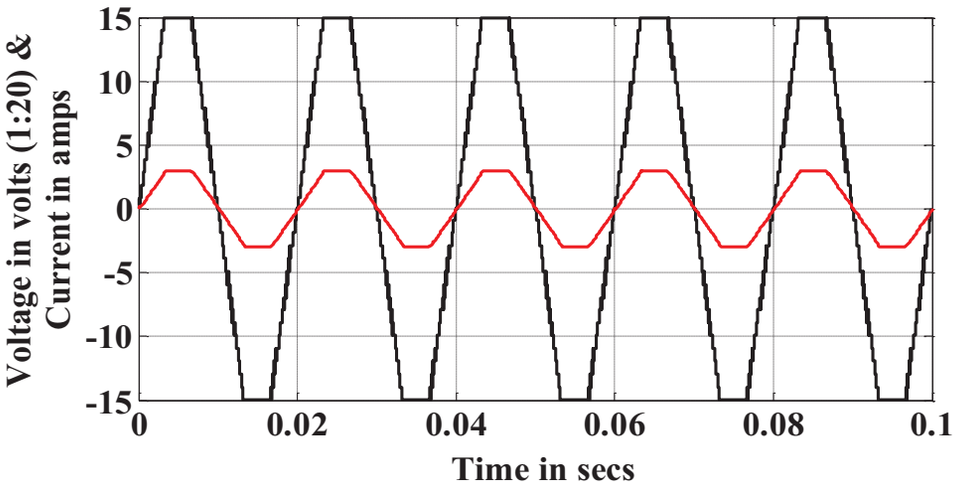


Figure 15. Simulation results for output voltage and current in proposed MLI.

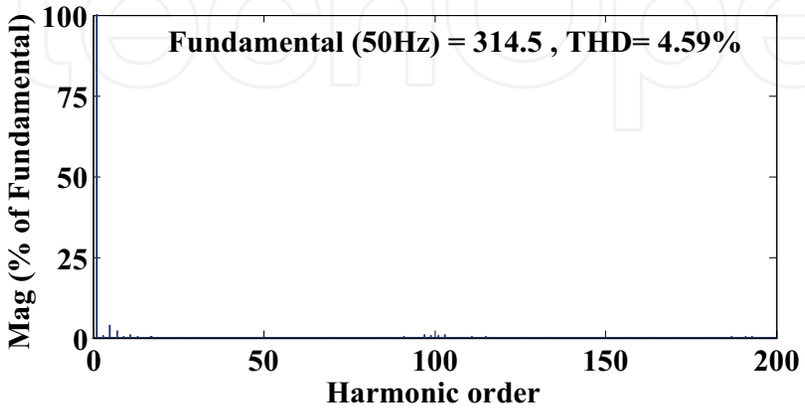


Figure 16. Harmonics plot for output voltage in proposed MLI.

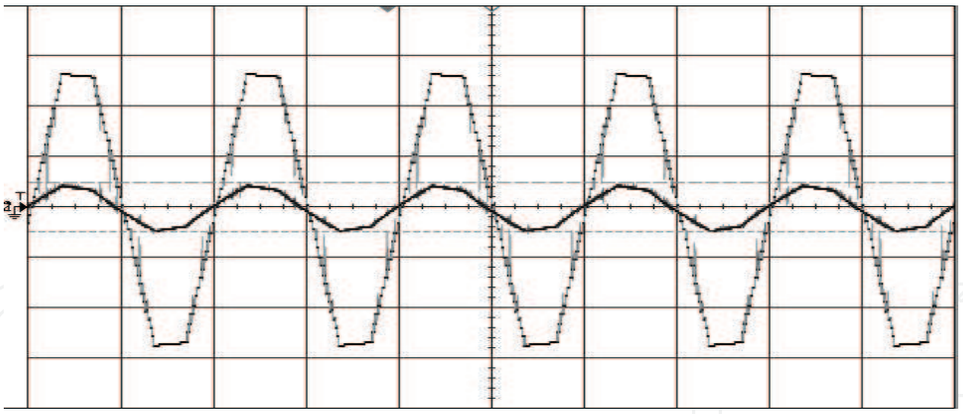
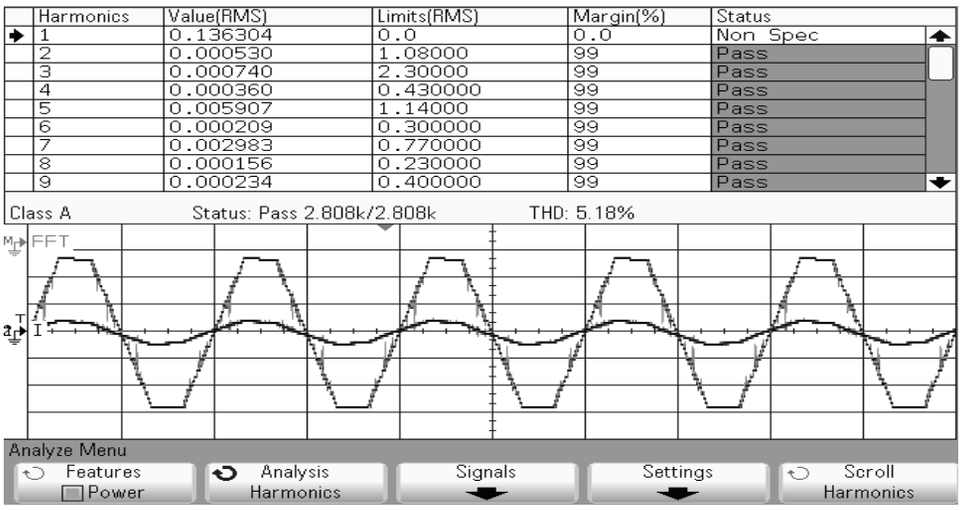


Figure 17. Experimental results for output voltage and current in proposed MLI (CH1: 100 V/div, CH2: 5 A/div).



Harmonics	Value(RMS)	Limits(RMS)	Margin(%)	Status
1	0.136304	0.0	0.0	Non Spec
2	0.000530	1.08000	99	Pass
3	0.000740	2.30000	99	Pass
4	0.000360	0.430000	99	Pass
5	0.005907	1.14000	99	Pass
6	0.000209	0.300000	99	Pass
7	0.002983	0.770000	99	Pass
8	0.000156	0.230000	99	Pass
9	0.000234	0.400000	99	Pass

Figure 18. Experimental harmonics plot for output voltage in proposed MLI.

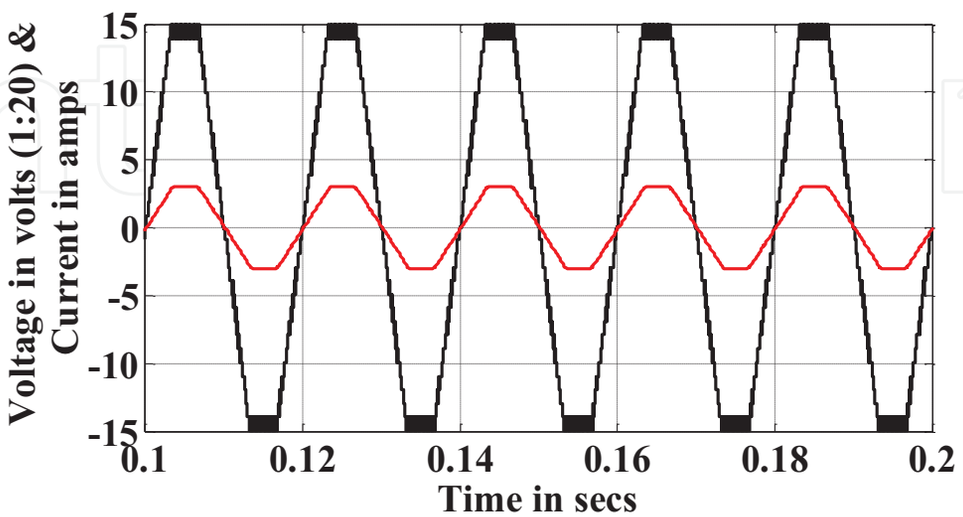


Figure 19. Output voltage and current for proposed MLI integrated with PV.

http://dx.doi.org/10.5772/67863

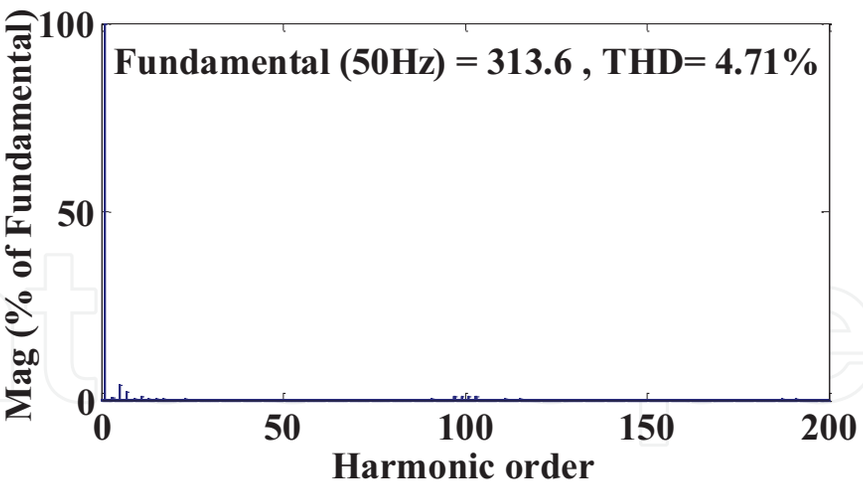


Figure 20. Harmonics plot for output voltage in proposed MLI integrated with PV.

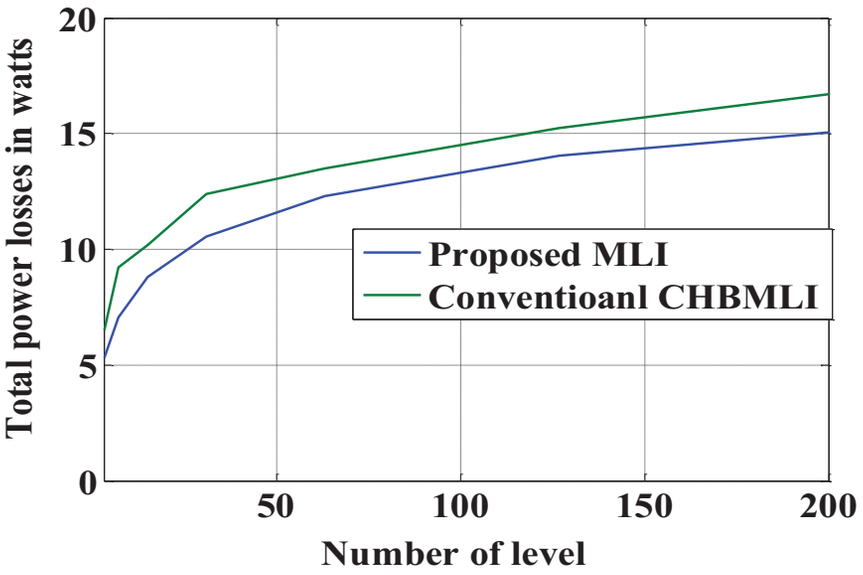


Figure 21. Power loss comparisons for proposed MLI with CHBMLI.

	DCMLI	FCMLI	CHBMLI	Proposed MLI
Number of switches	60	60	60	8
Number of DC sources	1	1	15	4
Total number of output voltage levels	31	31	31	31
Number of drive circuit	60	60	60	8
Clamping diodes	56	–	–	–
Clamping capacitors	–	28	–	–
DC bus capacitors	30	30	–	–
Conducting switches/diodes per voltage level	30	30	30	6

Table 4. Comparison table of proposed configuration with conventional MLIs for 31-level output voltage.

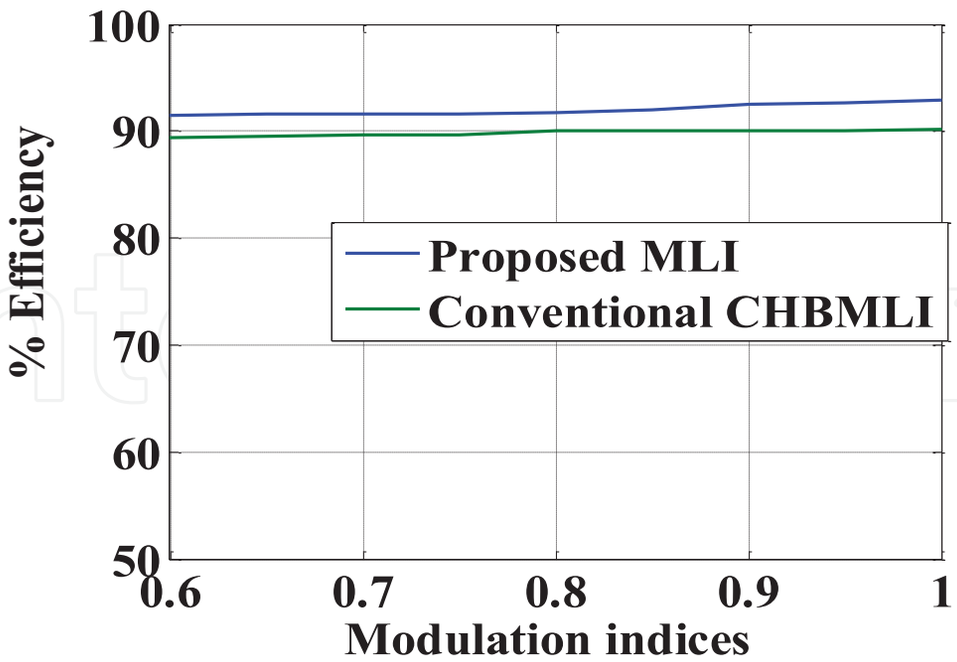


Figure 22. Efficiency comparisons for proposed MLI with CHBMLI.

Parameters	%THD without solar		%THD with solar
	Simulation	Experimental	Simulation
Conventional CHBMLI	13.56	17.31	14.53
Proposed MLI	4.59	5.18	4.71

Table 5. Comparison table of %THD for proposed MLI with conventional MLI.

losses. **Table 5** shows the %THD value for conventional CHBMLI and proposed MLI without integrated solar and with an integrated solar system. From **Table 5**, it is clearly understood that the proposed MLI with integrated solar system provides <5% THD value which satisfies IEEE519 harmonic standard.

6. Conclusion

Multilevel inverter topologies have been more popular in renewable energy application. The proposed reduced switch multilevel inverter configuration has many advantages such as reduction of switches, driver circuits and the DC source count. Also, it is operated at asymmetric condition so that it requires the minimum count of conducting switches per voltage level generation when compared with conventional MLI topologies. Therefore, the switching losses and conducting losses of this configuration are considerably low. The proposed configuration utilizes unipolar PWM strategies for improving the quality of output voltage. The operation of proposed configuration is tested with MATLAB/SIMULINK simulation, and it is verified in hardware set up using dSpace 1104 real-time

controller. The proposed configuration is tested with photovoltaic panels for proving the ability of it. As a result, the proposed configuration requires lesser component count for generating higher output voltage level with lower %THD, and it is well suitable for the photovoltaic system.

Nomenclature

MLI	Multilevel inverter
PV	Photovoltaic
THD	Total harmonic distortion
CHBMLI	Cascaded H-bridge multilevel inverter
PD	Phase disposition
SPWM	Sinusoidal pulse width modulation
PWM	Pulse width modulation
I_{PV}	Photovoltaic current
I_o	Saturation current
R_s	Series resistance of solar cell
R_p	Parallel resistance of solar cell
N_s	Solar cells connected in series
N_p	Solar cells connected in parallel
G	Irradiation on the device surface
L_c	Conducting losses
$L_{c,sw}$ and $L_{c,d}$	Conducting losses of switch and conduction losses of diode
DC	Direct current
DCMLI	Diode clamped multilevel inverter
FCMLI	Flying capacitor multilevel inverter
I-V	Current-voltage
P-V	Power-voltage
FFT	Fast Fourier transform
$I_{pv,n}$	PV current
V_t	Thermal voltage
$V_{oc,n}$	Open circuit voltage
$I_{sc,n}$	Short circuit current
K_V	Short circuit voltage or temperature co-efficient
K_I	Short circuit current or temperature co-efficient
G_n	Nominal irradiation
L_{sw}	Switching losses
E_{on} and E_{off}	Turn on energy loss and turn off energy loss
N_{sw}	Number of switch

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