Chapter 11

Review of Recently Progress on Neural Electronics and Memcomputing Applications in Intrinsic SiO_x-Based Resistive Switching Memory

Cheng-Chih Hsieh, Yao-Feng Chang,
Ying-Chen Chen, Xiaohan Wu, Meiqi Guo, Fei Zhou,
Sungjun Kim, Burt Fowler, Chih-Yang Lin,
Chih-Hung Pan, Ting-Chang Chang and Jack C. Lee

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.68530

Abstract

In this chapter, we focus on the recent process on memcomputing (memristor + computing) in intrinsic SiO_x-based resistive switching memory (ReRAM or called memristor). In the first section of the chapter, we investigate neuromorphic computing by mimicking the synaptic behaviors in integrating one-diode and one-resistive switching element (1D-1R) architecture. The power consumption can be minimized further in synaptic functions because sneak-path current has been suppressed and the capability for spike-induced synaptic behaviors has been demonstrated, representing critical milestones and achievements for the application of conventional SiO_x-based materials in future advanced neuromorphic computing. In the next section of chapter, we will discuss an implementation technique of implication operations for logic-in-memory computation by using a SiO_x-based memristor. The implication function and its truth table have been implemented with the unipolar or nonpolar operation scheme. Furthermore, a circuit with 1D-1R architecture with a 4 × 4 crossbar array has been demonstrated, which realizes the functionality of a one-bit full adder as same as CMOS logic circuits with lower design area requirement. This chapter suggests that a simple, robust approach to realize memcomputing chips is quite compatible with large-scale CMOS manufacturing technology by using an intrinsic SiO_x-based memristor.

Keywords: resistive switching, synaptic device, silicon oxide, neuromorphic computing

1. Background

In recent 20 years, emerging memory has drawn a lot of interest and attention as a promising candidate for next generation nonvolatile memory (NVM) [1–3]. Traditional "charge"-based NVM (Flash) will face the potential scaling challenge below the 10 nm node with reliability and power consumption issues [4, 5]. Resistive switching (RS) memory, or we call resistive random access memory (ReRAM), operates by controlling device "resistance" with an external electrical bias [6–9], leading to better electrical performance, smaller design area ($4F^2$), and excellent cycling endurance [10] based on the 2015 International Technology Roadmap for Semiconductors (ITRS) (ReRAM is one of two recommended candidate technologies (the other one is the STT-MRAM) for emerging memory devices) [11]. Moreover, RS-based memories represent a new class of devices compatible with applications that go beyond traditional electronics configurations, for example, three-dimensional (3D) stacking, nanobatteries, neuroelectronics, and Boolean logic operations [12–17].

In 1971, Chua presented the theoretical basis for a passive two-terminal circuit device called a "memristor" (a contraction of memory and resistor) [18]. If realized, the memristor would then join the resistor, inductor, and capacitor to provide four basic circuit elements. In 2010, researchers in HP lab realized the memristor in nanoscale titanium dioxide (TiO_2) cross-point structure [17], and the field has advanced quickly growth over the past decade as a result. Having demonstrated the existence of memristors in the lab, additional research efforts focused on the potential applications that this emerging new circuit element enables [19]. In recent years, memristors have been extensively studied as a nonvolatile memory called resistive random-access-memory (named ReRAM or RRAM) to potentially replace dynamic random-access-memory (DRAM) and flash memory [20]. Memristors have also gained tremendous interest in the field of neuroelectronics and synaptic electronics, which aims to build artificial synaptic devices that emulate the computations performed by biological synapses [21–25]. Jo et al. described possible applications in artificial intelligence using memristors as synapses in neuromorphic circuits [15]. Another interesting application is to use memristors for arithmetic/logic operations, such as an adder circuit or a multiplier circuit.

In the literature, arithmetic operations are proposed using the memristor as a: (1) switch, (2) programmable interconnect, and (3) computational element. In the first approach, crossbar arrays of memristor switches are connected to a row of weighting resistors and sensing logic to build an analog arithmetic processor [26]. The switches control the current flow (ON/OFF) through the weighting resistor, which then controls the analog voltage at the sensing amplifier end. The resistance of the weighting resistor assigns the appropriate bit significance to the each row's current contribution. The memristor-CMOS technology may be used to realize the same types of arithmetic circuits that are developed in CMOS/FPGA (field programmable gate array) technology [27, 28]. Last but not the least, a more universal approach for constructing the logic operations from memristors is via "material implication" (or an "IMP" operation). In 2010, researchers showed that all fundamental Boolean logic functions can be realized by using memristors with the IMP operation [17]. Later work built on these findings to construct larger logic blocks such as adders and multipliers [29–31], linear feedback shift

registers [32], and counters [32]. The advantages of memcomputing (memristor + computing) are not only to store and process information on the same physical platform, but also to allow massively parallel computations in a simple crossbar array architecture.

Otherwise, neuroelectronics and synaptic electronics are interesting applications for ReRAM that aim to build artificial synaptic devices that emulate the computations performed by biological synapses [15, 33]. These emerging fields of research potentially have better efficiency in solving complex problems and outperform real-time processing of unstructured data than conventional von Neumann computational systems [34]. There have been many studies of binary metal oxide-based and perovskite oxide-based resistance switching characteristics for synapse-like electronic device development [35, 36], which can have operating instability issues due to difficulty in controlling stoichiometric compositions [37, 38]. Therefore, a simple process that is compatible with conventional complementary metal-oxide semiconductor (CMOS) fabrication allows multilayer compositional engineering and provides good electrical stability and high yield, which are critical requirements for neuroelectronics realization [39]. Silicon oxide (SiO_x) has long been used as gate dielectrics for metal-oxide-semiconductor field-effect transistors. In addition to excellent insulating properties, resistive switching properties have been observed in SiO_x materials as early as 1962 by Hickmott and 1967 by Simmons and Verderber [40–42]. Yao et al. also have reported SiO_x-based RS behaviors in vacuum, indicating that this traditional material can be converted to an active component by controlling the external electrical manipulation [43–45]. Several recent reports describe using SiO_2 as the active switching medium in resistive switching memory devices [46–49]. We have further demonstrated a Si diode (1D) with low reverse-bias current integrated with a SiO_x-based memory element (1R) using nanosphere lithography and deep Si etching to pattern a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer [50].

2. Introduction

In this chapter, first SiO_x-based resistive switching memory elements (1R) are integrated with Si diodes (1D) using conventional CMOS processing to demonstrate a 1D-1R device with synaptic behaviors. Compared with our previous work (in most cases investigating only the 1R device system), the Si diode provides low reverse-bias current and high power efficiency for future neuromorphic computing array architectures. Unlike other binary or complex metal oxide materials [51], SiO_x has been used in CMOS manufacturing for over 50 years due to its excellent electrical isolation properties, low-cost, high chemical stability, compatibility with mainstream integrated circuit materials, high-throughput processing, and large-area production using chemical vapor deposition (CVD). A 1D-1R architecture fabricated at the wafer-scale using conventional CMOS processing can, therefore, be well controlled in thickness, size, and electrical characteristics by precisely controlling the doping levels of the diode layers and the temperature and flow-rate of the oxide CVD process [52]. Synaptic device performance is characterized in a prototype 1D-1R array configuration. Robust biological synaptic behaviors such as long-term potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP) are demonstrated with excellent uniformity, low

operational variability, and good suppression of static power consumption [51]. A bio-inspired proton exchange resistive switching model is used to help characterize this novel application for SiO_x materials. The SET transition in the resistive switching memory is modeled as hydrogen (proton) release from the $(Si\text{-}H)_2$ defect to generate a conductive hydrogen bridge, and the RESET transition is modeled as an electrochemical reaction (proton capture) that reforms nonconductive $(SiH)_2$. The synaptic behaviors exhibited by the 1D-1R device demonstrates good potential for using a simple and robust approach for large-scale integration of programmable neuromorphic chips using CMOS technology.

Second, the application of SiO_x-based memristors for material implication operations is examined. A bidirectional implication scheme is demonstrated and tested in an actual circuit using SiO_x-based memristors. The symmetric unipolar memristive behavior of the SiO_x-based memristor enables the use of two sets of implication voltage setups, one positive and the other negative, hence the name "bidirectional". Progressing one step further from the initial concept demonstrated by Borghetti et al. and our previous work, a one-bit full adder is realized by using the material implication technique on a crossbar structure with a one-diode one-memristor (1D-1R) array. Several potential application problems such as sneak current paths within an array and using a select transistor as the load resistor are discussed in detail. The results suggest that a memristor-enabled logic circuit is most suitable for applications requiring low-speed, low-power, and high-density.

3. Method and experiment

Secondary electron microscopy (SEM) images show a top-down view of a 1D-1R test structure (**Figure 1a**), a tilted (45°) view of the 1R device (**Figure 1b**) and a cross-section image of the 1R device showing layer information (**Figure 1c**). The devices were fabricated at XFAB in Lubbock TX using the XC06 CMOS process technology. The 1R device was fabricated by first implanting the Si substrate to form an n-type lower electrode. The active SiO_x memory layer was then deposited to a thickness of 40 nm using plasma-enhanced chemical vapor deposition (PECVD). This thickness is known to provide high electroforming yield and good memory endurance [53]. An n-type polysilicon layer was deposited onto the SiO_x layer to form the top electrode. An opening in the polysilicon layer was made after all thermal oxidation and implant anneal steps are complete (**Figure 1b**). A first dielectric layer was then deposited over the polysilicon top electrode. Tungsten plugs were used to make electrical contact to the n-type Si lower electrode and the polysilicon top electrode. After all the back-end dielectrics and a passivation layer were deposited, the back-end dielectric layers were removed using reactive ion etch (RIE) to the Si substrate. This RIE step cleared-out the SiO_x layer inside the hole, and created a SiO_x sidewall where the memory device is formed (**Figure 1c**). Polymer residue that remained after the post-RIE cleaning steps was removed by a 30-s buffered oxide etch (BOE). The pn diode used in the 1D-1R test structures was formed by an implanted p-well inside a deep n-well with 40 V reverse-bias breakdown voltage, 1 nA reverse-bias leakage current and 0.5 V forward voltage. The active memory area of the 1R device is $2 \times 2\ \mu m^2$ and the overall size including metal interconnects is $21.9 \times 21.9\ \mu m^2$. The overall size of the 1D device is $41 \times 19\ \mu m^2$. A lake shore cryotronics vacuum probe chamber (<1 mTorr) and Agilent B1500A device analyzer were used

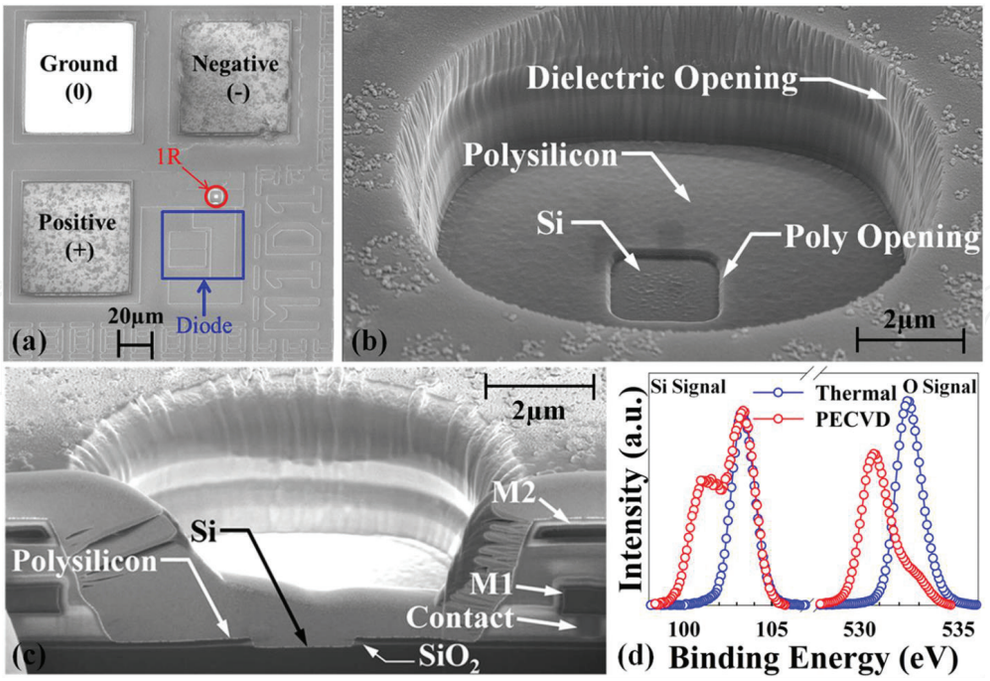


Figure 1. (a) Top-down SEM image of 1D-1R architecture. The 1R is adjacent to the 1D structure. The ground pad (0) is used to bias the substrate, the positive (+) and negative (−) terminals are for applying voltage to the 1D-1R device. (b) Tilted top-down SEM image of resistive memory device. (c) SEM cross-section image showing metal contact to polysilicon top electrode, metal 1 (M1) and metal 2 (M2) layers, and polysilicon/SiO_2/Si 1R device. (d) Si-$2p_{2/3}$ and O-1s XPS spectra for PECVD oxide and thermal oxide. Figure reprinted by [19].

to electroform devices and measure the DC/AC *I-V* response. The SET process programs the device to a conductive, low-resistance state (LRS). The RESET process programs each device to a low-conductance, high-resistance state (HRS). A Kratos Axis Ultra HSA X-ray photoelectron spectrometer (XPS) equipped with a monochromatized aluminum X-ray source was used to analyze several SiO_x materials deposited in our laboratory using different methods. Calibration of the binding energy scale was set by fixing the C-(C,H) peak at 284.4 eV. **Figure 1d** shows XPS analysis results for the O-1s and Si-2p binding energies in thermal oxide grown by low-pressure chemical vapor deposition (LPCVD) and PECVD oxide. The existence of stoichiometric SiO_2 can be observed in thermal oxide (binding energy Si: 103.2 eV; O: 532.5 eV) with essentially no suboxide bonding being detected. In contrast, the PECVD oxide has nonstoichiometric SiO_x (x is about 1.6 based on the peak position and orbital valence) composition in the switching layer, as indicated by the peak-binding energies in the XPS spectra (O: 530.5 eV; Si: 101.9 eV, and 100.9 eV) [54, 55], which may promote low-energy defect generation during the electroforming process.

4. Results and discussions

Figure 2a–d show *I-V* characteristics for DC voltage sweeps applied to the SiO_x-based 1D-1R devices fabricated by the conventional CMOS process. Voltage was applied to the 1D top electrode (p-type Si) with bottom 1R electrode (n-type Si) at ground. All testing was done in

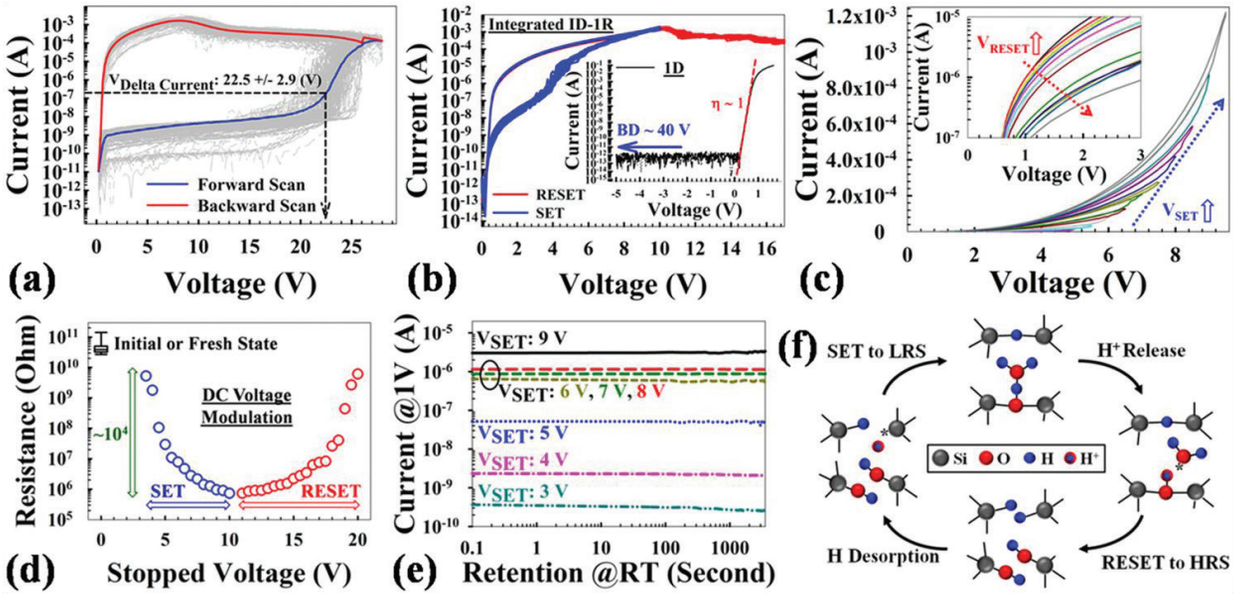


Figure 2. DC sweep resistive switching behaviors of 1D-1R architecture: (a) Forward/backward voltage sweeps during electroforming process averaged for 256 devices in a 16 × 16 array (gray curves). The electroforming voltage ($V_{\text{Delta Current}}$) is defined as the voltage where maximum current change occurs during the forward sweep. (b) 10 I-V resistive switching SET/RESET cycles. The inset shows the average of 100 measurement cycles of diode I-V behavior. (c) Effects of voltage modulation on I-V curves in SET process plotted on linear-scale, where the applied SET voltage sweep increases from 3.5 to 9.5 V in 0.5 V steps. The inset shows effects of voltage modulation on I-V curves in RESET process plotted on log-scale, where the applied RESET voltage sweep increases from 11.0 to 18.0 V in 0.5 V steps. (d) The resistance states of initial fresh device, SET DC voltage modulation, and RESET DC voltage modulation. For SET voltage sweep, increases from 3.5 to 10 V in 0.5 V steps; for RESET voltage sweep, increases from 11 to 20 V in 0.5 V steps. The resistance reads at 1V for each state. (e) Retention measurement results of multi-state programming obtained by controlling the SET voltage. (f) Proton exchange induced resistive switching model and defect transitions. Figure reprinted by [19].

vacuum. To establish reversible resistive switching in each SiO_x-based 1R ReRAM device, a forward/backward voltage sweep (**Figure 2a**) was used to electroform each device, where current is observed to increase dramatically at 22.5 ± 2.9 V during the forward voltage sweep. Electroforming is completed during the backward voltage sweep from the maximum sweeping voltage to 0 V, resulting in the formation of a conductive filament (CF) and setting the device to a LRS. After electroformation, RS performance of 1D-1R can be stabilized by 10 times cycles (**Figure 2b**). For SET process, a 10 V forward/backward sweep is applied without any compliance current limitation (CCL) to change the device from HRS to LRS; for RESET process, a 17 V, single sweep is done to change the device from LRS to HRS. The HRS/LRS resistance ratio can be read out at 1 V bias with satisfying sensing requirements (~10^3) [3, 26]. For diode characteristics, the forward current can reach 100 mA at 2 V (current density 1.15×10^{-5} A/μm^2 at 1 V), which indicates a forward current level high enough to support the RESET process. The reverse current is below 1×10^{-12} A at −5 V. Compared with Schottky diodes (potentially useful for 3D arrays), the advantages of Si-based PN diodes include low reverse current, high reverse-bias breakdown voltage, and fewer stability issues [45]. The quality of the Si-based PN diode can dramatically affect diode reverse or forward current characteristics, as well as power consumption (describe below). Also, the chosen Si-based PN diode configuration has high reverse breakdown voltage (>40 V), which is important for SiO_x-based ReRAM operating in an array. **Figure 2c** demonstrates the gradual change of

resistive states by modulating the voltage sweep range continuously during the SET and RESET (inset) process, respectively. Specifically, SET and RESET voltages were changed from 3.5 to 9.5 V in 0.5 V increments and from 11 to 18 V in 0.5 V decrements, respectively, thus potentially enabling multilevel programming in a single memory cell and demonstrate the status stability before/after sweeps. It may be noted that the electroforming voltages measured here (~ 28 V) are somewhat higher than those measured in previous work on metal-oxide-semiconductor device architectures or nanopillar type 1D-1R architectures [50, 56, 57], which may be due to fewer electrically active defects being near the SiO_x sidewall as a result of the fabrication process. For example, several high temperature steps (>650°C) were done after PECVD SiO_2 deposition, namely: polysilicon deposition, thermal oxidation, and implant anneals, which might densify the SiO_2 layer, reduce the as-deposited defect levels, increase the soft breakdown threshold, and thus increase the filament formation energy during the subsequent electroforming process (resulting in forming voltage increase). Interestingly, the RESET voltage (the voltage at which LRS current begins to decrease) has been found to be greater than or equal to the SET voltage (where HRS current increases sharply), which is a unique characteristic of the SiO_x-based ReRAM as compared to other materials systems [36, 58]. The difference between RESET and SET voltages can potentially be controlled by optimizing the series resistance in the circuit, choice of electrode materials, and by doping effects that modulate the interfacial contact resistance [59]. The switching voltage is largely independent of device size and SiO_x thickness. **Figure 2e** shows multilevel retention performance of SiO_x-based 1D-1R devices obtained by controlling the maximum SET voltage from 3 to 9 V. The readout current of LRS and HRS is measured at 1 V every 60 s after each programming operation. Although the state's stability still needs to be improved (no equal split of resistance states), the retention reliability test demonstrates ` operation by using different SET voltages, and no degradation is observed for more than 10^3 s, thus confirming the stable, nonvolatile nature of the SiO_x-based 1D-1R devices. In recent studies, a possible proton exchange model consistent with the observed resistive switching *I-V* response has been proposed, as shown in **Figure 2f** [59, 60]. Several studies have used transmission electron microscopy (TEM) to document the presence of Si nanocrystals within the CF [43, 61, 62], but it is not yet clear whether resistive switching (RS) is the result of an overall increase in nanocrystal size or whether switching occurs in "GAP" regions in between nanocrystals. Most models of ReRAM switching involve the drift or diffusion of O^{2-} ions (or oxygen vacancy defects) [39], but these models cannot explain the unconventional *I-V* response. For example, the backward scan effect (see **Figure 2a**, backward scan) is very difficult to explain using a simple oxygen vacancy-switching model. The backward scan effect is a phenomenon where the duration of the reverse sweep during electroforming or RESET determines whether a state change occurs, and has been characterized using DC and AC pulse response in a previous study investigating our resistive switching model [57]. In addition, ambient effects on resistive switching suggest that the defects responsible for switching are hydrogen-passivated or are in some way protected from direct reaction with ambient oxygen and water until a switching events occurs [56, 63]. The detailed interactions between ambient gases and proton (or cation) mobility is an important topic that may provide a deeper understanding of resistive switching mechanisms [64–68], specifically those in oxide-based valence change memory (VCM)-type ReRAMs [69–71]. The models used here to describe the possible

SiO_x-based RS mechanisms differ from most conventional models by considering that the defects responsible for RS may remain localized within the switching region so that resistive switching occurs when a collection of defects are driven between conductive and nonconductive forms [56]. A thorough review of the reported electrical and structural properties of known SiO_x defects has identified a plausible model for the conductive filament that is similar to models used to describe stress-induced leakage current and breakdown in SiO_x materials, where defect concentration increases as a result of electrical stress to the point where percolation pathways capable of conducting appreciable current (>1 uA) are formed [59]. Incorporating known proton exchange reactions that can dramatically alter the conductivity of specific defects further leads to a model where the LRS has a large concentration of conductive defects within the switching region, and, conversely, when the device is programmed to the HRS, most of the defects are converted to their nonconductive form. The electrically conductive hydrogen bridge (Si-H-Si) is viewed as the most likely defect responsible for the LRS due to the location of its energy levels relative to the oxide conduction band and its small effective bandgap energy [59, 60]. Adding a proton to Si-H-Si forms the nonconductive $(SiH)_2$ defect and proton desorption from $(SiH)_2$ reforms Si-H-Si, which are well-understood electrochemical reactions that could enable localized switching without incorporating ion diffusion or drift mechanisms into the model. The SET transition voltage from HRS to LRS occurs at ~2.5 V in the I-V response, and is very near the activation energy for proton desorption from SiH (~2.5 eV), thus making the defect transformation from $(SiH)_2$ to Si-H-Si a logical assignment for the SET transition [59, 60]. In this model, the proton that is lost from $(SiH)_2$ reacts electrochemically with $(SiOH)_2$, which is simply chemisorbed H_2O, to form the fixed positive charged H_3O^+ defect. The transition from LRS to HRS is modeled as being initiated by electron injection into H_3O^+ that induces proton release and electrochemical reaction with Si-H-Si to reform $(SiH)_2$ [59, 60]. The localized proton exchange switching model can thus be written as $(SiH)_2 + (SiOH)_2 \leftrightarrow$ Si-H-Si + Si_2=O-H_3O^+, where a voltage drop of ~2.5 V across the switching is required to drive the reversible reaction. The RS model not only provides insights into multilevel operational characteristics but also implies a possible biomimetic chemical reaction similar to reactive oxygen species (ROS-like) production for future device characterizations [72].

Figure 3a–h show contour plots of the current-change ratio achieved by modulating the AC pulse height and pulse width applied to 1D-1R devices for both SET and RESET switching events, leading to optimized waveform designs for a biological synaptic device. The current-change ratio is defined as $\log_{10}(I_{FINAL}/I_{INITIAL})$, where $I_{INITIAL}$ and I_{FINAL} are the currents measured at 1 V before and after applying the programing waveform, respectively. The SET/RESET sweeps from same initial resistance state (precondition programming) is to eliminate the accumulating SET/RESET effect after each cycle. One can observe by inspecting the contour lines in **Figure 3** that when larger pulse heights (higher voltages) are applied to the device, shorter pulse widths are needed to achieve a similar current-change ratio. In general, we find that a single 1R device operates at higher speed and requires lower programming voltages as compared to a 1D-1R device. The higher operating voltages and lower operating speed of the integrated 1D-1R device may result from higher parasitic resistance in the Si electrodes, their contacts and the diode, as well as higher parasitic

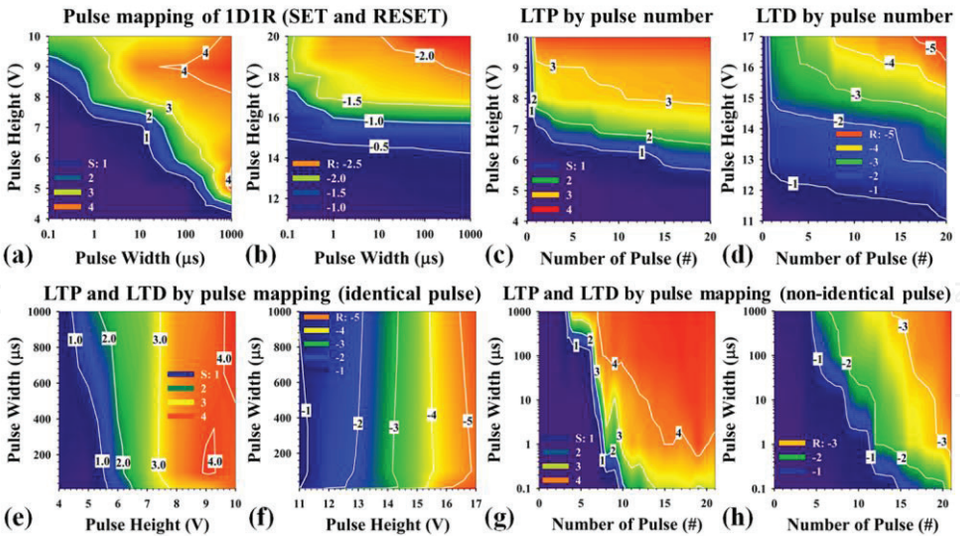


Figure 3. AC pulse mapping contour plots of current-change ratio by modulating pulse height and pulse width to demonstrate synaptic behaviors in 1D-1R architectures: (a) SET (S) and (b) RESET (R) mapping results of 1D-1R device. (c) and (e) Long-term potentiation (LTP) and (d) and (f) long-term depression (LTD) using the identical pulse method as a function of pulse width. For the identical pulse method, pulse height and pulse width are fixed. For LTP, the pulse height modulation changes from 11 to 17 V in 0.3 V increments for each loop, and pulse widths are fixed at 10 μs. The mapping results of using the identical pulse method for LTP are show in (e). By selection of final states (after 20 pulses), the conductance change is highly dependent on the pulse height. For LTD, the pulse height modulation changes from 4 to 10 V in 0.3 V increments for each loop, and pulse widths are fixed at 10 μs. The mapping results (f) are similar and the conductance change for LTD is also highly dependent on the pulse height rather than pulse width. (g) and (h) show the LTP and LTD using the non-identical pulse method as a function of pulse width, respectively. For the non-identical pulse method, pulse height modulation changes continuously from 4 to 10 V in 0.3 V increments (for a total of 21 steps) for LTP, and changes continuously from 11 to 17 V in 0.3 V increments (for a total of 21 steps) for LTD. The initial states for LTP and LTD mapping are determined by fixed DC conditions: a 17 V single sweep for HRS and a 10V double-sweep for LRS, respectively. "S" and "R" denote the increment/decrement of current state changes after applying the AC pulse (defined as Log_{10} (I_n/I_{nitial}), where $I_n/I_{Initial}$ is current ratio measured at 1 V after/before the pulse is applied). Figure reprinted by [19].

capacitance in the diode, all of which can act to degrade the pulse mapping results shown in **Figure 3a** and **b**. It should be noted that current sneak-path issues in arrays and writing disturbance of 1R devices would cause misread problems and state disturbance, and substantially increase standby power consumption and information instability. The 1D-1R devices are used to suppress sneak-path currents, and perform much better than 1R devices in an array architecture (potential 1 Gbit array support in 10% readout-margin at 1V read). From **Figure 3a** and **b**, it can be calculated that the switching energies to achieve at least a one-order-of-magnitude change in resistance in the 1D-1R architecture are about 0.01 pJ for SET and 1.54 nJ for RESET operations. However, due to the suppression of sneak-path current, the standby power during a 1 V read operation can be dramatically reduced in 1D-1R devices (1 pW) as compared to 1R devices (1 μW, due to 1R nonpolar switching behaviors) [73]. Minimizing the total power consumption due to sneak-path current is as crucial as reducing the synaptic dissipation.

Most importantly, the pulse mapping results not only demonstrate the potential for multilevel programming by properly designing the pulse waveforms for SET and RESET operations, but also demonstrate the potential to realize biological synaptic behaviors. **Figure 3c–h** demonstrate

the optimization waveform design for biological synaptic behaviors in 1D-1R SiO_x-based resistive switching memories. The long-term potentiation (LTP) and long-term depression (LTD) are a long-lasting enhancement/reduction in signal transmission between two neurons (similar with long-lasting conductance increase/decrease between HRS and LRS for resistive-type memory devices), which can be realized by designing the SET and RESET pulse waveform to use either identical (fixed pulse width and pulse height, as shown in **Figure 3c–f**) or nonidentical (variable pulse width or pulse height, as shown in **Figure 3g** and **h**) pulsing techniques. The trade-offs between high dynamic range and gradual multilevel programming performance (**Figure 3e–h**) needed to be considered, and it was found that the nonidentical pulse waveform method may have the advantages (larger than identical pulse waveform method). Although nonidentical pulsing might require a more complex neuromorphic circuit, our results show that this approach enables more efficient programming to target states while maintaining a larger dynamic range (**Figure 3g–h**). The use of nonidentical pulse heights ranging from 4 to 10 V in 0.3 V increments (for LTP) and ranging from 11 to 17 V in 0.3 V decrements (for LTD) allow the dynamic range to be mapped for pulse widths ranging from 100 ns to 1 ms, thereby realizing biological synapse behaviors in the SiO_x-based 1D-1R architecture (**Figure 3g–h**). The switching energy is defined as $I \times V \times \delta t$, where δt is the pulse width. For $\delta t = 100$ ns, the smallest switching energies are ~6 and ~130 pJ for LTP and LTD, respectively. The larger energy for LTD is mainly due to the lower resistance of the LRS (~93 kΩ) compared to the HRS (~260 MΩ), which results in higher switching current (118.28 μA) for the RESET process than for the SET process (15.38 nA). In order to minimize synaptic energy consumption all three components—programming current (~nA level switching), pulse amplitude (<1 V) and programming time (<10 ns)—need to be minimized. In SiO_x-based ReRAM and in other material systems, an exponential voltage–time relationship is commonly observed. A small increase in programming voltage will decrease programming time exponentially, as shown in **Figure 3a**. For RESET process (both 1R and 1D-1R structures, **Figure 3b**), the process integration may result in certain level of distortion (parasitic resistance/capacitance and possible parasitic depletion region capacitance from 1D) to affect the pulse mapping results. Hence, low programming energy is obtained by minimizing the programming time (traded off by increasing the pulse amplitude slightly) for ReRAM. Further decreases in synaptic energy consumption during the switching process to fJ levels will be challenging but important to build very large-scale systems (the designed pulse waveform optimization and generation is in process).

Such flexible artificial control built with synaptic devices could provide a suitable platform for a broad range of computing applications, as shown **Figure 4**. Some of the advantages that SiO_x-based synaptic devices provide over other resistive switching materials include a higher dynamic range (~10^4) [57] and the potential to achieve as many as 10–60 multilevel states (depend on the stability) in both LTP and LTD by changing the increment/decrement of the voltage step, as shown in **Figure 4a**. These advantages may arise as the result of there being a large number of defects within the switching region of the memory device. Switching is modeled as a change in conductivity of a group of defects within the switching region. In this framework, defects are not created or destroyed, but are simply driven between conductive and nonconductive forms by proton exchange reactions that are known to occur in SiO_x materials (**Figure 2f**) [60]. The SET and RESET switching transitions can be described in more

detail with the aid of the electron energy band diagrams shown in **Figure 4b**, which were constructed using the thermodynamic and switching charge-state energy levels reported by Blochl in 2000 [74]. The ideal energy band diagrams in **Figure 4b** represent only a single electron pathway through the memory device, whereas in reality there are likely many such percolation pathways in parallel. The SET transition is modeled as being the result of trap-assisted electron tunneling through $(SiH)_2$ defects (a voltage-triggered mechanism, due to less current flow in the initial stage of SET process) that stimulates H^+ desorption and reaction of H^+ with absorbed water $(SiOH)_2$ to form conductive Si-H-Si and H_3O^+ (**Figure 2f**). Trap-assisted tunneling can only occur when the bias across the switching region is ≥2.6 V, which is the effective bandgap of the $(SiH)_2$ defect and compares well with the observed minimum SET voltage of ~2.5 V in the *I-V* response [59, 60]. The RESET transition is modeled as being the result of Fowler-Nordheim electron tunneling into the H_3O^+ defect (possibly current-induced Joule heating due to large current flow through the filament) that stimulates proton release and electrochemical reactions to reform $(SiH)_2$ and $(SiOH)_2$ (**Figure 2f**) [60]. The band diagrams shown in **Figure 4b** are found to be consistent with measured electron energy barriers [60] and electroluminescence results reported for similar devices [62].

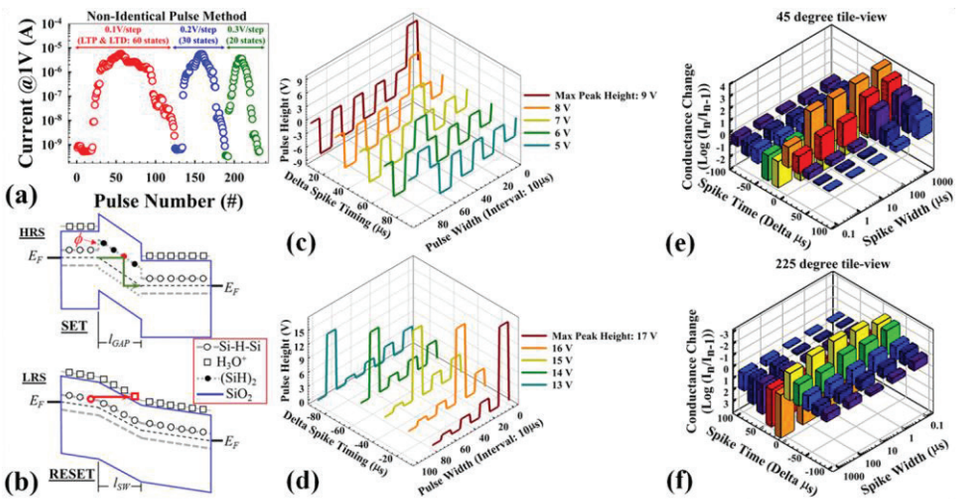


Figure 4. Demonstration of a SiO_x-based synaptic device. (a) Sequential LTP/LTD behaviors as a function of increment/decrement voltage steps (0.1, 0.2, and 0.3 V) by non-identical pulse form. For the non-identical pulse method, pulse height modulation changes continuously from 4 V to 10 V for LTP, and changes continuously from 11 to 17 V for LTD. Pulse width is fixed at 10 μs in both cases. (b) Energy band diagrams: For HRS and SET process, showing theoretical bandgap of $(SiH)_2$ defect within gap region of length l_{GAP}, theoretical bandgap of Si-H-Si defects outside the gap region, and trap-assisted-tunneling SET transition (green arrow). Barrier height to electron transport is ϕ ~ 0.8 eV. For the LRS and RESET process, showing theoretical bandgap of Si-H-Si, H_3O^+ energy level, switching region of length l_{SW}, and Fowler-Nordheim tunneling RESET transition (red arrow). (c–d) A pulse waveform design using the non-identical pulse method for demonstration of spike-timing-dependent plasticity (STDP) as a function of spike pulse width intervals. For the potentiation of conductance strength change, the overall pulse waveform (pulse width fixed at 10 μs in this case) based on the delay of spike timing between neurons is shown in (c). Similarly, for the depression of conductance strength change, the overall pulse waveform (pulse width fixed at 10 μs in this case) based on the delay of spike timing between neurons is shown in (d). (e–f) A demonstration of spike-timing-dependent plasticity (STDP) using the non-identical pulse method with different spike widths. Each colored bar shows the average of 3~5 measurements. (e) Emphasizes potentiation direction of STDP with positive delta time (45° tilted). (f) Emphasizes depression direction of STDP with negative delta time (225° tilted). The definition of conductance change is as Log_{10} (I_n/I_{nitial}), where $I_n/I_{Initial}$ is current ratio measured at 1 V after/before the pulse is applied. Figure reprinted by [19].

Figure 4c–f demonstrate that the SiO_x-based 1D-1R architecture can mimic spike-timing-dependent plasticity (STDP), a biological process that adjusts the strength of connections between two neurons in a synapse gap junction region that is an electrically conductive link between the pre- and postsynaptic neurons. Two pulse generator sources are used to simulate the pre- and postsynaptic neurons. This provides the pulse waveforms using the nonidentical pulse method (also used in various types of emerging memory devices or materials systems) for demonstration of STDP. By design of pre-neuron and postneuron spikes in neuromorphic circuits, the strength of the conductance change can be modulated based on the spike-timing delta (Δt) between the two neurons (**Figure 4c–d**). **Figure 4e–f** demonstrates a total of 10 different states of STDP biological behavior for depression and potentiation with $n = 2, 4, 6, 8, 10$ and as a function of spike width modulation, ranging from 100 ns to 1 ms. For example, the depression of conductance change strength can be achieved by using multistep spike heights from −4 to 0 V in the preneuron state and a single spike height fixed at 13 V in the postneuron state, with both neurons having a fixed pulse width of 10 μs and a firing period of 20 μs, as shown in **Figure 4e–f**. When the time delay difference is −10 × (n−1) μs, where n is an even number, the total spike waveform (postneuron spike minus preneuron spike) applied to the synapse gap junction region can adjust the conductance ratio between two neurons over the range from 10^{-3} to 0.1 in the depression direction (RESET process) as compared with the initial LRS conductance (**Figure 4f**). Similarly, the potentiation of conductance change strength can be achieved by using multistep spike heights from 4 to 8 V in the preneuron state and a single spike height also fixed at 13 V in the postneuron state, with both neurons having a fixed pulse width of 10 μs and a firing period of 20 μs. When the time delay difference is 10 × (n−1) μs, where n is an even number, the total spike waveform (postneuron spike minus preneuron spike) applied to the synapse gap junction region can in this case adjust the conductance ratio between neurons over the range from 10^3 to 0.01 in the potentiation direction (SET process) as compared with the initial HRS conductance (**Figure 4e**). It may be noted that the 1D-1R architecture not only avoids sneak-path issues and lowers standby power consumption, but also helps to realize STDP behaviors. Without the 1D rectification characteristics in reverse-bias polarity, the above spiking forms cannot be implemented due to the unipolar nature of the 1R device, specifically in the potentiation behaviors under negative bias. In the 1R case, an applied voltage above the RESET threshold voltage (for example, −9 V) can trigger the RESET process and induce depression behaviors instead of potentiation behaviors. Also, for depression behaviors, when the time delay difference is smaller than the spiking width, the remaining 4 V spike height in this case would not fire the synapse toward a LRS in the depression direction (see **Figure 3h**). Therefore, by carefully designing the firing pulses between neurons in the neuromorphic circuit, a biological synapse behavior can be demonstrated with 1D-1R SiO_x-based resistive switching memories.

The 1D-1R architecture with SiO_x-based resistance switching devices and the structure of artificial neural networks map naturally onto hybrid CMOS/synapse circuits that can be designed on a single chip (**Figure 5**) to provide predictable results with an ultimate scaling potential of CMOS technology to the sub-10-nm level, which could possibly challenge the complexity and connectivity of the human brain.

The other topic is material implication operations by using the same device architecture in SiO_x-based memristor (**Figures 1** and **5**). Based on our recent reports, implication operation

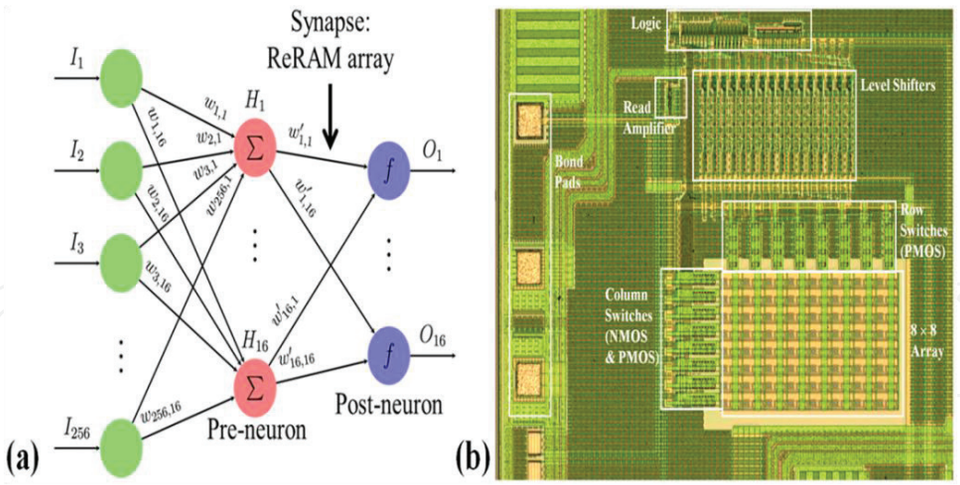
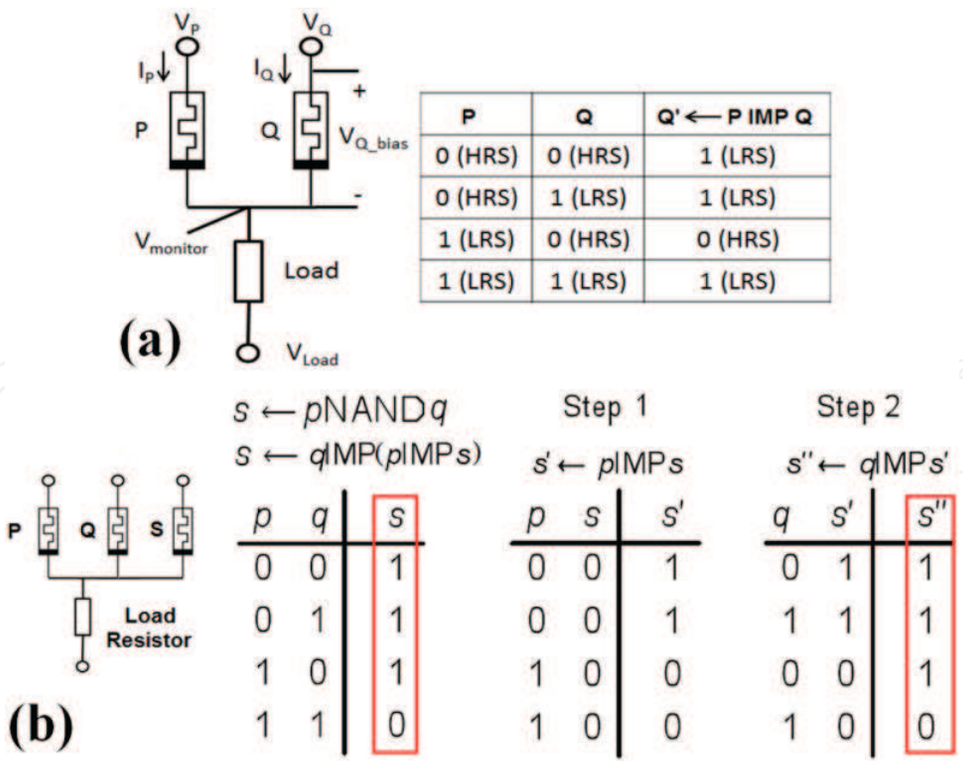


Figure 5. (a) Bio-inspired and mixed-signal information processing: hybrid CMOS/ReRAM circuits may also enable efficient analog dot-product computation, which is a key operation in artificial neural networks and many other information processing tasks. (b) A fabricated 8 × 8 artificial neural network array combined with CMOS transistors and logic control.

(IMP) has been performed by two SiO_x memristors and a 5.7 kΩ standalone resistor are configured as shown in **Figure 6a**. Furthermore, three memristors connected in the circuit shown in **Figure 6b** and two steps of IMP are required to perform a NAND operation. It may be noted



P	Q	Q' ← P IMP Q
0 (HRS)	0 (HRS)	1 (LRS)
0 (HRS)	1 (LRS)	1 (LRS)
1 (LRS)	0 (HRS)	0 (HRS)
1 (LRS)	1 (LRS)	1 (LRS)

p	q	s
0	0	1
0	1	1
1	0	1
1	1	0

p	s	s'
0	0	1
0	0	1
1	0	0
1	0	0

q	s'	s''
0	1	1
1	1	1
0	0	1
1	0	0

Figure 6. (a) Circuit for the implication scheme including two SiO_x memristor and one load resistor, with bias voltages and conducting currents marked out, and truth table for material implication [75]. (b) Circuit to perform NAND operation, and Truth table for NAND operation. Two steps performing NAND operation via implication with final results shown in red square. Figure reprinted by [75].

that the final logic value pNANDq is stored as the last value of memristor s, or s″ in **Figure 6b**. This row of three memristors, namely P, Q, S, can be expanded to a row consisting of more memristors all sharing the same load resistor. Implication operations can be performed on any two memristors in the row, as long as the rest of the memristors are kept unbiased. Since we are able to perform implication on one row, similarly, implication can be done on one column.

However, when we put multiple rows and columns together to form a crossbar array, several problems arise. The first issue is providing multiple voltage signals as well as a common load resistor to an arbitrary pair of memristor on the same row or column. Based on the crossbar RRAM structure, the bit-line/word-line selection transistor can serve as the common resistor. By varying the gate voltage bias of the select transistor, it can serve as an ON state switch, OFF state switch or a resistor with channel resistance of R_{Load}. From **Figure 6**, it is noted that four voltage signals (V_P, V_Q, V_S, and V_{Load}) are required during an implication operation, two different voltages along the same bit-line/word-line. Therefore, a total of four voltage lines, each connected to all NMOS select transistor, will provide voltage signals for implication operation.

The concepts are demonstrated by a 4 × 4 memristor crossbar array (**Figure 7a** and **b**) and a circuit with an 8 × 8 memristor crossbar array. In addition to 1D-1R device arrays (**Figure 5a**), the hybrid CMOS/1D-1R device architecture shown in **Figure 5e** has been successfully demonstrated as shown in **Figure 5f** by the *I-V* resistive switching plots. Using the NMOS/PMOS transistor also fabricated on the same chip (**Figure 5e**), an implication circuit is realized using two 1D1R memory elements and a transistor. In **Figure 7a** and **b**, the design is quite different from the RRAM crossbar array architecture, the circuit consists of two rows of bit select transistors for the same column of memristors, one on the top, and one on the bottom. Similarly, there are two column word select transistors for the same row of memristors, one on the left and one on the right. This redundancy ensures two distinctive voltage signals can be applied on any pair of memristors on the same bit line/word line. The implication voltages (V_P, V_Q, V_R)

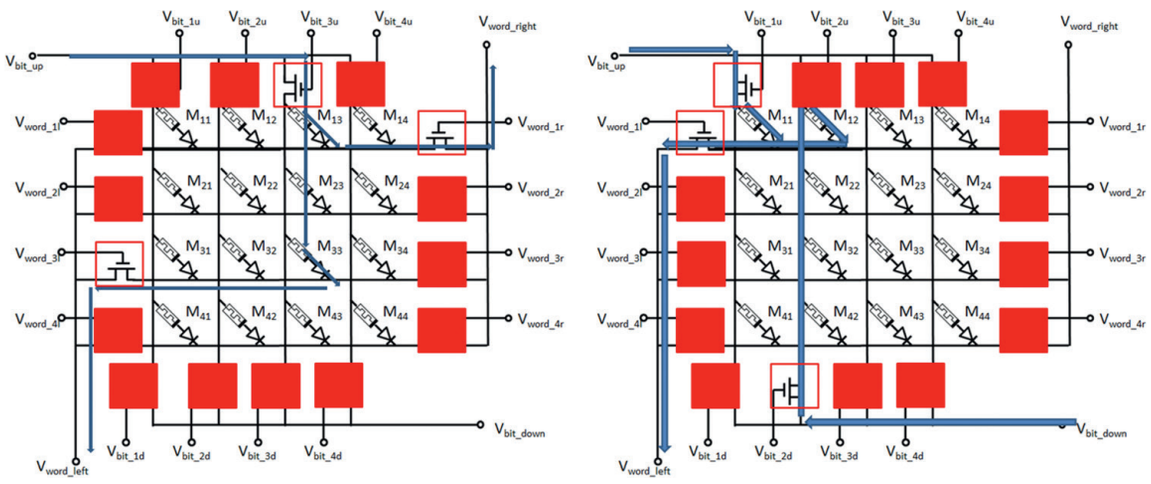


Figure 7. (a) and (b) demonstrate 4 × 4 crossbar structure memristor arrays with select transistors to achieve a one-bit full adder function. The implication circuit performs (a) M_{13} IMP M_{33} and (b) M_{11} IMP M_{12} on a 4 × 4 crossbar structure memristor array. Blue arrows show the current flow directions, and red solid squares cover all OFF-state transistors. Voltage signals and memristor numbers are labeled.

are biased on three of the four lines depending on the configuration, and the voltage applied to each line is labeled as follows, V_{bit_up}, V_{bit_down}, V_{word_left}, and V_{word_right}. The gate of each select transistor is also independently biased, to either isolate the bit lines/word lines from the implication voltages or provide that implication voltage to one particular bit line/word line.

To perform M_{13} IMP M_{33} (negative voltage implication operation performed along bit line 3): Assuming all memristors are initialized to HRS, bias $V_{bit\_up} = 2$ V, $V_{word\_left} = -1.5$ V, $V_{word\_right} = 0$ V, V_{word_1r}, and $V_{word\_3l} = V_{full\_on}$, $V_{bit\_3u} = V_{IMP}$, with all other transistor gate voltages at V_{full_off}. The equivalent circuit is shown in **Figure 5a** with the path of conduction current flow marked. In **Figure 5a–e**, P is M_{13}, Q is M_{33}, and the transistor bit_3u is used as the load resistor. The implication is a negative voltage scheme. All transistors that are biased at fully OFF states are covered by red squares, effectively keeping the voltages of irrelevant columns/rows floating; to perform M_{11} IMP M_{12} (positive voltage implication operation performed along word line 1): Assuming all memristors are initialized to HRS, Bias $V_{bit\_up} = 0$ V, $V_{bit\_down} = 1.5$ V, $V_{word\_left} = -2$ V, V_{bit_1u}, and $V_{bit\_2d} = V_{full\_on}$, $V_{word\_1l} = V_{IMP}$, with all other transistor gate voltages at V_{full_off}. This equivalent circuit is shown in **Figure 5b** with the current flow path marked. In **Figure 5b**, P is M_{11}, Q is M_{12}, and the transistor word_1l is used as the load resistor. In this case, the implication uses a positive voltage scheme. As before, all transistors biased to fully OFF states (covered by red squares) effectively keep the voltages of irrelevant columns/rows floating.

In **Figures 1a** and **5a**, each memristor is placed in series with a pn diode in order to avoid current sneak-path problems. Originating from the crossbar device structure itself, the sneak-path problem has been identified and analyzed by many previous researchers [20, 76–122]. Because the bit line or word line select transistor raises the voltage across the whole bit or word, a group of memristors in the LRS may form a highly conductive path and cause misreading of certain memristors. The solution to the sneak-path problem is using a selection element together with a memory element, as shown in **Figure 5f**. Such a selection element is used to allow current conduction in one direction while suppressing current flow in the other direction. The most common selection element is a low-leakage pn diode, limiting the current flowing through the sneak paths down to reverse the bias leakage current level and reducing the power consumption during implication operations.

5. Summary

In summary, we have demonstrated potentiation, depression and spike-timing-dependent plasticity in a synaptic device built using a SiO_x-based 1D-1R architecture. Proton-induced resistive switching behaviors in the SiO_x memory element were discussed, where the SET threshold is modeled as proton desorption from the $(SiH)_2$ defect to generate the conductive hydrogen bridge, Si-H-Si, and the RESET transition is modeled as proton release and capture to reform nonconductive $(SiH)_2$ [82–89]. The electrical results demonstrate that the technology has good potential for providing a simple and robust approach for large-scale integration of programmable neuromorphic chips using CMOS technology, and represent a critical milestone regarding the potential use of SiO_2-based resistive memory as a synaptic device in future synthetic biological computing applications. Moreover, a logic circuit consisting of a

4 × 4 array of crossbar structure memristor 1D1R memory elements and select transistors are proposed together with bidirectional implication schemes. Then a one-bit full adder is theoretically realized with a total of 48 operation steps performed on the circuit. A comparison between CMOS-enabled logic circuits and memristor-enabled circuits shows advantages in real estate and power consumption, as well as disadvantages in speed. This result suggests the memristor-enabled logic circuit is most suitable for high-speed, low-power, high-density applications. Further study is still required to make a few steps in various implication schemes as well as lower power consumption in synaptic computations.

Author details

Cheng-Chih Hsieh[1], Yao-Feng Chang[1]*, Ying-Chen Chen[1], Xiaohan Wu[1], Meiqi Guo[1], Fei Zhou[1], Sungjun Kim[2], Burt Fowler[1], Chih-Yang Lin[3], Chih-Hung Pan[3], Ting-Chang Chang[3] and Jack C. Lee[1]

*Address all correspondence to: yfchang@utexas.edu

1 Microelectronics Research Center, the University of Texas at Austin, Austin, TX, USA

2 Inter-university Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University, Seoul, Korea

3 Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan

References

[1] Lundstrom M. Science. 2003;**299**:210-211. DOI: 10.1126/science.1079567

[2] Ieong M, Doris B, Kedzierski J, Rim K, Yang M. Science. 2004;**306**:2057. DOI:10.1126/science.1100731

[3] Chen YY, Degraeve R, Clima S, Govoreanu B, Goux L, Fantini A, Kar GS, Pourtois G, Groeseneken G, Wouters DJ, Jurczak M. Techenical Digest. International Electron Devices Meet (IEDM); 2012. p. 482. DOI: 10.1109/TED.2012.2218607

[4] Kahng D, Sze SM. Bell System Technical Journal. 1967;**46**:1288-1295. DOI: 10.1109/T-ED.1976.18468

[5] Chang TC, Jiana FY, Chenc SC, Tsai YT. Materials Today. 2011;**14**:608-615. DOI: 10.1016/S1369-7021(11)70302-9

[6] Lu W, Lieber CM. Nature Materials. 2007;**6**:841. DOI: 10.1038/nmat2028

[7] Heath JR, Ratner MA. Physics Today. 2003;**56**:43. DOI: 10.1063/1.1583533

[8] Sawa A. Materials Today. 2008;**11**:28. DOI:10.1016/S1369-7021(08)70119-6

[9] Terabe K, Hasegawa T, Nakayama T, Aono M. Nature. 2005;**433**:47. DOI: 10.1038/nature03190

[10] Lee MJ, Lee CB, Lee D, Lee SR, Chang M, Hur JH, Kim YB, Kim CJ, Seo DH, Seo S, Chung UI, Yoo IK, Kim K. Nature Materials. 2011;**10**:625. DOI: 10.1038/nmat3070

[11] ITRS International Technology Roadmap for Semoconductors, (2013) edn; http://www.itrs.net

[12] Yu S, Chen HY, Gao B, Kang J, Wong HSP. ACS Nano. 2013;**7**:2320. DOI: 10.1021/nn305510u

[13] Song S, Cho B, Kim TW, Ji Y, Jo M, Wang G, Choe M, Kahng YH, Hwang H, Lee T. Advanced Materials. 2010;**22**:5048. DOI: 10.1002/adma.201002575

[14] Valov I, Linn E, Tappertzhofen S, Schmelzer S, van den Hurk J, Lentz F, Waser R. National Nature Communication. 2013;**4**:1771. DOI:10.1038/ncomms2784

[15] Jo SH, Chang T, Ebong I, Bhadviya BB, Mazumder P, Lu W. Nano Letters. 2010;**10**:1297. DOI: 10.1021/nl904092h

[16] Ohno T, Hasegawa T, Tsuruoka T, Terabe K, Gimzewski JK, Aono M. Nature Materials. 2011;**10**:591. DOI:10.1038/nmat3054

[17] Borghetti J, Snider GS, Kuekes PJ, Yang JJ, Stewart DR, Williams RS. Nature. 2010;**464**:873-876. DOI: 10.1038/nature08940

[18] Chua LO. IEEE Transactions on Circuit Theory. 1971;**18**:507. DOI: 10.1109/TCT.1971.1083337

[19] Chang YF, Fowler B, Chen YC, Zhou F, Pan CH, Chang TC, Lee JC. Scientific Reports. 2016;**6**:21268. DOI: 10.1038/srep21268

[20] Chen Y, Fowler B, Wang Y, Xue F, Zhou F, Chang YF, Lee JC. ECS Journal of Solid State Science and Technology. 2012;**1**:148. DOI: 10.1149/2.013203jss

[21] Carlos ZR, Luis AC, Jose AP, Timothée M, Teresa SG, Bernabé LB. Frontiers in Neuroscience. 2011;**5**:26. DOI: 10.3389/fnins.2011.00026

[22] Demming A, Gimzewski JK, Vuillaume D. Nanotechnology. 2014;**24**:380201. DOI: 10.1088/0957-4484/24/38/380201

[23] Serrano-Gotarredona T, Masquelier T, Prodromakis T, Indiveri G, Linares-Barranco B. Frontiers In Neuroscience. 2013;**7**:2. DOI: 10.3389/fnins.2013.00002

[24] Suri M, Querlioz D, Bichler O, Palma G, Vianello E, Vuillaume D, Gamrat C, DeSalvo B. IEEE Transactions on Electron Devices. 2013;**60**:2402. DOI: 10.1109/TED.2013.2263000

[25] Ambrogio S, Balatti S, Nardi F, Facchinetti S, Ielmini D. Nanotechnology. 2013;**24**:384012. DOI:10.1088/0957-4484/24/38/384012

[26] Hsieh CC, Roy A, Chang YF, Rai A, Banerjee S. 73rd Annual Device Research Conference (DRC). 2015. 101-102. DOI: 10.1109/DRC.2015.7175575

[27] Xia Q, Yang JJ, Wu W, Li X, Williams RS. Nano Letters American Chemical Society. 2009;**9**:3640. DOI: 10.1021/nl901874j

[28] Sills S, Yasuda S, Calderoni A, Cardon C, Strand J, Aratani K, Ramaswamy N. Symposium on VLSI Technology. 2015 T106. DOI: 10.1109/VLSIT.2015.7223639

[29] Chang YF et al. VLSI Technology, Systems, and Applications (VLSI-TSA). 2016. 1-2. DOI: 10.1109/VLSI-TSA.2016.7480497

[30] Guo M, Chen YC, Chang YF, Wu X, Fowler B, Zhao Y, Lee JC. Device Research Conference (DRC), 74th Annual. 2016. 1-2. DOI: 10.1109/DRC.2016.7548460

[31] Chen YC et al. ECS Transactions. 2016;**72**(2):25-33. DOI: 10.1149/07202.0025ecst

[32] Zhou J, Tang Y, Wu J, XFang X, Zhu X, Huang D. ICISEM. 2013. DOI: 10.1109/ICISEM.2013.87

[33] Indiveri G, et al. Frontiers in Neuroscience. 2011;**5**:73-96. DOI: 10.3389/fnins.2011.00073

[34] Yang JJ, Strukov DB, Stewart DR. Nature Nanotechnology. 2013;**8**:13-24. DOI:10.1038/nnano.2012.240

[35] Waser R, Aono M, Nature Materials. 2007;**6**:833. DOI:10.1038/nmat2023

[36] Rainer W, ReginaD, Staikov G, Szot K. Advanced Materials. 2009;**21**:2632-2663. DOI: 10.1002/adma.200900375

[37] Yang JJ et al., Nature Nanotechnology. 2008;**3**:429-433. DOI:10.1038/nnano.2008.160

[38] Szot K, Speier W, Bihlmayer G, Waser R. Nature Materials. 2005;**5**:312-320. DOI:10.1038/nmat1614

[39] Meijer GI. Science. 2008;**319**:1625-1626. DOI:10.1126/science.1153909

[40] HickmottTW. Journal of Applied Physics. 1962;**33**:2669-2682. DOI: 10.1063/1.1702530

[41] Simmons JG, Verderber RR, The Royal Society Proceedings of the London Series. 1967; A **301**:77. DOI: 10.1098/rspa.1967.0191

[42] Dearnaley G, Stoneham A M, Morgan DV. Reports On Progress In Physics. 1970;**33**:1129-1191. DOI:10.1088/0034-4885/33/3/306

[43] Yao J, Sun Z, L Zhong L, Natelson D, J M. Tour. Nano Letters. 2010;**10**:4105. DOI: 10.1021/nl102255r

[44] Yao J, Lin J, Dai Y, Ruan G, Yan Z, Li L, Zhong L, Natelson D, J M. Tour. Nature Communications. 2012;**3**:1101. DOI:10.1038/ncomms2110

[45] Wang G, Lauchner AC, Lin J, Natelson D, Palem KV, Tour JM. Advance Materials. 2013;**25**:4789. DOI: 10.1002/adma.201302047

[46] Lamb DR, Rundle PC, British Journal of Applied Physics. 1967;**18**:29. DOI: 10.1088/0508-3443/18/1/306

[47] Mehonic A, Cueff S, Wojdak M, Hudziak S, Jambois O, Labbé C, Garrido B, Rizk R, Kenyon AJ. Journal of Applied Physics. 2012;**1**:11, 074507. DOI: 10.1063/1.3701581

[48] Mehonic A, Cueff S, M. Wojdak M, Hudziak S, Labbé C, Rizk R, Kenyon AJ. Nanotechnology. 2012;**23**:455201. DOI:10.1088/0957-4484/23/45/455201

[49] Cavallini M, Hemmatian Z, Riminucci A, Prezioso M, Morandi V, Murgia M. Advance Materials. 2012;**24**:1197. DOI: 10.1002/adma.201104301

[50] Ji L, Chang YF, Fowler B, Chen YC, Tsai TM, Chang KC, Chen MC, Chang TC, Sze SM, Yu ET, Lee JC. Nano Letters. 2014;**14**:813-818. DOI: 10.1021/nl404160u

[51] Kuzum D, Jeyasingh RGD, Lee B, Wong HSP. Nano Letters. 2011;**12**:2179. DOI: 10.1021/nl201040y

[52] Cho B, Kim TW, Song S, Ji Y, Jo M, Hwang H, Jung GY, Lee T. Advanced Materials. 2010;**22**:1228. DOI: 10.1002/adma.200903203

[53] Chang YF, et al. Journal of Applied Physics. 2012;**112**:123702. DOI: 10.1063/1.4769218

[54] Dang TA, Chau C N. Journal of Electrochemical Society. 1996;**143**:302-305. DOI: 10.1149/1.1836427

[55] Alfonsettia R, et al. Applied Surface Sciences. 1993;**70**:222-225. DOI: 10.1016/0169-4332(93)90431-A

[56] Zhou F, et al. Applied Physics Letters. 2014;**105**:163506. DOI: 10.1063/1.4900422

[57] Chang YF, et al. Applied Physics Letters. 2013;**103**:193508. DOI: 10.1063/1.4829526

[58] Mehonic A, et al. Applied Physics Letters. 2015;**117**:124505-1245013. DOI: 10.1063/1.4916259

[59] Chang YF, et al. Applied Physics Letters. 2014;**116**:043708. DOI: 10.1063/1.4891242

[60] Chang YF, et al. Applied Physics Letters. 2014;**116**:043709. DOI: 10.1063/1.4891244

[61] Yao J, Zhong L, Natelson D, Tour JM. Scientific Reports. 2012;**2**:242-247. DOI: 10.1038/srep00242

[62] He C, et al. Advanced Materials. 2013;**25**:5593-5598. DOI: 10.1002/adma.201302447

[63] Chang YF, et al. Applied Physics Letters. 2013;**103**:033521. DOI: 10.1063/1.4816162

[64] Tappertzhofen S, Hempel M, Valov I, Waser R. Materials Research Society Symposia Proceedings. 2011;**1330**. doi:10.1557/opl.2011.1198

[65] Tappertzhofen S, et al. ACS Nano. 2013;**7**:6396-6402. DOI: 10.1021/nn4026614

[66] Tappertzhofen S, Waser R, Valov I. ChemElectroChem. 2014;**1**:1287-1292. DOI: 10.1002/celc.201402106

[67] Valov I. ChemElectroChem. 2014;**1**:26-36. DOI: 10.1002/celc.201300165

[68] Wedig A, et al. Nature Nanotechnology. 2015. DOI:10.1038/nnano.2015.221

[69] Messerschmitt F, Kubicek M, Rupp JLM. Advanced Functional Materials. 2015;**25**:5117-5125. DOI: 10.1002/adfm.201501517

[70] Lübben M, et al. Graphene-modified interface controls transition from VCM to ECM switching modes in Ta/TaOx based memristive devices. Advanced Materials. 2015;**27**:6202-6207. DOI: 10.1002/adma.201502574

[71] Jameson JR, Nishi Y. Role of hydrogen ions in TiO_2-based memory devices. Integrated Ferroelectrics. 2011;**124**:112-118. DOI: 10.1080/10584587.2011.573733

[72] Arnold W P, Mittal CK, Katsuki S, Murad F. Nitric oxide activates guanylate cyclase and increases guanosine 3′,5′-cyclic monophosphate levels in various tissue preparations. Proceedings of National Academy of Sciences U.S.A. 1977;**74**:3203-3207. DOI: 10.1073/pnas.74.8.3203

[73] Chang YF, et al. Applied Physics Letters. 2012;**101**:052111-052115. DOI: 10.1063/1.3294632

[74] Blöchl PE. Physics Review B. 2000;**62**:6158-6179. DOI: 10.1103/PhysRevB.62.6158

[75] Zhou F, Guckert L, Chang YF, Swartzlander EE Jr, Lee J. Applied Physical Letters. 2015;**107**:183501. DOI: 10.1063/1.4934835

[76] Liou JJ, Liaw SK, Chung YH. Nano Devices and Sensors, De Gruyter. Walter de Gruyter GmbH & Co KG. 2016. ISBN: 978-1-5015-0153-1

[77] Chang YF, et al. VLSI Technology, Systems, and Applications (VLSI-TSA), 2013. DOI: 10.1109/VLSI-TSA.2013.6545589

[78] Strukov DB, Snider GS, Stewart DR, Williams RS. The missing memristor found. Nature. 2008;**453**:80-83. DOI: 10.1038/nature06932

[79] Pickett MD, Strukov DB, Borghetti JL, Yang JJ, Snider GS, Stewart DR, Williams R S. Journal of Applied Physics. 2009;**106**:074508. DOI: 10.1063/1.3236506

[80] Sun X, Li G, Ding L, Yang N, Zhang W. Applied Physics Letters. 2011;**99**:072101. DOI: 10.1063/1.4934835

[81] Linn E, Rosezin R, Kügeler C, Waser R. Complementary resistive switches for passive nanocrossbar memories. Nature Materials. 2010;**9**:403. DOI: 10.1038/nmat2748

[82] Fowler B, Chang YF, Zhou F, Wang Y, Chen PY, Xue F, Chen Y T, Bringhurst B, Pozder S, Lee JC. RSC Advances. 2015;**5**:21215. DOI: 10.1039/C4RA16078A

[83] Zhou F, Chang YF, Chen YC, Wu X, Zhang Y, Fowler B, Lee JC, Physical Chemistry Chemical Physics. 2016;**18**:700. DOI: 10.1039/C5CP06507K

[84] Chang YF, Fowler B, Zhou F, Chen YC, Lee JC. Applied Physical Letters. 2016;**108**:033504. DOI: 10.1063/1.4940203

[85] WangY, Chen YT, Xue F, Zhou F, Chang YF, Fowler B, Lee JC. Applied Physical Letters. 2012;**100**:083502. DOI: 10.1063/1.3687724

[86] Chen YT, Fowler B, Wang Y, Xue F, Zhou F, Chang YF, Chen P Y, Lee JC. IEEE Electron Device Letters. 2012;**33**:1702. DOI: 10.1109/LED.2012.2218566

[87] Wang Y, Fowler B, Zhou F, Chang YF, Chen YT, Xue F, Lee JC. Applied Physical Letters. 2013;**103**:213505. DOI: 10.1063/1.4832595

[88] Wang Y, Fowler B, Chen YT, Xue F, Zhou F, Chang YF, and Lee Wang JC. Applied Physical Letters. 2012;**101**:183505. DOI: 10.1063/1.4765356

[89] Zhou F, Chang YF, Byun K, Fowler B, Lee JC. Applied Physical Letters. 2014;**105**:133501. DOI: 10.1063/1.4896877

[90] Chu TJ, et al. IEEE Electron Device Letters. 2013;**34**(4):502-504. DOI: 10.1109/LED.2013.2242843

[91] Feng LW, Chang CY, Chang YF, Chen WR, Wang SY, Chiang PW, Chang TC. Applied Physical Letters. 2010;**96**:052111. DOI: 10.1063/1.3294632

[92] Chang KC, et al. Nanoscale Research Letters. 2015;**10**(1):1. DOI: 10.1186/s11671-015-0740-7

[93] ChangYF, Chang TC, Chang CY. Journal of Applied Physics. 2011;**110**(5):053703. DOI: 10.1063/1.3630119

[94] Yang S, et al. Advanced Materials. 2016;**27**(41):6423-6430. DOI: 10.1002/adma.201502386

[95] Feng LW, Chang CY, Chang YF, Chang TC, Wang SY, Chen SC, Lin CC, Chen SC, Chiang PW. Applied Physics Letters. 2010;**96**:222108. DOI: 10.1063/1.3428777

[96] Feng LW, Chang CY, Chang TC, Tu CH, Wang PS, Chang YF, Chen MC, Huang HC. Applied Physics Letters. 2009;**95**:262110-262113. DOI: 10.1063/1.3279131

[97] Zhou F, Chang YF, Fowler B, Byun K, Lee JC. Applied Physics Letters. 2015;**106**:063508. DOI: 10.1063/1.4909533

[98] Zhou F, Chang YF, Wang Y, Chen YT, Xue F, Fowler BW, Lee J C. Applied Physics Letters. 2014;**105**:163506. DOI: 10.1063/1.4900422

[99] Xue F, Jiang A, Chen YT, Wang Y, Zhou F, Chang YF, Lee J. Electron Devices Meeting (IEDM), 2012 IEEE International, 27.5. 2012;1-27.5. 4. DOI: 10.1109/IEDM.2012.6479116

[100] Feng LW, Chang YF, Chang CY, Chang TC, Wang SY, Chiang PW, Lin CC, Chen SC, Chen SC. Thin Solid Films. 2010;**519**:1536. DOI: 10.1016/j.tsf.2010.08.165

[101] Chang YF, Chen YT, Xue F, Wang Y, Zhou F, Fowler B, Lee JC. Device Research Conference (DRC), 70th Annual. 2012. 49. DOI: 10.1109/DRC.2012.6256972

[102] Hsieh CC, Roy A, Rai A, Chang YF, Banerjee SK. Applied Physics Letters. 2015;**106**:173108. DOI: 10.1063/1.4919442

[103] Xue F, Jiang A, Chen YT, Wang Y, Zhou F, Chang YF, Lee JC. IEEE Transactions on Electron Devices.2014;**61**:2332. DOI: 10.1109/TED.2014.2320946

[104] Zhou F, Xue F, Chang YF, Lee JC. Device Research Conference (DRC), 2014 72nd Annual. 2014. 207. DOI: 10.1109/DRC.2014.6872370

[105] Chang YF, Feng LW, Chang TC. Materials Chemistry and Physics. 2011;**131**:262. DOI: 10.1016/j.matchemphys.2011.09.037

[106] Cheng CC, Chien CH, Luo GL, Liu JC, Chen YC, Chang YF, Wang SY, Kei CC, Hsiao CN, and Chang CY, Journal of Vacuum Science & Technology B. 2009;**27**:130. DOI: 10.1116/1.3058724

[107] Xue F, Chen YT, Wang Y, Zhou F, Chang YF, Fowler B, Lee JC, ECS Transactions. 2012; **45**:245. DOI: 10.1149/1.3700959

[108] Chang YF, Tsai YT, Syu YE, Chang TC. ECS Journal of Solid State Science and Technology. 2012;**1**:Q57. DOI: 10.1149/2.020203jss

[109] Chang YF, Tsai YT, Chang GW, Syu YE, Tai YH, Chang TC. ECS Journal of Solid State Science and Technology. 2012;**1**:Q91. DOI: 10.1149/2.003205jss

[110] Chang YF, Fowler B, Zhou F, Lee JC, ECS Transactions. 2016;**69**(5):149-164. DOI: 10.1149/06905.0149ecst

[111] Chang YF, Fowler B, Chen YC, Lee JC, Progress in Solid State Chemistry. 2016;**44**(3):75-85. DOI: 10.1016/j.progsolidstchem.2016.07.001

[112] Chen YT, Fowler B, Chang YF, Wang Y, Xue F, Zhou F, Lee JC. ECS Solid State Letters. 2013;**2**:N18. DOI: 10.1149/2.009305ssl

[113] Hsieh CC, Roy A, Chang YF, Shahrjerdi D, Banerjee SK, Applied Physics Letters. 2016;**109**(22):223501. DOI: 10.1063/1.4971188

[114] Chang YF, Fowler B, Zhou F, Byun K, Lee JC, VLSI-TSA, 2015. 1-2. DOI: 10.1109/VLSI-TSA.2015.7117558

[115] Ji L, et al., IEEE International Electron Devices Meeting. 8.6. 2014. 1-8.6. 3. DOI: 10.1109/IEDM.2014.7047013

[116] Ji L, et al. 72nd Device Research Conference; 2014. pp. 243-244 DOI: 10.1109/DRC.2014.6872388

[117] Chang YF, Fowler B, Chen YC, Ji L, Zhou F, Lee JC, 72nd Device Research Conference, 2014. 1. DOI: 10.1109/DRC.2014.6872349

[118] Zhou F, Xue F, Chang YF, Lee J, 72nd Device Research Conference, 2014. 207-208. DOI: 10.1109/DRC.2014.6872370

[119] Chang YF et al., VLSI-TSA, 2014. 1-2. DOI: 10.1109/VLSI-TSA.2014.6839674

[120] Chang YF, Chen YC, Li J, Xue F, Wang Y, Zhou F, Fowler B, Lee JC, Device Research Conference (DRC), 71st Annual, 2013. 135-136. DOI: 10.1109/DRC.2013.6633830

[121] Wang Y, Chen YT, Xue F, Zhou F, Chang YF, Lee JC. ECS Transactions. 2013;**50**(4):151-156 DOI: 10.1149/05004.0151ecst

[122] Chen YC, Chang YF, Wu X, Zhou F, Guo M, Lin CY, Hsieh CC, Fowler B, Chang TC, Lee JC, RSC Advances. 2017;**7**. DOI: 10.1039/c7ra00567a