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Organic Field-Effect Transistor: Device Physics, Materials, and Process

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Abstract

Organic field-effect transistors have received much attention in the area of low cost, large area, flexible, and printable electronic devices. Lots of efforts have been devoted to achieve comparable device performance with high charge carrier mobility and good air stability. Meanwhile, in order to reduce the fabrication costs, simple fabrication conditions such as the printing techniques have been frequently used. Apart from device optimization, developing novel organic semiconductor materials and using thin-film alignment techniques are other ways to achieve high-performance devices and functional device applications. It is expected that by combining proper organic semiconductor materials and appropriate fabrication techniques, high-performance devices for various applications could be obtained. In this chapter, the organic field-effect transistor in terms of device physics, organic materials, device process, and various thin-film alignment techniques will be discussed.

Keywords: organic field-effect transistors, device physics, organic semiconductor materials, device process, thin-film alignment

1. Introduction

Organic field-effect transistors (OFETs) have received much attention for plastic electronics due to their good solution processability, low temperature deposition, low cost, and compatibility with large-area printing technology. Although the conventional amorphous silicon-based semiconductors have achieved much progress with charge carrier mobility around 1.0 cm^2 V^{-1} s^{-1}, the thin-film deposition of conventional semiconductor usually needs high temperature process and dustless conditions which significantly increase the fabricating cost. Most importantly, the silicon-based materials are rare to be processed on flexible substrates due to their poor stretching characteristics. Nevertheless, compared to the conventional silicon-based semiconductors, the organic-based semiconductors exhibit low cost, good processability and can be fabricated on

flexible substrates. Hence, using organic semiconducting materials has become an important topic in the development of low-cost, large area, flexible, and lightweight devices.

Organic-based semiconductors have various applications as key components of numerous electronic and optoelectronic devices, including field-effect transistors (FETs), photovoltaics (PVs), and light-emitting diodes (LED). Especially for the field-effect transistor, a lot of efforts have been done to develop new organic materials to improve device performance with high charge carrier mobility and good air stability. Anyhow, OFETs have been considered as a key component of organic integrated circuits for application in flexible smart cards, low-cost radio frequency identification (RFID) tags, sensor devices, organic active matrix displays, and so on [1–6]. However, it is still far from satisfactory for practical applications. The focus of recent attention has been devoted to improving device performance and stability, reducing the fabrication cost, exploring new applications, and developing simple fabrication techniques. Overcoming these challenges relies on the novel organic semiconductor development and device optimization.

In this chapter, organic field-effect transistors will be discussed from three aspects: the device physics, device materials, and device processing. The first section will talk about the charge transport and related mechanisms in organic semiconductor materials and the techniques used to characterize the charge carrier mobility, such as time of flight, field-effect transistor, and space-charge limited current (SCLC) technique. In the second section, we discuss the organic field-effect transistor from basic principle, device structure, and the main parameters, such as charge carrier mobility, current on/off ratio, threshold voltage, subthreshold voltage, and the corresponding influence factors in the OFET. The third section will talk about the organic materials selection, including mostly used aromatic p-type semiconductors and n-type semiconductors. The forth section will discuss the fabrication techniques in the organic field-effect transistors, including vapor deposition, solution deposition, and some thin-film alignment methods.

2. Device physics

2.1. Charge transport and related mechanisms

The study of electron and hole transport in organic materials has a long history which dates back to 60 years ago. Many groups have done their efforts on this topic. In the mid-1970s, Scher group laid the theoretical description of hopping transport in disordered materials by using the continuous-time random walk model [7]. Until today, the exact nature of charge transport in organic semiconductors is still open to debate. However, a general idea can be obtained using the disordered semiconductors and highly ordered organic single crystals as the standards. In organic semiconductors, the charge carrier transport mechanism depends on the degree of order and falls between the band and hopping transport which are the two extreme transport cases. Typically, band transport could be observed in highly purified molecular crystals at low temperatures. However, the bandwidth in organic semiconductors is smaller than that in inorganic semiconductors (typically a few kT at room temperature only) due to the

weak electronic delocalization [8]. Hence, the mobility value in molecular single crystals at room temperature reaches only in the range from 1 to 10 cm^2 V^{-1} s^{-1}. In the other extreme case of an amorphous organic solid, hopping transport prevails, which leads to much lower mobility values (at best around 10^{-3} cm^2 V^{-1} s^{-1}).

When localization occurs in conjugated organic materials, the polarons resulting from the conjugated chain deformation under the charge action could be formed (or the charge is self-trapped by the deformation) [9]. This mechanism of self-trapping is often described through the creation of localized states in the gap between the valence and the conduction bands.

To better understand the charge transport in organic materials, a one-dimensional, one-electron model, the small polaron model, has been developed by Holstein [9]. In this model, the electron-electron interactions are assumed to be neglected, and the lattice energy, electron dispersion energy, and the polaron banding energy are the three terms which constitute the total energy of the system [9].

The charge carrier mobility is temperature and field dependence. For temperature-dependent mobility, when the mobility is extrapolated at the zero-field limit, the Monte Carlo (MC) fitting results lead to the following expression:

$$\mu(T) = \mu_0 \exp\left[-\left(\frac{T_0}{T}\right)^2\right]$$

(1)

where μ_0 is the mobility at room temperature and T_0 is the room temperature. Since the temperature helps in overcoming the barriers introduced by the energetic disorder in the system, the temperature talked about here only depends on the amplitude of the diagonal disorder width. This expression deviates from an Arrhenius-like law, and this expression generally fits the experimental data well, as a result of the limited range of temperatures available.

The impact of an external electric field is to lower the energy barrier for the electron conduction band transport since part of this energy could be provided by the driving force of the electric field. In the presence of energetic disorder only, the Monte Carlo results generally yield a Poole-Frenkel behavior when electric fields are larger than 10^4–10^5 V/cm:

$$\mu(E) = \mu_0 \exp(\beta\sqrt{E})$$

(2)

where μ_0 is the low field mobility, β is Poole-Frenkel coefficient, and E is the applied electric field [10]. The field dependence becomes more pronounced as the extent of energetic disorder grows. The increase in electric field amplitude is also accompanied by an increased diffusion constant.

2.2. Characterization of charge carrier mobility

Charge carrier mobility can be determined by various techniques [11, 12]. The mobility measured by the methods with the measurement over macroscopic scales (~1 mm) is often dependent on the material order and purity. Instead, when the mobility measurement is over

microscopic scales, the measurement result is less dependent on these characteristics. In this section, the basic principle of most used mobility measurement techniques, time-of-flight (TOF), field-effect transistor (FET), and space-charge limited current (SCLC) will be briefly described.

2.2.1. Time-of-flight (TOF)

For the TOF measurement, a few micron thick organic active layer is sandwiched between two metal electrodes (**Figure 1**). As shown in **Figure 1**, first, the material is irradiated to generate charges by a laser pulse near one electrode. Then, the photo-generated holes or electrons migrate across the material toward another electrode depending on the polarity of the applied bias and the corresponding electric field (in the 10^4–10^6 V/cm range). After that, the current at that electrode is recorded as a function of time. Finally, for ordered materials, a sharp signal will be obtained, while for disordered systems, a broadening of the signal will occur because of the distribution of transient times across the material. The hole or electron mobility is estimated via the following equation:

$$\mu = \frac{v}{F} = \frac{d}{Ft} = \frac{d^2}{Vt} \tag{3}$$

where d is the distance between the electrodes, F is the electric field, t is the averaged transient time, and V is the applied voltage. TOF measurements clearly show the impact of structural defects present in the material on charge carrier mobility. Charge carrier mobilities in organic materials were first measured with the TOF technique by Kepler [13] and Leblanc [14].

2.2.2. Field-effect transistor (FET) configuration

The electrical characteristics measured in a field-effect transistor (FET) configuration could also be used to extract the charge carrier mobilities (**Figure 2**). As previously Horowitz talked about [15], the derived current-voltage expressions for inorganic-based transistors in both
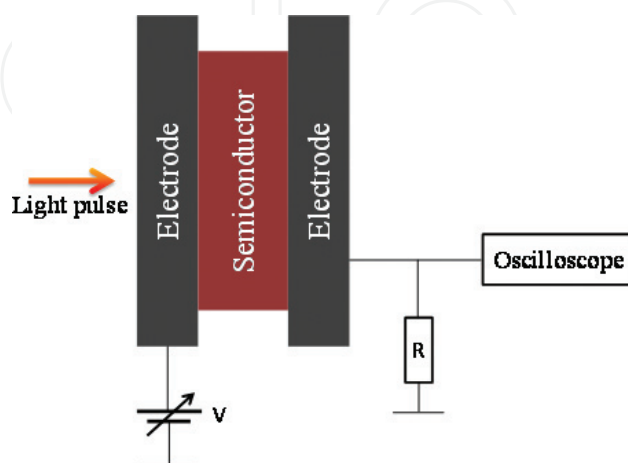

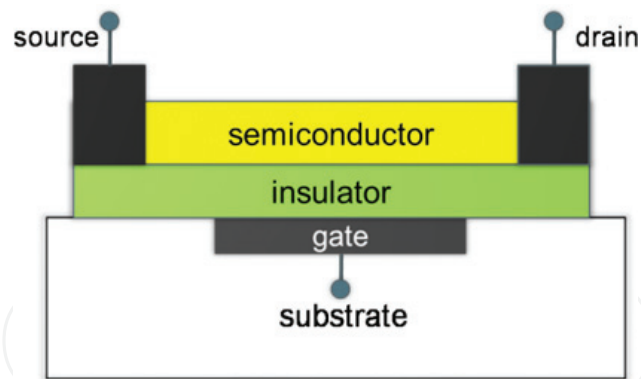**Figure 1.** The setup of the TOF technique.

Figure 2. The structure of thin-film transistor.

linear and saturated regimes are also applicable to organic field-effect transistors (OFETs). These expressions in the linear regime are:

$$I_{DS} = \frac{W}{L} C_i \mu (V_G - V_T) V_D, V_D < V_G - V_T, \tag{4}$$

and in the saturated regime:

$$I_{DS} = \frac{W}{2L} C_i \mu (V_G - V_T)^2, V_D > V_G - V_T. \tag{5}$$

Here, I_{DS} and V_{DS} are the current and voltage bias between source and drain, respectively, V_G denotes the gate voltage, V_T is the threshold voltage, C_i is the capacitance of the gate dielectric, and W and L stand for the width and length of the conducting channel, respectively. In FETs, the charges migrate at the interface between the organic semiconductor and the dielectric within a few nanometer-wide channel [16, 17]. There are several factors that affect the charge transport, such as structural defects at the interface within the organic layer, the dielectric surface morphology and polarity, and the traps existing at the interface (that depends on the chemical structure of the gate dielectric surface). Contact resistances at the source and drain metal/organic interfaces also play significantly important roles, and when the channel length decreases and the transistor operates at low fields, it becomes more important. Anyhow, its effect can be accounted for via four-probe measurements [18].

The charge carrier mobilities extracted from the FET current-voltage curves in the saturated regime are generally higher than those in the linear regime due to different electric-field distributions. The mobility was found to be gate-voltage dependent [19], and it is often related to the presence of traps which is usually caused by structural defects and/or impurities and/or charge carrier density (which is modulated by V_G) [20].

The dielectric constant of the gate insulator is another important parameter. For instance, measurements on rubrene single crystals [21] and polytriarylamine chains [22] show that the charge carrier mobility decreases with the increased dielectric constant because of polarization effects across the interface. At the dielectric surface, the polarization induced by the charge

carriers within the conducting channel of organic semiconductors couples to the carrier motion, which can be cast in the form of a Frolich polaron [23, 24].

2.2.3. Space-charge limited current (SCLC)

The mobilities can also be extracted from the electrical characteristics measured in a diode configuration with an organic layer sandwiched between two metal electrodes (**Figure 3**). In this case, we are assuming that carrier transport is bulk limited instead of contact limited. The electrode is chosen in such a way that at low voltage, only electrons or holes are injected. In the absence of traps and at low electric fields, the behavior of the current density J quadratically scaling with applied bias V is a space-charge limited current (SCLC) characteristic, and it corresponds to the current obtained when the number of injected charges reaches a maximum because their electrostatic potential prevents the injection of additional charges [25]. In this case, the charge density is maximum approaching the injecting electrode instead of uniform across the material [26]. In this regime, when diffusion contributions are neglected, we can describe J-V characteristics as:

$$J = \frac{9}{8} \varepsilon_0 \varepsilon_r \mu \frac{V^2}{d^3} \tag{6}$$

where ε_r is the dielectric constant of the active layer and d denotes the device thickness. (Note that at high electric fields, it has to consider a field-dependence of the mobility.) With the presence of traps, the J-V curves become more complex. First, a linear regime with injection-limited transport is exhibited in the J-V curves. Then, a sudden increase occurs in the intermediate range of applied biases. Finally, the V^2 dependence of the trap-free SCLC regime is reached. The extent of the intermediate region is governed by the spatial and energetic distribution of trap states, which is generally modeled by a Gaussian [27] or exponential distribution [28].
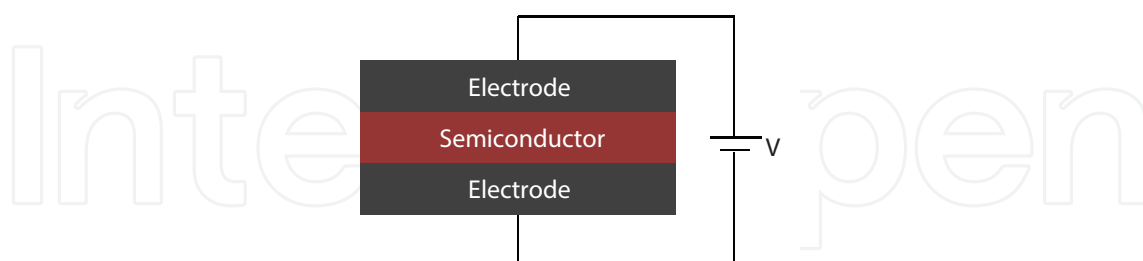

Figure 3. The structure of a SCLC-based device.

3. Organic field-effect transistors

3.1. Basic principles of field-effect transistors

In 1962, Weimer first introduced the concept of the thin-film transistor (TFT) [29]. This structure is well adapted to low conductivity materials and is currently used in amorphous silicon

transistors. As shown in **Figure 2**, ohmic contacts are formed directly between the source and drain electrodes with conducting channel. Compared with the metal-insulation-semiconductor field-effect transistor (MISFET) structure, there are two crucial differences in the TFT structure. First, the depletion region to isolate the device from the substrate is absent. Second, instead of the inversion regime, the TFT operates in the accumulation regime although it is an insulated gate device. As a result, it should be especially careful when transferring the drain current equations from the MISFET to the TFT. In fact, the absence of a depletion region leads to a simplification of the equation as the following [30]:

$$I_d = \frac{W}{L} C_i \mu \left(V_G - V_T - \frac{V_D}{2} \right) V_D \tag{7}$$

Here, the threshold voltage is the gate voltage, and the channel conductance (at low drain voltages) is equal to that of the whole semiconducting layer.

3.2. Important parameters in OFET

3.2.1. Mobility

The FET *J-V* characteristics in different operating regimes can be analytically expressed by the gradual channel approximation assumption which means that the electric field parallel to the current flow generated by the drain voltage is much smaller compared with the field perpendicular to the current flow created by the gate voltage [30, 31].

In the linear regime, the drain current is directly proportional to V_G, and the field-effect mobility in the linear regime (μ_{lin}) can be extracted from the gradient of I_D versus V_G at constant V_D.

$$I_D = \frac{W}{L} C_i \mu \left(V_G - V_T - \frac{V_D}{2} \right) V_D, V_D < V_G - V_T \tag{8}$$

In the saturation regime, the channel is pinched off when $V_D = V_G - V_T$. The current cannot increase anymore and saturates. The square root of the saturation current is directly proportional to the gate voltage.

$$I_{Dsat} = \frac{W}{2L} C_i \mu (V_G - V_T)^2, V_D > V_G - V_T \tag{9}$$

$$\sqrt{I_{Dsat}} = \sqrt{\frac{W}{2L} C_i \mu} (V_G - V_T) \tag{10}$$

Eq. (10) predicts that plotting the square root of the saturation current against gate voltage would result in a straight line. The mobility is obtained from the slope of the line, while the threshold voltage corresponds to the extrapolation of the line at zero current. However, in the saturation regime, the density of charge varies largely along the conducting channel, from a maximum near the source electrode to practically zero at the drain electrode. Hence, the mobility in organic semiconductors largely depends on various parameters, including the density of charge carriers. Meanwhile, in the saturation regime, the mobility is not constant

along the channel and the extracted value only represents a mean value. Therefore, it is often more rational to extract the mobility in the linear regime, in which the density of charge is more uniform. This is usually done through the transconductance g_m, which follows from the first derivative of Eq. (3) with respect to the gate voltage [30].

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} C_i \mu V_D \qquad (11)$$

This equation assumes that the mobility is gate voltage independent. However, the mobility is actually gate voltage dependent. In this case, an extra term $\partial \mu / \partial V_G$ should be involved in Eq. (5), so that this method is only applicable when the mobility varies slowly with the gate voltage [30]. Moreover, this method is very sensitive to the charge injection limitation and retrieval at source and drain electrodes.

3.2.2. Current on/off ratio

The current on/off ratio is another important FET parameter that can be extracted from the transfer characteristics. It is the ratio of the drain current in the on-state (at a particular gate voltage) and the drain current in the off-state (I_{on}/I_{off}). For best performing behavior of the transistor, this value should be as large as possible. When neglected the contact resistance effects at the source-drain electrodes, the on-current mainly depends on the mobility of the semiconductor and the capacitance of the gate dielectric. The off-current is mainly determined by gate leakage current. It can be increased for unpatterned gate electrodes and semiconductor layers due to the conduction pathways at the substrate interface and the bulk conductivity of the semiconductor. Moreover, the unintentional doping could also increase the off-current [31].

3.2.3. Threshold voltage

Threshold voltage originates from several effects and strongly depends on the organic semiconductor and dielectric used. Generally speaking, the threshold voltage could be caused by interface states, charge traps, built-in dipoles, impurities, and so on [31, 32]. And it can be reduced by increasing the gate capacitance, which induces more charges at lower applied voltages. In many cases, the threshold voltage is not always constant for a given device. The V_{th} tends to increase when organic transistors are operated under an extended time scale. This is called bias stress behavior, and it has a significant effect on the applicability of organic transistors in electric circuits and real applications. And thus is presently under intense investigation [33, 34]. A current hysteresis could be caused by the shift of the threshold voltage on the time scale of current-voltage measurements. Large stable threshold shifts, for example, induced by polarization of a ferroelectric gate dielectric, can be used in organic memory devices.

4. Organic semiconductor materials

The mobilities of organic semiconductors have achieved significant progress in OFETs from the initially reported 10^{-5} cm^2 V^{-1} s^{-1} for polythiophene in 1986 [35] to 10 cm^2 V^{-1} s^{-1} for

present diketopyrrolopyrrole (DPP)-based polymers [36]. The high mobility of organic semi-conductors over conventional amorphous silicon indicates large potential application of organic electronic devices. The remarkable progress of organic semiconductors provides a road for organic electronic industry. Generally, for high-performance organic semiconductors, some critical factors, such as molecular structure, molecular packing, electronic structure, energy alignment, and purity, play important roles. Among them, tuning the molecular packing is especially important for high-performance semiconductors since the charge carrier transport is along the molecular π orbitals. Hence, the overlap degree of neighboring molecular orbitals significantly determines the charge carrier mobility. Molecular packing with strong intermolecular interactions is favorable for efficient charge transport and high field-effect mobility. The electronic structure and energy levels are crucial for the materials and device stability. In order to obtain the high-performance and stable organic semiconductors, structural modification with electron donors and acceptors are necessary. Except the above talked aspects, the film morphologies such as grain boundaries also could affect the charge carrier transport. The grain boundaries and disordered domains could hamper the efficient intermolecular charge hopping between them. Hence, increasing the crystal grain size and film uniformity could efficiently improve the charge transport and mobility. In this section, we introduce some feature compounds with mobility of/over amorphous silicon and/or with high stability.

4.1. P-type semiconductors

In the last two decades, p-type semiconductor materials have achieved much progress because of their simple design and synthetic approach. P-type organic semiconductors mainly contain acene, heteroacene, thiophenes, as well as their correlated oligomers and polymers, and two-dimensional (2D) disk-like molecules. Several comprehensive reviews have given detailed information about these compounds [32, 36]. Among them, the polycyclic aromatic hydrocarbons are most representative of the class of compounds due to their unique features. Some representative p-type semiconductors are shown in **Chart 1**.

Pentacene (**1**), as the benchmark of organic semiconductors, was first reported in 1970s, but the numerous OFET applications were only conducted recently [37, 38]. With strong intermolecular interactions and herringbone packing motif, pentacene exhibits efficient charge transport. Hence, polycrystalline thin film of pentacene (**1**) and tetracene (**2**) showed surprisingly high mobility approaching 0.1 cm^2 V^{-1} s^{-1} [37] and 3.0 cm^2 V^{-1} s^{-1} [39], respectively. The substituted tetracene derivative rubrene (**3**) showed the highest charge carriers mobility with 20 cm^2 V^{-1} s^{-1} for single crystal device in the FET configuration [40]. This implies that the conjugated acene is a good building block for the p-type semiconductors. Later on, phthalocyanines (**4**) and more core-extended hexa-*peri*-benzocoronenes (HBC) (**5**) containing two-dimensional (2D) aromatic core were reported and showed typically discotic columnar liquid crystalline phases. As a result, the HBC showed enhanced mobility along the column due to the solid-state organization. Moreover, HBC-based OFETs by zone casting method exhibited a high mobility up to 0.01 cm^2 V^{-1} s^{-1} [41]. The chemistry based on acene has paved the way for designing efficient p-type semiconducting materials.
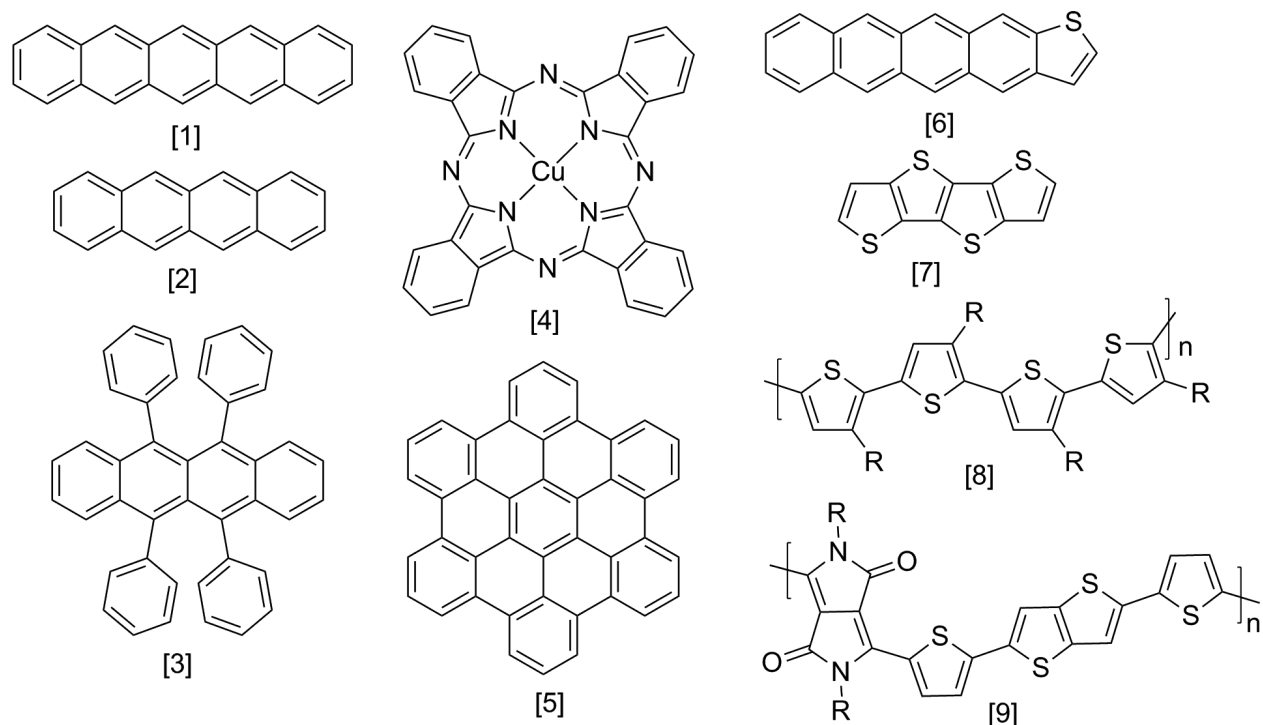
Chart 1. Chemical structures of some p-type semiconducting materials.

The sulfur containing heteroacenes and their derivatives constitute another large group of p-type aromatic hydrocarbons, as shown in **Chart 1**. The thienoacenes and their derivatives were also synthesized and investigated as semiconductors for p-type materials. The asymmetric oligoacene, such as the tetraceno-thiophene (**6**), was also synthesized and showed similar mobility (0.3 cm^2 V^{-1} s^{-1}) compared to their centrosymmetric counterparts processed in the same conditions [42]. The tetrathienoacene (**7**) with aryl groups had a higher mobility up to 0.14 cm^2 V^{-1} s^{-1} by vapor deposition [43]. The sulfur-sulfur interaction in the packing motif was believed to enhance the charge carrier transport. The introduction of sulfur and other heteroatoms induced different energy alignments and crystal packing, which promotes the development of p-type materials.

Among the p-type polymers, poly(3-hexylthiophene) (P3HT) (**8**) has been studied extensively and showed high mobility due to its good crystalline properties and well-ordered lamella structure which facilitates the efficient charge transport [44]. And it has been widely used as electron donor in organic solar cells. DPP-based polymers, such as PDDPT-TT (**9**), have been shown as high-performance semiconductor materials with hole mobility over 10 cm^2 V^{-1} s^{-1}. Moreover, the device exhibited excellent shelf life and operating stabilities under ambient conditions. Finally, exceptionally high-gain inverters and functional ring oscillator devices on flexible substrates have been demonstrated [45, 46].

4.2. N-type semiconductors

Although the p-type semiconductor materials have achieved much progress, the development of n-type organic semiconductors still lags behind that of p-type organic semiconductors due

to low device performance, ambient instability, and complex synthesis. Owing to their important roles in organic electronics, such as p-n junctions, bipolar transistors, and complementary circuits, it is desirable to develop stable n-type semiconductor materials with high charge carrier mobility for organic field-effect transistors.

To date, n-type organic semiconductors with high mobility are relatively rare and significantly lagging behind p-type semiconductors, and most of the n-type materials are still air unstable in ambient conditions due to its high lowest unoccupied molecular orbital (LUMO) energy level. De Leeuw et al. reasoned that the air unstable problem is due to redox reaction with oxygen and water [47]. Based on this result, we can calculate the LUMO energy level and it should be lower than -3.97 eV in order to be stable toward water and oxygen. N-type organic semiconductors mainly contain halogen or cyano-substituted n-type semiconductors that could be converted from p-type materials, perylene derivatives, naphthalene derivatives, fullerene-based materials, and so on (**Chart 2**).

The important n-type semiconductor material perfluoropentacene (**11**) was first reported by Sakamoto et al. [48]. This molecule adopted similar crystal packing to pentacene, and transistors fabricated from vacuum-deposited films showed a high mobility up to 0.11 $cm^2 V^{-1} s^{-1}$ and an on/off ratio of 10^5. It was thought that attaching fluorine atoms could lower the LUMO energy level of this compound. However, the LUMO energy level is not low enough to make the OFET device stable in the ambient condition. Similarly, the 2,5,8,11,14,17-hexafluoro-hexa-*peri*-hexabenzocoronene was synthesized by Kikuzawa et al. from hexakis(4-fluorophenyl)-benzene [49]. This fluorinated compound was also suitable for the fabrication of n-channel transistors due to the decreased LUMO energy level, showing a mobility of 1.6×10^{-2} $cm^2 V^{-1} s^{-1}$ and an on/off ratio of 10^4. Based on these results, they showed that the halogen substitution is a proper way to obtain n-type semiconductors.
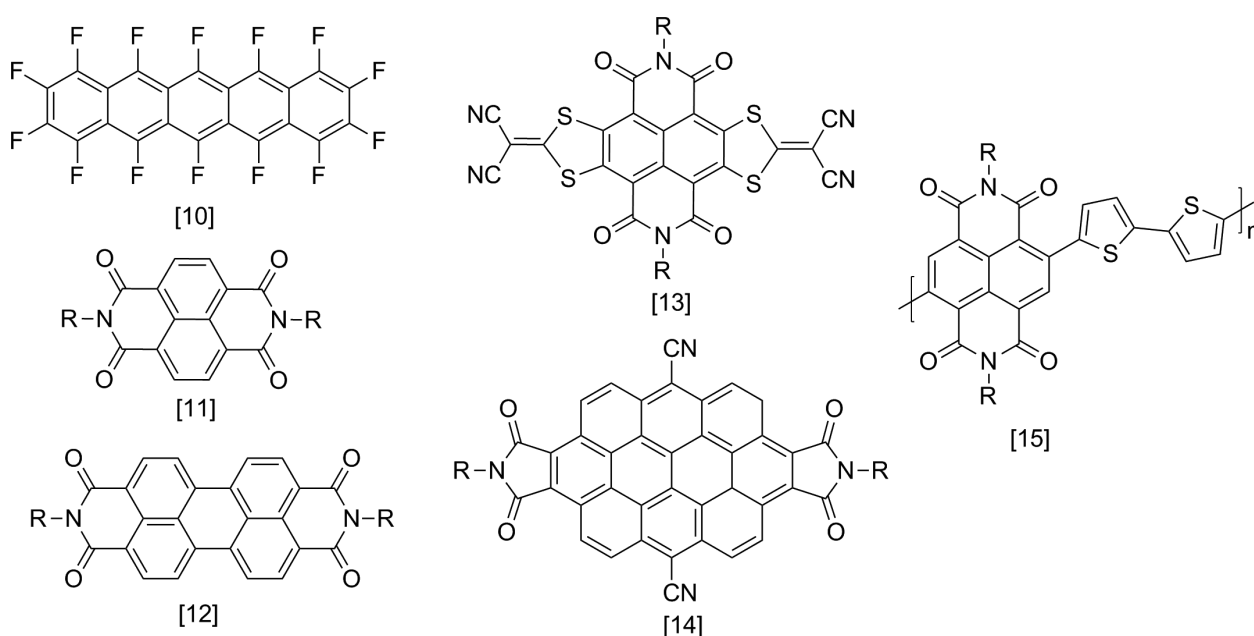

Chart 2. Chemical structures of some n-type semiconducting materials.

Naphthalene diimide (**12**) and perylene diimide (**13**) derivatives are two of the most studied n-type materials used in OFETs. Simple naphthalene and perylene diimides can be prepared from bisanhydrides and primary amines. Generally, the aromatic diimide in transistors shows an n-type character due to imide functionalization. Then, cyano or halogen was introduced to improve the air stability. Naphthalene diimide substituted with electron-withdrawing CN groups at the core position was reported by Jones et al. [50]. This molecule showed a mobility as high as 0.11 cm^2 V^{-1} s^{-1} as well as good ambient stability compared to unsubstituted compound. Cyano-substituted perylene diimide was also reported by the same group [51]. The good air stability was also observed, which indicates that cyano substituent is another efficient way to lower the LUMO energy level and achieve stable n-type materials. Later on, the core-expand NDI bearing two 2-(1,3-dithiol-2-ylidene)malonitrile moieties at the core (**14**) needs to be mentioned due to its good solution processability and good air stability [52].

Based on these results, it could be concluded that there is an efficient way to achieve stable n-type materials by combining imide functionalization and cyano or halogen substitutions. Electron-deficient aromatic diimides, such as ovalene diimide (ODI-CN), have attracted increasing attention as promising n-type semiconductors for OFETs (**15**) [53]. The materials of this class showed not only highly planar conjugated backbone but also easily tunable electronic properties through core and imide-nitrogen substituents with electron withdrawing groups and alkyl chains, respectively.

Similar to organic small molecules, the high-performance n-type polymers reported so far are much scarcer than that of p-type polymers. However, in order to achieve complementary circuits and plastic electronics, developing high-performance polymeric semiconductor with good air stability is essential. According to the previous works, the most promising results for n-type polymers is naphthalene-based polymer (P(NDI2OD-T2)), which exhibited an unprecedented high performance, with a mobility of >0.1 cm^2 V^{-1} s^{-1} (up to 0.85 cm^2 V^{-1} s^{-1}) and on/off ratio of 10^6 and excellent air stability in ambient conditions. Furthermore, the semiconductors could be processed by gravure, flexographic, and inkjet printing technique, and achieve all-printed polymeric complementary inverters (with gain 25–65) [54].

5. Fabrication techniques

The deposition of semiconductors is the determining step of the OFET fabrication. And it will decide the performance of the devices significantly. Here, we will introduce some important techniques commonly used in the OFET fabrication.

5.1. Vacuum evaporation

This technique allows for deposition and purification of small molecule organic semiconductors. The process is performed in an ultrahigh vacuum environment. The organic semiconductor material is placed in a metal boat and heated by Joule effects or electron gun, and the substrate is placed above the boat to allow growth and formation of the organic materials. In principle, high molecular weight organic semiconductors cannot be deposited by this way,

because they are too heavy to evaporate and tend to decompose at high temperatures. The main advantages of the vacuum evaporation are the facile control of the purity and thickness of the deposited film. Meanwhile, that highly ordered crystalline thin films can be realized by controlling the deposition rate and the temperature of the substrate. Its major deficiency is that it requires complicated instruments. This is different with the solution processing technique which is simple and low-cost.

5.2. Liquid deposition

Liquid deposition process is an important part of most OFET fabrication process, either to deposit the active layers or to manipulate layers deposited through other means. Many organic semiconductor materials have been engineered to be soluble or dispersible in solution, which gives a possibility toward the device fabrication. Many strategies have been applied to the deposition of organic semiconductors for utilization in OFETs. The common deposition methods include spin-coating, drop-casting, dip-coating, spray-coating, and roll-coating techniques (**Figure 4**) [55].

Printing comprises a family of techniques and can simultaneously deposit and pattern a target material. This technique mainly contains ejected drop printing, contact stamp printing, indirect and offset printing methods, and capillary stylus dispensing. The comparison of these techniques in terms of advantages and disadvantages has been reported by some comprehensive reviews [55, 56]. Among them, piezo inkjet printing has dominated OFET fabrication printing techniques due to its excellent compatibility and the availability of sophisticated print heads to the development community. In this technique, some parameters like ink viscosity, ink surface tension, and substrate surface energy are crucial for ejection and deposition of the droplets. It is necessary to control the droplet spreading and drying to avoid "coffee ring" effect and form
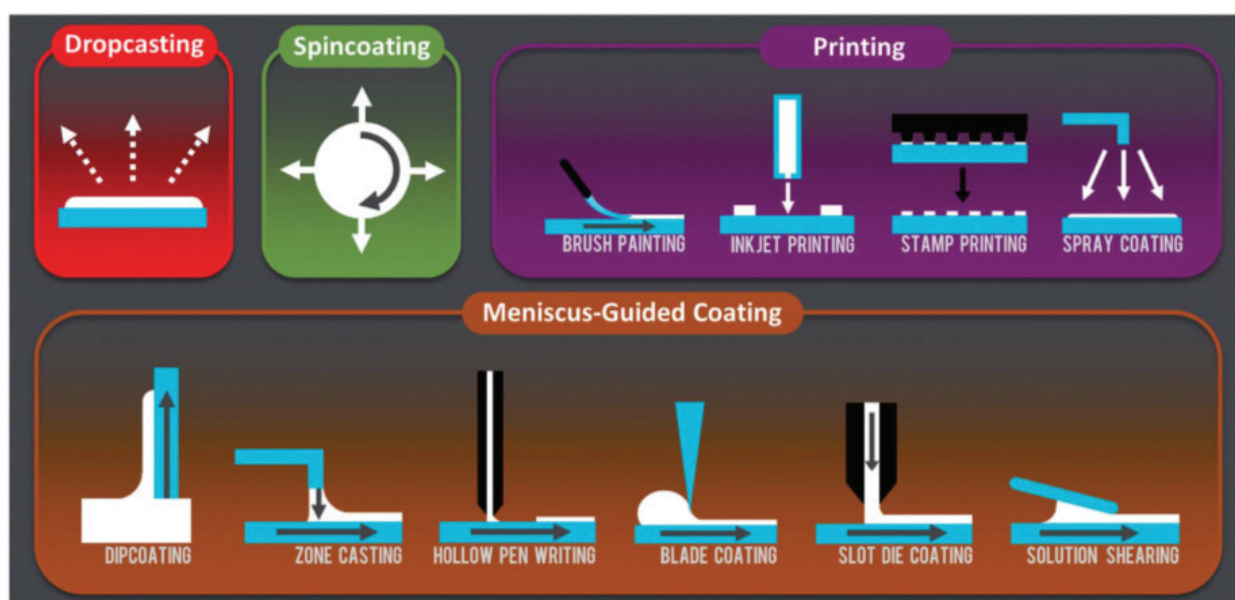

Figure 4. A schematic summary of the solution-based deposition techniques discussed. Reproduced with permission from Ref. [55]. Copyright 2014, The Royal Society of Chemistry.

precisely patterned arrays. Some method such as combining the antisolvent crystallization and inkjet printing has been used to produce highly crystalline organic semiconducting thin films. By this approach, thin-film transistors with average carrier mobilities as high as 16.4 cm^2 V^{-1} s^{-1} have been achieved based on single crystalline thin films of 2,7-dioctyl[1]benzothieno[3, 2-b][1] benzothiophene (C8-BTBT) [57].

5.3. Thin-film alignment

Depositing of crystalline organic semiconductors with controlled in-plane orientation is one important issue for high-performance OFETs. It is generally accepted that charge transport in organic materials occurs via the hopping mechanism, which depends on the degree of orbital overlap between the molecules. Since charge carriers are preferentially transported along the π-π stacking direction in organic semiconductors, macroscopically aligned organic films have potentially higher mobilities and provide more unusual properties, such as optically and electrically anisotropic characteristics. Therefore, many deposition techniques have been investigated for patterning and alignment of organic semiconductors [56]. The techniques mainly contain (1) mechanical forces alignment, such as friction-transfer, nanoimprinting, and the Langmuir-Blodgett (LB) technique; (2) depositing the organic semiconductors directly on the alignment layers prepared by different methods, such as rubbing and photoirradiation; (3) growing the organic semiconductors on inorganic single crystals; (4) using magnetic or electric field-induced alignment; (5) using solution-processed technique to align organic semiconductors on isotropic substrates.

Among the solution processing techniques, the traditional techniques such as spin-coating and drop-casting cannot control the thin-film orientation. Therefore, some methods have been used to overcome this issue. For example, zone-casting offers a route to control the orientation of the deposited layers. In this process, a continuously supplied hot solution is deposited by means of a nozzle onto a moving, thermally controlled support. Under appropriate rates of solution supply and solvent evaporation, a stationary gradient of concentration is formed within the meniscus, which gives rise to directional crystallization [58]. Dip-coating is another technique to give a better thin-film alignment in solution-processed devices [59, 60]. This process can be controlled by the substrate lift rate, solvent evaporation, and capillary flow. Solvent choice is especially important because of its effect on the rate of solvent evaporation. The drying speed which influences the thin-film morphologies can be quantitatively controlled during the dip-coating process by adjusting the substrate lifting rate.

Solution-sheared deposition is a recently developed approach that can deposit highly crystalline and aligned thin films on isotropic substrates [61]. This method is related to doctor blading, which employs a blade to distribute a viscous solution over a substrate. A small volume of a diluted organic solution is sandwiched between two preheated silicon substrates, which move relatively to each other at a controlled speed. The top wafer acts as the shearing tool and is treated to be hydrophobic and the bottom wafer acts as the device substrate. The motion of the wafers exposes a liquid front that quickly evaporates to form a seeding film comprising multiple crystal grains. These crystals act as nucleation sites and allow the remaining molecules in solution to grow along the direction of the shearing direction (**Figure 5**) [61].
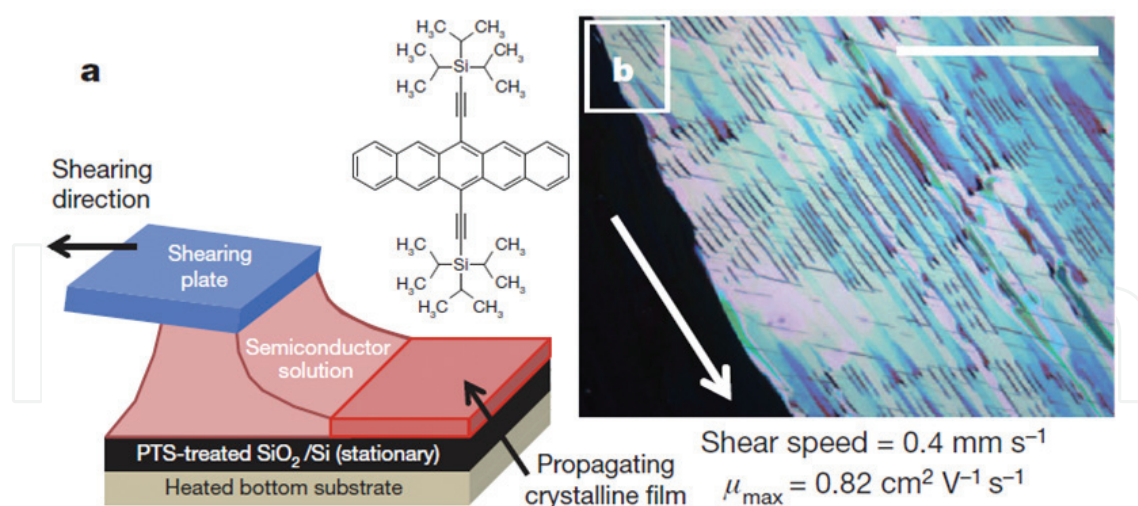
Figure 5. Schematic diagram of the solution-shearing method (a) and (b) cross-polarized optical microscope images of solution-sheared TIPS-pentacene thin films, formed with shearing speeds of 0.4 mm/s. Adapted with permission from Ref. [62]. Copyright 2011, Nature Publishing Group.

It has been reported that by using this method, metastable molecular packing motifs (or lattice-strained crystal structure) could be formed, which can alter the intermolecular π-π stacking distance and enhance the charge transport properties [62].

Slot-die coating is also a promising technique to control the thin-film alignment and self-assembly process for OFET applications. It has been proved to be a simplistic and manufacturable approach to fabricate large area high-performance field-effect transistors. This technique saves raw materials and controls film uniformity reliably, accurately, and reproducibly. The slot die coating is scalable to large areas and, therefore, applicable for the fabrication of large area low-cost electronics. We first applied this technique in the OFET fabrication [63]. **Figure 6** schematically illustrates this process. A temperature-controlled vacuum suction plate was used to fix and preheat the substrates to a certain temperature. A small volume of organic solution is deposited onto the modified substrate surface by a slot die with different coating gaps ranging
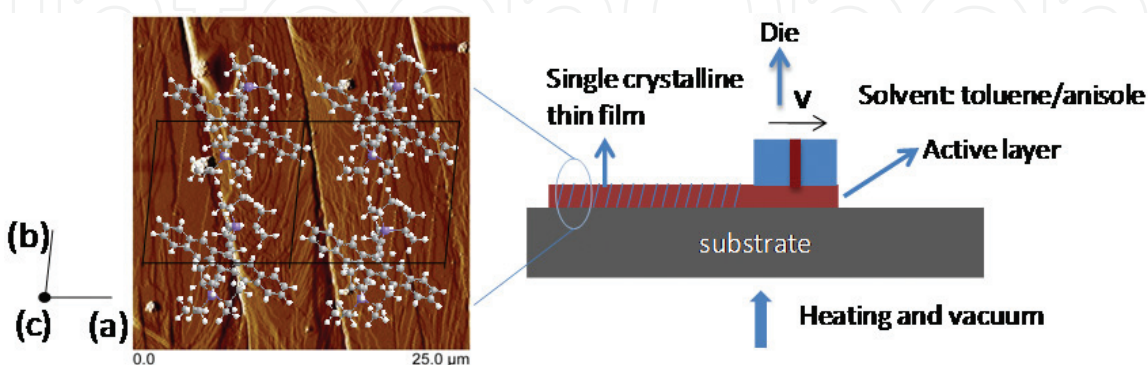

Figure 6. Schematic of slot-die coating and the AFM image of the film with molecular structure superimposed. (a), (b) and (c) indicate the crystal axises of the crystal structure. Adapted with permission [63]. *Copyright 2013, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.*

from 15 to 90 μm. The depositing speed is controlled within the range of 0.1–19.9 mm/s. The pre-exposed seeding film can act as nucleation sites and allow the remaining molecules in the solution to grow along the coating direction [63].

6. Conclusions and future outlook

In general, impressive progress has been accomplished in the design, synthesis, and processing of organic semiconductors in the past few years. In the future, organic semiconductors will become more attractive due to comparable performance to traditional amorphous inorganic semiconductor materials, and their near-infinite tunability. Meanwhile, for large-scale fabrication of low-cost devices, solution-based film deposition processes at low temperatures with high charge carrier mobility are highly desirable.

Currently, more attention is focused on the solution-processable, air-stable high-performance organic n-type semiconductor; the relationship between the molecular structure of the organic semiconductor and device performance; and large area semiconductor thin-film alignment. Meanwhile, some important issues still need further investigation such as operational stability, low-cost and large area fabrication process, device integration, as well as functionalization in sensor fields. The study of the defect electronic structure of organic semiconductors will also be the important subject in the coming years.

In summary, although organic materials and devices still have some deficiencies, they can be improved and used in a wide range of low-cost functional devices to meet the needs of different markets, and they are sure to become a unique feature of our life in the future.

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