Chapter 5

High-Efficiency Front Junction *n*-Type Crystalline Silicon Solar Cells

Yuguo Tao and Ajeet Rohatgi

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/65023

Abstract

This chapter aims to provide students/workers in the field of photovoltaics with the valuable information and knowledge needed to understand the physics and operation of high-efficiency front junction *n*-type crystalline silicon solar cells. The surface recombination and passivation mechanisms, and several promising passivation schemes for front and back cell surfaces, are addressed and reviewed. The advanced cell structures and their fabrication schemes to achieve higher efficiency are described and discussed, including selective emitter on the front and locally doped back surface filed or carrier selective rear contact composed of tunnel oxide and phosphorus-doped polycrystalline silicon thin film. These advanced cell design features have become highly active areas of investigations in the photovoltaic industry for next-generation production cells.

Keywords: front junction, recombination, surface passivation, selective emitter, tunnel oxide passivated contact, high efficiency

1. Introduction

Solar cells depend upon the photovoltaic effect for their operation that converts the incident energy of sunlight directly into electricity using the electronic properties of semiconducting materials. In the past few decades, silicon wafers have been used to fabricate the overwhelming majority of solar cells in the very dynamic photovoltaic industry because of the abundance and non-toxicity of silicon, the simplicity of cell fabrication process, and the vast amount of processing knowledge developed and accumulated in the microelectronics industry. Simply speaking, silicon wafer-based solar cells generate electricity via absorbing photons and

generating electron-hole pairs that are separated by a *pn*-junction and then flow to electrical contacts on the front and back sides to perform work in external circuit, as shown in the **Figure 1**. In addition, due to several advantages of *n*-type (typically phosphorus-doped) silicon wafers over *p*-type (typically boron-doped), including better tolerance to common impurities (e.g. iron) [1], higher bulk lifetime and no light-induced degradation (LID) [2], *n*-type silicon solar cells with high efficiency can be potentially more cost-effective than *p*-type silicon solar cells. Hence, the focus in this chapter will be on high-efficiency front junction *n*-type crystalline silicon solar cell with both sides passivated and contacted, including their operating principle, advanced cell structures, surface passivation and fabrication schemes.

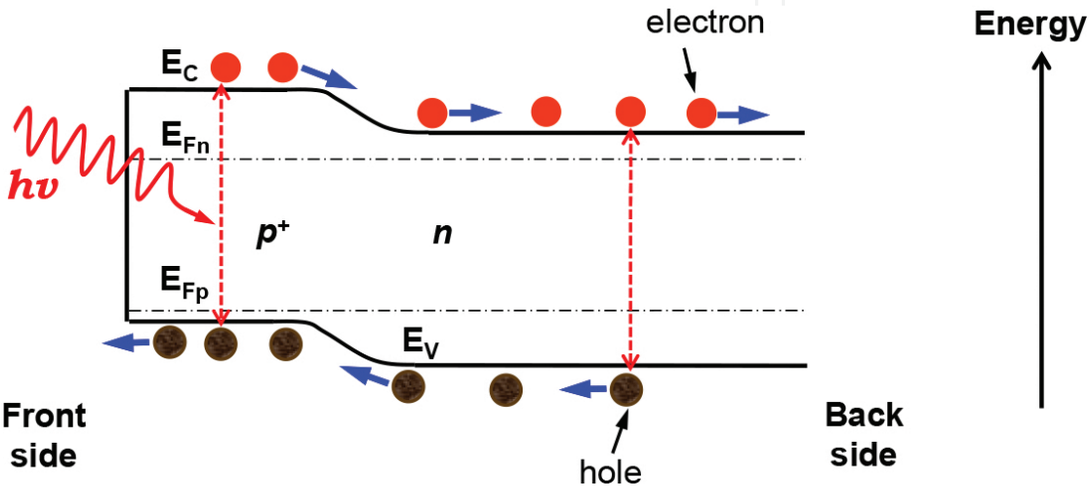

Figure 1. Schematic energy band diagram of a front junction *n*-type silicon solar cell in a non-equilibrium (with illumination), including photon absorption, carrier generation and separation.

2. Operating principle of a front junction *n*-type silicon solar cell

The operating principle of a front junction *n*-type silicon solar cell is described in **Figure 1** via the band diagram. The p^+ emitter region is formed by 'doping' the front side of a *n*-type silicon wafer with boron dopants in high concentration, and the conjunction of the p^+ region and the *n* substrate forms the *pn*-junction. Due to the doping concentration gradient across the *pn*-junction, electrons flow by diffusion from the *n* region into the p^+ region, and holes flow from the p^+ region to the *n* region [3]. This leaves behind exposed charges on ionized boron and phosphorus doping atoms at lattice sites, which form the space charge region. These exposed charges build up an electric field that opposes the natural flow of electrons and holes until and equilibrium scenario is reached with a fixed space charge width and electric field [4]. This built-in electric field also causes a bending of the conduction band (E_C) and the valence band (E_V) (**Figure 1**). When the solar cell is illuminated, photons with energy greater than the silicon band gap energy (E_g) are absorbed to excite electrons from the valence band to the conduction band, which generates an electron-hole pair. The generated electrons and holes can diffuse within the bulk of the solar cell until they reach the space charge region, if they avoid recombination or trapping by defects. Then, the electric field at the *pn*-junction separate

these carriers by sweeping electrons to the n region and holes to the p^+ region. In the case of illumination, quasi-Fermi levels (E_{Fn} for electrons and E_{Fp} for holes) are used to analyse the solar cell in non-equilibrium (**Figure 1**). The electrical contact to the front p^+ emitter region is described as an ohmic contact while the metal contact to n region, without any heavy doping, is generally a Schottky-type because the metal contact to n silicon induces a barrier to majority carrier (electrons) [3]. In order to obtain high cell efficiency, proper doping profiles in both the p^+ and the n regions are necessary to reduce the contact resistance and the metal-induced recombination.

2.1. Solar cell parameters

According to the *ideal diode law* (one diode model), an actual silicon solar cell with parasitic series resistance (R_s) and shunt resistance (R_{sh}) can be described by an equivalent circuit containing one diode as shown in **Figure 2** and is often expressed as [3, 4]

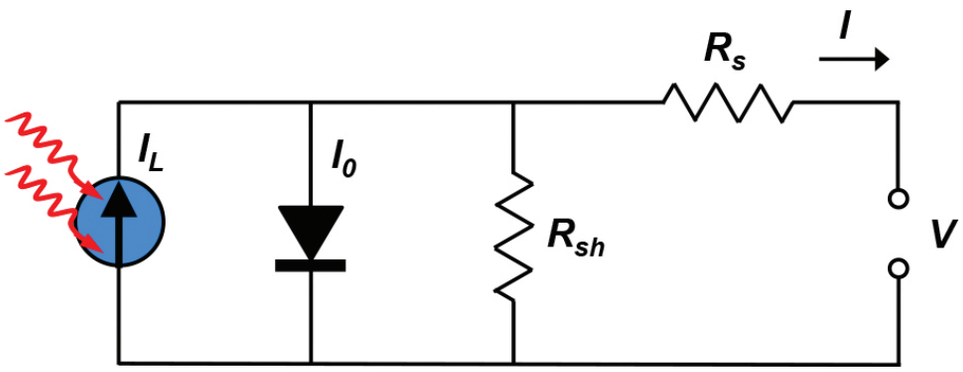

Figure 2. Equivalent circuit of a front junction n-type silicon solar cell with parasitic series resistance (R_s) and shunt resistance (R_{sh}) [3, 4].

$$I = I_L - I_0\left\{\exp\left[\frac{V + IR_s}{\left(\frac{nkT}{q}\right)}\right] - 1\right\} - \frac{V + IR_s}{R_{sh}} \quad (1)$$

where I is the terminal current, I_L is the light-generated current with illumination, I_0 is the saturation current (the solar cell leakage current in the dark), V is the terminal voltage, q is the electronic charge, k is the Boltzmann's constant, T is the absolute temperature and n is the ideality factor that is typically in the range of 1 and 2.

The resulting *I-V* curve with illumination is often plotted as output power, as shown in **Figure 3**. The maximum power point (MPP) is also indicated at (V_{mp}, I_{mp}). The fill factor (*FF*) is another important parameter determining cell performance, and it is a metric of the *pn*-

junction quality and the parasitic resistance of a finished silicon solar cell [3]. *FF* is a measure of the squareness of the *I-V* curve and defined as

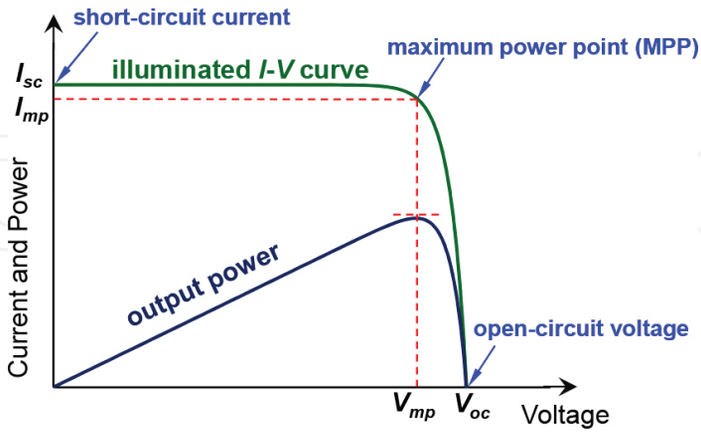

Figure 3. A typical representation of an illuminated *I-V* curve as well as output power curve as a function of voltage, including indication of short circuit current (I_{sc}), open circuit voltage (V_{oc}) and the maximum power point (V_{oc} and I_{sc}) [3, 4].

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \tag{2}$$

where I_{mp} and V_{mp} are the corresponding current and voltage at the maximum power point, I_{sc} is the current at short circuit condition ($V = 0$) and V_{oc} is the voltage at open circuit condition ($I = 0$) [3, 4]. Finally, the most important metric of solar cell performance is the energy conversion efficiency and is defined as

$$\eta = \frac{I_{sc}V_{oc}FF}{P_{in}} \tag{3}$$

where P_{in} is the total incident light power striking the solar cell [3]. According to the detailed balance limit of efficiency, the maximum efficiency of an ideal single-junction crystalline silicon solar cell with E_g of 1.12 eV at 25°C is about 30% [5]. Its major fundamental mechanisms of power loss include (1) photons with energy less than 1.12 eV ($<E_g$) cannot be absorbed and directly transmitted through the cell, (2) the excessive energy in photons with high energy ($>E_g$) is wasted via thermallization as the generated electron-hole pair relax back to the edges of carrier band, (3) each absorbed photon creates only one electron-hole pair regardless of its energy, and (4) as shown in **Figure 1**, quasi-Fermi levels (E_{Fn} and E_{Fp}) stay within energy gap ($\left|E_{Fn} - E_{Fp}\right| < E_g$), hence *pn*-junction silicon solar cells are inherently capable of giving voltage output smaller than the potential corresponding to its band gap energy [3, 5].

http://dx.doi.org/10.5772/65023

2.2. *pn*-junction formation

To form the *pn*-junction on *n*-type crystalline silicon wafers, a typical approach is to diffuse boron atoms into the silicon substrates at high temperature. This can be accomplished by several techniques including depositing boron-doped silicon oxide via atmospheric pressure chemical vapour deposition (APCVD) and then thermal annealing at high temperature [6]. The boron emitter can be also formed by spinning-on orthoboric acid (H_3BO_3) solutions [7, 8], which is considered to be a hydrate of boric trioxide (B_2O_3). During the subsequent thermal annealing, the boron oxide reacts with silicon to form SiO_2 and B, which diffuses into silicon at high temperature, as described by

$$2B_2O_3 + 3Si \rightarrow 3SiO_2 + 4B \tag{4}$$

Screen-printed boron emitters have also been explored by printing proper boron-containing paste followed by a thermal drive-in diffusion [9]. Another promising and widely used technology is called 'BBr_3 diffusion' that involves a direct thermal diffusion of boron atom from a liquid boron tribromide (BBr_3) source [10]. In this process, pure nitrogen (N_2) carrier gas flows into a bubbler containing liquid BBr_3, which creates and transports gaseous BBr_3 into the quartz tube and deposits on the surface of silicon wafers loaded in a quartz boat [11]. During this deposition stage, a boron oxide layer is formed on the silicon wafer surface in the oxygen (O_2) ambient according to

$$4BBr_3 + 3O_2 \rightarrow 2B_2O_3 + 6Br_2 \tag{5}$$

This thin boron oxide layer contains very high concentration of inactive boron element on the silicon surface. So, a high temperature anneal (typically ≥950°C) is necessary to activate boron atoms and diffuse them into silicon bulk to form the p^+ region through the reaction (4) [11]. During this process, a SiO_2/B_2O_3 stack or the borosilicate glass (BSG) layer is formed on the surface that has to be removed to achieve better dielectric surface passivation quality. By controlling gas flow rate, diffusion temperature and duration, proper boron dopant profiles can be engineered [12].

Because all of these junction formation technologies suffer from wrap-around or naturally double-sided diffusion process, etching off one side or depositing a mask layer on one side is needed to prevent junction shunting. Therefore, ion implantation has been investigated and implemented as a promising alternative technology that has a unique characteristic to provide single-sided diffusion and facilitates the development of next-generation cells [13]. It can simplify the junction formation process by eliminating the extra processes of masking and etching. In addition, ion implantation offers other technical advantages, including (1) high junction uniformity, (2) flexibly and precisely controlled dopant profiles, (3) elimination of the edge isolation process, (4) capability of patterned doping for selective doping and (5) elimination of the dopant glass (i.e. BSG layer) removal process [14]. It is important to note that ion implantation forms an amorphous layer on the surface [15], therefore, a very high temperature

(≥1000°C) is needed to recover lattice damage and activate dopants [16, 17]. In addition, proper ion dose, implant energy and anneal conditions are essential to obtain desired dopant profiles [18, 19]. Current ion implantation tools have throughput of more than 2000 wafers per h but the capex and maintenance is much higher than the traditional diffusion tubes [13]. **Figure 4** shows two examples of boron emitter profiles measured by electrochemical capacitance-voltage (ECV) profiling technique, revealing that the boron concentration decreases towards the silicon wafer surface due to the higher solubility of boron in the SiO_2 layer than in silicon bulk [20].

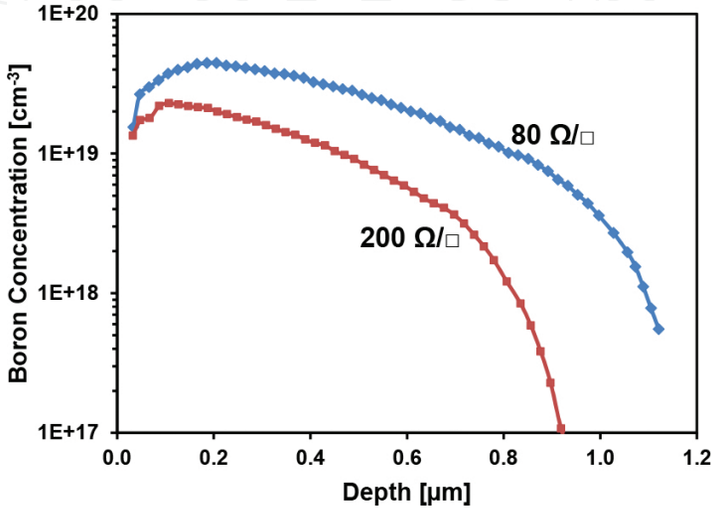

Figure 4. Two measured ECV profiles of ion-implanted boron emitters with sheet resistance of 80 and 200 Ω/□ [16, 20].

2.3. Metallization

In order to extract electrical power from a silicon solar cell, metal contacts have to be applied to the front emitter and the rear base to collect the generated electron-hole pairs. The collected electrons flow through the n^+ regions into the external circuit to power the load and then recombine with the generated holes. In order to minimize the power loss, the electrical contact needs to have low contact resistance with doped silicon regions, low metallic resistance in the formed structure, good adhesion to silicon and reliable solderability for cell interconnection for module production [21]. There are several metallization technologies that are typically used in photovoltaic industry for research and production. First, the screen printing of metal pastes to form electrical contact is the most widely applied technology to manufacture silicon solar cells in photovoltaic industry today because it is very robust, simple, high-throughput, low-cost and reliable method [21]. Its first application dates back to 1970s. In this metallization process, a metal paste is printed through a patterned screen with well-designed openings onto a wafer lying under the screen. This screen acts as a mask, consisting of a mesh of wires partially covered with an emulsion. By properly optimizing some key process parameters, including the snap-off distance between screen and wafer, the printing pressure (pressing the screen against the wafer surface and pushing the metal paste onto wafer surface) and the printing

http://dx.doi.org/10.5772/65023

speed, printed gridline with high aspect ratio can be obtained today with line width of ≤60 μm and height of ~25 μm (**Figure 5(A)**) [16]. Then, the contact formation is realized by a firing process in a conveyor belt furnace that fires the metal pastes through the passivation layer and anti-reflection coating (typically silicon nitride SiNx) on the front. During this firing process, hydrogen (H) is released from the hydrogen-rich SiNx layer into the crystalline silicon to passivate bulk and interface defects to increase the cell performance [23, 24].

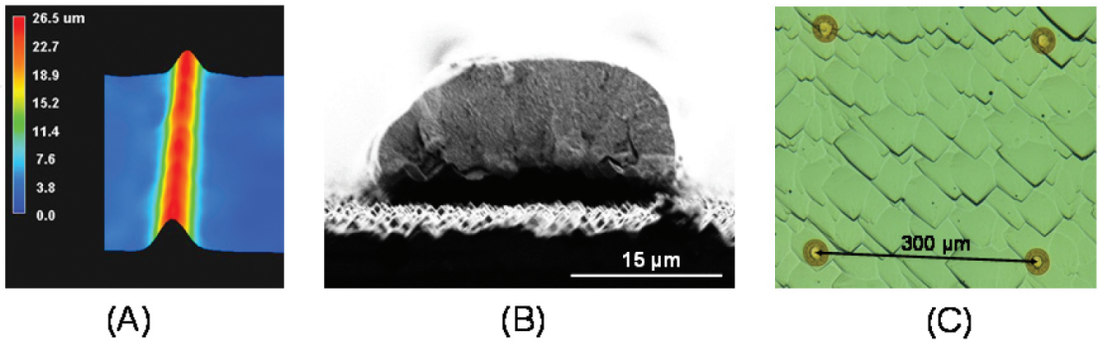

Figure 5. (A) Optical scope image of screen-printed gridline. (B) Scanning electron microscope image of photolithographically defined and plated gridline. (C) Optical scope image of laser-opened point contact pattern for physical vapour deposited metallization [16, 22].

Second contact technology involves metal plating approach that offers low contact resistivity, good gridline conductivity and narrow gridline width (low metal shading). Thus, it is a promising alternative to the screen-printing technology but metal plating typically requires an initial patterning step to create openings in a dielectric masking layer for the subsequent self-aligned metallization [21]. The openings can be defined by photolithography [10] or laser ablation, and then the contacts are applied by electroless plating [25] or a combination of light-induced plating (LIP) and electroplating in an inline plating machine [26]. For industrially feasible plated metallization, nickel (Ni) layer is typically used, first to obtain low contact resistivity and prevent copper (Cu) diffusion followed by copper plating to provide excellent line conductivity and low material cost (compared to silver) [27]. The gridline width after plating is typically around 30 μm, with height of ~15 μm, as shown in **Figure 5(B)**.

Third contact technology involves physical vapour deposition (PVD) that is attractive because of its potential advantages of lower specific contact resistance [28], reduced wafer breakage and processing of thinner wafers due to non-contacting process. In addition, a thin (1~2 μm) PVD aluminium (Al) on the entire rear area is sufficient to meet the required electrical conductance for large area silicon solar cells, which can lead to less wafer bow and less metal material consumption [22]. In order to form the contact between silicon and PVD metal, patterned openings through a dielectric masking layer are needed for the subsequent PVD metallization, which is typically created by laser ablation. **Figure 5(C)** shows an example of rear point contact pattern (300 × 300 μm^2) after laser ablation, with the opening diameter of ≤40 μm and metal coverage of ≤1.4% [22]. To obtain a good solder contact to the PVD Al side, deposition of a double layer of Ni:V/Ag on top of PVD Al layer is often implemented to provide an excellent solderability and long-term stability for module manufacturing [29].

2.4. Optical, resistive and recombination losses in a solar cell

Theoretical maximum J_{sc} of ~44 mA/cm^2 can be achieved for a single-junction crystalline silicon solar cell, if all the striking photons with energy higher than silicon band gap ($E_{photon} \geq E_g$) are absorbed and all the electron-hole pairs generated contribute to the cell current [3]. However, several optical losses can cause lower current density in real cells, including reflection at the front side (metal gridline and front surface), absorption in the metal and dielectric layers on both sides, absorption via free-carrier absorption in highly doped regions and transmission (without being absorbed in the cell). It is important that the front metal shading should be as low as possible without contributing to significant increase in series resistance. Therefore, grid pattern needs to be optimized to minimize the resistive and optical losses. Finally, the size of pyramid on the front side should be as small as possible after the saw damage removal and texturing process to minimize the line width due to spreading of screen-printed metal.

Actual silicon solar cells also suffer from ohmic losses due to parasitic resistance R_s and R_{sh}. R_s is mainly attributed to the sheet resistance of doped regions (p^+ emitter and n^+ back surface field) in the case of two dimensional current flow, bulk resistance of silicon substrate, metallic resistance of gridline and specific contact resistance between silicon and metal. Each of these resistive components can be approximately estimated by using a model and calculation approach [30] to minimize total R_s and achieve high *FF*. R_{sh} is a factor monitoring the non-ideality of the *pn*-junction and some defects near junction, especially edge shunting. Both high R_s and low R_{sh} can result in low *FF* and cause power loss.

Apart from optical and ohmic losses, recombination of generated carriers can reduce J_{sc} and V_{oc} and limit the cell performance. There are two different intrinsic recombinations in semiconductor materials, namely Auger recombination and radiative recombination. Auger recombination is dominant in the heavily doped p^+ and n^+ regions. Auger recombination represents the process in which electron and hole recombine first by band-to-band radiative recombination and use the excess energy to excite another majority carrier (electron) in the conduction band for n^+ silicon or hole in the valence band in the case of p^+ silicon. Then, this excited carrier thermalizes towards the band edge by emitting phonons. Auger recombination strongly depends on majority carrier density; hence it is very effective in the heavily doped regions (p^+ emitter and n^+ back surface field). Radiative recombination refers to a process in which electron makes direct band-to-band transition to recombine with a hole in the valence band while emitting light. Because silicon is an indirect band gap material and a phonon is required for the band-to-band transition, this recombination mechanism is often neglected in silicon solar cell. A third and important bulk recombination mechanism is called SRH recombination (named after Shockley, Read and Hall [31, 32]), which is initiated by the energy levels created within the forbidden gap by impurities or defects. These energy levels form a stepping stair to facilitate the recombination of holes and electrons, which is a function of energy level location, trap density and its capture cross-sections [31, 32]. Generally, mid-gap or deeper traps are more efficient recombination centres. Because all three recombination mechanisms occur in parallel, the silicon substrate bulk lifetime (τ_{bulk}) is expressed as

$$\frac{1}{\tau_{\text{bulk}}} = \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{radiative}}} + \frac{1}{\tau_{\text{SRH}}} \tag{6}$$

where τ_{Auger} is the Auger lifetime, $\tau_{\text{radiative}}$ is the radiative lifetime and τ_{SRH} is the SRH lifetime.

In addition to these three bulk recombination mechanisms, surface recombination is also very critical for cell performance. This is because dangling bonds present at both surfaces of the wafer induce defect levels within the forbidden band gap. Surface recombination is characterized by a surface recombination velocity that is a function of surface state density and cross-section of surface traps [31]. To account for all the four recombination mechanisms, an effective lifetime (τ_{eff}) is used, and given by

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2s}{d} \tag{7}$$

where s is the surface recombination velocity (SRV) and d is the silicon wafer thickness. All recombination processes not only reduce the maximum short circuit current density (J_{sc}) but also diminish the maximum V_{oc}. According to Eq. (8), the total saturation current density ($J_{0,\text{total}}$) in Eq. (1) strongly influences V_{oc} because

$$V_{\text{oc}} = \frac{nkT}{q} \ln\left(\frac{J_{\text{sc}}}{J_{0,\text{total}}} + 1\right) \tag{8}$$

$$J_{0,\text{total}} = J_{0e} + J_{0b,\text{bulk}} + J_{0b}' \tag{9}$$

where J_{0e}, $J_{0b,\text{bulk}}$ and J_{0b}' are the saturation current density contributions from front emitter, bulk wafer and back side, respectively. These parameter values can be directly measured and extracted from the quasi-steady-state photoconductance (QSSPC) technique [33]. Due to the progress and availability of high lifetime wafers and current photovoltaic industry trend towards thinner wafers for cost reduction, passivation of front and rear surfaces is becoming vitally important for achieving higher efficiency silicon solar cells.

3. Surface passivation of crystalline silicon solar cells

At the silicon wafer surface, the covalent silicon-silicon bonds of crystal lattice are broken during wafer slicing, which creates non-saturated ('dangling') bonds that are often referred as 'surface states' and can easily trap electrons from the conduction band or holes from the valence

band as some of the energy levels are located near mid-gap. In order to keep surface recombination losses at a tolerable level, the wafer surfaces must be electronically well passivated. According to the Shockley-Read-Hall theory [31], the SRV depends on several features, including the properties of the surface states, state density, their capture cross-sections for electrons and holes, the injection level at the surface and the wafer doping level [34]. Therefore, SRV can be decreased by two technical approaches: (1) the chemical passivation by reducing the surface state density via depositing or growing a passivating dielectric film on the silicon surface and (2) the field-effect passivation by reducing the concentration of one charge carrier type (either electrons or holes) at the surface via forming an internal electric field below the silicon surface with doping profile or electrical charges in dielectric insulator. Practically, these two fundamental passivation approaches are often applied together to minimize the SRV. For front junction *n*-type crystalline silicon solar cells, the electronic quality of front boron emitter and back surface are usually expressed and quantified by J_{0e} and J_{0b}'. In a typical solar cell, there are two fundamentally different types of surface regions: metallized and non-metallized. Non-metallized surface regions are usually covered with dielectrics and are referred to as passivated regions. In order to achieve high cell efficiency, both J_{0e} and J_{0b}' should be as low as possible.

3.1. Front boron emitter passivation

In order to take the advantages of high bulk lifetime *n*-type crystalline silicon wafers, excellent passivation of the boron emitter is essential to reduce the SRV or the emitter saturation current density of the passivated region ($J_{0e,\,pass}$). It is well known that aluminium oxide (Al_2O_3) contains a high density of built-in negative charges on the order of ~10^{13} cm^{-2} [35], so the majority carrier (hole) is accumulated and minority carrier (electron) concentration is effectively reduced at the Al_2O_3-passivated boron emitter surface, and consequently, the SRH recombination on the surface or the SRV is reduced. Experimentally, very low $J_{0e,\,pass}$ in the range of 10~30 fA/cm^2 has been demonstrated on 150 and 54 Ω/□ is the standard unit to describe a sheet resistivity for emitter or back surface field for silicon solar cells in the photovoltaic field. sheet resistance p^+ emitters with surface doping concentrations around 10^{19} cm^{-3} (prepared by BBr_3) and Al_2O_3 passivation synthesized by plasma-assisted atomic layer deposition (ALD) (**Figure 6**) [36].

It is also shown that with ALD-Al_2O_3 passivation, ion-implanted boron emitters (post-implant anneal at 1040°C for 1 h) demonstrate noticeably higher $J_{0e,\,pass}$ at <150 Ω/□ sheet resistance, but similar passivation performance for ≥150 Ω/□ sheet resistance, compared to the BBr_3-prepared emitters (oxidation anneal at 1050°C). This is due to higher surface doping concentration (~5 × 10^{19} cm^{-3}) resulted from lower oxidation temperature and shorter oxidation time. In addition, thermally grown silicon oxide (SiO_2) also demonstrates decent surface passivation for the boron emitters with $J_{0e,\,pass}$ in the range of 60~110 fA/cm^2. However, silicon nitride (SiNx) deposited by plasma-enhanced chemical vapour deposition (PECVD) does not effectively passivate boron-doped emitters (**Figure 6**) due to the presence of positive built-in charge. Furthermore, hydrogen-rich amorphous silicon yields the passivation performance comparable to SiO_2 [37].

http://dx.doi.org/10.5772/65023

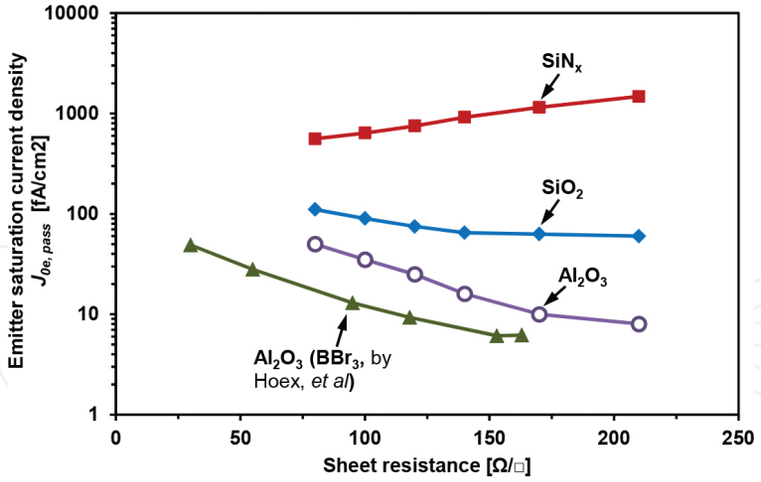

Figure 6. Measured emitter saturation current density on passivated region $J_{0e,pass}$ as a function of the sheet resistance for ion-implanted boron emitters passivated by SiNx, thermal SiO_2 and Al_2O_3. BBr_3-prepared and Al_2O_3-passivated boron emitter reported in Ref. [36] is cited for comparison purpose.

3.2. Rear surface passivation

In practice, there are two different types of surfaces on the rear side of front junction *n*-type silicon solar cells: diffused and non-diffused. Thermal SiO_2 film is very effective in passivating *n*-type silicon surface because it not only reduces the surface state density but also leads to a field-effect passivation due to positive fixed oxide charge [38]. It can reduce non-diffused *n*-type silicon surface SRV values below 10 cm/s [39]. Thermally grown SiO_2 is also very effective in passivating phosphorus-doped silicon surfaces. Since the phosphorus dopants in the diffused back surface of a *n*-type cell have the same polarity as the *n*-type silicon wafer, this doping profile creates a high-low junction (n^+n), the so-called back surface field (BSF). The corresponding electric field formed by the rear high-low junction of a BSF can very effectively shield holes from the rear surface, dramatically reducing rear surface recombination losses.

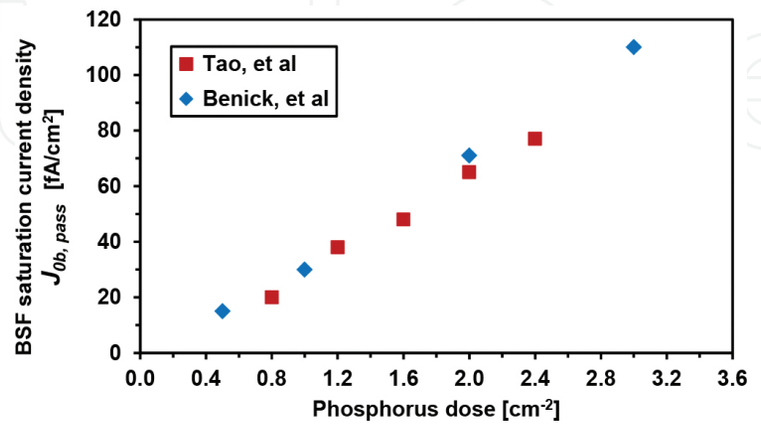

Figure 7. Saturation current density of phosphorus-doped and planarized rear surface $J_{0b,pass}$ as a function of the ion-implanted phosphorus dose [41, 42].

SiNx formed by PECVD provides excellent passivation for *n*-type surfaces because of its field-effect passivation provided by positive interface charges and the properties of the capture cross-sections of the dominant interface defects. Although the surface state density at Si-SiNx interface is much higher than that in the case of thermally grown Si-SiO_2 interfaces, SiNx demonstrates additional advantages for silicon solar cells: (1) excellent anti-reflection coating (ARC) on the rear side, which is suitable for bifacial architecture and (2) releasing large amounts of hydrogen during a high temperature (~800°C) contact firing process to passivate interface and bulk defects ('hydrogen passivation' [40]).

In front junction *n*-type silicon solar cells, phosphorus-doped rear surfaces are typically passivated by the combination of thermal SiO_2 and SiNx stacks. **Figure 7** shows that very low saturation current density has been demonstrated on planarized back surface with ion-implanted BSF $J_{0b,pass}$ of ≤20 fA/cm^2 for low phosphorus dose and $J_{0b,pass}$ of ~80 fA/cm^2 for high phosphorus dose with doping concentration of ~2×10^{20} cm^{-3}, which is compatible with screen printing [41, 42]. The $J_{0b,pass}$ of ≤100 fA/cm^2 has also been reported for SiO_2/SiNx-passivated ion-implanted and $POCl_3$ formed BSF on textured surface [42, 43], which are suitable for fully screen-printed bifacial front junction *n*-type silicon solar cells [17].

3.3. Carrier selective tunnel oxide passivated rear contact

Current high-efficiency front junction *n*-type silicon solar cells are often limited by the recombination in the heavily doped regions and at the metal/silicon contacts. A possible solution for minimizing doping and contact recombination is to insert a passivating material with offset bands between the metal and silicon, also known as passivated contact. One approach to accomplish this is to use an amorphous silicon-based heterojunction (HIT solar cell), which suppresses recombination effectively and which has resulted in outstanding cell V_{oc} of 750 mV [44]. However, this passivation scheme can withstand only low temperature (≤250°C) back-end process, hence is not compatible with the industry standard screen-printing and firing metallization technology [45]. Another approach to achieve a passivated contact involves a chemically grown ultra-thin (~15 Å) tunnel oxide capped with phosphorus-doped n^+ polycrystalline silicon (as shown in **Figure 8(A)**) and metal contact on the entire back side

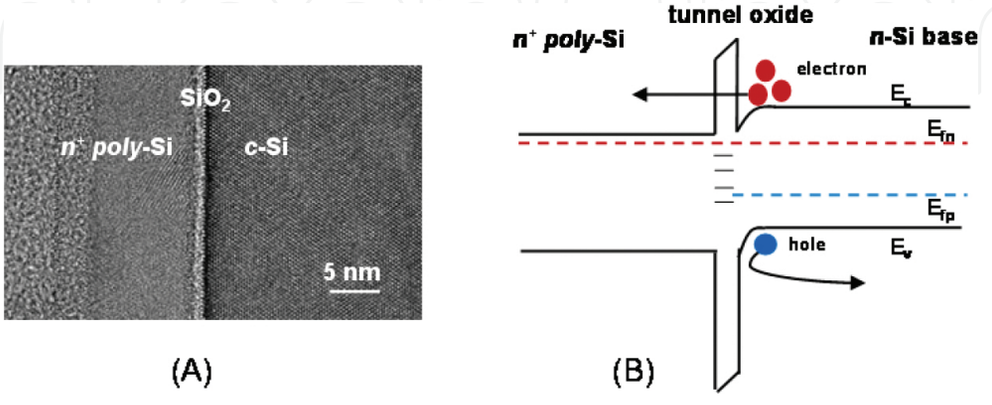

Figure 8. (A) Transmission electron microscopy image and (B) schematic band diagram of tunnel oxide passivated contact structure [45].

of *n*-type silicon cell [45], which is referred to as the tunnel oxide passivated contact (TOPCON) [46, 47].

In this TOPCON structure, four parallel mechanisms contribute to carrier selectivity (as shown in **Figure 8(B)**) [45]. (1) Heavily doped n^+ polycrystalline silicon creates an accumulation layer at the absorber surface due to the work function difference between the n^+ polycrystalline silicon and the n^- silicon absorber. This accumulation layer or band bending provides a barrier for holes to get to the tunnel oxide while electrons can migrate easily to the oxide/Si interface. (2) Tunnel oxide itself provides the second level of carrier selectivity because it presents a 4.5 eV barrier for holes to tunnel relative to 3.1 eV for electrons [48]. (3) There are very few or no states on the other side of the dielectric for holes to tunnel through because the valence band edge of n^- silicon absorber is facing the forbidden gap of n^+ polycrystalline silicon. (4) Even if a hole is able to tunnel through the oxide, it sees much higher resistance due to the n^+ polycrystalline silicon regions to get to the metal contact for recombination while the majority carrier electrons can easily get there. Last but not least, due to the full area metal contact on the back, there is one-dimensional (1D) current flow. This eliminates the lateral transport resistance (2D carrier flow), resulting in much higher *FF*. Therefore, this passivated contact is highly carrier selective and allows the flow of majority carriers via tunnelling while blocking minority carriers.

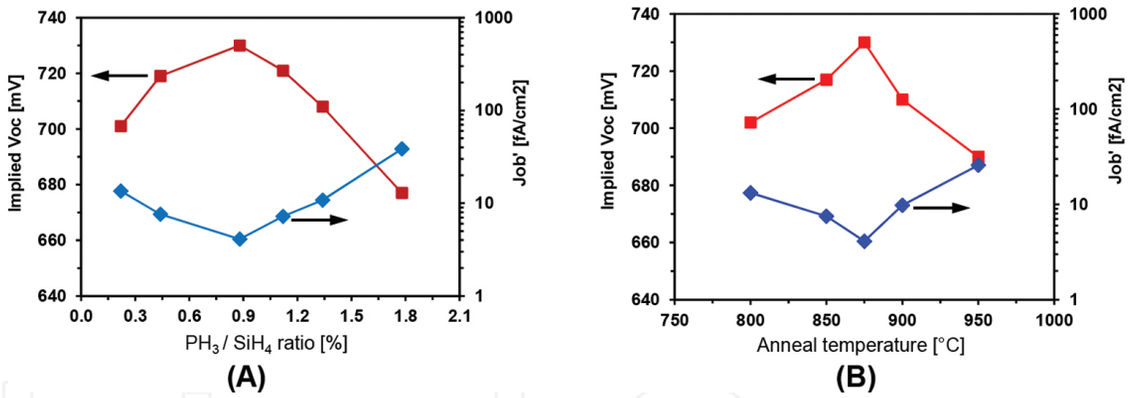

Figure 9. (A) Implied V_{oc} and J_{0b}' as a function of the PH_3/SiH_4 ratio during PECVD. (B) Implied V_{oc} and J_{0b}' as a function of the polysilicon anneal temperature [45].

To obtain an efficiently doped n^+ polycrystalline silicon layer to maintain the quasi-Femi level splitting in silicon absorber (high V_{oc}), a proper PH_3/SiH_4 ratio during PECVD is required for forming the phosphorus-doped amorphous silicon layer [45]. **Figure 9(A)** displays that if the PH_3/SiH_4 ratio is too high (high doping level in as-deposited amorphous silicon layer), the surface passivation quality degrades as indicated by low implied V_{oc} (iV_{oc}) and high saturation current density J_{0b}' obtained on symmetrical TOPCON structure. This is because more phosphorus dopants diffuse from the n^+ polycrystalline silicon layer through the tunnel oxide into the silicon absorber, resulting in high Auger recombination, as well as high recombination at the silicon/SiO_2 interface [49]. However, very low PH_3/SiH_4 ratio also causes inferior surface passivation due to the small band bending or weak accumulation layer created by the reduced

doping in the n^+ silicon layer, resulting in very weak field-effect passivation. In addition, to facilitate the solid-phase crystallization and activate the phosphorus dopants in the as-deposited n^+ amorphous silicon layer, a proper polysilicon anneal temperature is necessary as shown in **Figure 9(B)**. However, a strong degradation in the interface passivation quality is observed if the anneal temperature is too high (≥900°C), again due to more dopant diffusion into the silicon base causing high Auger recombination and possible local disruption of tunnel oxide due to polycrystalline silicon grain growth and more interface defects [45, 46]. It has also been demonstrated that both the tunnel oxide growth temperature in nitric acid and the high temperature firing process can affect the passivation quality. A very low J_{0b}' of ≤5 fA/cm^2 has been achieved by optimizing the TOPCON fabrication processes [50]. Similar passivation performance has also been achieved by depositing intrinsic amorphous silicon layer on top of the tunnel oxide layer followed by ion implantation of phosphorus and thermal annealing [51].

4. High-efficiency front junction *n*-type crystalline silicon solar cells

All front junction *n*-type crystalline silicon solar cell structures fabricated to date feature some degree of surface passivation. In the following section, we discuss several types of advanced high-efficiency front junction solar cells that have been developed on *n*-type silicon substrates.

4.1. Passivated emitter with rear totally diffused (PERT) cells

Even though *p*-type silicon solar cells dominate the PV market today, in recent years, several academic groups and companies have started to investigate front junction *n*-type crystalline silicon solar cells. The schematic of front junction *n*-type PERT 'passivated emitter rear totally diffused' [52, 53] cell is shown in **Figure 10**. PERT cell structure featuring a bifacial architecture is shown in **Figure 10(A)**, which can collect radiation from the rear side of the solar cell, hence has the potential to achieve an increased energy yield (5~20%) in certain module configurations. The PERT cell structure in **Figure 10(B)** shows the rear point contact that can reduce the rear metal-induced recombination due to lower metal coverage, as well as reduce the lateral resistance due to smaller contact pitch [22].

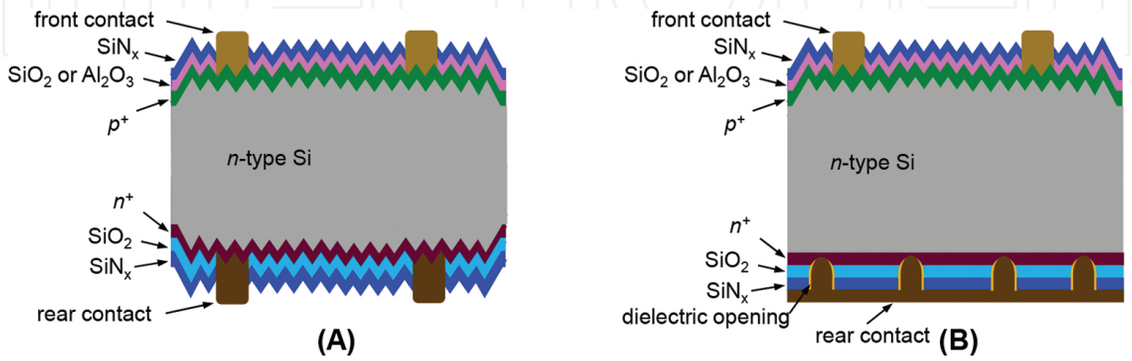

Figure 10. (A) Schematic of front junction *n*-type PERT cell with bifacial feature [52, 53]. (B) Schematic of front junction *n*-type PERT cell with rear point contacts [22].

Table 1 shows that 21.9% cell efficiency has been reported on thermal SiO_2-passivated boron emitter formed by BBr_3 diffusion [53] while 22.7% cell efficiency has been achieved via Al_2O_3-passivated boron emitter formed by ion implantation and photolithography on small area *n*-type float zone (Fz) substrates [54] with rear point contacts. To make manufacturable *n*-type PERT cells, screen-printing metallization has been applied on large area *n*-type Czochralski (Cz) silicon substrate with excellent cell efficiencies approaching 21% featuring bifacial architecture [17, 55], as listed in **Table 1**.

Literature	η (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	Area (cm^2)	Structure	Year
[54]	21.9	695	41.1	76.5	4 (FZ)	Rear point contact	2002
[55]	22.7	691	40.9	80.2	4 (FZ)	Rear point contact	2014
[56]	20.5	655	39.5	79.1	239 (CZ)	Bifacial	2014
[57]	21.0	665	39.8	79.3	239 (CZ)	Bifacial	2015

Table 1. Light *I-V* results of high-efficiency front junction *n*-type PERT silicon solar cells.

The detailed characterization and analysis show that the 22.7% efficient PERT cell is largely limited by the rear side recombination (J_{0b}') due to the totally diffused BSF layer ($J_{0b,\text{pass}}$), with J_{0b}' ($J_{0b,\text{pass}} + J_{0b,\text{metal}} = 29 + 4$) = 33 fA/cm^2, J_{0e} ($J_{0e,\text{pass}} + J_{0e,\text{metal}} = 12 + 16$) = 28 fA/cm^2 and $J_{0b,\text{bulk}}$ = 10 fA/cm^2 [54]. Therefore, to further improve the cell performance, the recombination in this heavily doped full BSF layer needs to be reduced. This can be accomplished by locally diffused BSF (PERL) structure on the rear side.

4.2. Passivated emitter with rear locally diffused (PERL) cells

The concept of 'passivated emitter rear locally diffused (PERL)' structure was introduced and developed in 1990s [56], in order to reduce the recombination from the rear side. The PERL schematic is shown in **Figure 11(A)**, which can diminish the heavy doping effect by using locally phosphorus-diffused area and decrease the metal-induced recombination simultaneously via heavy doping (n^{++}) underneath the contact metal. By upgrading from PERT to PERL structure, the J_{0b}' can be significantly reduced (from 33 to 15 fA/cm^2), which can lead to an increase in V_{oc} from 691 to 704 mV [10]. However, because the rear metal contact of PERL cell is restricted to a small fraction (<1%) of the rear surface, the carrier flow towards contact is constricted, which is beneficial for minority carriers (holes) but detrimental for majority carriers (electrons). On one hand, for minority carriers, such constriction is equivalent to reducing the conductance in the direction of the rear contact, which facilitates the build-up of their concentration inside the solar cell resulting in higher V_{oc}. However, for majority carriers, a lower conductance causes higher lateral resistive losses resulting in lower *FF* [57]. Hence, a trade-off between V_{oc} and *FF* needs to be considered. By optimizing the cell fabrication process to reduce contact resistance, a 23.9% efficient front junction PERL cell on small area *n*-type Fz substrate with photolithography contacts was reported [58] with V_{oc} of 705 mV and *FF* of 82.5%. The detailed characteriza-

tion and analysis shows that this 23.9% efficient PERL cell is limited by metal recombination on the front ($J_{0e,\text{metal}}$) and the rear side recombination J_{0b}', with total J_{0e} of 30 fA/cm^2 ($J_{0e,\text{pass}} = 10, J_{0e,\text{metal}} = 20$), $J_{0b,\text{bulk}}$ = 10 fA/cm^2 and J_{0b}' = 15 fA/cm^2 [54]. To further reduce recombination losses, selective emitter with heavier and deeper boron doping profile underneath front contact metal is typically implemented, as shown in **Figure 11(B)**, which can dramatically decrease the front metal-induced recombination (from 1800 to 200 fA/cm^2) resulting in $J_{0e,\text{metal}}$ reduction from 20 to 2 fA/cm^2 on the contacted region assuming ~1.1% metal coverage [10, 59].

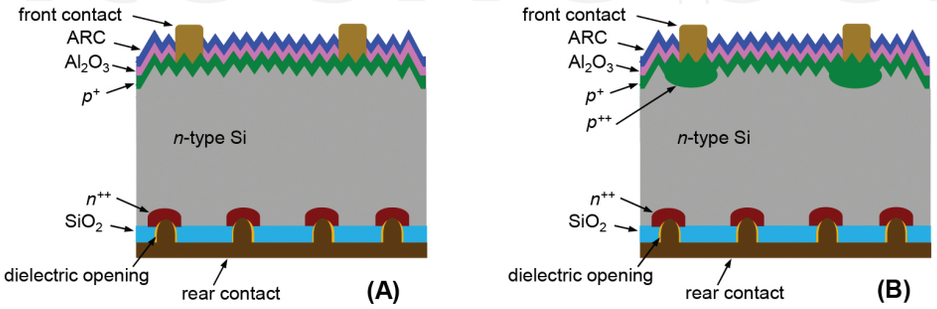

Figure 11. Schematic of front junction *n*-type PERL cell (A). (B) Front junction *n*-type PERL cell with selective emitter [56, 58].

4.3. Tunnel oxide passivated contact cells

The implementation of polysilicon tunnel junction as an alternative to either totally or locally diffused junction to reduce the recombination at the contact of silicon solar cells has been reported in the 1980s [60]. Because of its excellent surface passivation and carrier selectivity, a full area TOPCON shown in **Figure 12(A)** was applied, which also enables one-dimensional (1D) carrier transport on the rear side to eliminate *FF* losses due to 2D/3D carrier transport in the PERT and PERL cells.

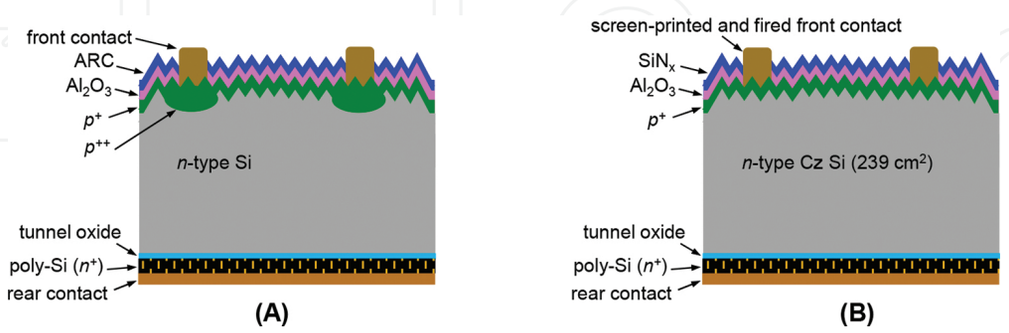

Figure 12. (A) Schematic of front junction *n*-type TOPCON cell with selective emitter [59, 61]. (B) Schematic of large area front junction *n*-type TOPCON cell with screen-printed and fired front contact [45].

In addition, because both the heavy doping effect and the metal-induced recombination are minimized in TOPCON structure, J_{0b}' is dramatically reduced from ≥15 fA/cm^2 in a PERL cell

to ≤8 fA/cm^2 in TOPCON cell [50, 54, 59]. A small area (4 cm^2) 24.9% efficient TOPCON cell has been reported [59] with selective boron emitter and photolithography contacts on the front in conjunction with TOPCON back (**Figure 12(A)**). This cell had a V_{oc} of 719 mV, J_{sc} of 41.5 mA/cm^2 and *FF* of 83.4% [59]. More recently, an efficiency of 25.1% is reported by moving the busbars outside the cell with J_{sc} of 42.1 mA/cm^2 [61].

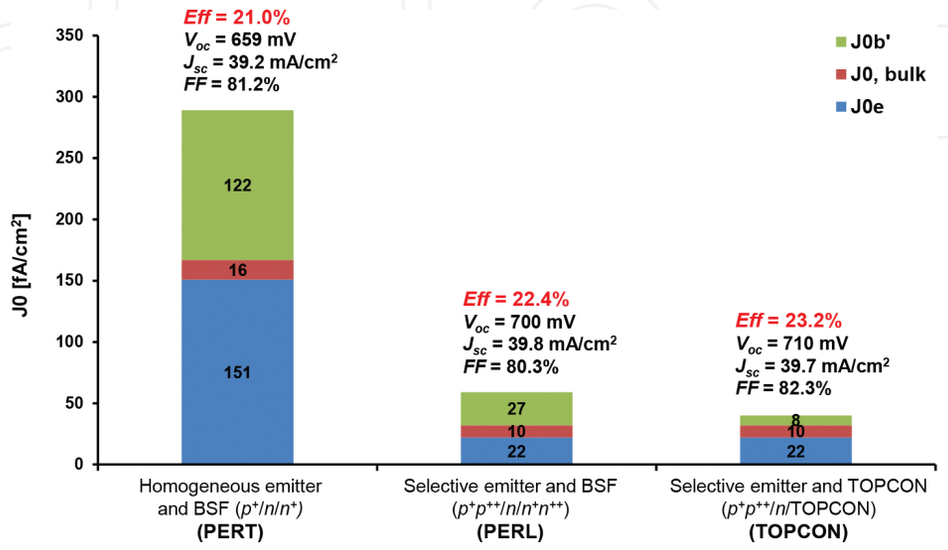

Figure 13. Simulated J_0 decomposition with each technology for large area front junction *n*-type PERT, PERL and TOPCON cells [62, 63].

To implement TOPCON on a more manufacturable cell structure, large area front junction n-type Cz silicon solar cells have been developed with ion-implanted boron emitter, SiNx anti-reflection coating and screen-printed front contact, as shown in **Figure 12(B)**, and cell efficiency of 21.4% with evaporated rear contact has been reported [45]. **Figure 13** shows the simulated road map to achieve ≥23% efficient large area front junction *n*-type silicon solar cells, including the reduction of all the J_0 components (J_{0e}, $J_{0b,\,bulk}$ and J_{0b}') in the cell [62, 63]. It is clearly shown that selectively doping is one of the most manufacturable and elegant way to reduce J_0 of the metallized and diffused regions simultaneously. This is because heavy diffusion underneath grid reduces metal J_0 and light diffusion in between the gridlines reduces J_0 of the diffused region. The 2D modelling shows that the cell efficiency can be increased from 21.0 to ~22.5% (bifacial architecture) by applying selectively doped emitter and BSF on large area *n*-type Cz wafers. Moreover, implementing TOPCON structure on the rear side can raise the cell efficiency over 23% with screen-printed contact on the front in combination with improved bulk material (10 Ω-cm, 3 ms lifetime).

5. Summary and outlook

In this chapter, the physics and operation of front junction *n*-type silicon solar cells is described, including detailed cell parameters, *pn*-junction formation, metallization approaches and

fundamental power loss mechanisms. To reduce surface recombination velocity for achieving high cell efficiency, Al_2O_3 has been approved to be very efficient on passivating heavily boron-doped front emitter and thermal SiO_2 is very effective to passivate phosphorous-diffused regions. In addition, to minimize the metal-induced recombination, implementation of selective boron emitter on the front side and locally-diffused back surface field on the rear side are preferred. Furthermore, TOPCON passivation scheme shows even better performance by simultaneously reducing the metal-induced recombination and the heavy doping effect, and allowing for 1D carrier transport. However, it is only suitable for being applied on the rear side of solar cell because the heavily doped polysilicon layer can absorb significant amount of incoming photons (hence low J_{sc}), if it is located on the front side.

High-efficiency front junction *n*-type silicon solar cells, including PERT, PERL and TOPCON cells, are reviewed and analysed. In combination with low-cost screen-printed metallization technology, PERT bifacial cell structure with homogeneous doping profiles on both front and back sides is a promising candidate of next-generation solar cells for industrial application in terms of process simplicity and energy yield while the recently developed cell structure with TOPCON on the rear and selective boron emitter on the front demonstrates the promise of this technology option for higher cell efficiency.

Acknowledgements

The authors would like to thank all other group members of UCEP in Georgia Tech and R&D department of Suniva, Inc. for their great support. This work was supported by the DOE FPACE I and the FPACE II contracts, as well as the DOE Solarmat1 and the DOE Solarmat2 contracts.

Author details

Yuguo Tao* and Ajeet Rohatgi

*Address all correspondence to: yuguo.tao@ece.gatech.edu

Georgia Institute of Technology, School of Electrical and Computer Engineering, University Center of Excellence for Photovoltaics, Atlanta, GA, USA

References

[1] Macdonald D, Geerligs LJ. Recombination activity of interstitial iron and other transition metal point defects in p-and n-type crystalline silicon. Applied Physics Letters. 2004; 85(18):4061–4063.

[2] Glunz SW, Rein S, Lee JY, Warta W. Minority carrier lifetime degradation in boron-doped Czochralski silicon. Journal of Applied Physics. 2001; 90(5):2397–2404.

[3] Green MG. Solar Cells: Operating Principles, Technology, and System Applications. Englewood Cliffs, NJ: Prentice-Hall, Inc.; 1982; 288 p.

[4] Green MA, Wenham SR, Watt ME. Applied Photovoltaics. Australia: National Library of Australia, Centre for Photovoltaic Devices and Systems, UNSW; 1997.

[5] Shockley W, Queisser HJ. Detailed balance limit of efficiency of p-n junction solar cells. Journal of Applied Physics. 1961; 32(3):510–519.

[6] King R, Gruenbaum P, Sinton R, Swanson R. Passivated emitters in silicon solar cells. In: 21st IEEE Photovoltaic Specialists Conference; Kissimmee, FL, USA; 1990. p. 227–232.

[7] Kim DS, Das A, Nakayashiki K, Rounsaville B, Meemongkolkat V, Rohatgi A. Silicon solar cells with boron back surface field formed by using boric acid. In: 22nd European Photovoltaic Solar Energy Conference; Milan, Italy; 2007.

[8] Das A, Ryu K, Rohatgi A. 20% Efficient screen-printed n-type solar cells using a spin-on source and thermal oxide/silicon nitride passivation. IEEE Journal of Photovoltaics. 2011; 1(2):146–152.

[9] Ryu K, Upadhyaya A, Ok YW, Xu H, Metin L, Rohatgi A. High efficiency n-type solar cells with screen-printed boron emitters and ion-implanted back surface field. In: 38th IEEE Photovoltaic Specialists Conference (PVSC); Austin, TX; 2011. p. 2247–2249.

[10] Benick J, Hoex B, Van de Sanden MC, Kessels WM, Schultz O, Glunz SW. High efficiency n-type Si solar cells on Al2O3-passivated boron emitters. Applied Physics Letters. 2008; 92(25):253501–253504.

[11] Schiele Y, Fahr S, Joos S, Hahn G, Terheiden B. Study on boron emitter formation by BBr3 diffusion for n-type Si solar cell applications. In: 28th European Photovoltaic Solar Energy Conference and Exhibition; Paris, France; 2013. p. 1242–1247.

[12] Werner S, Lohmuller E, Belledin U, Vlooswijk AHG, Naber RCG, Mack S, Wolf A. Optimization of BBr3 diffusion processes for n-type silicon solar cells. In: 31st European Photovoltaic Solar Energy Conference; Hamburg, Germany; 2015.

[13] Hieslmair H, Latchford I, Mandrell L, Chun M, Adibi B. Ion implantation for silicon solar cells. Cell. 2010; 18:17.

[14] Rohatgi A, Meier DL, McPherson B, Ok YW, Upadhyaya AD, Lai JH, Zimbardi F. High-throughput ion-implantation for low-cost high-efficiency silicon solar cells. Energy Procedia. 2012; 15:10–19.

[15] Hermle M, Benick J, Rüdiger M, Bateman N, Glunz SW. N-type silicon solar cells with implanted emitter. In: 26th European Photovoltaic Solar Energy Conference; Hamburg, Germany; 2011. p. 875–878.

[16] Tao Y, Rohatgi A. High-efficiency large area ion-implanted n-type front junction Si solar cells with screen-printed contacts and SiO_2-passivated boron emitters. In: 40th IEEE Photovoltaic Specialist Conference; Denver, CO, USA; 2014. p. 3654–3658.

[17] Boscke TS, Kania D, Schollhorn C, Stichtenoth D, Helbig A, Sadler P, Braun M, Dupke M, Weis M, Grohe A, Lossen J. Fully ion implanted and coactivated industrial n-type cells with 20.5% efficiency. IEEE Journal of Photovoltaics. 2014; 4(1):48–51.

[18] Florakis A, Janssens T, Rosseel E, Douhard B, Delmotte J, Cornagliotti E, Poortmans J, Vandervorst W. Simulation of the anneal of ion implanted boron emitters and the impact on the saturation current density. Energy Procedia. 2012; 27:240–246.

[19] Müller R, Benick J, Bateman N, Schön J, Reichel C, Richter A, Hermle M, Glunz SW. Evaluation of implantation annealing for highly-doped selective boron emitters suitable for screen-printed contacts. Solar Energy Materials and Solar Cells. 2014; 120:431–435.

[20] Taniguchi K, Kurosawa K, Kashiwagi M. Oxidation enhanced diffusion of boron and phosphorus in (100) silicon. Journal of the Electrochemical Society. 1980; 127(10):2243–2248.

[21] Hahn G, Joos S. State-of-the-art industrial crystalline silicon solar cells. In: Willeke GP, Weber ER, editors. Semiconductors and Semimetals. 1st ed. London, UK: Elsevier Inc.; 2014. p. 1–62.

[22] Tao Y, Payne A, Upadhyaya VD, Rohatgi A. 20.7% efficient ion-implanted large area n-type front junction silicon solar cells with rear point contacts formed by laser opening and physical vapor deposition. Progress in Photovoltaics: Research and Applications. 2014; 22(10):1030–1039.

[23] Jiang F, Stavola M, Rohatgi A, Kim D, Holt J, Atwater H, Kalejs J. Hydrogenation of Si from SiNx (H) films: characterization of H introduced into the Si. Applied Physics Letters. 2003; 83(5):931–933.

[24] Hahn G, Käs M, Herzog B. Hydrogenation in crystalline silicon materials for photovoltaic application. Solid State Phenomena. 2010; 156:343–349.

[25] Mason N, Artigao A, Banda P, Bueno R, Fernandez JM, Morilla C, Russell R. The technology and performance of the latest generation buried contact solar cell manufactured in BP Solar's Tres Cantos facility. In: 19th European Photovoltaic Solar Energy Conference; Paris, France; 2004.

[26] Lennon A, Yao Y, Wenham S. Evolution of metal plating for silicon solar cell metallisation. Progress in Photovoltaics: Research and Applications. 2013; 21(7):1454–1468.

[27] Bartsch J, Kamp M, Hartleb D, Wittich C, Mondon A, Steinhauser B, Feldmann F, Richter A, Benick J, Glatthaar M, Hermle M. 21.8% efficient n-type solar cells with industrially feasible plated metallization. Energy Procedia. 2014; 55:400–409.

[28] Katkhouda K, Martinez-Limia A, Bornschein L, Koseva R, Geppert T, Grohe A, Krokoszinski HJ, Schaaf P. Aluminum-based rear-side PVD metallization for nPERT silicon solar cells. IEEE Journal of Photovoltaics. 2014; 4(1):160–167.

[29] Jung V, Heinemeyer F, Kšntges M. Long-term stable encapsulated solder joints on an Al/Ni: V/Ag metallization for silicon solar cells. Energy Procedia. 2012; 21:84–91.

[30] Meier DL, Good EA, Garcia RA, Bingham BL, Yamanaka S, Chandrasekaran V, Bucher C. Determining components of series resistance from measurements on a finished cell. In: Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion; Waikoloa, HI; 2006. p. 1315–1318.

[31] Shockley W, Read Jr WT. Statistics of the recombinations of holes and electrons. Physical Review. 1952; 87(5):835.

[32] Hall RN. Electron-hole recombination in germanium. Physical Review. 1952; 87(2):387.

[33] Sinton RA, Cuevas A. Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data. Applied Physics Letters. 1996; 69(17):2510–2512.

[34] Aberle AG. Surface passivation of crystalline silicon solar cells: a review. Progress in Photovoltaics: Research and Applications. 2000; 8(5):473–487.

[35] Agostinelli G, Delabie A, Vitanov P, Alexieva Z, Dekkers HF, De Wolf S, Beaucarne G. Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge. Solar Energy Materials and Solar Cells. 2006; 90(18):3438–3443.

[36] Hoex B, Schmidt J, Bock R, Altermatt PP, Van de Sanden MC, Kessels WM. Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al_2O_3. Applied Physics Letters. 2007; 91(11):112107.

[37] Altermatt PP, Plagwitz H, Bock R, Schmidt J, Brendel R, Kerr MJ, Cuevas A. The surface recombination velocity at boron-doped emitters: comparison between various passivation techniques. In: 21st European Photovoltaic Solar Energy Conference; Dresden, Germany; 2006. p. 647–650.

[38] Aberle AG, Glunz S, Warta W. Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si-SiO_2 interface. Journal of Applied Physics. 1992; 71(9):4422–4431.

[39] Stephens AW, Aberle AG, Green MA. Surface recombination velocity measurements at the silicon-silicon dioxide interface by microwave-detected photoconductance decay. Journal of Applied Physics. 1994; 76(1):363–370.

[40] Kimura K. Recent developments in polycrystalline silicon solar cells. In: 1st International Photovoltaic Science and Engineering Conference; Kobe, Japan; 1984. p. 37–42.

[41] Benick J, Müller R, Bateman N, Hermle M, Glunz S. Fully implanted n-type PERT solar cells. In: 27th European Photovoltaic Solar Energy Conference and Exhibition; Frankfurt, Germany; 2012. p. 676–679.

[42] Tao Y, Ok YW, Zimbardi F, Upadhyaya AD, Lai JH, Ning S, Upadhyaya VD, Rohatgi A. Fully ion-implanted and screen-printed 20.2% efficient front junction silicon cells on 239 cm n-type CZ substrate. IEEE Journal of Photovoltaics. 2014; 4(1):58–63.

[43] Wolf A, Kimmerle A, Werner S, Maier S, Belledin U, Meier S, Biro D. Status and perspective of emitter formation by POCl3 diffusion. In: 31st European PV Solar Energy Conference and Exhibition; Hamburg, Germany; 2015.

[44] Taguchi M, Yano A, Tohoda S, Matsuyama K, Nakamura Y, Nishiwaki T, Fujita K, Maruyama E. 24.7% record efficiency HIT solar cell on thin silicon wafer. IEEE Journal of Photovoltaics. 2014; 4(1):96–99.

[45] Tao Y, Upadhyaya V, Huang YY, Chen CW, Jones K, Rohatgi A. Carrier selective tunnel oxide passivated contact enabling 21.4% efficient large-area n-type silicon solar cells. In: 43rd IEEE Photovoltaic Specialist Conference; Portland, OR, USA; 2016.

[46] Feldmann F, Bivour M, Reichel C, Hermle M, Glunz SW. Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics. Solar Energy Materials and Solar Cells. 2014; 120:270–274.

[47] Moldovan A, Feldmann F, Zimmer M, Rentsch J, Benick J, Hermle M. Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO_2 layers. Solar Energy Materials and Solar Cells. 2015; 142:123–127.

[48] Lee WC, Hu C. Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction-and valence-band electron and hole tunneling. IEEE Transactions on Electron Devices. 2001; 48(7):1366–1373.

[49] Steinkemper H, Feldmann F, Bivour M, Hermle M. Numerical simulation of carrier-selective electron contacts featuring tunnel oxides. IEEE Journal of Photovoltaics. 2015; 5(5):1348–1356.

[50] Tao Y, Upadhyaya V, Chen CW, Payne A, Chang EL, Upadhyaya A, Rohatgi A. Large area tunnel oxide passivated rear contact n-type Si solar cells with 21.2% efficiency. Progress in Photovoltaics: Research and Applications. 2016; 24:830–835.

[51] Romer U, Peibst R, Ohrdes T, Lim B, Krugener J, Wietler T, Brendel R. Ion implantation for poly-Si passivated back-junction back-contacted solar cells. IEEE Journal of Photovoltaics. 2015; 5(2):507–514.

[52] Zhao J, Wang A, Green MA. 24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates. Progress in Photovoltaics: Research and Applications. 1999; 7(6):471–474.

[53] Zhao J, Wang A, Altermatt PP, Green MA, Rakotoniaina JP, Breitenstein O. High efficiency PERT cells on n-type silicon substrates. In: 29th IEEE Photovoltaic Specialists Conference; New Orleans, LA, USA; 2002. p. 218–221.

[54] Benick J, Steinhauser B, Muller R, Bartsch J, Kamp M, Mondon A, Richter A, Hermle M, Glunz S. High efficiency n-type PERT and PERL solar cells. In: 40th IEEE Photovoltaic Specialist Conference; Denver, CO; 2014. p. 3637–3640.

[55] Institute for Solar Energy Research in Hamelin (ISFH). Ion implanted, co-annealed and fully screen-printed bifacial n-type PERT solar cells with efficiencies of 21% and bifaciality factors exceeding 97% [Internet]. Sep 4th, 2015. Available from: http://www.isfh.de

[56] Zhao J, Wang A, Green M. 24% efficient PERL structure silicon solar cells. In: 21st IEEE Photovoltaic Specialists Conference; Kissimmee, FL; 1990. p. 333–335.

[57] Cuevas A. Electrons and holes in solar cells with partial rear contacts. Progress in Photovoltaics: Research and Applications. 2014; 22(7):764–774.

[58] Glunz SW, Benick J, Biro D, Bivour M, Hermle M, Pysch D, Rauer M, Reichel C, Richter A, Rüdiger M, Schmiga C. N-type silicon-enabling efficiencies>20% in industrial production. In: 35th IEEE Photovoltaic Specialists Conference; Honolulu, HI; 2010. p. 50–56.

[59] Hermle M, Feldmann F, Eisenlohr J, Benick J, Richter A, Lee B, Stradins P, Rohatgi A, Glunz SW. Approaching efficiencies above 25% with both sides-contacted silicon solar cells. In: 42nd IEEE Photovoltaic Specialist Conference; New Orleans, LA; 2015. p. 1–3.

[60] Yablonovitch E, Gmitter T, Swanson RM, Kwark YH. A 720 mV open circuit voltage SiOx:c-Si:SiOx double heterostructure solar cell. Applied Physics Letters. 1985; 47(11): 1211–1213.

[61] Glunz SW, Feldmann F, Richter A, Bivour M, Reichel C, Steinkemper H, Benick J, Hermle M. The irresistible charm of a simple current flow pattern -25% with a solar cell featuring a full-area back contact. In: 31st European Photovoltaic Solar Energy Conference and Exhibition; Hamburg, Germany; 2015.

[62] Chen CW, Hermle M, Benick J, Tao Y, OK YW, Upadhyaya A, Tam A, Rohatgi A. Modeling the potential of screen-printed front and tunnel oxide passivated back contact Cz silicon solar cell. Progress in Photovoltaics: Research and Applications. Forthcoming.

[63] Tam AM, Huang Y, OK Y, Rohatgi A. Design of selective emitter profiles for high efficiency solar cells under manufacturing technology constraints. In: 43rd IEEE Photovoltaic Specialist Conference; Portland, OR; 2016.

IntechOpen