Chapter 3

Heteroepitaxial Growth of III–V Semiconductors on 2D Materials

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Additional information is available at the end of the chapter

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Abstract

Quasi van der Waals epitaxy (QvdWE) of III-V semiconductors on two-dimensional layered material, such as graphene, is discussed. Layered materials are used as a lattice mismatch/thermal expansion coefficient mismatch-relieving layer to integrate III-V semiconductors on any arbitrary substrates. In this chapter, the epitaxial growth of both III–V nanowires and thin films on two-dimensional layered materials is presented. Also, the growth challenges of thin film on two-dimensional materials using QvdWE are discussed through density functional theory calculations. Furthermore, optoelectronic devices of III-V semiconductors integrated on two-dimensional layered material based on QvdWE are overviewed to prove the future potential and importance of such type of epitaxy.

Keywords: van der Waals, heteroepitaxy, graphene, III–V semiconductor, thin films, nanostructures

1. Introduction to van der Waals epitaxy

Heteroepitaxial growth of III–V semiconductor on complementary metal-oxide-semiconductor (CMOS)-compatible substrates has been a subject of research over the last 40 years [1–10]. Unfortunately, these long-period and extensive scientific efforts devoted to the direct growth of III–V materials on such target substrates have resulted in little success. The primary obstacle to success is the lattice and thermal expansion mismatches between semiconductor compounds of interest and the substrate materials. Therefore, the heteroepitaxy of high-quality three-dimensional (3D) materials requires an alternative technique, which can eliminate the limitation of inherent lattice matching [11–15].

Thanks to the two-dimensional (2D)-layered materials whose unique and promising properties enable to open up a new route of heteroepitaxy without the aforementioned constraints. Recently, the so-called van der Waals epitaxy (vdWE), a new paradigm of epitaxial growth for III–V semiconductors, has been the focus of significant research interest, which is evidenced by a search in Google Scholar, leading to 12,200 hits in the years 2011 through 2015 [16–21]. Needless to say, this new research area of heteroepitaxy is mainly dictated by the surface properties of emerging 2D materials, which also have many novel electrical, optical, thermal, and mechanical properties [22–34].

Recently, different research groups already used few 2D atomic-layered materials as a semiconductor substrate for the growth of 3D semiconductors [35–37]. Among them, graphene, hexagonal boron nitride (hBN), transition metal dichalcogenides (TMDs), and topological insulator materials are the most frequently used ones. The main reason why these 2D materials are advantageous to be used as a semiconductor substrate is that the overgrown film materials float on top of the dangling-bonds-free 2D substrate surface instead of being rigidly bound to it, thereby mitigating lattice and thermal mismatch between 3D materials and the underlying 2D substrate. Besides, due to the crystalline surface with triangular lattice or honeycomb atomic arrangement, 2D materials are structurally compatible with many 3D semiconductors of zinc-blend (ZB), wurtzite (WZ), and diamond crystal structures. Furthermore, most of the 2D materials are thermally stable, which exhibit high decomposition temperature, thus making it an ideal material of choice for many fabrication processes.

The integration of III–V semiconductors on 2D materials is feasible using the epitaxial growth by molecular beam epitaxy (MBE) or metal organic chemical vapor phase deposition (MOCVD). Layered materials can be grown directly on the target substrates using either chemical vapor deposition (CVD) or MBE [38, 39]. Then, the layered material can be mechanically transferred onto any substrate after being grown if needed. Graphene is found to be one of the most popular 2D materials for van der Waals (vdW) epitaxial growth. A number of studies are undertaken to achieve high-quality MBE-grown GaAs nanowires (NWs) on a graphene/silicon substrate. High-density, vertical, coaxially heterostructured InAs/InGaAs NWs on graphene over a wide tunable ternary compositional range is demonstrated using MOCVD.

Using graphene as a 2D material for relieving thermal/lattice mismatch, the proof-of-principle demonstrations for the epitaxial growth of GaAs [36, 40], InAs [41], and GaN [23, 42, 43] on silicon substrates are already presented in several studies. Hence, these early demonstrations show a great promise of vdW heteroepitaxy for integrating III–V semiconductors on silicon using 2D materials as a buffer layer. Both nanostructures and thin films of these compound semiconductors are addressed by these preliminary studies. Most importantly, the results obtained from these studies motivate to realize high-quality epitaxial thin film or nanostructures of other III–V semiconductors, for example, InP, GaSb, InAs on silicon using graphene buffer layers. In such a way, the epitaxial growth on 2D material platform will have significant implications for a wide variety of optoelectronic devices, such as light-emitting devices [26, 42] and a new generation of solar cells for flexible applications [44].

Given the significant research interest in vdW heteroepitaxy for III–V compound semiconductors utilizing 2D materials, there is an obvious need for a comprehensive book chapter, which describes the recent progress and research activities. The aim of this chapter is to give a precise picture of the current status of vdW heteroepitaxy for 3D semiconductors on 2D materials, targeting mainly for optoelectronic device applications.

In this chapter, the difference between vdWE associated with layered materials and conventional epitaxy is first briefly discussed in Section 2. The work of several groups worked on nanowires grown on graphene using vdW epitaxial growth is then described in Section 3. Different types of grown 3D III–V thin films on 2D materials already demonstrated are mentioned in Section 4. Finally, a summary on the future prospects of the vdW epitaxy concept in case of growth of 3D materials on a layered material substrate is presented in Section 5.

2. vdWE vs. conventional epitaxy

VdWE was first introduced by Koma in 1984 where he successfully grew $NbSe_2/MoS_2$ system using vdW weak interactions [18, 45]. In this type of epitaxy, the growth is driven by the vdW forces between the 2D layers with neither surface dangling bonds nor passivation. These weak vdW interactions between the layers during the epitaxy releases any stress stored in the strained films, yielding high-quality material with reduced threading dislocation densities. This kind of epitaxy is different from the conventional growth where lattice-matching conditions are very important to have high-quality single-crystal semiconductors. As an intermediate type of epitaxy between vdWE and the conventional epitaxy, quasi van der Waals epitaxy (QvdWE) emerged recently by integrating 3D conventional semiconductors on layered substrates. In QvdWE, the interface interactions are not purely based on the vdW interaction but a midpoint where the dangling bonds of the grown 3D semiconductor have an effect on the epitaxial growth [46]. Importantly, the concept of QvdWE can be applied for the deposition of different types of grown structures including nanowires and thin films, as schematically shown in **Figure 1**. In the following sections, several demonstrations by different research teams worldwide for such structures utilizing QvdWE are discussed.

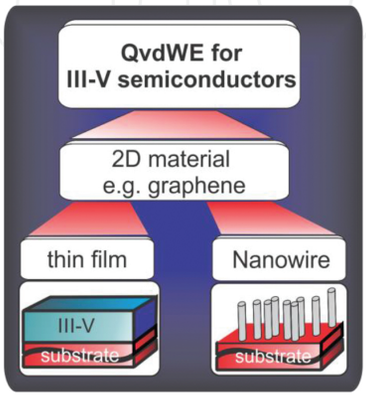


Figure 1. Different types of growth structures.

3. III-V nanowires QvdWE on layered materials

Munshi et al. proposed a generic atomic model that relates the epitaxial growth configurations of various III-V nanowires on graphene to the lattice mismatch between graphene and the grown semiconductor, as in **Figure 2**(**a**–**d**) [47]. The experimental verification of the model was undertaken through the use of molecular beam epitaxy (MBE). In this study, the self-catalyzed vapor liquid technique was used to create regular hexagonal cross-sectional shapes with

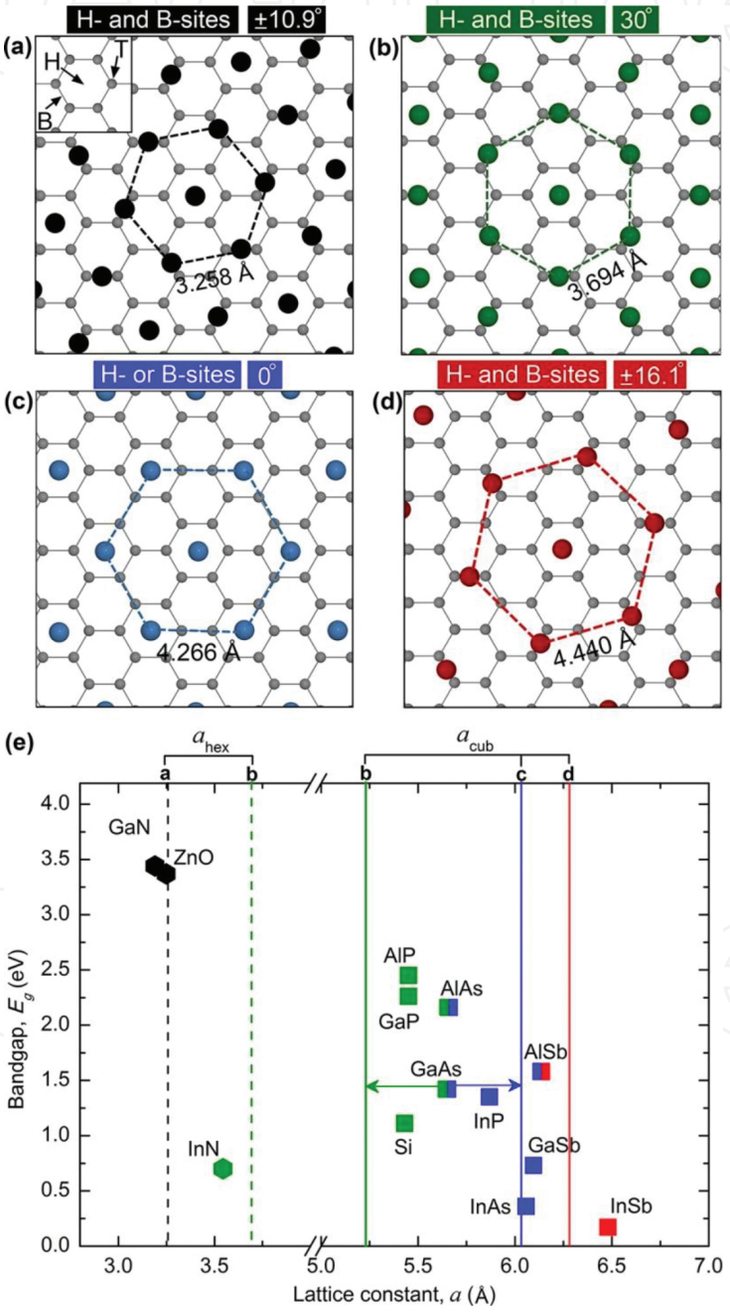


Figure 2. (a–d) Different possible arrangements of semiconductor atoms in the (111) plane of cubic crystal on graphene. (b) III/V semiconductor bandgaps versus lattice. The vertical lines represent the lattice matching condition for different III/V semiconductor arrangements in (a–d) on graphene. Reproduced with permission from Ref. [47].

uniformity in diameter and length. To increase the nanowire density on graphene, two-temperature growth strategy was used to facilitate the nucleation prior to the nanowire growth. A TEM image of GaAs nanowire grown on graphene shows that the bottom part of the nanowire has a mixture of ZB and WZ segments with twins and stacking faults, whereas the rest of the nanowire is nearly defect-free ZB configuration. In this demonstration, authors showed that despite the quite large mismatch in two different configurations, that is, cubic GaAs on graphene, 6.3% lattice mismatch for blue configuration and 8.2% for the green configuration (**Figure 2e**), they were still able to achieve high quality epitaxial growth, hinting that QvdWE can overcome the lattice mismatch constraints.

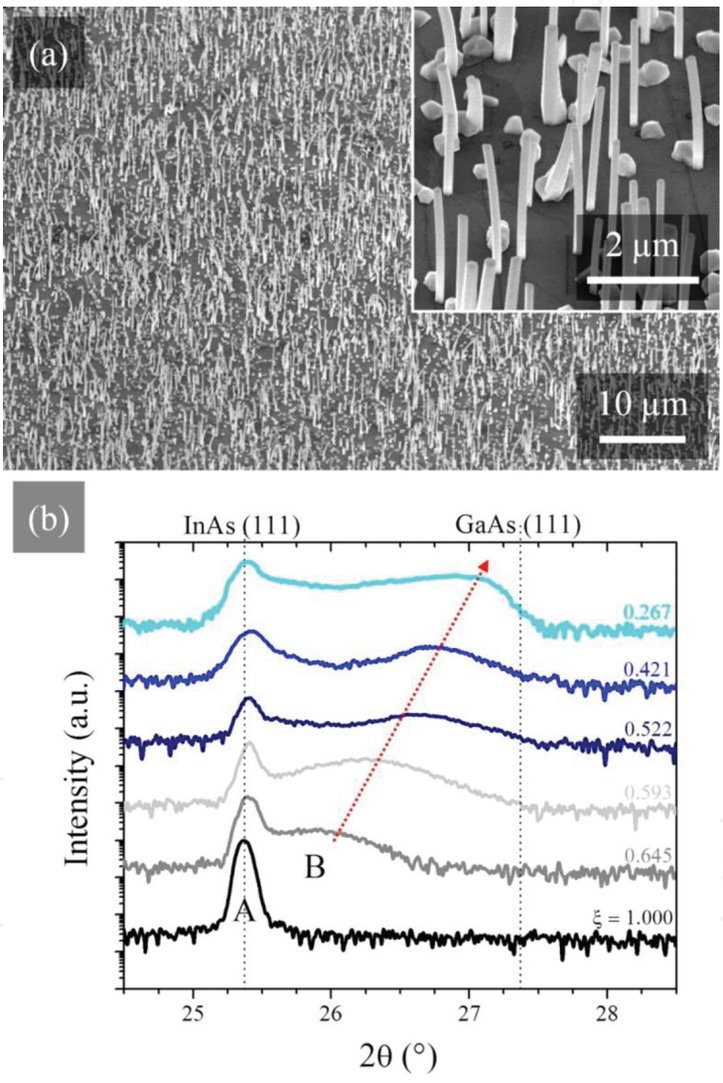


Figure 3. (a) Tilted scanning electron microscopy (SEM) image of $In_{0.39}Ga_{0.61}As$ NWs, with a higher magnification image shown in the inset. (b) Normalized XRD rocking curves of different In compositions plotted on a logarithmic scale. The B peak represents the position of the InGaAs peak. Reproduced with permission from Ref. [48].

Mohseni et al. have reported a self-organized method for the formation of coaxially heterostructured InAs/$In_xGa_{1-x}As$ NWs, over a wide tunable ternary compositional range grown

directly on graphene substrates [48]. In this growth, metalorganic chemical vapor deposition (MOCVD) was used to integrate the III-V semiconductor on the graphene. The growth of InGaAs nanowires led to spontaneous separation of phase from the start of the growth, which eventually led to a well-defined InAs/$In_xGa_{1-x}As$ ($0.2 < x < 1$) core-shell structure. The axial growth of InAs-$In_xGa_{1-x}As$ ($0.2 < x < 1$) started without change in diameter of nanowires. After about 2 μm in height, those nanowires were grown in the form of core-shell structures. The shell composition of InAs-$In_xGa_{1-x}As$ changes as a function of indium flow; however, the thickness of the shell and core and the start of nonsegregated InAs-$In_xGa_{1-x}As$ are independent of the composition of indium (**Figure 3**). Moreover, the authors found out that no InGaAs phase segregation was observed when growing on MoS_2 or through the Au-assisted vapor-liquid-solid (VLS) technique on graphene. This work demonstrated that QvdWE of InAs on graphene could facilitate phase segregation phenomenon causing a self-organized InAs core/InGaAs shell nanowires. This phase segregation is driven mainly by lack of strain between InAs and graphene layers interface due to the weak vdW forces at this interface.

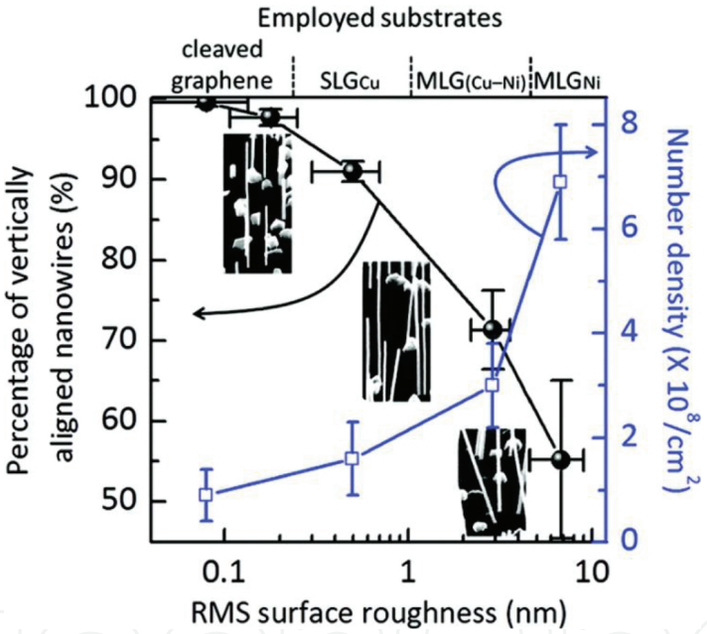


Figure 4. The percentage of vertically well-aligned InAs nanowires (*black solid circles*) and the density of nanowires (*blue empty squares*) relationship to the rms surface roughness of the graphene substrates. Reproduced with permission from Ref. [41].

Hong et al. found out that the density of InAs nanowires arrays integrated on graphene films increases with the number of graphene layers [41]. This is mainly because the nucleation of InAs is more likely on the surface potential wells formed by surface ledges in the graphene. However, the use of single-layer graphene as a substrate will encourage the growth of vertically well-aligned InAs arrays of nanowires with high levels of strong vdW attraction (**Figure 4**). The QvdW epitaxial relationship between InAs and graphene is confirmed by the InAs's hexagonal morphology with six ZB sidewall facets, aligned in a sixfold within a single domain of graphene.

QvdWE of III-V nanowires on 2D materials has brought a new momentum due to the introduction of new and attractive properties to the grown 1D nanostructure. However, the increased speed of investigation in developing nanostructures on 2D materials does not lack its issues and drawbacks. There is a challenge in accurate regulation of dopant circulation inside the semiconductor nanostructures, the direction of growth, dimensionality, and consistency in size. In addition, high surface recombination, poor thermal management, and highly resistive ohmic contacts are other few inherent aspects of nanostructures, which must be overcome to realize the potential of nanowires [49].

4. III–V thin films by QvdWE on 2D materials

4.1. GaAs thin films

The integration of III–V thin films on 2D materials opened a new and unique opportunity by releasing the lattice/thermal expansion mismatches between any 3D semiconductors and 2D material. Moreover, the weak vdW force of the layered materials allows reusing the 2D substrate multiple times by peeling off the grown semiconductors from the layered materials [42]. The demonstration of III-As-based thin films growth on graphene was reported by Alaskar et al. where ultra-smooth planar GaAs was deposited on silicon substrate using graphene as a buffer layer was performed, as presented in **Figure 5** [36]. In addition, the challenges that face the epitaxial growth of III-V semiconductors atop 2D materials, especially graphene, were highlighted. From a thermodynamics perspective of the growth, the low surface free energy of the layered materials yields an island growth mode where the surface of the layered 2D substrate is nonwetting.

The surface free energies of 3D semiconductors are two orders of magnitude higher than layered materials (**Table 1**), which make this type of epitaxial growth challenging. Indeed, engineering tricks are needed to overcome this issue [50–52].

The adsorption and migration energies of III-V-based atoms on graphene, as listed in **Table 2**, indicate that the growth of GaAs on graphene should be initiated with gallium for its higher adsorption and migration energies compared to arsenic, indium, or aluminum.

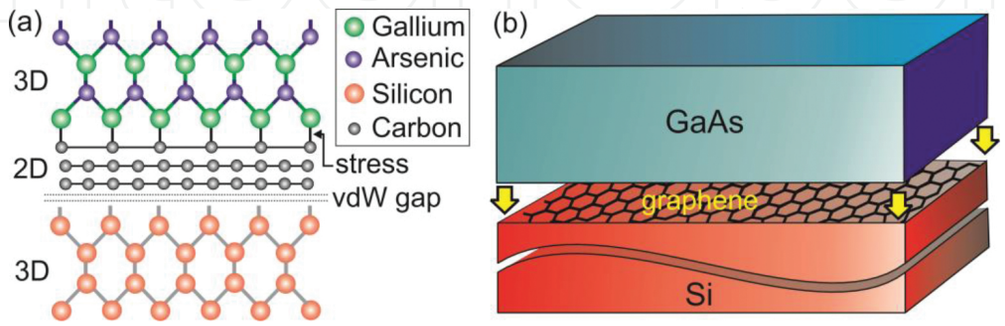
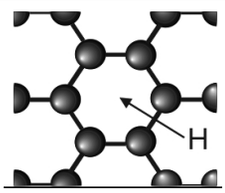
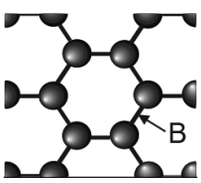
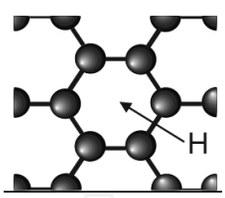
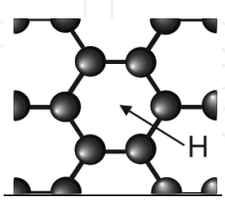


Figure 5. (a) The atomic geometry of GaAs/graphene/Si structure using (b) the schematic view of multilayered graphene used as a buffer layer for GaAs on silicon. Reproduced with permission from Ref. [36].

Materials	Surface free energy (mJ m^{-2})
Si (111)	1467 [53]
GaAs (111)	1697 [53]
Graphene	48
Multilayer graphene (MLG)	52
Bismuth selenide (Bi_2Se_3)	180 [54]

Note: Reproduced with permission from Ref. [36].

Table 1. The surface free energies of different 3D semiconductors and layered semiconductors.

Atom	Favored adsorption site	Adsorption energy E_b (eV)	Migration energy E_m (eV)
Gallium		1.5	0.05
Arsenic		1.3	0.21
Indium		1.3	0.06
Aluminum		1.7	0.03

Note: Reproduced with permission from Ref. [36].

Table 2. Adsorption and migration energies of Ga, As, In, and Al adatoms adsorbed on most favorable site of bilayer graphene based on density functional theory (DFT) calculation, taking into account vdW forces.

Utilizing the superior kinetic properties of gallium, the growth was initiated by two monolayers of Ga atoms at room temperature. This was followed by arsenic overpressure while elevating the growth temperature to 400°C and the deposition of 25 nm GaAs atop graphene

at a rate of 0.15 Å/s. The GaAs morphology showed a smooth surface with an RMS value of 0.6 nm. The crystal quality was characterized using both Raman spectroscopy and X-ray diffraction (XRD) [40]. The two GaAs Raman signature peaks at 268 (TO) and 292 (LO) cm^{-1} can be seen in the micro-Raman spectrum (**Figure 6a**). **Figure 6b** shows the rocking curve full width at half maximum (FWHM) value for the GaAs(111) plane around 245 arcsec (0.068°), indicating high defect density. This is still encouraging since the direct growth of GaAs with the same thickness shows much higher defect density [2].

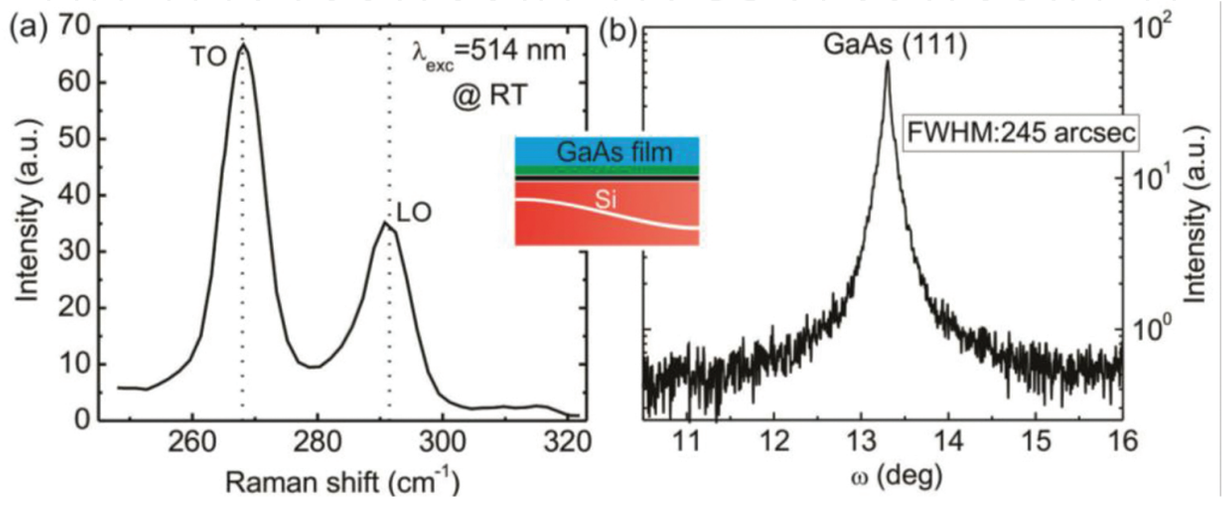


Figure 6. (a) Room temperature micro-Raman spectrum of GaAs on graphene/silicon shows TO and LO peaks at 268 and 292 cm^{-1}, respectively, where the TO peak is the dominant one. (b) XRD rocking-curve of GaAs (111) peak. Reproduced with permission from Ref. [36].

4.2. GaN thin films

So far, the thin-film growth of nitride-based semiconductors on graphene is more successful and promising compared to III-As semiconductors. This is mainly because of the high adsorption energy of nitrogen on graphene of (4.6 eV) compared to arsenic or phosphide [55, 56].

An IBM research group demonstrated the QvdWE growth of high-quality GaN on graphene/SiC substrates. The weak vdW forces between GaN and graphene help to reuse an expensive graphene/SiC substrate for multiple transfers and direct bonding to GaN/Si substrate enhanced by atomically smooth-released interface [42]. Compared to the conventional laser lift-off process, this novel technique is more advantageous since the extra surface treatment after releasing GaN layer on graphene is not required for further repetition. In addition, the high roughness of released surfaces out of laser lift-off process does not allow the released layer for direct bonding to other substrates. By using graphene grown on silicon carbide (SiC) substrate, the edged steps on the graphene surface were used to nucleate GaN on the inert graphene (**Figure 7**).

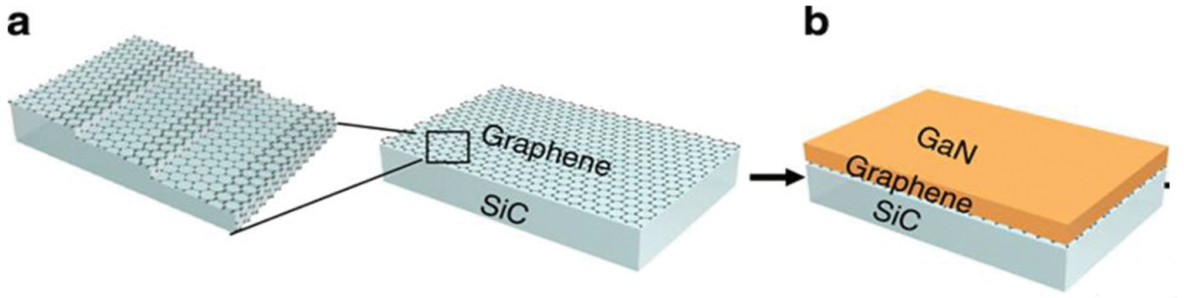


Figure 7. (a) Schematic showing the edged steps on the graphene/SiC surface. (b) Schematic of the final structure after GaN growth on graphene/SiC substrate. Reproduced with permission from Ref. [42].

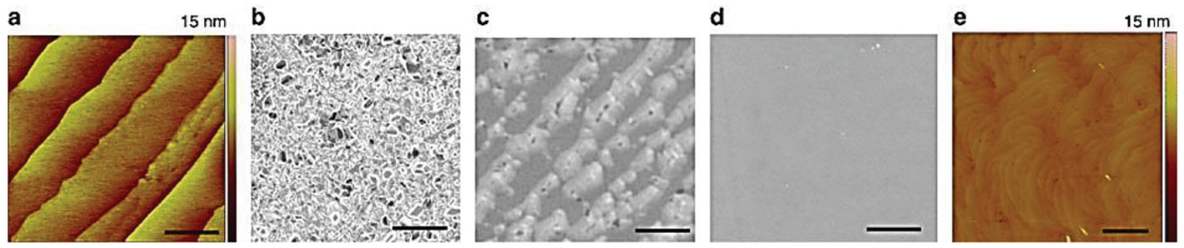


Figure 8. (a) AFM image of graphene/SiC surface. (b) SEM image of GaN films grown on graphene by two-step growth (580 and 1150°C). (c) SEM image of GaN films grown on graphene by one-step growth at 1100°C. (d) SEM image of GaN films grown on graphene by modified two-step growth (1100 and 1250°C). (e) AFM image of GaN films using the modified two-step method with RMS roughness of 3 Å. (scale bar, 10 μm). Reproduced with permission from Ref. [42].

Material	Substrate	Epitaxial mismatch (%)	Threading dislocation density (cm^{-3})	AFM RMS roughness (Å)	XRD (0002) $2\theta/\omega$ scan	
					2θ peak (°)	FWHM (arcsec)
GaN	GaN	0	3×10^6	1.18	34.86	90 [57]
GaN	Al_2O_3	14	9×10^8	1.74	34.54	220 [58, 59]
GaN/AlN	Al_2O_3	14	6×10^8	2.14	34.22	380 [60]
GaN/AlN	Si(111)	17	3×10^9	>6.0	34.56	380 [60, 61]
GaN/AlN	SiC	3	2×10^9	1.80	34.55	200 [62]
GaN	Graphene/SiC	23	1×10^9	2.98	34.57	222 [42]

Note: Reproduced with permission from Ref. [42].

Table 3. Comparison of GaN/graphene crystalline quality to GaN films grown on other substrates.

Direct QvdWE of high-quality single-crystalline GaN on epitaxial graphene/SiC substrates was performed through an optimized two-step growth temperature. Using low nucleation temperature (580°C) will form 3D-faceted GaN clusters while using one-step growth of high temperature (1100°C) will form continuous GaN stripes aligned along the SiC steps. To obtain a smooth GaN surface, the nucleation preferentially formed at 1100°C along the periodic step

edges, that are 5–10 nm height and 5–10 μm apart, then the growth advanced laterally to coalesce at a higher temperature of 1250°C (**Figure 8a–d**). The resulted GaN has a root mean square surface roughness of 3 Å (**Figure 8e**). The average dislocation density of the grown GaN on graphene was reported to be ~1×10^9 cm^{-2}, which is comparable to AlN-buffer-assisted GaN films that were grown on other substrates using MOCVD (**Table 3**).

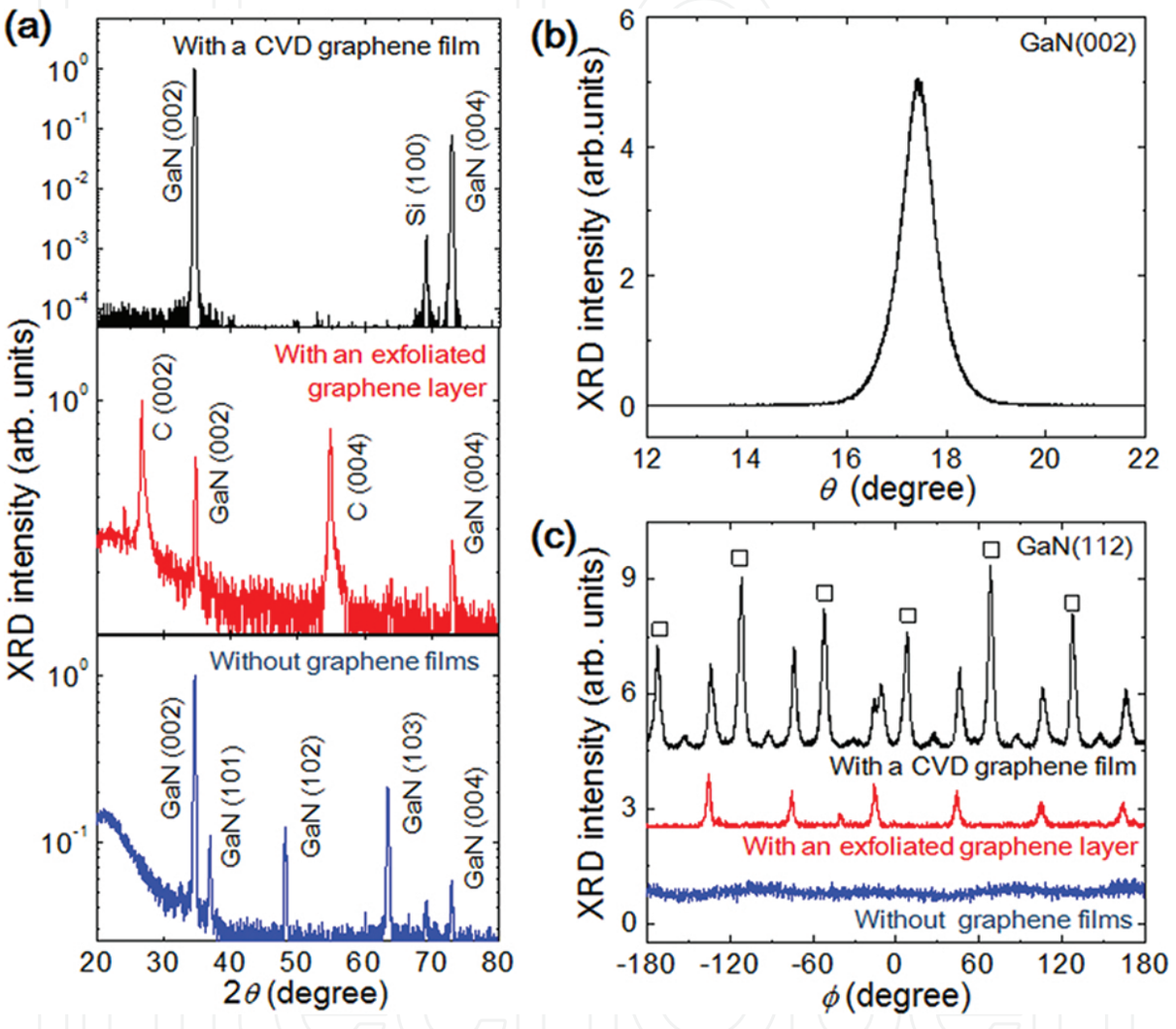


Figure 9. X-ray diffraction (XRD) scans of GaN films grown on (a) CVD graphene/SiO_2 substrates, (b) grown on exfoliated graphene layer/SiO_2 and (c) grown directly on SiO_2. (d) XRD rocking curve of GaN films grown on CVD graphene/SiO_2. (e) ϕ-Scans of GaN films grown on CVD graphene SiO_2, on exfoliated graphene layers/SiO_2, and directly on SiO_2 without graphene layers. Reproduced with permission from Ref. [43].

Chung et al. reported the growth of GaN layer on graphene/fused silica substrate. Compared to the growth of GaN on fused silica directly, GaN grown on graphene using interlayer ZnO nanowalls as a buffer layer showed a significant improvement [43]. To facilitate the growth on graphene, it was exposed to oxygen plasma at 30 W and 100 mT of oxygen for 1 s. This treatment increased the wettability of the graphene surface for a proceeding GaN/ZnO layers. In this study, MOCVD was used to grow ZnO walls first followed by three-step growth of GaN. The

height and density of the ZnO nanowalls were 200–400 nm and 10^{10} cm^2, respectively. The first step of GaN was at a low temperature 560–600°C to prevent the reaction between GaN and underlayer ZnO. Second step was to grow at a higher temperature of 1100°C to promote lateral growth of GaN under hydrogen ambient gas. Finally, the growth at 1200°C was to smoothen the surface and achieve a good-quality GaN layers. The crystal quality of GaN grown on graphene, GaN grown on exfoliated graphene and GaN grown on SiO_2 were examined by XRD. XRD spectra of the GaN/graphene peaks correspond to the (002) and (004) orientations of WZ GaN. However, multiple peaks were observed when no graphene layer was used. For GaN films grown on the substrates with CVD graphene films, the FWHM value of the X-ray diffraction rocking curves was as small as 0.8°, as shown in **Figure 9**.

5. Applications of QvdWE of III/V semiconductors on layered materials

Optoelectronic devices have been fabricated based on the integration of III/V semiconductors on 2D materials [26, 44]. In the following, two examples of such devices are presented. The first is the demonstration of a blue light-emitting diode (LED) in which an IBM group successfully reused the same substrate of graphene/SiC multiple times to grow GaN by depositing a nickel (Ni) stressor on top of the GaN that has stronger adhesion to the GaN than the weak vdW attraction to graphene/SiC substrate [42]. Multiple quantum wells (MQW) of InGaN/GaN sandwiched between p-GaN and n-GaN layers were grown to create to the blue LED device. The transmission electron microscope (TEM) image of the LED stack is shown in **Figure 10**(**a–d**). The *I–V* curve of the device shows a diodic behavior. Moreover, the electroluminescence spectrum confirming the blue emission at 440 nm of the LED is shown in **Figure 10f–g**.

The second application is a solar cell demonstrated by other group used radial and axial junctions of InGaAs/InAs nanowires grown epitaxially on multilayer graphene [63]. This solar cell is based on dense arrays of InGaAs nanowires, where graphene serves as the conductive back contact and growth template for vdW epitaxial assembly of vertical nanowires. In this study, three different junctions are schematically represented in **Figure 11a–c**. The first set shows an axial junction of n-InGAs and p-InGaAs doped by Si and Zn, respectively. The second set is fabricated using radial InGaAs p-n junction. Finally, the third set is same as the second but with a shell of p-GaAs passivation layer. The device contacts are shown in **Figure 11d**. Among the three sets, the last one demonstrates a core-shell p-n junction $In_{0.25}Ga_{0.75}As$ nanowire arrays with conversion efficiency of 2.51%. The figures of merits, such as open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF), the power conversion efficiency (PCE), and the ideality factor (n) for these three sets of devices are summarized in **Table 4**. Radial junction has higher short circuit currents hinting that carriers generated at various lengths along the NW are effectively swept by the p-n junction built-in electric field. Furthermore, the GaAs passivation shell quenched surface defects and the SRH recombination centers.

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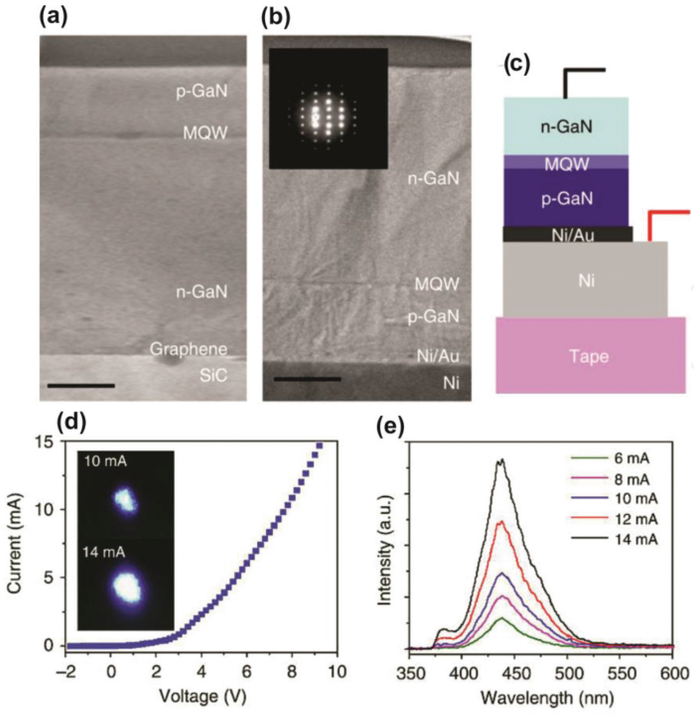

Figure 10. (a) Cross-sectional TEM image shows (p-GaN/MQW/n-GaN) LED stacks grown on a graphene/SiC substrate (scale bar, 1 μm). (b) TEM image of a released LED stack from a graphene/SiC substrate: n-GaN/MQW/p-GaN/Ni. A selected area electron diffraction pattern is displayed in an inset. (c) Schematic of a transferred visible LED device on the tape. (d) I–V curve of a transferred LED stack. (e) Electroluminescence (EL) spectra of a transferred LED stack as a function of injection current. Reproduced with permission from Ref. [42].

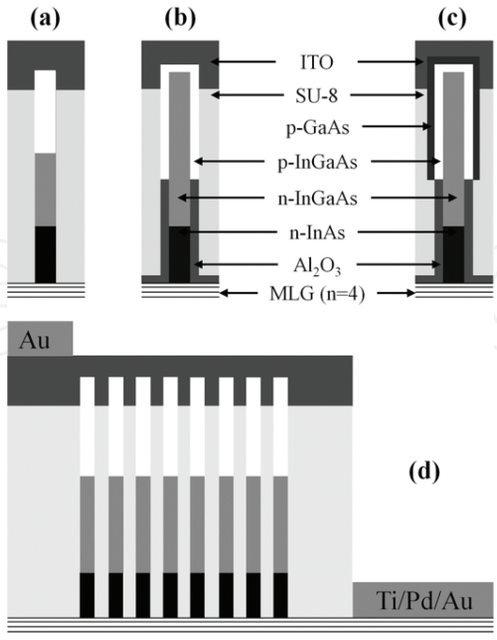

Figure 11. (a–c) Schematic structure of the three different nanowires based solar cell junctions. (d) Schematic structure of the device including the metallic contacts. Reproduced with permission from Ref. [63].

Device group	Device structure	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	PCE (%)	*n*
A	Axial junction	0.18	13.14	38.43	0.91	1.93
B	Radial junction	0.20	16.20	40.24	1.32	1.91
C	Radial junction with passivation	0.26	17.16	55.32	2.51	1.54

Note: Reproduced with permission from Ref. [63].

Table 4. The main performance and figure of merits obtained from the NW array on graphene solar cell presented in this study.

6. Future directions and conclusion

In summary, this chapter has provided a detailed overview of the recent progress of the QvdW heteroepitaxial growth of III–V semiconductors on layered materials. The growth demonstrations of several III–V semiconductors, such as GaAs, GaN, InAs, are mainly included in this chapter. Most of these demonstrations used graphene as a buffer 2D material. Many studies have reported nonplanar nanostructures, for example nanowire arrays, whereas few of them are focused on planar structures, for example thin films. The suitability of such grown structures in various applications in electronics, photonics, and optoelectronics is also discussed in this chapter.

The more versatility of the vdWE over conventional heteroepitaxy is the possibility to achieve epitaxial growth of III–V semiconductors without the strict requirements of lattice matching. On top of that, the idea of vdWE can be applied to rather a wide variety of materials. The materials extend from 1D to 3D and even to organic. In such a way, it is possible to integrate 3D/2D to create new types of junctions. Such inherent features of vdWE could have widespread consequences and real-life applications. These are the reasons why the research area of vdWE is gaining extensive interest recently in the research community.

In spite of great technological advances and efforts, nanostructure-based devices are still suffering from several carrier loss mechanisms, surface-states induced band bending, Fermi level pinning, poor ohmic contacts, and controlled incorporation of *n*- and *p*-type dopants. Due to the poor performance caused by these aforementioned issues, thin films or planar structures are still gaining more attention. In this context, vdWE, historically developed for planar structures, can be a great solution on the way toward successful heteroepitaxial growth on a target substrate. However, the main challenge is the low surface energy of the 2D materials. Therefore, finding a way to increase the wettability and the surface free energy of the 2D materials will make integration much easier in the future.

Although most of the literature studies so far are focusing on using graphene, we consider other 2Ds such as TMDs have the potential to be a good fit for this integration, as long as they are stable at high temperature. The reason is that they have higher surface free energy, can be monolithically integrated at UHV chamber making the interfaces purer from any organics, and

would open a new window for creating new type of junctions between III-V and 2D materials without the need for unpractical transfer processes.

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