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Printing of Fine Metal Electrodes for Organic Thin-Film Transistors

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Additional information is available at the end of the chapter

Abstract

Attributed to the excellent mechanical flexibility and compatibility with low-cost and high-throughput printing processes, the organic thin-film transistor (OTFT) is a promising technology of choice for a wide range of flexible and large-area electronics applications. Among various printing techniques, the drop-on-demand inkjet printing is one of the most versatile ones to form patterned electrodes with the advantages of mask-less patterning, non-contact, low cost, and scalability to large-area manufacturing. However, the limited positional accuracy of the inkjet printer system and the spreading of the ink droplets on the substrate surface, which is influenced by both the ink properties and the substrate surface energy, make it difficult to obtain fine-line morphologies and define the exact channel length as required, especially for relatively narrow-line and short-channel patterns. This chapter introduces the printing of uniform fine silver electrodes and down scaling of the channel length by controlling ink wetting on polymer substrate. All-solution-processed/printable OTFTs with short channels (<20 μm) are also demonstrated by incorporating fine inkjet-printed silver electrodes into a low-voltage (<3 V) OTFT architecture. This work would provide a commercially competitive manufacturing approach to developing printable low-voltage OTFTs for low-power electronics applications.

Keywords: inkjet printing, metal electrodes, thin-film transistors (OTFTs), all-solution-processed, low voltage

1. Introduction

Following the well-known Moore's Law, metal-oxide-semiconductor field-effect transistor (MOSFET) has been the key semiconductor device platform for silicon (Si) microelectronics since the 1960s [1]. In the past few decades, with the significantly growing demand for display-related information exchange, thin-film transistor (TFT) technology for display backplanes has attracted more and more attention [2]. Similar to MOSFET in Si microelectronics, TFT is considered to be a key component for large-area electronics (display included).

According to different semiconductor materials, TFTs can be mainly divided into amorphous Si (a-Si) TFT [3], metal oxide TFT [4], low-temperature poly-silicon (LTPS) TFT [5] and organic TFT (OTFT) [6]. The liquid crystal display (LCD) has been dominated by a-Si TFT since the 1980s [7]. Lately, metal oxide TFT and LTPS TFT have shown great potential for being used in driving organic light emitting diode (OLED) display [8, 9]. Meanwhile, OTFT is becoming another hot topic in both academy and industry due to its potential applications in low-cost, large-area flexible electronics [10].

Compared with strong covalent bonds in inorganic materials, the van der Waals bonds in organic molecules are much weaker, which brings high degree of intrinsic mechanical flexibility in OTFTs [10]. On the other hand, organic materials have the advantages of good molecule-level design flexibility and bio-degradability. More importantly, low cost and low temperature solution-based processes can be used to fabricate OTFTs, such as spin-coating, blade-coating, slot-die coating, spray coating, bar-coating, ink-jet printing, gravure printing, roll-to-roll printing, and so on. The printing processes make OTFTs very competitive due to the advantages of low energy consumption, high throughput, and good customization. Based on different application requirements, OTFTs can be manufactured on arbitrary substrates including flexible plastic, paper, and fabric over large area.

In the past decades, apart from research activities on OTFTs in a variety of global universities, lots of companies including Plastic Logic, Polyera, SmartKem, NeuDrive, and ISORG have also been established for the commercialization of OTFTs. With the continuous development, the reported device performance of OTFTs has been far beyond that of a-Si TFTs, and even close to metal oxide TFTs.

The attractive features of superior intrinsic mechanical flexibility, low-cost printable processes, and sustainable performance improvement for OTFTs make them suitable for being used in applications of ubiquitous sensors [11], digital/analog circuits [12], radio frequency identification (RFID) tags [13], smart memories [14], flexible display backplanes [15], and wearable devices [16].

2. Basics of OTFTs

2.1. Device architecture

OTFTs consist of five parts including substrate, gate (G) electrode, source and drain (S/D) electrodes, gate insulator (GI), and organic semiconductor (OSC). According to different gate

electrode configurations (top-gate and bottom-gate) and S/D electrodes configurations to OSC (bottom-contact for OSC on the S/D electrodes and top-contact for OSC under S/D electrodes), there are four kinds of architectures for OTFTs as shown in **Figure 1**: (a) bottom-gate bottom-contact (BGBC) structure, (b) bottom-gate top-contact (BGTC) structure, (c) top-gate bottom contact (TGBC) structure, and (d) top-gate top-contact (TGTC) structure. In terms of G configuration, bottom-gate architecture has been widely used because gate electrode and GI are prepared before deposition of the organic solvent-sensitive OSC, eliminating the possible degradation in OTFT performance. With the BG architecture, other additional processes applied onto G electrodes and OGI as well as for via holes fabrication can be employed without damage to the OSC [17]. The advantage of top-gate architecture is the ease to pattern high-resolution S/D electrodes and the GI naturally acts as a passivation layer for protecting the OSC underneath. However, the relatively rough upper surface of the OSC, especially for small molecular materials, usually causes degradation in carrier transporting and reduces the OTFT's mobility [18]. Moreover, in order not to damage the OSC when depositing GI, an orthogonal solvent for GI is usually required, which greatly restricts selections of GI materials. In terms of contact, top-contact devices usually show superior performance than bottom-contact counterparts for certain organic semiconductors, which results from reduced contact resistance between the S/D electrodes and OSC due to the increase in charge injection area [19]. Each of these architectures has particular advantages and disadvantages, either in performance or in fabrication. Therefore, the proper structure should be carefully considered, which depends mainly on the actual situation and application.
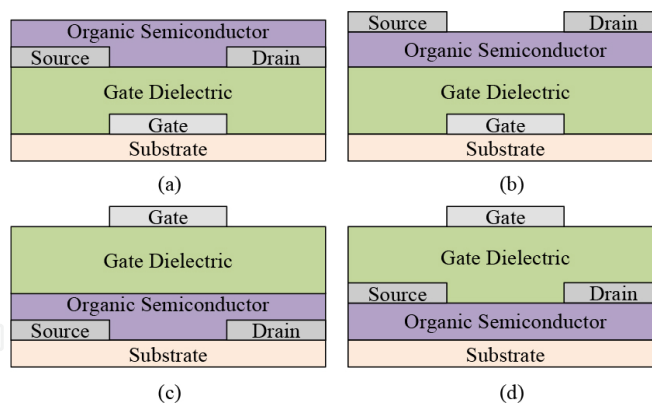

Figure 1. Schematic diagram of the four typical OTFT device structures: (a) bottom-gate bottom-contact, (b) bottom-gate top-contact, (c) top-gate bottom-contact, and (d) top-gate top-contact.

2.2. Work principle

As an active voltage-controlled current source, the conductivity of the channel in the semi-conductor can be modulated by controlling the carrier density in the channel through electric field for a typical field-effect transistor (FET). The representative FETs were metal-oxide-semiconductor field-effect transistors (MOSFETs), where channel conductivity is dependent on the formation of inverse channel. Unlike MOSFETs, semiconductor in OTFTs is a sort of

intrinsic semiconductor without doping, so OTFTs operate in enhancement mode rather than inverse mode. Take p-type BGBC OTFTs as an example, OTFTs can be seen as parallel-plate capacitor. One side of the parallel-plate capacitor is the G electrode and the other side is the semiconductor channel between the S/D electrodes. The density of carriers in the channel is modulated by the voltage of the G electrode (V_{GS}), and the source/drain electrodes inject/collect carrier into/from semiconductor. For p-type semiconductor transporting holes, a negative V_{GS} is needed to generate the corresponding electric field to form the conductive channel. When the V_{GS} hasn't reached the threshold voltage (V_{th}), the drain current (I_D) is usually small enough that can be neglected. It's important to note that the definition of V_{th} in MOSFETs refers to the minimum V_{GS} needed to create an inversion conducting channel between the S/D electrodes. However, there is no inversion in OTFTs, so the definition of V_{th} is not the same as the traditional MOSFETs; however, the V_{th} can also mark the transition of the different regions of operation. When V_{GS} is larger than V_{th}, mobile carriers begin to increase to form the channel layer, as shown in **Figure 2(a)**. If a negative drain source voltage (V_{DS}) is applied, the holes will flow from the source to drain along the channel to generate the I_D in **Figure 2(b)**.
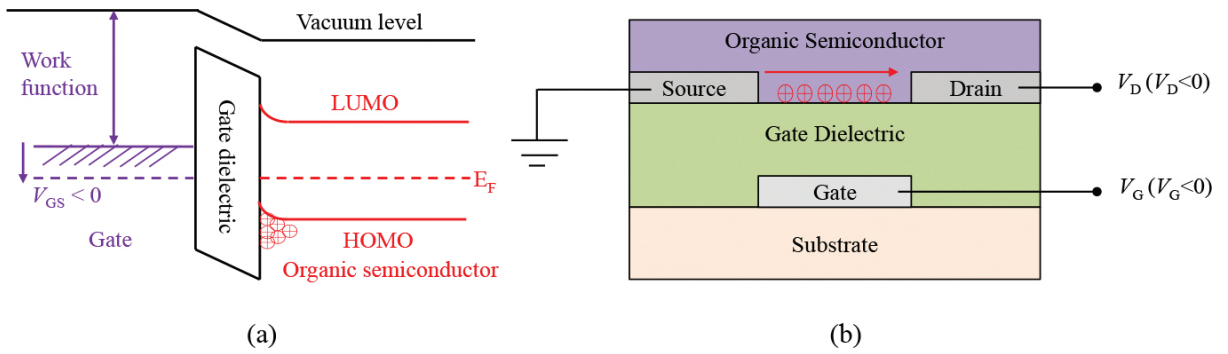

Figure 2. (a) Energy-level diagram of the p-type OTFT with a negative V_{GS} bias. (b) Schematic diagram of working principle for p-type OTFT.

When $|V_{DS}| < |V_{GS}-V_{th}|$, the transistor is turned on and I_D increases linearly as the increase of V_{DS}, and OTFTs operate in the linear region. When $|V_{DS}| \geq |V_{GS}-V_{th}|$, since the channel is cut off by the strong electric field between S/D, I_D is no longer modulated by the V_{DS} and OTFTs operate in the saturated region. The current-voltage characteristics can be described as following [6]:

For $|V_{DS}| < |V_{GS}-V_{th}|$ (linear region)

$$I_D = \mu C_i \frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \tag{1}$$

For $|V_{DS}| \geq |V_{GS}-V_{th}|$ (saturated region)

$$I_D = \frac{1}{2}\mu C_i \frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \qquad (2)$$

where μ is effective mobility, C_i is the gate dielectric capacitance per unit area, W is the channel width and L is the channel length.

2.3. Materials and processes

2.3.1. Organic semiconductor (OSC)

OSC materials can be classified into small molecular and polymer OSC materials based on the chemical structures of molecules, while they are also divided into p-type and n-type OSC materials according to the type of charge carriers. Some representative solution-processable OSC materials commonly used are as follows: 1. p-type small molecular, such as TIPS-pentacene, diF-TES-ADT, and C8-BTBT; 2. p-type polymer, such as poly(3-hexylthiophene-2,5-diyl) (P3HT), indacenodithiophene-co-benzothiadiazole (IDTBT), PCDTPT, and poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophenes) (PBTTT); 3: n-type small molecular, such as C60, NDI3HU-DTYM2, and 6,13-bis((triisopropylsilyl)ethynyl)-5,7,12,14-tetraazapentacene (TIPS-TAP); and 4: n-type polymer OSC materials, such as P(NDI2OD-T2), NDI-Ph, and NDI-DTYA2.

2.3.2. Gate insulator

Dielectric plays an important role in the operation of OTFTs, which is often used for carrier accumulation at the semiconductor/dielectric interface and prevention of the leakage current. The materials available for the GI can be divided into two kinds: organic polymer dielectrics and inorganic dielectrics. The most commonly used organic polymer dielectrics reported in literature are poly (4-vinylphenol) (PVP), polystyrene (PS), poly(vinyl alcohol) (PVA), polymethylmethacrylate (PMMA), poly(vinyl cinnamate) (PVC), poly(vinylidenefluoride-co-trifluoroethylene) (P(VDF-TrFE-CFE)), and CYTOP. Besides, the traditional vacuum or solution-processed inorganic materials can also be used as the GI for OTFTs, such as SiO_2, Al_2O_3, Si_3N_4, HfO_2, TiO_2, and so on.

2.3.3. Gate and source/drain electrodes

Common conductive metals (such as Au, Ag, Cu, and Al) and polymer (such as PEDOT:PSS) can be used for gate (G) electrode in OTFT. Different from G electrode, source/drain (S/D) electrodes, which contact directly with the OSC and are in charge of carrier injection and collection, have great impacts on the OTFTs' performance. In order to reduce contact resistance with the OSC, the work function of S/D electrodes should match with the highest occupied molecular orbital (HOMO) for p-type OSC or lowest unoccupied molecular orbital (LUMO) for n-type OSC. Hence, the S/D electrodes usually choose high work function Au electrode or self-assembled monolayer modified Ag or Cu electrodes. In addition, two-dimension materials such as graphene are also demonstrated as the S/D electrodes of OTFTs.

2.3.4. Basic processes

OTFTs can be fabricated with vacuum deposition process, such as sputter, thermal evaporation, chemical vapor deposition, plasma-enhanced chemical vapor deposition. However, compared with vacuum processes, low-cost solution processes could effectively decrease the fabrication cost of OTFTs. The common solution processes for OTFTs fabrication are drop-casting and spin-coating methods, which are usually used in the laboratory for OSC deposition for their simple processes [20]. A scalable process method called spray-coating is also developed and mostly applied to many kinds of materials for GI and OSC. With the advantage of direct patterning and drop-on-demand, ink-jet printing has gained a lot of attention in fabrication OSC [21] and electrodes [22]. The dip-coating method is very suitable for OSC formation with well-controlled crystallization direction [23]. Some traditional coating methods such as blade-coating and slot-die coating have also been applied into OTFTs' OSC [24]and GI [25] fabrication. Recently, a "solution shearing" method was proposed by Bao's group in Stanford University [26]. In addition, many other large-area printing/coating methods such as gravure printing [27], roll-to-roll printing [28], bar coating [29], and brush coating [30] are also being used for OTFTs' fabrication.

3. Requirements and technical challenges of printed electrodes

Despite its low-cost and simpleness, printing electrodes for OTFT suffer from several technical issues. Integration of printed electrodes in a multi-layered OTFT structure for circuits would be challenging, since poor interfacial contacts and/or intermixing of the printed electrodes with the semiconductor or dielectric layer during the successive layer deposition processes would adversely affect the device performance. Nevertheless, good control of the cross-sectional profile of the printed electrodes and their geometry shapes is also required.

Normally, the request for high uniformity of overlaying layers and the desire to achieve reliable operation in a multi-layer OTFT lead to uniform profile in the cross-section for lower printed electrodes. Otherwise, the fluctuation of lower electrodes' thickness will interfere with the flatness and uniformity associated with overlaying functional layers, resulting in poor yield over large area. Moreover, the fully printed OTFT devices may also suffer breaking down issue arising from the potential leakage due to relatively higher potential for electrical shorts at the abnormal peak point located on the lower electrodes [31]. As such, the issue of "coffee-ring effect" has received considerable critical attention especially when fabricating OTFTs by utilizing inkjet-printed electrodes. Besides the cross-sectional profile, the parallel source/drain electrode pairs need to be of smooth edges in order to ensure a uniform channel length along the whole channel [32].

On the other hand, to meet the intended requirements of high operation frequency (f_T) of organic integrated logic circuits, there is an urgent need to achieve short channels and small parasitic capacitances. From the organic semiconducting material design point of view, great efforts have been given to develop organic semiconductors for printable OTFTs with mobility similar to or even over amorphous silicon a-Si [33–36], mainly taking performance comparable

to that of conventional silicon electronics, that is, usually 100 kHz at a short channel length less than 10 μm, into consideration [37]. However, it is still far from being able to fabricate high-speed OTFT circuits, which are mainly constrained by the limits of device geometry features when using current printing technology. This is because, in fact, f_T is also dominantly dependent on the device geometry features as shown in the following equation: $f_T \approx u_{eff}(V_{GS} - V_{th})/2\pi L (L + 2L_c)$, where u_{eff} is the effective carrier mobility, L is the channel length representing the distance between source and drain electrodes, and L_C is the contact length representing the length of overlap between drain-source electrodes and gate electrode [38]. However, the limited positional accuracy of the inkjet printer system and the complicated dynamics of the inks impacting the substrate surface make it difficult to obtain relatively narrow-line and short-channel patterns as required. It is well known that as the distance between two parallel printed electrodes decreases, the failure probability caused by shorting will significantly increase at the same time. Due to the manufacturing limits subject to currently available printing systems, short channel of less than 10 μm and small overlap length that is less than 5 μm are not practically achievable yet. As a consequence, it is now very challenging to mass-print short TFT channel and precisely align the gate electrodes to source/drain electrodes toward manufacturing fully printed OTFT logic circuits with high operating frequencies.

4. Review of printing methods for metal electrodes in OTFTs

4.1. Gravure printing

Gravure printing is an intaglio printing process with a cylinder, which is engraved with wells. When the cylinder rolls over a passing substrate, the ink is carried from the fountain to the substrate, and the excess is wiped using a doctor blade, leaving the ink pattern on the substrate. Recently gravure printing has received great attention to fabricate printable OTFTs due to advantages such as low cost, high throughput, and high speed [39]. Optimization of the printing parameters has been systematically studied to help well understand the process [40–42] At the same time, the optimization of ink formulations for metal ink, dielectric, and semiconductor was conducted [43], enabling clearer understanding of the gravure process . However, to achieve the high performance OTFT devices, the long channel length (~50 to 100 μm) is a persistent limitation due to the different materials' properties and higher quality requirements [44]. Using a combination of rotogravure and ink-jet printing, Vornbrock et al. fabricated highly scaled gravure-printed OTFTs with channel lengths below 20 μm on plastic substrates, offering the highest switching speeds among fully-printed transistors [45]. Kang et al. [27] further developed a novel large-area femtoliter-scale microgravure printing process for high-speed (MHz) printing pBTTT semiconductor and demonstrated highly scaled (10 μm channel length) bottom-gate OTFTs on flexible plastic substrates. Voigt et al. [46] reported the fabrication of polymer OTFTs by nearly-all gravure printing process on plastic substrates with pre-patterned indium tin oxide source and drain contacts with a high speed. Although the scale and resolution are still the limitations of the gravure compared to the lithography-based

technique, the advantages of high speed and high throughout show huge potential in fabrication of low-cost printable OTFTs.

4.2. Flexography printing

Flexographic printing is a type of transfer printing like a modern version of the letter press. In this printing process, ink may be transferred to an anilox roll with textures to get a specific amount of ink, and then picked out from the anilox roll with the reliefs on the elastic printing plate, followed by printing onto various substrate, including plastic, metal, and paper, using an impression cylinder. This high-throughput, low-cost, and high-speed process is potential for the mass-production of flexible OTFT electronic devices [39]. It is normally combined with other print process to realize roll-to-roll OTFT fabrication. Schmidt et al. [44] combined the flexography with gravure and offset processes to achieve the printing OFET using PEDOT:PSS —source/drain electrodes with a yielded channel length of only 10 μm and realized the fully printed flexible audio system [47, 48]. As another practical application example, Pastorelli et al. [28] demonstrated an electrochromic display cell driven by OTFT with flexography-printed silver source/drain electrodes.

4.3. Screen printing

Screen printing is a printing technique originally applied for art work. It uses a mesh and a blade usually moving across the whole area to fill the open mesh with the ink to print pattern on a substrate. The advantage of this process is obvious: the whole technique is simple and it needs no complex equipment. What's more, the printing speed can be very high and there is no limit on the printing area theoretically and the technique is available for nearly all kinds of conventional flat substrates, such as glass, plastic, or even paper. However, a main problem of this technique for fabricating OTFT is that the thickness of the formed electrodes is dependent on the thickness of the mesh and it is very difficult to be reduced to nanometer level. At the same time, the uniformity of the thickness is also hard to be guaranteed. Thus, screen printing is believed to be unsuitable for OTFT fabrication. Interestingly, a recent work by Peng et al. [49] successfully applied screen printing to form 6μm-thick silver gate and source/drain electrodes to construct high-performance OTFTs on a piece of paper and demonstrated OTFT active-matrix LED array.

4.4. Reverse-offset printing

Reverse-offset printing technology as a type of ink-transfer method is also widely used to fabricate printable OTFTs. Compared with other printing methods, it has higher throughput and the minimum line width and space to about 1 μm can be guaranteed [50]. However, this printing method requires the specific ink formulation to prevent from incomplete and excess printing, impeding the widespread use of the reverse-offset printing for OTFT fabrication. By newly developed silver nanoparticle inks, Fukuda et al. demonstrated printed high-performance OTFT devices with wide reverse-offset printed channel length from 0.6 to 100 μm, enabling a systematic investigation of short-channel effects in printed organic TFT devices.

This scalable, high-resolution printing technique will pave a way to fabricate printed circuits with high integration and fast operation over large area.

4.5. Inkjet printing

Drop-on-demand inkjet printing has emerged as a versatile method of increasing interest to manufacture printable OTFTs, due to advantages such as maskless patterning, non-contact, low cost and scalability to large-area manufacturing [51]. There are an increasing number of published studies that utilize inkjet printing to form source/drain and gate electrodes for OTFT fabrication.

To direct-write these conductive electrodes and interconnects, if necessary, a broad spectrum of ink formulations, including polymer PEDOT:PSS and metal nanoparticle inks are available. Recently printing of metal nanoparticles has attracted increasing attention because they can provide robust, highly conductive patterned S/D electrodes with a low annealing temperature, which is particularly important to fabricate devices on flexible plastic substrates. Wu et al. [52] demonstrated the printing of n-butanethiol-functionalized gold (Au) nanoparticles as source/drain electrodes and fabricated high-mobility ($0.15 \, cm^2V^{-1}s^{-1}$) poly(didodecylquaterthiophene) (PQT-12) OTFTs with no noticeable contact resistance observed. However, the high cost of gold is against the attributes of this otherwise appealing printing approach for low-cost electronic applications. Not surprisingly, the same group then tried to develop silver nano-particles as potentially much lower cost alternatives. They found improved carboxylic acid-stabilized silver nanoparticles represented ideal printable precursors to highly conductive elements for use in low-cost printed OTFT circuits. The printed silver electrode was of high electrical conductivity similar to the vacuum-deposited silver conductor and enabled fabricated OTFTs with an ohmic contact formation as the energetic mismatch issue of silver electrode with PQT-12 semiconductors was addressed via in situ modification of their interfacial properties [53, 54]. These works demonstrated the ease of printed low-cost silver electrodes as conductive elements for high-performance printed OTFTs.

In most cases, a standard inkjet printer produces a line feature size of above 20 μm corresponding to droplet volumes of tens of picoliter (pL), but offers a limited smallest channel length. To overcome the switching speed limitation and fabricate high-speed OTFT circuits, the channel size defined between printed source/drain electrodes needs to reduce, which has been achieved by several methods. Sirringhaus et al. [55] proposed a hybrid approach to creating short channels that range from several micrometers to hundreds of nm with the help of lithographically patterned hydrophobic polyimide banks, or a hydrophobic self-assembled monolayer (SAM) mesa-like structure by e-beam lithography as an alternative [56], or well-defined polymethyl methacrylate (PMMA) trenches with hydrophilic bottom and hydrophobic walls to contain conducting polymer solutions by combination of nanoimprint lithography and inkjet printing [57].

However, the utilization of various high-resolution lithography tools inevitably leads to more processing complexity and increases the production cost. Therefore, a more cost-effective approach was suggested to create sub-micron channels, most of which were focused upon self-aligning printing (SAP). Generally, the SAP technique is based on two-step printing, that is,

printing of a first conductive electrode line, followed by modifying its surface to more hydrophobic either with plasma treatment or with a self-assembled monolayer (SAM) so that it becomes repulsive to the successively deposited inks, and then printing of a second conductive electrode line along the edge of the first electrode, such that the ink droplets self-aligned off the first conductive electrode, forming a submicron gap of <500 nm in between the two printed electrodes [58–61]. Although the SAP method is simpler and capable of creating shorter channel length than the lithography-based technique, it still requires an undesirable intermediate processing step of surface modification for the firstly deposited electrode. Doggart et al. [62] proposed a facile method for printing source and drain electrodes with very reproducible narrow channel length but free of any intermediate processing steps, which is particularly interesting for a fully complete roll-to-roll fabrication process. This is achieved via engineering ink formulated using organoamine as a stabilizer for silver nanoparticles, allowing a hydrophobic boundary around the first-printed electrodes to be formed during the printing process. Then the ink subsequently printed in the vicinity of the original electrode is repelled and self-aligned by this boundary. Despite the sacrifice of creating a narrow channel only as low as 10 μm, this self-alignment–based printing method allows for printed source/drain arrays with a very narrow distribution of channel length. Moreover, this method is very useful for the development of all printed low-cost OTFT devices.

5. Inkjet-printed fine silver electrodes for OTFTs

In the following research, a metal-organic precursor-type ink (Jet-600C, Hisense Electronics, Kunshan, China) was used for the printed electrodes, which contained 15 wt% silver with viscosity of 12 cps and surface tension of 23.5–24 dyne/cm, and was printed with a piezoelectric inkjet printer (Dimatix, DMP 2831) using a 10 pL cartridge. Cross-linked polymer polyvinyl-alcohol (PVA) coated on glass or PEN plastic foil was used for the printing substrate as it not only presented a flat homogeneous surface, but also served as a good gate dielectric material for OTFT fabrication.

The surface roughness of the PVA was exceptionally small with a root mean square (RMS) roughness of about 0.3 nm measured using a BioScope™ Veeco atomic force microscope (AFM), which was the prerequisite to form controllable and even-printed features [22]. Indeed, an ideal circle shape with a uniform diameter was formed in an array of IJP Ag dots as shown in **Figure 3(a)**. When these isolated droplets overlap each other and merge, a track is then formed. However, the final morphologies of the formed Ag tracks are significantly dependent on drop spacing (Ds) (**Figure 3(b)**). To print Ag tracks with smooth edges, Ds is optimized to be smaller than 50 μm to obtain a straight line with a uniform width. Further decrease of Ds results in increase of the line width of the uniform Ag tracks, meaning the narrowest available Ag track is constrained to about 70 μm wide. The uniform IJP Ag electrodes' surface profiles measured by a surface profiler (KLA-Tencor D-120) present a smooth cross-section without any bulges or coffee rings as shown in **Figure 3(c)**.
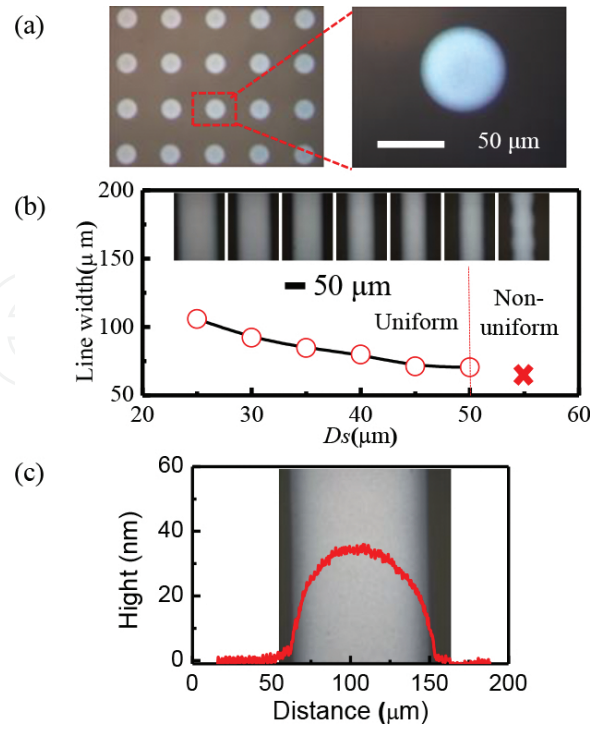
Figure 3. (a) Optical microscopic image of an array of IJP Ag dots. (b) The width of the IJP Ag tracks as a function of the drop spacing (Ds) (inset: the top-view optical microscope image of the IJP Ag tracks and their line width). (c) Top-view optical micrograph image of the printed Ag track by using Ds of 30 μm with the measured surface profile.

The printed electrode width can be described according to the following equation [63]:

$$W = \sqrt{\frac{2\pi d_0^3}{3D_s\left(\dfrac{\theta}{\sin^2\theta} - \dfrac{\cos\theta}{\sin\theta}\right)}}$$

(3)

where d_0 is the ink droplet diameter, Ds is drop spacing and θ is the measured contact angle using the printed ink as the test liquid. This equation indicates that for a given printer cartridge with a fixed d_0, to improve the printing feature resolution, theoretically Ds and θ are the two parameters which can be optimized. However, it is found that to obtain fine uniform tracks with smooth edges and good conductivity, Ds cannot be too small. Then the contact angle turns to be the only alternatively optimized parameter, which is relevant to surface energy of the substrate and also the material ink. An effective method to modulate the surface wettability of the PVA would be using a fluoroalkyl silanes-trichloro(1H,1H,2H,2H-perfluorooctyl)silane (FOTS) self-assembled monolayers (SAMs) [64]. It can be seen that the PVA surface became much less wettable after FOTS modification with the measured water contact angle increasing from 54° to 118° and ink contact angle from 15° to 52°, respectively, as shown in **Figure 4(a)**. The corresponding surface free energy of PVA notably thus reduces from 50.0 mN/m to 10.3 mN/m after modification by FOTS. In this case, the line width of uniform fine Ag tracks could change from about 106 μm for IJP Ag tracks on bare PVA to about 35 μm for those on FOTS-

PVA when an identical D_S of 25 μm is used as shown in **Figure 4(b)**. The reduced spreading behavior of ink droplets on FOTS-PVA mainly attributes to the formation of narrower Ag tracks, demonstrating the feasibility of the developed approach for fabricating narrower fine electrodes (**Figure. 4(c)**).
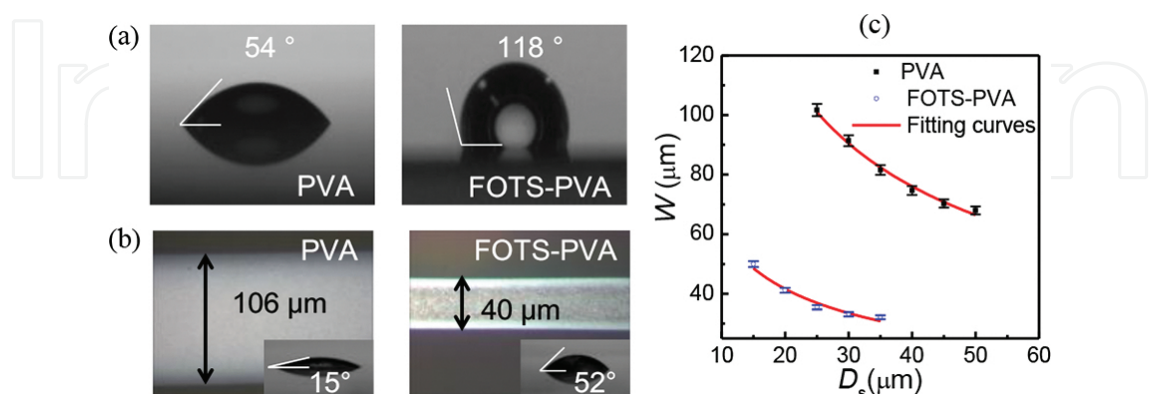

Figure 4. (a) The measured contact angles on bare PVA and FOTS-PVA, respectively. (b) The optical microscopy images of printed Ag lines using a drop spacing (Ds) of 25 μm on PVA and FOTS-PVA, respectively (insets: the measured ink contact angles on the two different surfaces, respectively). (c) The width of the IJP Ag tracks as a function of Ds and the fitting curves.

Then the further challenge would be to form pairs of IJP Ag tracks with small separation for relatively short channels. One reason is due to the limited registration accuracy of common inkjet printer equipment. Another reason is that after the kinetic energy contained in the printed droplet drives it to spread to a certain maximum radius on the substrate, the surface energy of the substrate could finally drive the droplet to recede to a certain radius, which will extend the channel length and also make it difficult to control the channel length [65]. As illustrated in **Figure 5**, the channel length (L) is related to the lateral track spreading width (R) which is dependent of D_S. Thus, to obtain uniform IJP Ag tracks with a short separation, selecting a proper D_S is very crucial.
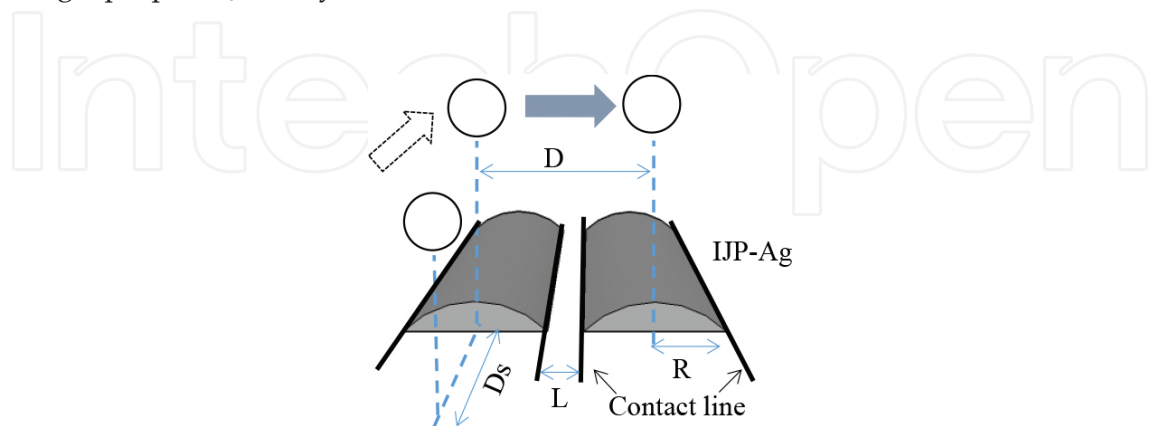

Figure 5. Illustration of the mechanism for inkjet printing uniform electrodes and forming short channels through controlling the ink droplet spreading. Drop spacing (Ds); the track spreading width (R); the moving distance of the printer (D); the channel length (L).

The static contact angle of the Ag ink droplet on the PVA surface is about 11° by the pendant drop method and the receding contact angle approximates zero [22]. These highly hydrophilic properties mean the retraction of the ink droplets is insignificant and the formed tracks are pinned by the contact line (the drop edge) after they monotonously spread to reach the maximum diameter [66, 67]. This surface-energy-limited retracting behavior of inks makes it possible to form the shortest channels at a given moving distance of printer in a controllable manner. By setting a D_S of 45 μm and a printer head moving distance (D) two times of the D_S, formation of parallel S/D electrodes with a separation of about 20 μm was realized with R of about 35 μm as shown in **Figure 6(a)**. To evaluate the process, 100 samples fabricated in arrays were measured with nearly 60% of a gap distance of around 20 μm as shown in **Figure 6(b)**. However, the channel length could be also reduced like the line width by controlling the surface wettability. It has been found that Ag electrodes printed on FOTS-modified PVA are much narrower due to the reduced spreading of inks. Another merit of the formation of narrower Ag tracks on the hydrophobic substrate would be enabling pairs of parallel electrodes to print closer for shorter channel lengths. By setting the printer head moving distance to 50 μm, channels as short as about 15 μm were realized on the FOTS-PVA layer (**Figure 6(c)**), and showed very good yield and uniformity by evaluating 280 test structures (**Figure 6(d)**). Different from utilizing the high-surface-energy-limited "pinning effect" to inhibit retraction after deposition of ink droplets for more wettable surface, the formation of short channels for more unwettable surface instead relies on the low-surface-energy-constrained lateral spreading not only to produce narrower lines but also makes it possible to print two electrodes closer for shorter channels, thus resulting in higher resolution of printing features.
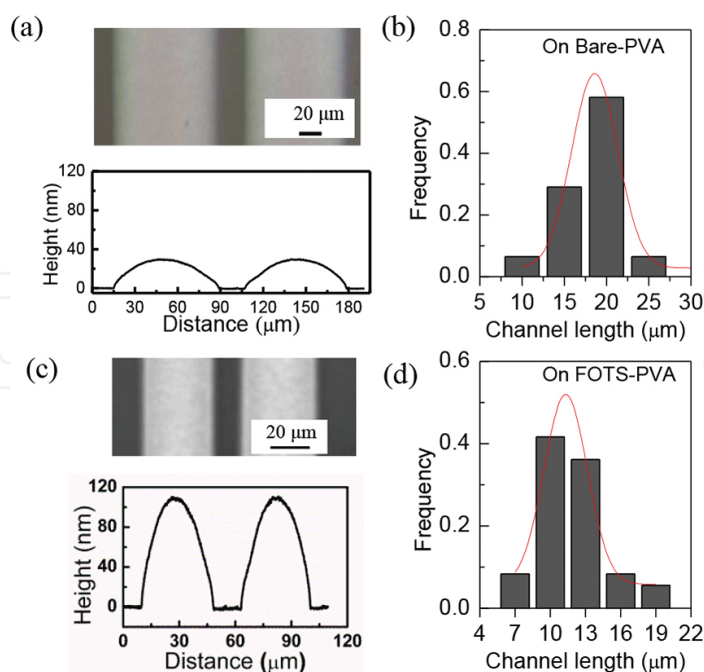

Figure 6. Top-view optical micrograph images of the parallel IJP Ag S/D electrodes and the measured surface profile (a, c) and statistical distributions of the formed channel length (b, d) on PVA and FOTS-PVA substrate, respectively.

Figure 7 shows that the printed Ag electrodes quickly become conductive after 2 min annealing at 150°, a temperature compatible with the PEN plastic substrate. These Ag electrodes have good conductivity calculated with a four-point measurement structure in the range of 5×10^4 S cm^{-1} to 9×10^4 S cm^{-1}. In addition, the electrodes also present a smooth surface (RMS of 1.8 nm) comparable to the thermally evaporated Ag. Combined with uniform morphologies and shapes, these excellent characteristics are attractive for enabling printed electrodes to conduct high current, form good interface, and enable high device performance in practical low-cost OTFT applications.
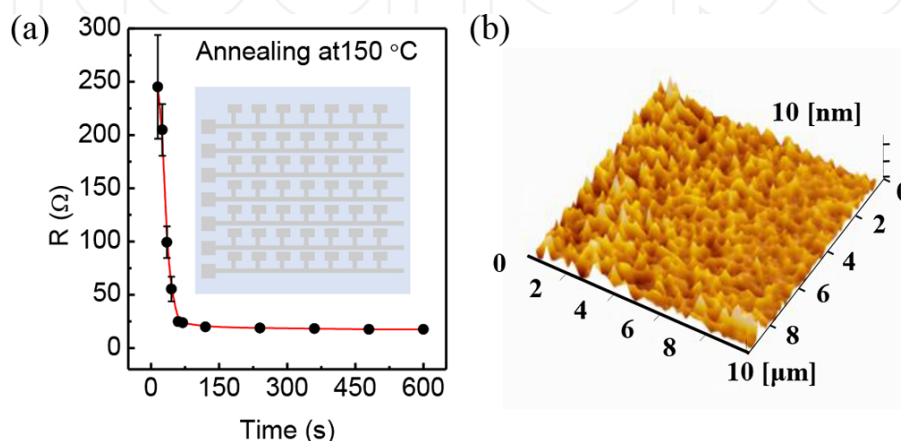

Figure 7. (a) Plot of resistance of printed Ag electrodes versus annealing time at 150° on a hot plate. A four-point measurement structure is also indicated in the inset. (b) Atomic force micrograph (AFM) image of the surface of the inkjet-printed Ag electrodes, with the measured RMS roughness of about 1.8 nm.

The feasibility of printing Ag electrodes enables fabrication of OTFTs by low-cost all-solution or fully-printable processing. Incorporation of fine inkjet-printed silver (IJP Ag) source/drain (S/D) and gate electrodes into recently developed low-voltage OTFT architecture with an ultra-thin high crystalline channel formed by inducing phase separation with the blend of TIPS-pentacene/PS [68], the first demonstration of all-solution-processed low-voltage OTFTs with IJP Ag electrodes was reported [22]. As shown in **Figure 8**, OTFTs present good device performance with a low operation voltage below 2 V, mobility of 0.3 cm^2/V.s, and an ON/OFF current ratio larger than 10^4. It is found that the overlaying dielectric layer was of high quality for low leakage current that was comparable to that in thermally evaporated gate electrode-based OTFTs, thanks to the low flat surface profile of IJP gate electrodes (**Figure 9(a)**). It is also found that the contact resistance extracted according to the transfer line method was about 0.42 MΩ cm, much smaller than that of previously reported BGBC OTFTs, indicating the formation of fine electrode/channel interfaces even with printed Ag electrodes (**Figure 9(b)**). Furthermore, the printed fine Ag electrodes were also incorporated into OTFT logic gate to fabricate all-solution-processed low-voltage inverter on PEN substrate [69]. The demonstrated inverter presents good switching performance with a high dc voltage gain of 67.3 at a supply voltage of about 3 V. It is fair to point out that printing of fine conductive metal electrode and the corresponding low-temperature all-solution-processed device technology is promising for developing low-power fully printable organic-integrated circuits on cheap plastic substrates.
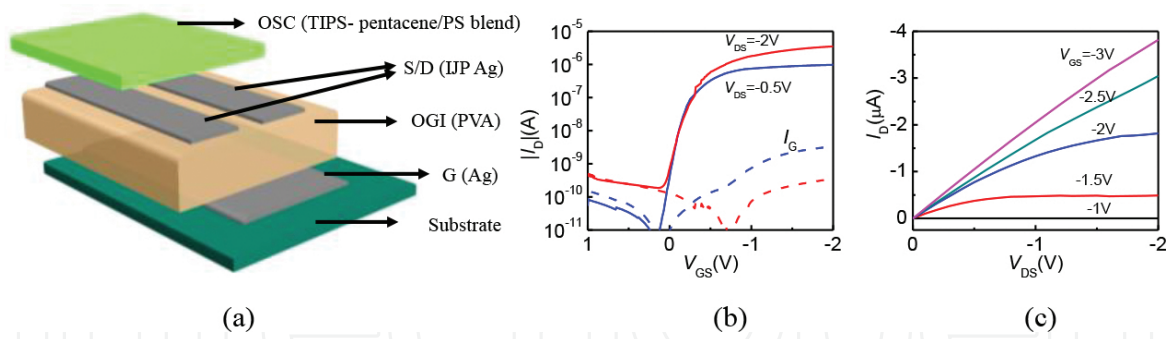
Figure 8. (a) Schematic of the bottom-gate bottom-contact OTFT devices with inkjet-printed silver (IJP Ag) as the gate (G) and source/drain (S/D) electrodes, cross-linked polyvinyl-alcohol (PVA) as the gate dielectric layer, and the blend of TIPS-pentacene/PS is used as the channel. (b) Transfer and (c) output electrical characteristics for the all-solution-processed OTFTs using an IJP Ag gate with a W/L=1200 μm/20 μm [22].
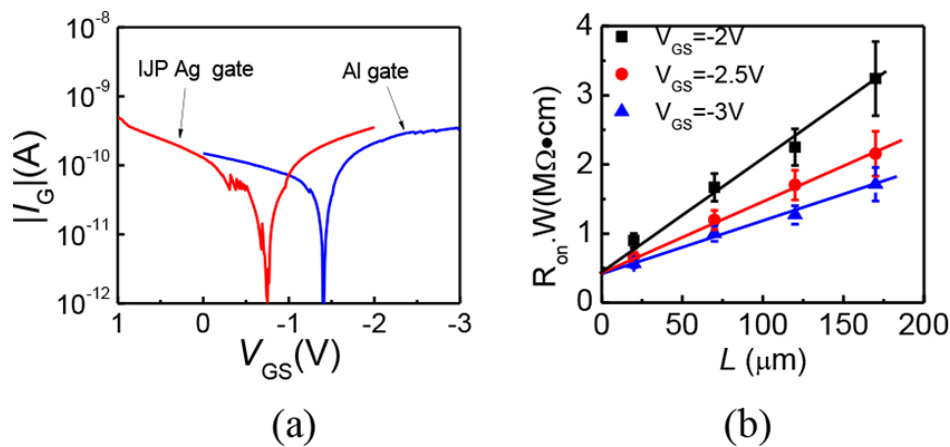

Figure 9. (a) The measured gate leakage current (I_G) as a function of the gate-to-drain bias (V_{GS}) for the Al gate and IJP Ag gate devices. (b) The transmission line method (TLM) results for OTFTs with IJP Ag S/D electrodes to extract the contact resistance [22].

However, since the polar PVA film contains rich hydroxyl groups and tends easily to absorb water from ambience, the unencapsulated OTFT devices present poorer ambient operational and storage stabilities. Moderate gate leakage is also another issue for low-power OTFT circuit applications. To address these issues, PVA dielectric was then replaced by several commercially available low-k polymers. For example, all-solution-processed low-voltage (< 5 V) OTFT was realized by using 1-micrometer-thick (1.16 μm) commercial SU8 photoresist, which presents an ultra-low gate leakage current of less than 1 pA in the whole operation regime and can also well sustain high-voltage (> 40 V) operation [70]. More importantly, it is found that the small dielectric capacitance provides the fabricated device with better power efficiency than conventional low-voltage OTFTs, which is promising for constructing low-voltage power-efficient logic circuits. Alternatively, printable OTFTs using a hydroxyl groups-free PVC gate dielectric present highly stable electrical properties subject to continuously prolonged bias stressing for hours or being shelved for weeks with the channel being exposed to the ambient air [71]. Nevertheless, with these material advancements, such a fully-printable

low-voltage OTFT technology is believed to practically benefit from inkjet printing of fine metal electrodes.

6. Conclusion

In summary, fine Ag electrodes have been obtained by inkjet printing on PVA polymer substrate and incorporated into all-solution-processed OTFTs and circuits. By controlling the surface wettability of the PVA dielectric layer by coating FOTS SAMs, resolution of the printing feature is improved with S/D electrodes as narrow as about 35 μm and channels as short as 15 μm. The printed Ag electrodes present fine morphology, smooth surface, and high electrical conductivity. Based on these Ag electrodes, all-solution-processed/fully printable low-voltage OTFTs and circuits are further demonstrated and presented excellent device performance, indicating the potential of inkjet-printed metal electrodes for the strict requirements of the S/D and gate electrodes for OTFT fabrication. For further development, highly efficient printable OTFTs and low-cost sensors can be achieved by combination of utilization of more reliable gate dielectric materials. Therefore, the developed printable low-voltage OTFT technology would provide a promising platform for developing general low-cost low-power electronics applications.

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