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Innovative Wireless Power Receiver for Inductive Coupling and Magnetic Resonance Applications

Young-Jun Park, Hongjin Kim, Hyung-Gu Park and Kang-Yoon Lee

Additional information is available at the end of the chapter

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Abstract

This chapter presents a wireless power receiver for inductive coupling and magnetic resonance applications. The active rectifier with shared delay-locked loop (DLL) is proposed to achieve the high efficiency for different operation frequencies. In the DC–DC converter, the phase-locked loop is adopted for the constant switching frequency in the process, voltage, and temperature variation to solve the efficiency reduction problem, which results in the heat problem. An automatic mode switching between pulse width modulation and pulse frequency modulation is also adopted for the high efficiency over the wide output power. This chip is implemented using 0.18 μm BCD technology with an active area of 5.0 mm \times 3.5 mm. The maximum efficiency of the active rectifier is 92%, and the maximum efficiency of the DC–DC converter is 92% when the load current is 700 mA.

Keywords: wireless power receiver, high efficiency, active rectifier, DC–DC converter, inductive coupling, magnetic resonance

1. Introduction

In recent years, research on wireless charging system (WCS) has been actively carried out with the rapid development of smartphones and wearable devices. **Figure 1** shows the annual wireless power revenues by application. Since wireless charging techniques are applied not only for consumer electronics or mobile devices, but also for military applications and electric vehicles, the market is predicted to continue to keep expanding to over 11.8 billion dollars by 2020.

Especially, for recent technology such as Internet of Things (IoT), The WCS is essential since sensor and communication functions need to be embedded in a single chip and energy need to be supplied simultaneously, while the user is communicating with other objects.

The remainder of this chapter is organized as follows. In **Section 2**, the WCS is described. **Section 3** provides a description of building blocks including the active rectifier, DC–DC converter, successive approximation register (SAR) ADC, and low drop out (LDO) regulator. **Section 4** shows the experimental results from the implementation of a 0.18 μm BCD, and **Section 5** concludes the chapter.

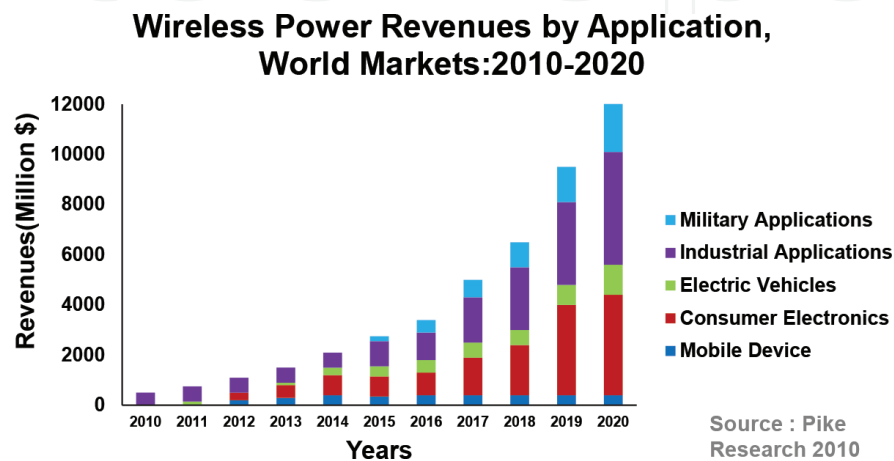


Figure 1. Annual wireless power revenues by application.

2. Wireless power receiver architecture

The WCS involves two major methods: inductive coupling and magnetic resonance. **Table 1** shows the characteristics of these two methods.

The inductive coupling method is used for distance <0.5 cm, and its transfer frequency ranges from 85 to 375 kHz. In-band communication is used for transmitting and receiving packets. This method applies to two standards: Wireless Power Consortium (WPC) and Power Matters Alliance (PMA). **Figure 2a** shows the conventional inductive coupling method WCS structure [1].

Method	Inductive coupling	Magnetic resonance
Power transfer distance	<0.5 cm	>1 cm
Power transfer frequency	85–357 kHz	6.78 MHz
Communication scheme	In-band communication	2.4 GHz BLE communication
Standard	WPC, PMA	A4WP

Table 1. Characteristics of inductive coupling method and magnetic resonance method.

The magnetic resonance method is used for distances over 1.0 cm, and its transfer frequency is 6.78 MHz ISM band. For the communication, 2.4 GHz Bluetooth Low Energy (BLE) communication is used, and the standard is Alliance for Wireless Power (A4WP). **Figure 2b** shows the conventional magnetic resonant method WCS structure [2]. The main differences between the two methods are the frequency and communication scheme, which means the two methods have different types of circuit implementations or issues.

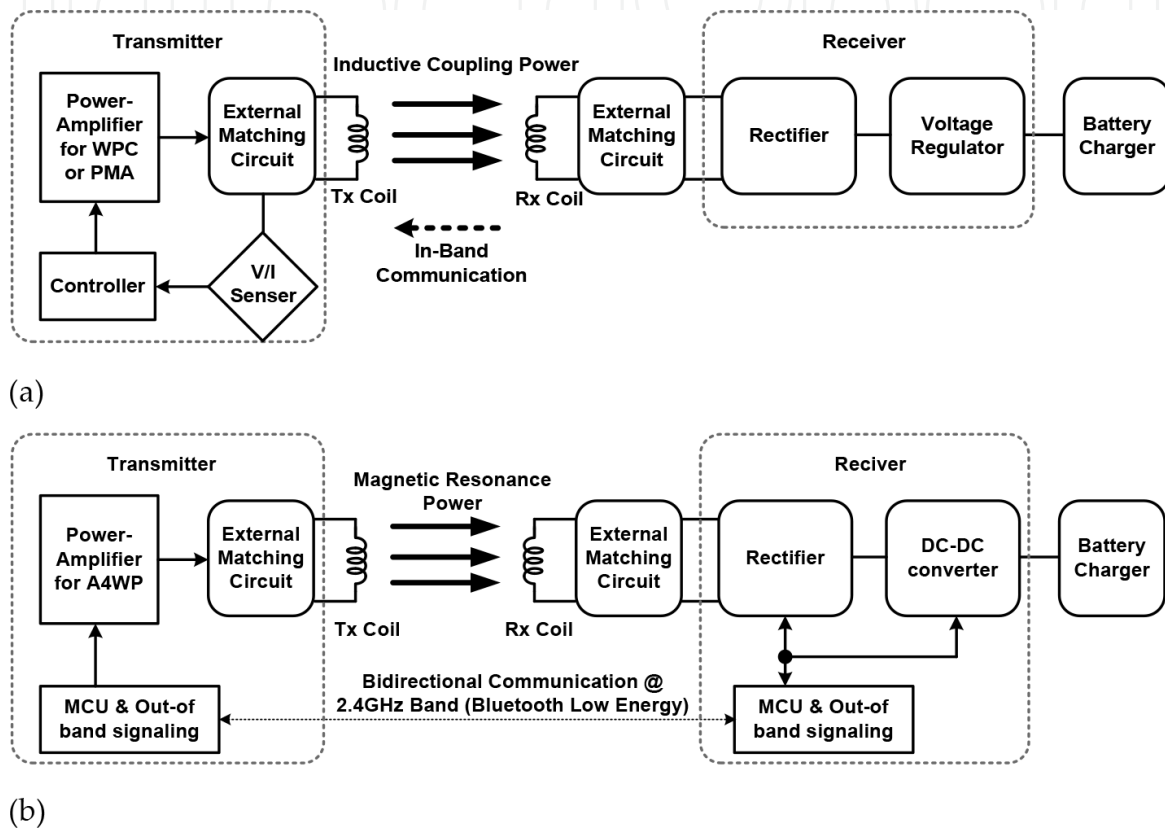


Figure 2. Conventional WCS (a) inductive coupling method (WPC, PMA), (b) magnetic resonance method (A4WP).

The issues of the two different charging methods are as follows. Compared to the inductive coupling method, the magnetic resonance method is a powerful WCS since it maintains high efficiency; even the distance between the transmitter and receiver is significantly more than several meters. However, since the frequency of the magnetic resonance method is 6.78 MHz, enhancing the efficiency of the rectifier (which accounts for the largest portion of the total efficiency of the receiver) is a very challenging task [2, 3].

The switching loss is relatively smaller for the inductive coupling method than that for the magnetic resonance method since its transfer frequency of 100–400 kHz is much lower than that of the magnetic resonance method. Although its charging distance is short, the inductive coupling method can achieve higher receiver efficiency. However, the on-resistance of the active rectifier and reverse leakage current should be minimized to enhance efficiency.

As explained above, the most important issue is the need to maintain high efficiency regardless of which charging method is used because heat from the chip caused by low efficiency will cause various problems. In WCSs, since the input power at the normal operation is above 5 W, the heat caused by the receiver inefficiency further reduces the efficiency of the receiver, which is a catch-22 situation [4, 5].

Figure 3 shows the detailed top block diagram of the receiver for the inductive coupling wireless battery charging system. The AC voltage at the Rx input is converted into a DC voltage by the rectifier. The power efficiency of the rectifier is very critical, as it provides the DC power supply to the following stages [6].

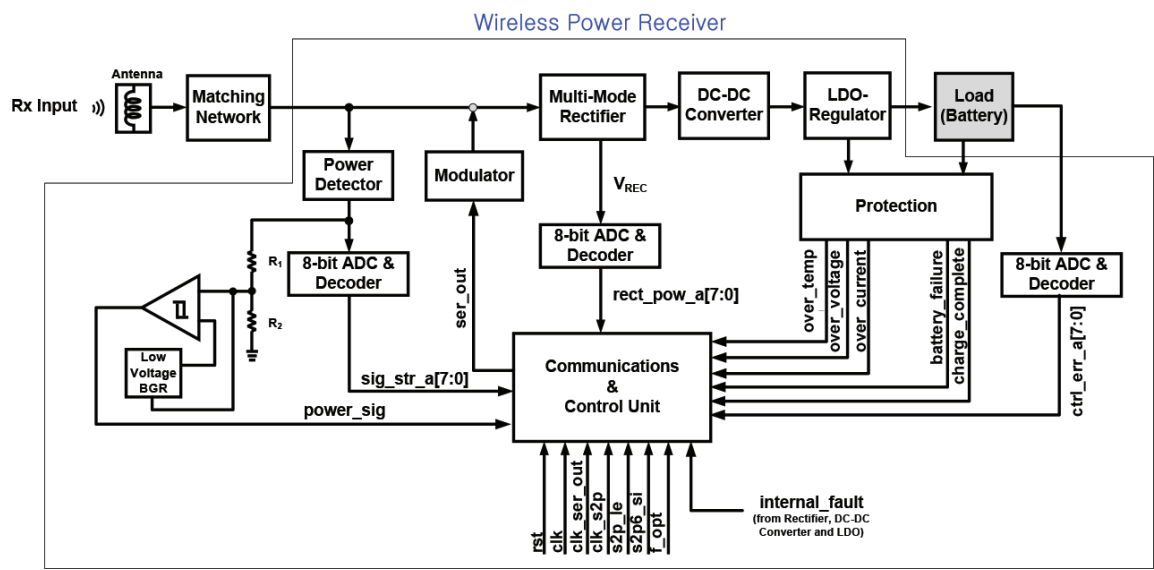


Figure 3. Top block diagram of the inductive coupling wireless power receiver [6].

The output of the multi-mode rectifier is converted into the desired DC voltage level through the DC–DC converter. LDO regulator generates the clean DC voltage required for the Battery. The power level of the input signal is measured at the power detector and converted into the digital code, sig_str_a[7:0], by the 8-bit ADC and decoder. The DC output of the multi-mode rectifier, V_{REC} , is converted into the digital code, rect_pow_a[7:0], by the 8-bit ADC and decoder. The communications and control unit receives various information from other blocks and configures the packet based on them [6].

Figure 4 shows the top block diagram of magnetic resonance wireless power receiver.

Power is transferred from the transmitter to the receiver through the coil and matching networks. The rectifier converts the AC voltage at the receiver input to DC voltage. The output of the rectifier is converted into the desired DC voltage level through the DC–DC converter [5].

The DC output of the rectifier, V_{RECT} , is converted into digital code, by the 10-bit SAR ADC. The output of the ADC is then transferred to the transmitter through the digital control block.

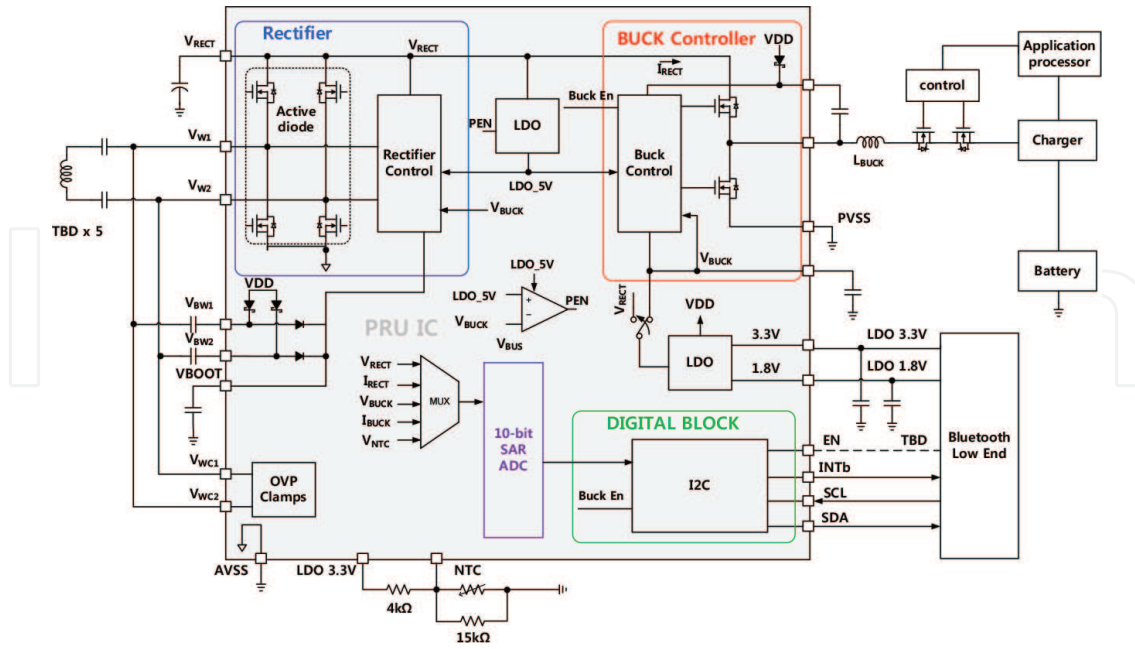


Figure 4. Top block diagram of the magnetic resonance wireless power receiver.

3. Building blocks of wireless power receiver

a. Active rectifier

Eq (1) defines the power conversion efficiency (PCE) of rectifier [7].

$$PCE = \frac{V_{OUT}}{V_{IN}} \times \frac{I_{OUT}}{I_{IN}} \quad (1)$$

$$= \frac{V_{OUT}}{V_{OUT} + V_{LOSS}} \times \frac{I_{OUT}}{I_{IN} + I_{LOSS}}$$

where V_{IN} , V_{OUT} , V_{LOSS} , I_{IN} , I_{OUT} , and I_{LOSS} are the amplitude of the input AC voltage, output DC voltage, voltage drop, input AC current, output DC current, and current loss of the rectifier, respectively.

Figure 5 shows the structure of a conventional passive full-wave rectifier. During the positive half cycle of the supply, diodes D_1 and D_2 conduct in series, while diodes D_3 and D_4 are reverse biased and the current flows through the load. Otherwise, during the negative half cycle of the supply, diodes D_3 and D_4 conduct in series, while diodes D_1 and D_2 are reverse biased. The current flowing through the load is the same direction as that for the positive half cycle of the supply. To generate a steady DC voltage, the load capacitor should be added to the output of the rectifier. The load capacitor converts the full-wave rippled output of the rectifier into a smooth constant DC output voltage.

The conventional rectifier using diodes has frequently been used in many applications since it is simple to implement. However, P-N junction diodes induce large forward voltage drops which directly lead to critical conduction loss. Although Schottky diodes have low dropout voltages, they also have a high leakage current and are not available in most standard CMOS/BCD processes.

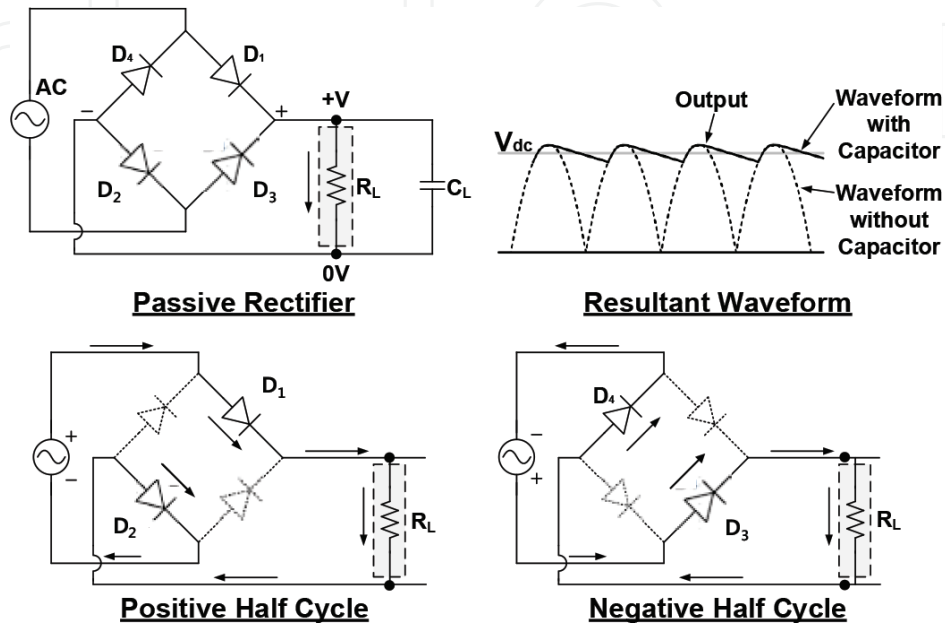


Figure 5. Conventional passive full-wave rectifier.

To address the issues explained above, a full-wave active rectifier which replaces diodes with MOSFETs should be designed. By implementing the active rectifier, voltage drop can be reduced to $2V_{DS}$, which is in the mV range when a single diode forward voltage drop is about 700 mV.

Figure 7a–c shows the active rectifier structures in prior works. Figure 6a shows the p-channel metal-oxide semiconductor (PMOS) diode connection structure with the bootstrap technique. This structure has the critical drawback of considerable conduction loss generated by the threshold voltage of 0.7 V from diode connection structure [8].

In the case of the comparator-based gate control structure shown in Figure 6b, the comparator is used to control a gate signal of active rectifier [8]. Since the delay caused by the comparator cannot be compensated in this structure, reverse leakage current occurs and efficiency is decreased. The structure in Figure 6c includes a zero delay circuit to compensate for the delay of the comparator [9]. The high-side MOSFET of this structure, however, consists of a PMOS cross-coupled structure, so that the size would be extremely large if the same on-resistance was used as that of an n-channel metal-oxide semiconductor (NMOS). As can be seen from the structures of Figure 7a–c, PMOS is used as high-side MOSFET. However, MOSFET involves a break issue since the maximum V_{SG} voltage of PMOS is designated as 5 V in the recent BCD process, which means that high voltage cannot be generated by the rectifier.

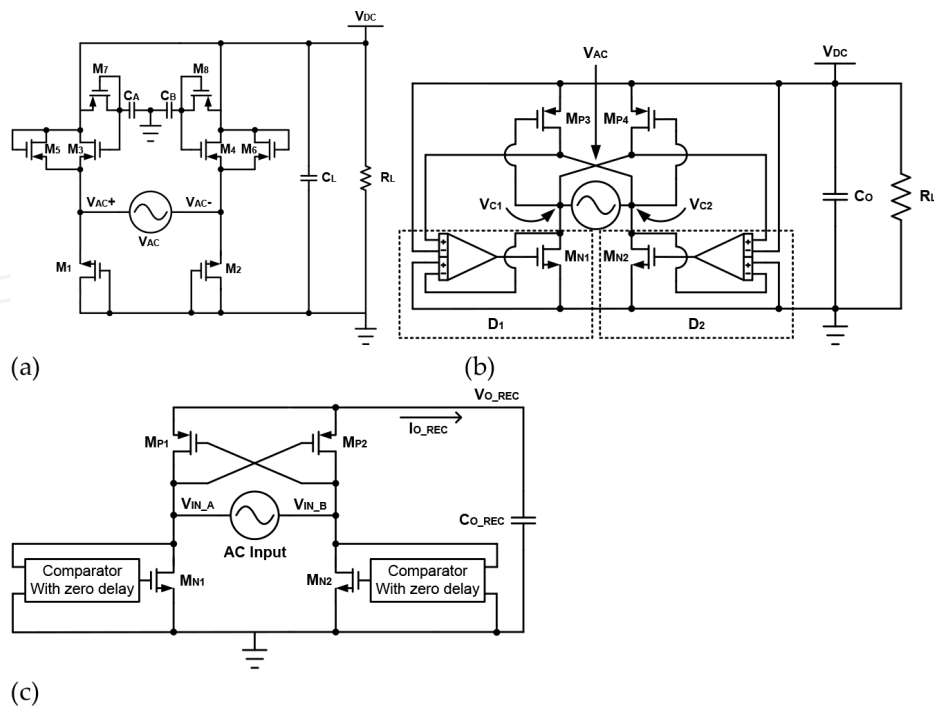


Figure 6. Active rectifier structures in prior works (a) PMOS diode connection structure [8], (b) comparator-based gate control structure [7], and (c) active rectifier with zero delay circuit [9].

A block diagram of the proposed active rectifier is illustrated in **Figure 7**. If a rectifier was implemented with passive diodes, the efficiency would be limited by the forward voltage drop of the passive diodes [5, 7, 10].

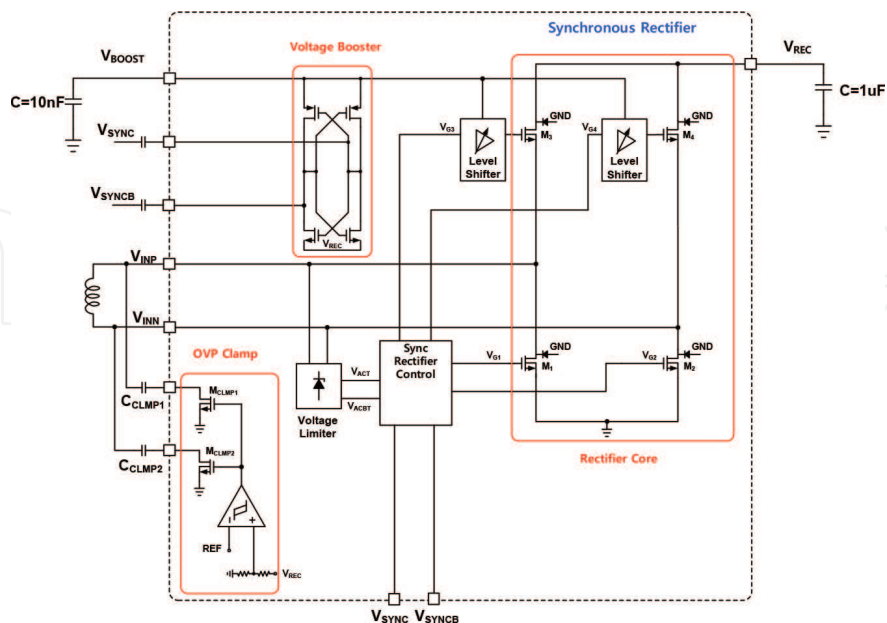


Figure 7. Block diagram of the proposed active rectifier.

In this work, the active rectifier is designed, where the MOS transistors are actively turned on and off depending on the polarity of the received AC input voltage. The voltage drop across the MOS transistors can be made to be significantly less than that of a diode-based passive rectifier, therefore achieving higher-power conversion efficiency [5].

Unlike passive diodes, however, the current flow through the MOS transistors is bidirectional, which means that the current can flow from the DC output to the AC input. This reverse leakage current severely degrades the power conversion efficiency (PCE) [9, 11, 12].

The frequency of the input power is 6.78 MHz for the A4WP standard. A propagation delay of the circuit generates reverse current; it then reduces the PCE. The frequency range of input power according to the WPC standard is from 85 to 205 kHz [1], while that according to the PMA standard is from 277 to 357 kHz [13].

Firstly, in the A4WP mode, DLL operates to maximize the efficiency while the adaptive zero current sensing (AZCS) circuit is off. The proposed active rectifier uses a shared DLL to compensate for the delay caused by the limiter, buffer, and level shifter. By compensating for the delay, the reverse leakage current can be removed while maximizing efficiency.

In the case of wireless charging standards such as WPC or PMA that specify hundreds of kHz frequencies, conduction loss is the most significant factor determining the total efficiency [1]. However, in the A4WP standard where the operating frequency is 6.78 MHz, the switching loss due to the high-voltage MOSFETs drastically increases. In order to reduce the conduction loss, MOSFETs should be designed to be as large as possible to minimize the on resistance [5].

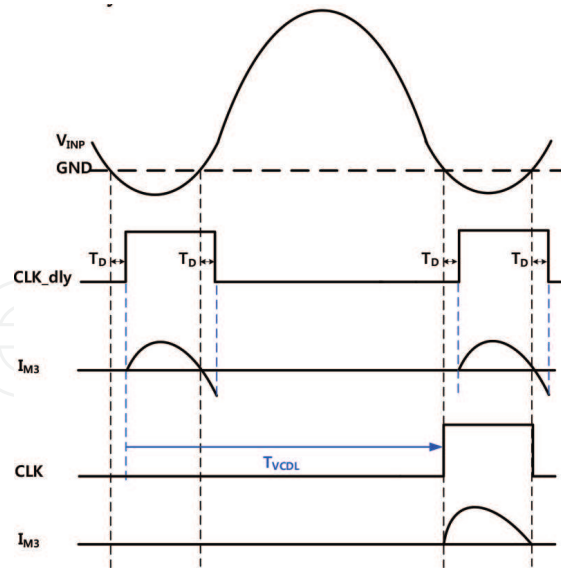


Figure 8. Timing diagram of the active rectifier with DLL.

Secondly, an AZCS is used to define the current path of the input current, I_{AC} . AZCS is only used in the WPC or PMA mode. The WPC and PMA modes do not have a constant frequency; the frequency is changeable. The active rectifier needs to operate switching according to the

input frequency. When the WPC or PMA mode is selected, the DLL circuit is turned off and only the voltage limiter, edge detector, and SR latch are operated.

The timing diagram of the active rectifier with the DLL is illustrated in **Figure 8**. As can be seen in **Figure 8**, the reverse leakage current is mainly due to the finite delay of the limiter, buffer, and level shifter that drive the power MOSFETs, which are large enough to minimize the voltage drop across them. The delayed turn-on of the power MOSFETs is not problematic because it does not cause any reverse leakage current. The delayed turn-off, however, results in reverse current flow which degrades the power conversion efficiency.

The measurement results of the WPR in A4WP mode for the output power of 6 W are shown in **Figure 9a**. The power efficiency of the WPR can be calculated using Eq (2) [5].

$$P_{IN} = \frac{V_{IN_PEAK} \times I_{IN_PEAK}}{2} \times \cos(\theta_V - \theta_I) \quad (2)$$

$$P_{OUT} = V_{BUCK} \times I_{LOAD} \quad (3)$$

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 \quad (4)$$

In Eq (4), V_{IN_PEAK} , I_{IN_PEAK} , θ_V , θ_I , V_{BUCK} , and I_{LOAD} are the input peak voltage, input peak current, phase of input voltage, phase of input current, output voltage of buck DC-DC converter, and load current, respectively.

Figure 9b shows the measured power efficiency of the proposed active rectifier in A4WP mode. When the shared DLL function is used, the maximum efficiency of the active rectifier is 92% in A4WP mode.

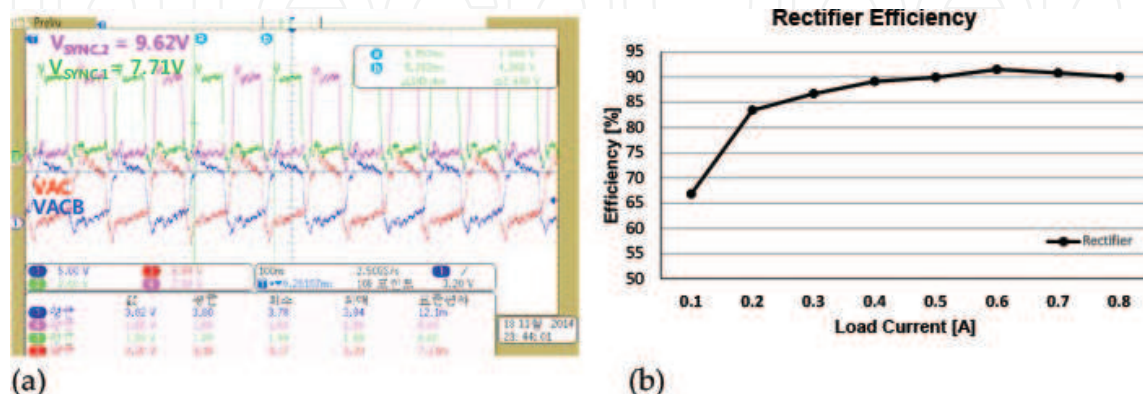


Figure 9. (a) Measured waveform (b) power efficiency of the active rectifier.

b. DC–DC converter

Figure 9 shows the structure of the conventional buck DC–DC converter.

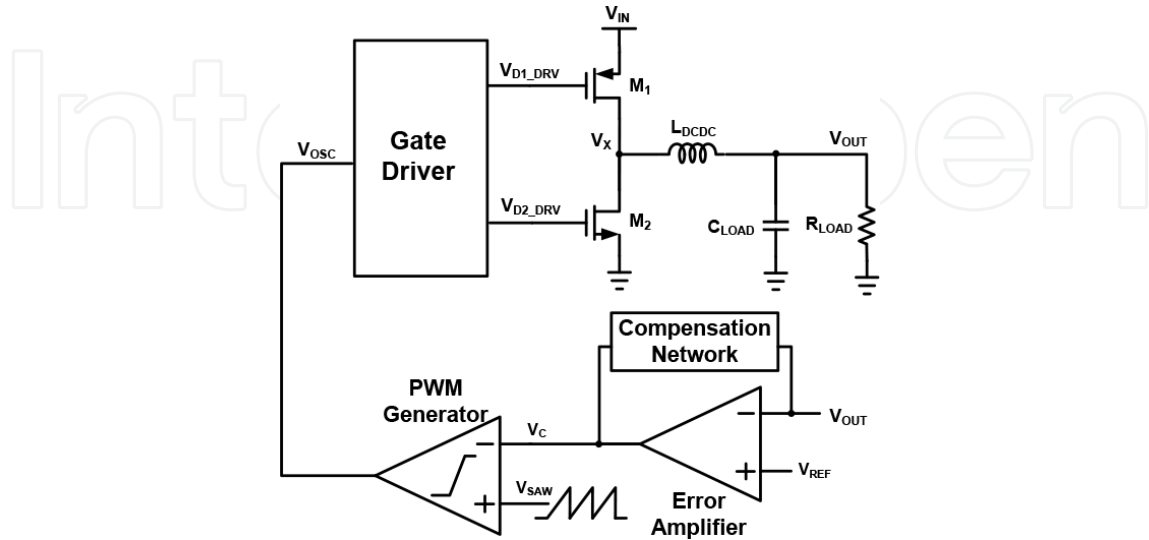


Figure 9. Block diagram of the conventional DC–DC converter.

M_1 energizes the inductor current, while M_2 de-energizes it. Therefore, both energized and de-energized inductor current flow to the load. The PWM generator activates the switch to regulate the outputs. The error amplifier and compensation network generate V_C voltage which is controlled by V_{OUT} voltage. The PWM generator determines the switching threshold by comparing V_{SAW} and V_C voltage. During this process, load current is changed by a feedback loop for DC output voltage [14].

There are several issues with the conventional DC–DC converter. First of all, the efficiency is reduced in the event of PVT variation since the switching frequency is varied. To solve this problem, phase-locked loop (PLL) is set to have a constant switching frequency regardless of PVT variation.

Secondly, the efficiency is reduced in light load condition. One of the drawbacks of the PWM method is a low efficiency in light load conditions. In the PWM method, switching loss is almost the same in the wide load current range because of the fixed switching frequency. In contrast to the PWM method, switching frequency in the PFM method changes in proportion to the load current. By changing the switching frequency, it is possible to reduce the switching loss at low load current conditions. By exploiting the two different methods, the proposed DC–DC converter adopts the PWM method in heavy load condition and adopts the PFM method in light load condition.

Figure 10 shows a block diagram of the proposed DC–DC converter.

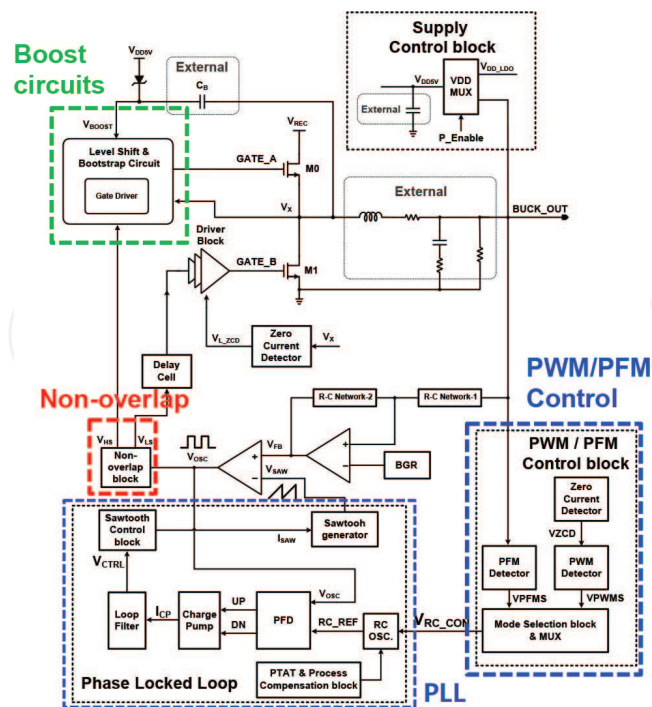


Figure 10. Block diagram of the proposed DC–DC converter.

The proposed DC–DC buck converter adopts a PLL to generate a constant frequency in spite of PVT variation and external circumstances [5].

Figure 11a shows the duty variation of the proposed DC–DC converter. As can be seen from the results, duty is varied by load current. When the load current is 700 mA, duty ratios of GATE_A and GATE_B are 335 ns (67%) and 160 ns (32%), respectively, also with about a 1% non-overlap period.

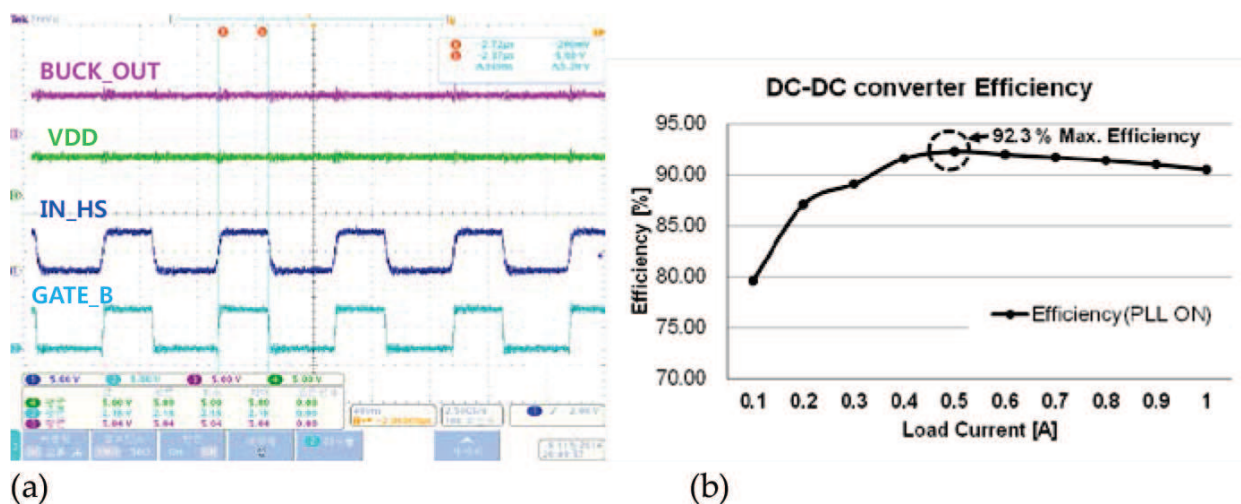


Figure 11. (a) Measured waveforms (b) measured efficiency of proposed DC–DC converter for load current of 700 mA.

Figure 11b shows the measured power efficiency of the proposed DC–DC converter. When the PLL function is used, the maximum efficiency of the DC–DC converter is 92% at the load current of 700 mA.

c. SAR ADC

Figure 12 shows the block diagram of conventional SAR ADC. In the conventional SAR ADC, the capacitance of capacitor digital-to-analog converter (CDAC) is changed and compared to the sampling value, using a binary searching mechanism to define the output code from the most significant bit(MSB) to the least significant bit(LSB).

The capacitor for CDAC should have $2^N C$ capacitance to satisfy the output resolution. This means that size becomes extremely large when designing high-resolution ADCs and the power consumption of the reference generator used as the charging and discharging capacitor increases as a result [15].

Since the proposed dual-sampling SAR ADC structure can be compared to the MSB signal through a sampling process, CDAC can be designed to have $2^{(N-1)}C$ capacitance.

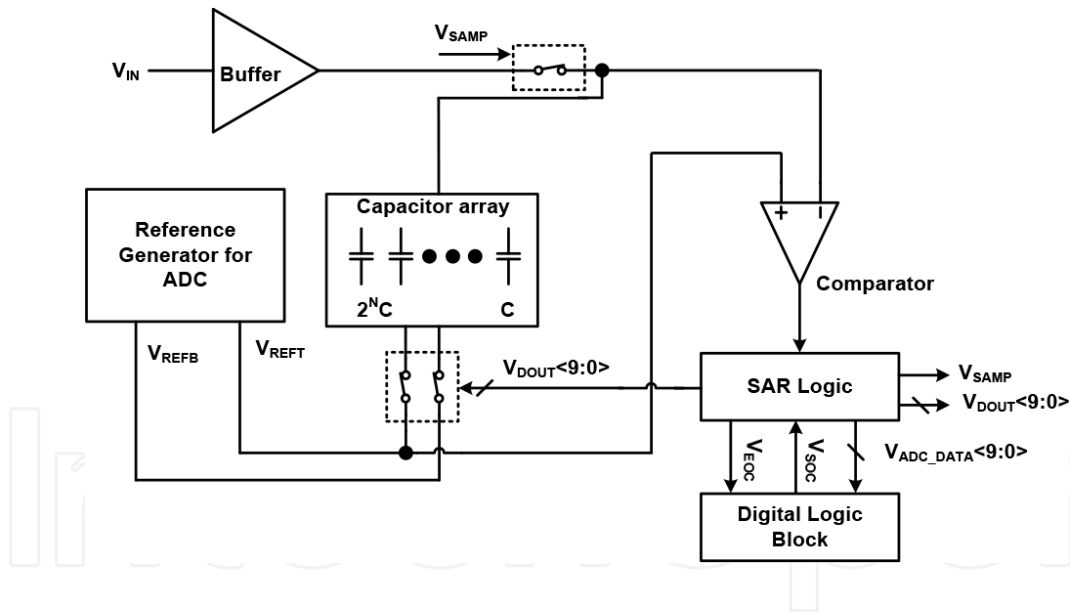


Figure 12. Block diagram of the conventional SAR ADC.

This means that the MSB capacitor can be reduced, and consequently, the size and power consumption can be reduced. Moreover, by adopting the adaptive power control (APC) technique for the comparator, power consumption can be reduced and overall system efficiency can be optimized.

A block diagram of the proposed SAR ADC is presented in **Figure 13** [5]. It consists of a simple analog block, including a DAC, comparator, reference voltage generator, and SAR.

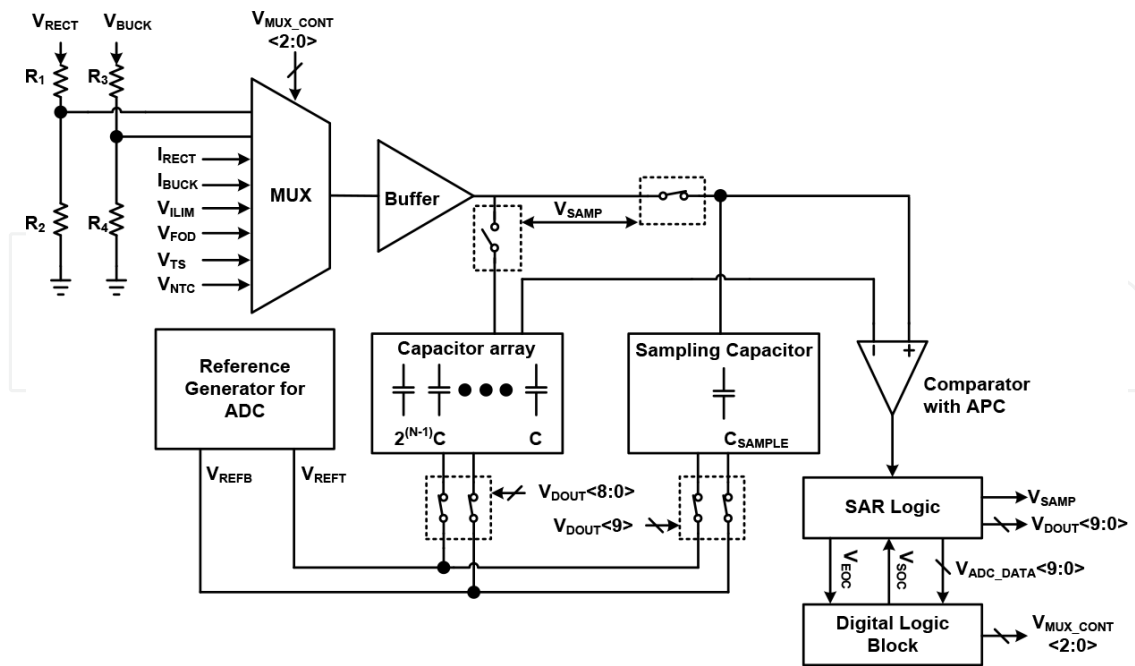


Figure 13. Block diagram of the proposed SAR ADC.

The proposed SAR ADC processes the voltage and current for the rectifier and DC-DC converter as well as information from the temperature sensing block through a MUX.

Figure 14 shows the timing diagram of the proposed SAR ADC.

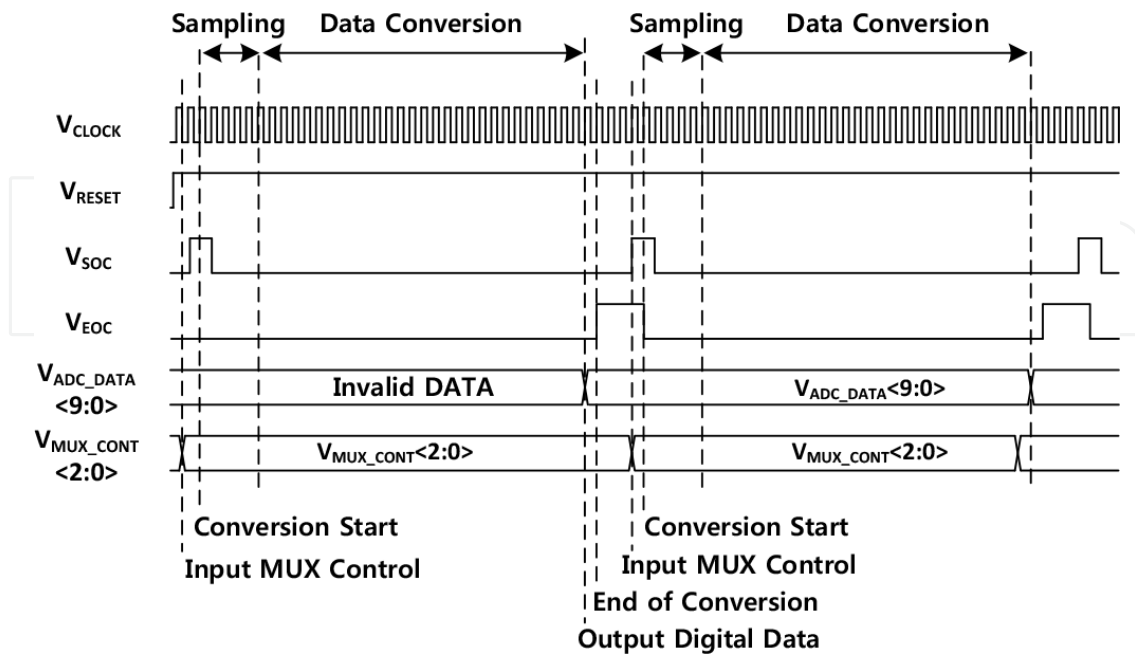


Figure 14. Timing diagram of the proposed SAR ADC.

In the MUX, the selection signal $V_{MUX_CONT<2:0>}$ was composed to save the data and processing during three cycles right after the EOC signal and then controlled by I²C [5].

d. LDO regulator

The input voltage range of conventional LDO regulators is decided by the rated voltage of the components. In general, the rate voltage of CMOS has a maximum of 5 V, so high output voltage from the rectifier cannot be processed. The proposed LDO regulator can operate at high voltage using laterally diffused mOS (LDMOS) as the power MOSFET and the input range of the LDO regulator is increased to a maximum of 20 V by using a high-voltage buffer for efficient driving. Moreover, a capacitor feedback circuit is proposed for power supply rejection ratio (PSRR) and fast settling.

Figure 15 shows a block diagram of the proposed LDO regulator. The output voltage drop due to rapid and large load variation could be minimized with a fast regulation loop.

Application of this fast transient LDO regulator is useful for low noise at wide input ranges and transient response (high voltage at rectifier input).

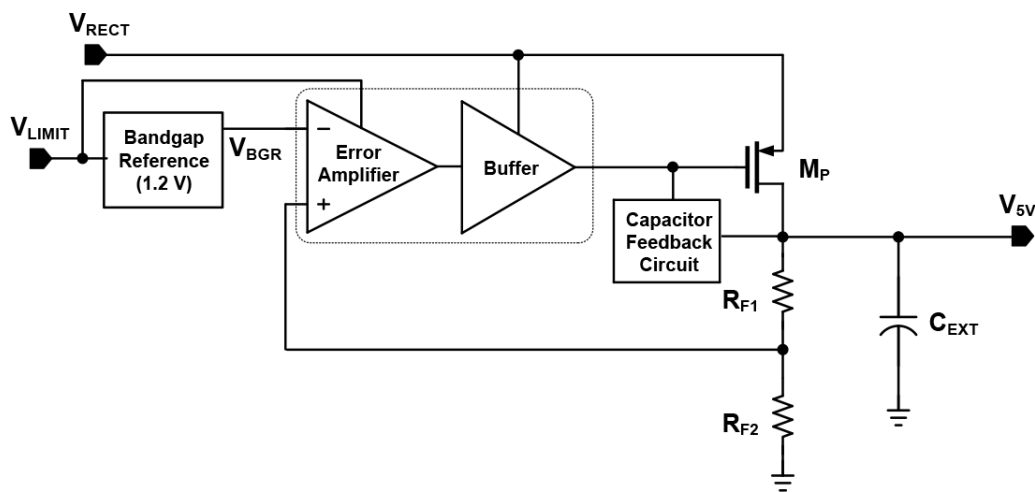


Figure 15. Block diagram of the LDO regulator.

In addition, the push-pull structure of the capacitor feedback circuit can provide a fast path for discharging and charging the gate of the pass transistor, which can respond to transient input with a buffer.

4. Experimental results

The chip was fabricated using the 0.18 μm BCD process with, a single poly layer, four layers of metal, MIM capacitors, and high sheet resistance poly-resistors. The chip microphotograph of the WPR is shown in **Figure 16**. The die area of the WPR is 5.0 mm \times 3.5 mm.

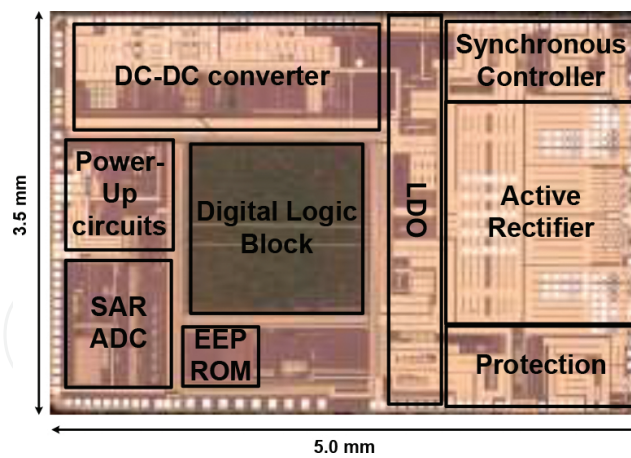
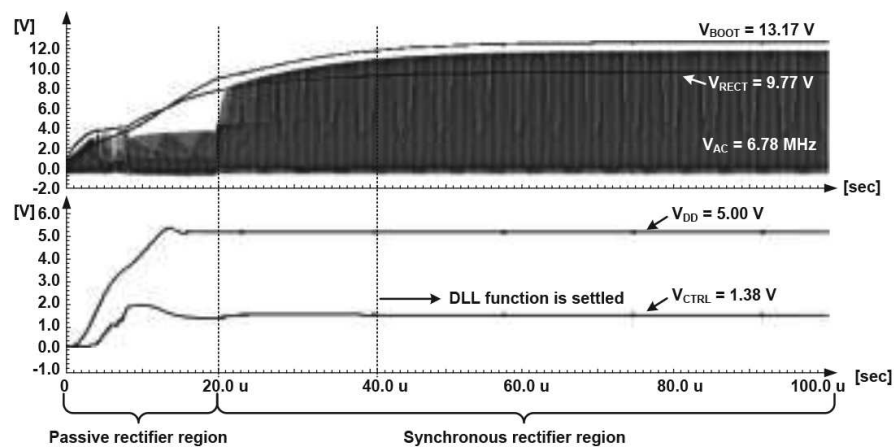
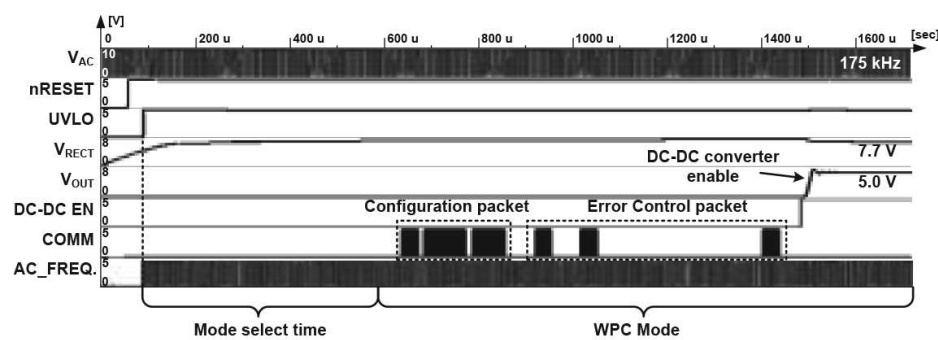


Figure 16. Chip microphotograph of the WPR.

Figure 17a shows the simulation results for the WPR in A4WP mode. Since the voltage for operation of the active rectifier is not generated at initial operation, the rectifier operates with the passive diode from the high-voltage MOSFET.



(a)



(b)

Figure 17. Simulation results of the active rectifier (a) A4WP mode (b)WPC mode.

When the output of the rectifier increases above 5.2 V, the active rectifier also begins to operate without any help from the passive diode [5].

As can be seen from the simulation results, with 7.5 W input and 13.83 Ω output load, a maximum power of 6.9 W and an efficiency of 92% were achieved at the maximum efficiency condition when DLL was locked.

Figure 17b shows the simulation waveform of WPR in WPC mode. WPR is supplied by VAC power, UVLO increases, detecting mode during mode select time. The frequency of VAC is 175 kHz, WPC mode is selected to send not only configuration packets but also error control packets.

The measurement board for the WPR is illustrated in **Figure 18a**. The Tx coil and Rx coil were located at the bottom and top sides, respectively. The power was transferred from the WPT board to the WPR board through the Tx and Rx antenna.

Figure 18b shows the measured system efficiency of the proposed WPR. The maximum system efficiencies are 84 and 86% in A4WP and WPC/PMA modes, respectively.

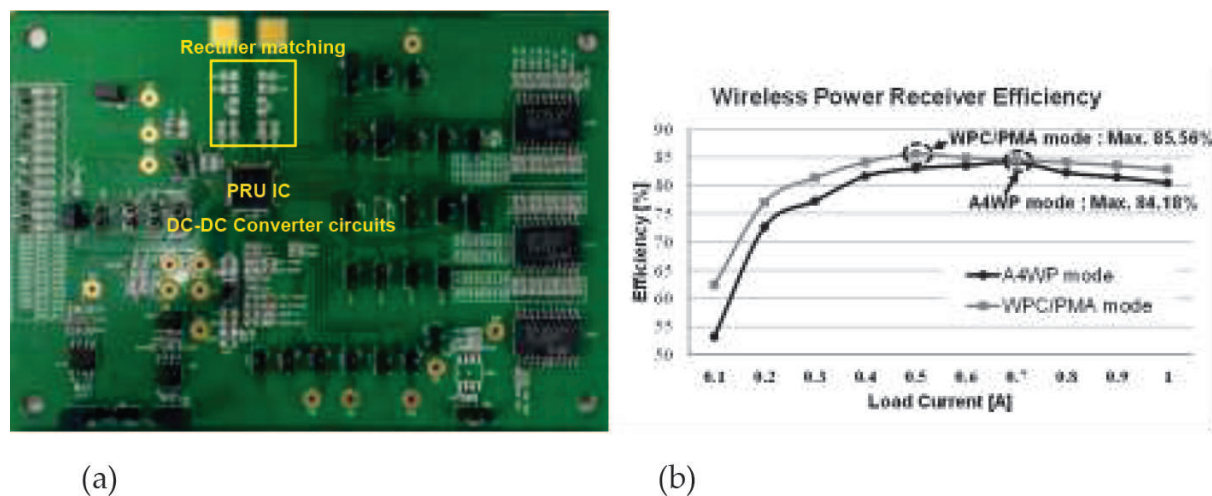


Figure 18. (a) Measurement board and (b) measured system efficiency of the WPR.

The comparison between the reported-related WPRs, and this work is summarized in **Table 2**. As can be seen from **Table 2**, the proposed WPR is the only chip that supports three different types of standards, namely A4WP, WPC, and PMA and shows the highest overall efficiency. Moreover, the results show that the proposed WPR has a wider input voltage range than the other references [2, 9, 16, 17], which is from 3 to 20 V.

5. Conclusion

This chapter presents a WPR for inductive coupling and magnetic resonance applications. Especially for the rectifier, which consumes the most significant portion of overall efficiency,

shared DLL and AZCS structures are proposed to improve the efficiency at different frequencies. In the DC–DC converter, PLL was adopted for a constant switching frequency during PVT variation to solve the efficiency reduction problem, especially due to heat.

References	[2]	[9]	[16]	[17]	This work
Technology	0.35 μm BCD	0.35 μm BCD	0.5 μm CMOS	0.18 μm CMOS	0.18 μm BCD
Supported standard	A4WP	A4WP	–	A4WP	A4WP, WPC/ PMA
Overall system efficiency (%)	86 (Off Chip Rectifier)	75/68	77 (rectifier only)	50	A4WP, 84 WPC/PMA, 86
Power transfer frequency (MHz)	6.78	3.23/6.78	13.56	6.78	6.78, 0.085–0.375
Input voltage range (V)	20	4–8	2.15–3.7	20	3–20
Maximum output power (W)	6	3	0.037	1	10.8
Output voltage (V)	5	5	3.1	3.1	5 or 9
Die area (mm^2)	5.52 (w/o rectifier)	18.3	0.585	6.25	17.5
Maximum output power/die area (W/mm^2)	1.09 (w/o rectifier)	0.16	0.06	0.16	0.62

Table 2. Performance summary of the WPR.

This chip is implemented using 0.18 μm BCD technology with an active area of 5.0 mm \times 3.5 mm. The maximum efficiency of the active rectifier is 92%. The maximum efficiency of the DC–DC converter is 92% when the load current is 700 mA. Total system efficiency for the A4WP mode is a maximum 84% with 700 mA load current. Also, for the WPC/PMA mode, the maximum system efficiency is 86% with 500 mA load current.

In the future, the power conversion efficiency of the WPR needs to be improved since the maximum output power level is increasing more and more. The die area should be minimized for mobile applications at the same time.

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