Chapter 12

Advanced Scanning Tunneling Microscopy for Nanoscale Analysis of Semiconductor Devices

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Additional information is available at the end of the chapter

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Abstract

Significant attention has been addressed to high-spatial resolution analysis of modern sub-100-nm electronic devices to achieve new functions and energy-efficient operations. The chapter presents a review of ongoing research on charge carrier distribution analysis in nanoscale Si devices by using scanning tunneling microscopy (STM) employing advanced operation modes: a gap-modulation method, a molecule-assisted probing method, and a dual-imaging method. The described methods rely on detection and analysis of tunneling current, which is strongly localized within an atomic dimension. Representative examples of applications to nanoscale analysis of Si device cross-sections and nanowires are given. Advantages, difficulties, and limitations of the advanced STM methods are discussed in comparison with other techniques used in a field of device metrology.

Keywords: scanning tunneling microscopy, semiconductor devices, charge carrier distribution, resonant electron tunneling, silicon-on-insulator, photocarrier profiling, fullerene molecule

1. Introduction

Since invention of solid-state electric junctions, charge carrier distribution has become the primary requirement of electronic device design to achieve desirable device performance. Typically, a spatial distribution of charge carriers in semiconductor devices is created by introduction of electronic impurity atoms with particular electron configuration allowing to donate a free electron to the host semiconductor (donor impurity) or to trap a valence electron (acceptor impurity) from the host material. Thus, the host semiconductor with donor impuri-

ty atoms has become a negative-charge (electrons) conductor and is called *n-type*. The host semiconductor with acceptor impurity atoms has become a positive-charge (holes) conductor and is called *p-type*. Typical semiconductor devices have concentration of impurity atoms in a range of 10^{15}–10^{21}/cm^3, which is less than 1 % of total number of atoms. Defects and atom vacancy often behave like impurity atoms.

Early days, charge carrier distribution was derived from spatial distributions of impurity atoms in semiconductor materials. Secondary ion mass spectrometry (SIMS) has been used to obtain a depth distribution profile of impurity atoms in semiconductor materials by sputtering with high-energy ions. As modern high-performance Si devices such as complementary metal-oxide-semiconductor (CMOS) transistors are less than 100 nm in size, and have complex material structures, the 1D SIMS profiling becomes inadequate. **Figure 1** shows a typical structure of a metal-oxide-semiconductor field effect transistor (MOSFET) consisting of gate, channel, and source/drain regions with high impurity concentrations.

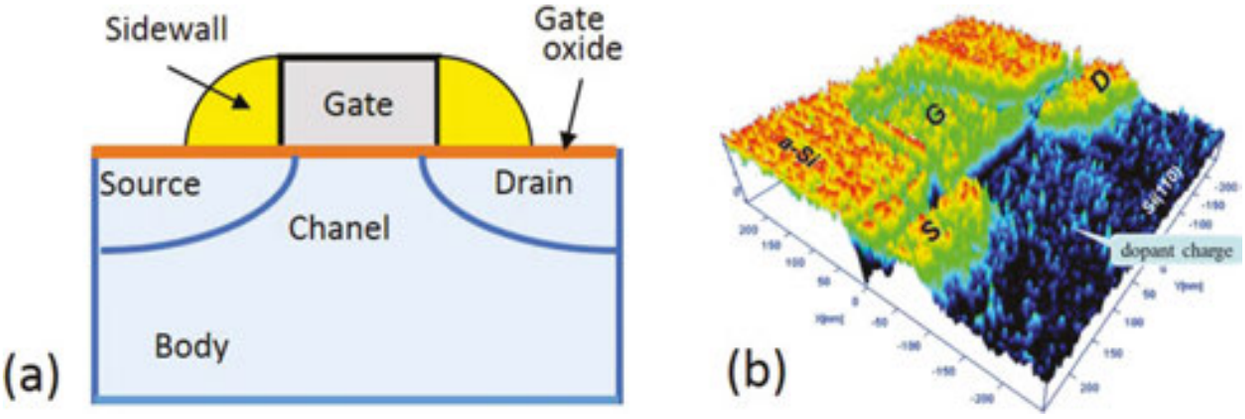

Figure 1. (a) A sketch of a MOSFET device in a cross-section. (b) 3D view of a charge distribution in a MOSFET measured by the STM gap modulation method. Charge concentration is emphasized by color: blue color for low charge concentration in p-Si channel and red color for high charge concentration in source (S), drain (D), and gate (G).

Recently, a new technique of tree-dimensional (3D) atom mapping, which is called atom probe tomography, was introduced based on counting of atom ions ejected from a needle-like device specimen [1–6]. Aside from complexity of the sample preparation and 3D data reconstruction of the atom probe technique, the charge carrier distribution is assumed to be equal to that of impurity atoms. However, the carrier distribution deviates significantly from the impurity atom distribution as a result of internal electric field at material interfaces, trapped charges in oxide, and fractional activation of impurity atoms in areas of high impurity concentration. Therefore, techniques allowing to measure local distribution of charge carriers within the electronic device interior have been a focus of attention from scientific and practical points of view.

Significant attention has been addressed to high-spatial resolution analysis of modern sub-100-nm electronic devices, nanowire devices which meet miniaturization to less than 10 nm in order to achieve new functions and energy-efficient operation. Last decade, various techniques have been developed for charge carrier mapping. A common high-resolution imaging

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technique, scanning electron microscopy (SEM), has been upgraded with an energy-filtering option, allowing us to obtain the image contrast as a function of the surface electrostatic potential [7–10].

Scanning probe techniques are an important tool for local probing of electric properties and have played important roles in scientific research on electronic materials and in evaluations of device structures in fabrication processes. Scanning probe microscopy (SPM) techniques are based on the ability to position a sharp probe electrode in very close proximity with high precision to the sample surface under investigation [11]. Different physical quantities can be measured by the probe including electric tunneling current, atomic and electrostatic forces, or other types of probe-sample interactions. By moving the probe laterally over the sample surface and performing measurements at different locations, two-dimensional distributions of surface atomic structure, electric current, electrostatic potential, or other properties can be obtained.

SPM techniques employed in local electrical measurements are atomic force microscopy with a conductive probe (c-AFM) [12], scanning spreading resistance microscopy (SSRM) [13], scanning Kelvin probe microscopy (SKPM) [14], and scanning tunneling microscopy (STM) [15]. These scanning probe techniques create two-dimensional (2D) maps of variations in the surface electric potential or electric current density along a cross-section of a semiconductor device, when the surface states, defects, adsorbates, and foreign particles on the cross-sectional surface do not affect the initial charge carrier distribution. In majority of cases, certain surface treatments of the cross-sectional surface are applied prior to measurements to eliminate undesirable surface effects. Quantitative impurity profiles by SSRM and SKPM have been demonstrated for high impurity concentrations, where a spatial resolution on the order of the probe tip radius (~5 nm) was obtained under optimum conditions [16–19].

STM has been used for impurity distribution measurements in Si devices by analyzing current-voltage spectra [20–23]. To derive quantitatively variation in the charge carrier distribution from STM measurements, one must analyze complex dependence of the tunneling current on the bias voltage, the tunneling gap, and the band-bending potential beneath the STM probe tip on a semiconductor surface. Thus, simulations of STM operation are an essential part of the data analysis.

In this chapter, we focus on advanced STM-based spectroscopy techniques as nanoscale methods for two-dimensional (2D) charge carrier analysis. It represents original development of scanning probe microscopy methods for Si device metrology with ultimate spatial resolution. We describe the principles of the advanced STM methods and give representative examples of applications to nanoscale analysis of Si CMOS devices and nanowires. Advantages, difficulties, and limitations of the advanced STM modes will be discussed in comparison with other techniques used in a field of device metrology.

The chapter begins with description of device cross-section preparation methods and essential features of STM measurements on a semiconductor surface. Measurement principles of original STM-based techniques and application examples will be given. Current development

in STM simulations will be outlined. Prospects toward research in new 2D materials will be elaborated.

2. Preparation of Si device cross-sections

Figure 2 shows a common way for making solid crystal cross-sections. The process includes a number of steps. (1) Cleavage and/or *dicing* of a thin crystal wafer are used to define a desired location of the cross-sectional plane. (2) *Chemical-mechanical planarization-polishing* (CMP) and focus ion beam (FIB) techniques are applied to tune location of the cross-sectional plane with a sub-micrometer accuracy. (3) Chemical and electric *passivation* of the cross-sectional Si surface by hydrogenation or thin oxide is carried out to prevent distortion of original charge carrier distributions by surface states and contamination.

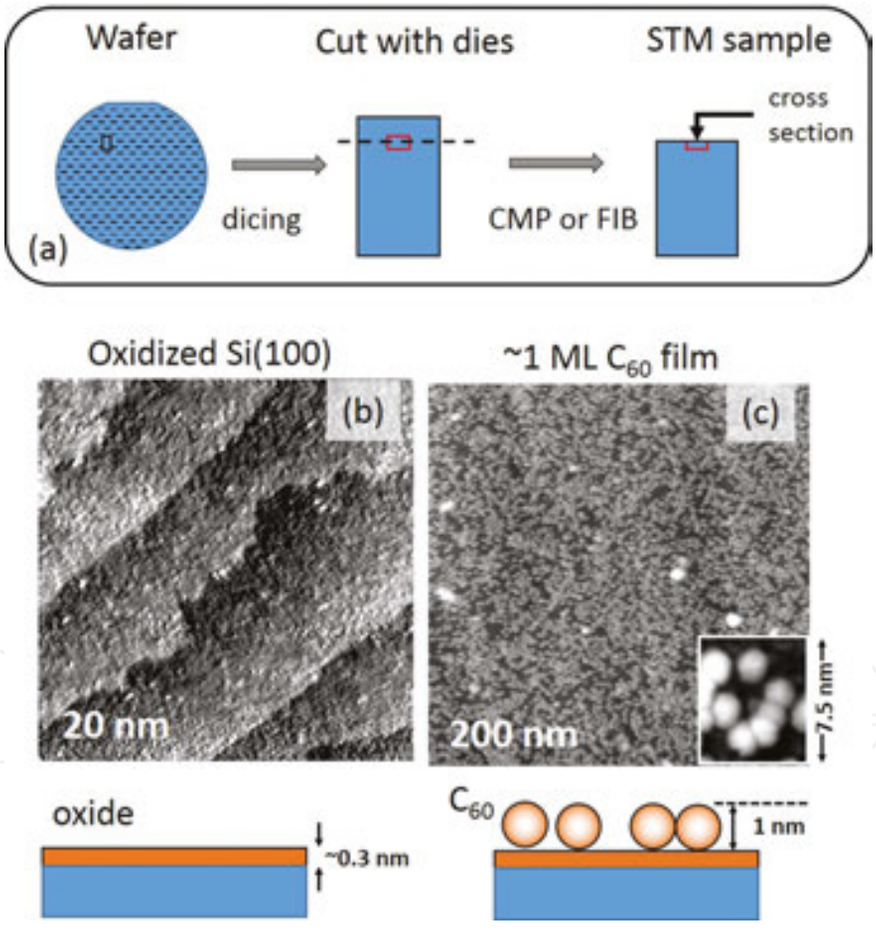

Figure 2. (a) Fabrication of a device cross-section for STM measurements. (b)–(c) STM images (a set-point: 300 pA, 2.0 V) of an oxide-passivated Si surface before (b) and after (c) 1 ML C_{60} film formation. Color scale is 0.8 nm (b) and 2.5 nm (c). Insert shows an image of 10 C_{60} molecules.

Chemical and electric passivation of solid surfaces is the subject of extended research in catalysis to control on charge transfer process and chemical reactions in solid-liquid and solid-

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gas interfaces [24]. Moreover, chemical and electric passivation of semiconductor surfaces are a basic process in fabrication of modern Si devices, enabling to reduce off-state leakage current and photocarrier losses in solar cells [25]. Without passivation treatment, silicon surfaces have pronounced bands of surface states, which dominate the contrast of the STM images, so that it becomes difficult to characterize the underlying electrical interfaces. Therefore, passivation of Si surfaces by hydrogenation or oxidation has been employed in order to reproducibly prepare uniform surfaces of device cross-sections and to obtain very low density of surface states.

2.1. Passivation by hydrogenation

Hydrogenation of Si surfaces is achieved by etching in fluoric acid solutions. Etching removes the native Si oxide and terminates the Si dangling bonds with hydrogen atoms making a stable, passivated surface with very low density of surface states in the Si band gap [26]. A number of investigations have confirmed that tunneling spectra of such stabilized Si surfaces show variation with dopant type and concentration due to passivation of dangling bond states and the suppression of surface states [27–32].

Si(111) surfaces can be atomically flattened by wet treatment in NH_4F aqueous solutions [33]. In the procedure, the samples were dipped in a 5% HF solution to remove the residual oxide layer, then immersed in a 40% NH_4F solution at room temperature, and rinsed in ultrapure water for 1 min. This treatment renders the Si surface mono-hydride, well suited for STM analysis. In this treatment, hydrogen also reacts with near-surface impurity atoms forming electrically inactive complexes, thus, changing the initial charge distribution. To reactivate the impurity atoms, heating of the samples around 200–250°C is necessary [33, 34].

To prepare atomically flat Si(001) surfaces, a combined process is adopted, which consists of wet treatment using a fluoric acid solution and subsequent annealing in H_2 atmosphere at ~600°C and a pressure of ~2×10^3 Pa [35]. The authors showed the formation of an atomically flat Si(001) surface that have well-ordered step-terrace structures in the active device area. The flattening was attributed to the enhanced migration of Si atoms when anisotropic etching was suppressed.

2.2. Passivation by an ultrathin oxide

Hydrogenation of Si surfaces may not always be compatible with processing steps in a particular application, as Si surface etching usually introduces topographic contrast due to etching rate dependence on doping concentration, crystal orientation, and material composition. An alternative way to passivate Si surface is oxidation. The passivation of Si surfaces by controlled growth of ultra-thin oxide layer relies on the layer-by-layer oxidation kinetics at low oxygen pressure [36–38]. We adopted the preparation of cross-sectional surfaces of Si devices as follows [39, 40]. First, dicing and ultra-fine polishing are used to expose either (100) or (110) surfaces of the device. The polished surfaces are cleaned by few cycles of etching in dilute fluoric acid solution and wet-oxidation in H_2SO_4:H_2O_2 (3:1) solution to remove a damage layer. Finally, ultra-thin (~0.3 nm) oxide layer is grown at ~600°C under an O_2 pressure of 3 ×

10^{-3} Pa following etch-cleaning in HF:HCl (1:19). This procedure left a flat surface without any ordered structure as seen in **Figure 2(b)**, where the atomically flat terraces are separated by atomic steps of 0.24–0.27 nm in height. The oxide thickness was 0.32–0.35 nm as determined by x-ray photoelectron spectroscopy, and by scanning reflection electron microscopy (SREM). The low-pressure oxidation process results in a residual density of surface state traps of ~10^{12} cm^{-2} for Si(100) surfaces [24, 41, 42], which is suitable for STM spectroscopy analysis.

2.3. Formation of C_{60} monolayer films

When a well-defined mono-molecular layer is prepared on a passivated surface, its molecular level can be utilized to quantitatively analyze the electrical properties of the underlying substrate. We call this method as a molecule-assisted spectroscopy. For this purpose, mono-molecular thick films of C_{60} (fullerene) were formed by vapor sublimation of C_{60} to the oxidized Si surfaces to a thickness of 3–5 molecular layers. The excess of C_{60} layers was removed by sample heating at 170–190°C for 10 min. Because electrostatic interaction between the molecule and the underlying Si is stronger than the Van der Waals interaction between molecules within the film, a C_{60} molecules adjacent to the Si surface remain at high coverage (~80%) as seen in **Figure 2(c)** [41].

3. Tunneling microscopy: basics

The STM operation principle is based on quantum mechanical phenomenon—electron tunneling through a potential barrier formed by a gap between the outermost atoms on the metal tip and the sample. When the gap is about 1 nm or less, electrons from the STM tip can penetrate into the sample with certain probability owing to the wave nature of the quantum particle.

Under external electric field, electron tunneling creates a measurable electric current, the tunneling current. In the single particle approximation, the tunneling current density is given by a difference in the particle flow across the gap from the STM tip and that from the semi-conductor and is expressed as an integral over particle's energy

$$J_{tun} = J_{\rightarrow} - J_{\leftarrow} = \int_0^{\infty} \rho_{tip}(E) \cdot f(E) \cdot \rho_{sample}\left(qV_{gap} - E\right) \cdot \left[1 - f\left(qV_{gap} - E\right)\right] \cdot T\left(Z, E, V_{gap}\right) dE, \quad (1)$$

where $T(Z, E, V)$, the transmission factor, is a function of gap width (Z), electron energy (E), and external gap voltage (V_{gap}). $\rho_{tip}(E)$ and $\rho_{sample}(E)$ are the density of electron states at the surface of the STM tip and the sample, respectively. $f(E)$ is the Fermi function describing which energy states are occupied with electrons.

Here, we outline the important features of the STM technique essential for analysis of charge carrier distribution in semiconductors. They are

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- tunneling barrier shape,
- sharing of applied voltage between the tunnel gap and a surface band-bending region, and
- surface charge density in the semiconductor beneath the STM probe electrode.

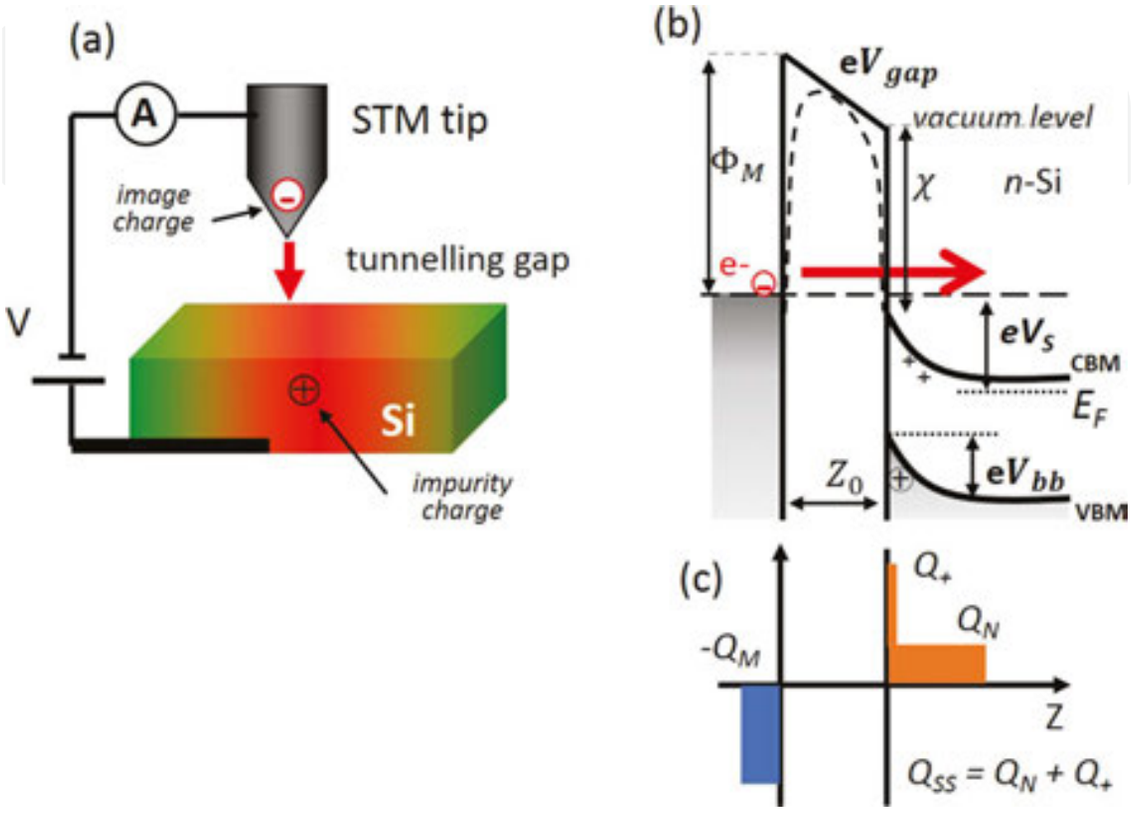

Figure 3. The principle of scanning tunneling microscopy of a semiconductor. (a) An STM setup, (b) an energy band diagram of a tunnel junction, and (c) a charge balance diagram.

The tunneling barrier shape determines the electron transmission factor and the value of the tunneling current. **Figure 3** shows an STM measurements setup and an energy band diagram of an ideal STM junction for n-type Si. Rectangular shape of the tunneling barrier is used in simple STM models. The actual potential barrier profile is different because of image potential lowering ($\Delta\phi$) owing to strong Coulomb interaction between charge and image charge in conductive materials [43–45]. Also, the tunneling gap may include an insulating layer such as ultrathin oxide and a molecular film with different dielectric properties. Therefore, the tunneling electrons experience an effective potential barrier of a barrier height (BH) given by

$$BH = \left(\Phi_{\mathrm{M}} + E_F - qV_{gap}\right)/2 - \Delta\phi, \tag{2}$$

where Φ_M is the work function of the metal tip and E_F is the Fermi energy of the semiconductor, q is the elementary charge. For electron energy smaller than BH, the transmission factor is approximated by [46].

$$T(E,V) = \exp\left(-\alpha \cdot \sqrt{BH} \cdot Z\right), \tag{3}$$

The tunneling constant α = 10.2 when the gap width is in units of nanometer and BH – in eV.

Because electric charge density in semiconductors is lower than that in metals, applied electric field penetrates deep beneath the semiconductor surface. To maintain the charge neutrality, a band-bending region is created beneath the STM probe. The applied voltage V_S is shared between the gap and the band-bending region and is given by

$$V_S = V_{gap} + V_{bb} + \phi_{MS}, \tag{4}$$

where last term ϕ_{MS} = (Φ_M − E_F) is an electrostatic potential difference between the work function of the STM tip and the semiconductor Fermi energy, and χ is the electron affinity of the semiconductor. In thermal equilibrium and $V_S = 0$, the charge neutrality is conserved, and the electric charge in the STM tip (Q_M) is equal to the local electric charge at the semiconductor surface beneath the STM tip. At V_S = 0, the band-bending region is created owing to the electrostatic potential difference ϕ_{MS}. **Figure 3** illustrates the case when an electron depletion region is formed for n-type Si under an external positive bias voltage $V_S > 0$ to the sample. For n-Si, the surface charge (Q_{SS}) includes positive charge of impurity atoms (Q_N) and mobile carriers (holes) (Q_+):

$$Q_M = Q_{SS} = Q_+ + Q_N, \tag{5}$$

According to the Gauss law [43, 47, 48], the voltage across the gap is given by

$$V_{gap} = \frac{|Q_{SS}|}{\in_0} \cdot Z_0, \tag{6}$$

where $\in_0$, and $\in_{Si}$ are the permittivity of the vacuum gap and Si, respectively. The depth of the band-bending region (w) depends on the electric field screening by the electric charge in the semiconductor and is given by

$$w \cong \sqrt{\frac{2 \in_{Si} V_{bb}}{Q_{SS}}}, \tag{7}$$

It is straightforward that the tunneling current strongly depends on the local electric charge at the semiconductor surface. When there were surface states and interface traps, these trapped charges would alter the initial charge carrier distribution, and great care must be taken to prepare clean, well-defined cross-sectional surfaces. In fact, conventional furnace oxidation

produces a gap-state density of about 10^{10} cm^{-2} for Si(100) and less than 10^{12} cm^{-2} for Si(111) surfaces [47]. Low-pressure oxidation below 600°C results in a density of ~10^{12} cm^{-2} for Si(100) surfaces [26, 41, 42]. The surface oxidation effectively reduces density of surface states on Si surfaces, making that the current behavior becomes dependent on charge carrier concentration in the Si bulk beneath the STM probe.

Topographic STM images of a sample surface are formed when the STM probe is moved along the surface while keeping pre-determined tunneling current value (I_{tun}) at an applied voltage (V_S) by adjusting the gap width with a piezoelectric scanning unit. The STM technique offers ultimate spatial resolution down to a sub-nanometer range because tunneling current is strongly localized around the outermost atom of the STM tip owing to exponential current decay with the tip-sample distance. Three advanced STM-based modes discussed below rely on measurements and analysis of the tunneling current and, thus, offer high spatial resolution. Details of the SPM system construction and operation have been reviewed in original papers and textbooks [11].

4. Advanced STM modes

To study charge carrier distribution in semiconductor devices, we describe three STM-based techniques: a vacuum gap modulation method, a molecule-assisted probing method, and a dual-imaging method.

4.1. Vacuum gap modulation method

A vibrating electrode technique was used to measure the surface potential on solid surfaces by using the Kelvin method [49]. Present-day noncontact atomic force microscopy (nc-AFM) uses vibrating probes for detecting atomic, electrostatic and magnetic forces [50]. In metals, mechanical modulation of the tunnel barrier has been applied as a method to evaluate local work function of the sample [46, 51–54]. In semiconductors, a model of STM junction considering both transparency of the tunnel barrier and the band-bending potential was elaborated [22, 23].

When the STM probe vibrates normal to the sample surface, the gap width changes as

$$Z = Z_0 - dz \cdot \sin(\omega t), \tag{8}$$

where $\omega = 2\pi \bullet f$ is the angular frequency, dz is an amplitude of the vibration. For small vibration amplitude, $dz \ll Z_0$, the transmission factor periodically changes with the time-dependent change of both the gap width and the gap voltage. When the STM probe approaches toward the surface, V_{gap} is reduced while increasing the surface potential (V_{bb}). A change of the gap voltage V_{gap} is related to the mean charge Q_{SS} at the surface by the Gauss law [43, 47, 48] and is expressed as

$$dV_{gap} = -d\psi = -\frac{|Q_{SS}|}{\epsilon_0} \cdot dz, \tag{9}$$

where $d\psi$ is a change of the band-bending potential.

To determine the tunneling current response (dI) to a time-dependent variation of the gap width, the tunneling current is expressed as

$$I_{tun}(\omega t) = I_0 + dI_1 \cdot \sin(\omega t), \tag{10}$$

where I_0 is the mean tunneling current. In the linear approximation [46], the current response is dominated by variation of the mean transparency of the vacuum gap. Thus, in-phase amplitude of the tunneling current response is given as

$$dI_1 \propto I_0 \cdot \frac{|Q_{SS}|}{\epsilon_0} \cdot dz. \tag{11}$$

In our experiments, the mean tunneling current I_0 is held constant; thus, the quantity (dI_1/dz) is proportional to the local charge density at the surface beneath the STM tip under the bias voltage. There is a 90°-phase-shifted current component representing a displacement current owing to change in the STM junction capacitance as discussed in details in Reference [55]. We used the capacitive signal for fine-tuning of the signal phase in the measurements of in-phase current by a lock-in technique.

In the model above, terms due to the shape of the tunnel barrier and capacitance effects associated with modulation of the band-bending region beneath the STM probe are neglected, albeit the effects are essential at high frequency and low impurity concentration [55].

When the modulation of band-bending region is taken into account, the tunneling current response is given by two terms (Appendix A)

$$\left(\frac{dI}{dz}\right) \propto I_0 \cdot K_3;\ K_3 = \alpha\sqrt{BH} - \left(\frac{\alpha Z_0}{4\sqrt{BH}} + \beta\right) \cdot \frac{|Q_{SS}|}{\epsilon_0},. \tag{12}$$

The first term represents the contribution of the gap width modulation, and the second term accounts for variations of V_{gap} and V_{bb} .

It is constructive to take a look at origin of charge Q_{SS} for n-type and p-type Si under positive bias voltage. In *n*-Si in **Figure 3**, the electric field from the STM probe repels mobile electrons deep into the bulk creating a surface depletion region, and $Q_{SS} = Q_N + Q_+ \approx Q_N > 0$. The larger the bias voltage, the larger the amount of positive charge accumulated beneath the STM probe. As a consequence, the amplitude of the current response (dI) depends predominant-

ly on density of accumulated positive charge. On the contrary, in p-type Si under the same polarity bias, the electric field attracts mobile majority carriers (holes) to the surface reducing amount of negative charge of acceptor impurities (Q_P) beneath the STM probe. As a consequence, the amplitude of the current response (dI) depends predominantly on small amount of accumulated positive charge, and $Q_{SS} = Q_P + Q_+ \approx Q_+$. At the position of electrical p-n junction, the balance of positive and negative charges exists, and $Q_{SS} \approx 0$. Thus, we are able to derive position of electrical p-n junction through analysis of the (dI/dz) profiles. In addition, detection of charge centres near the Si surface at a depth of ~1 nm has been reported for epitaxial Si layers [56].

Experimentally, differential tunneling current (dI/dZ) maps were obtained by vibrating the STM probe normal to the sample surface. The STM probe-sample gap was vibrated at a frequency of 12–50 kHz and an amplitude of 20–50 pm while keeping the vacuum gap at constant mean tunneling current I_0 (the constant current mode). In-phase current response dI was measured with a lock-in amplifier at each point in the topographical image. The vibration frequency was selected sufficiently larger than the feedback circuit bandwidth (~10 kHz) and away from the electromechanical resonances of the STM measurement system.

4.2. Molecule-assisted probing method

The ability of specific molecules to selective reactions on the surface is well known in catalysis. Recently, functionalization of SPM probes by attaching functional groups to achieve the chemical selectivity in recognition of DNA sequences and biological molecules has been performed, for example, see [57–59].

The method described here is different. A molecule-assisted probing method makes use of a discrete energy level of an adsorbed molecule as a *marker* of the local Fermi energy. It takes advantage of resonant electron tunneling (RET) to monitor the energy level of the marker molecule, such as fullerene C_{60}, introduced into a tunneling barrier between the STM probe and the oxidized Si surface. The fact that the C_{60}-derived conductance peaks shift in energy depending on dopant concentration in the underlying substrate makes this technique usable as a probing method of the charge carrier profiling on semiconductors [39, 41, 60]. The C_{60} molecule was selected as it satisfies the selection criteria: small size, chemical stability, and an energy position of molecular orbital outside of the Si energy band gap.

A model of a double-barrier junction (DBJ) was elaborated based on the theory of planar resonant tunnel diodes [61] and alignment of molecular states [62]. **Figure 4(a)** and **Figure 4(b)** show the experimental setup and an energy band diagram of an ideal DBJ consisting of the vacuum gap (B1), the C_{60} layer and the thin oxide (B2) under a resonant injection bias V_{RET}. E_A is the electron affinity of the C_{60} layer, and E_i is the Fermi energy for intrinsic Si. At the resonance condition, the Fermi energy of the STM tip aligns with the lowest unoccupied molecular orbital (LUMO), and thus, the strength of electric field in the vacuum gap is given by $F = (\Phi_M - E_A)/Z_0$. For an ideal oxide and neutrality of C_{60}, continuity of the electric displacement is preserved across the DBJ, and the RET voltage is given by

$$V_{RET} = \epsilon_{Si} F \cdot \left(Z_0 + \frac{d_{C_{60}}}{\epsilon_{C_{60}}} + \frac{d_{ox}}{\epsilon_{ox}} \right) + V_{bb}, \tag{13}$$

where d_{60} and d_{ox} are the thickness of C_{60} molecule and the oxide, respectively. $\in_{C60}$ and $\in_{ox}$ are the permittivity of C_{60} and oxide, respectively. V_{bb} voltage is obtained as a function of the electric field F at the Si surface by solving the 3D Poisson equation at quasi-equilibrium.

To measure the RET voltage, mono-molecular fullerene films were prepared by vapor sublimation of C_{60} to the oxidized Si surfaces at room temperature followed by re-evaporation of excess molecules as described in Section 2.3. Differential conductance $(dI/dV) - V$ spectra in **Figure 4(c)** were obtained at a constant probe-sample gap by using a lock-in technique where a small *ac* voltage (20 mV_{pp}, 50 kHz) was superimposed on the sample bias voltage. The initial tunneling conditions were set with a tunneling current of 200 pA at a set-point voltage of 2.5 V. Each $(dI/dV) - V$ spectrum was fitted to Lorentzian function to determine a voltage of the C_{60}-derived conductance peak, the RET voltage [41, 64]. For high conductance of the tunnel gap, the STM tip is close to the molecule layer, and another transport mechanism, the single electron tunneling [66], becomes apparent and hinders the RET voltage detection. Thus, optimization of the gap width is required.

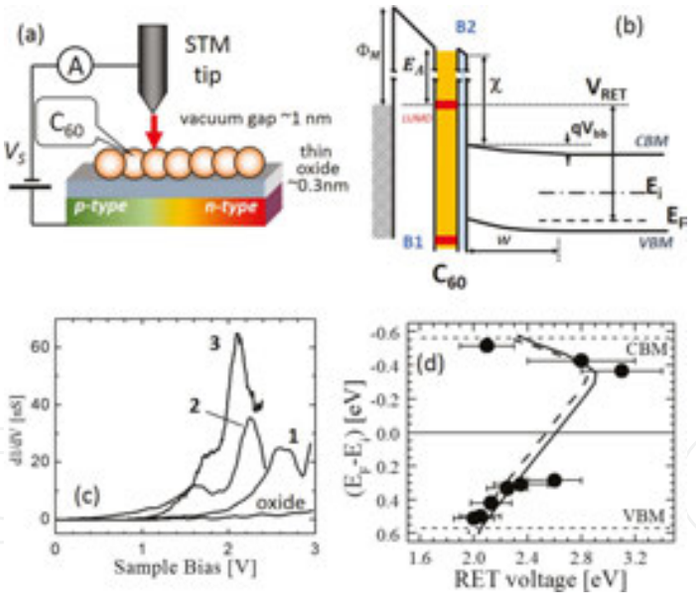

Figure 4. Molecule-assisted probing method. (a) A setup. (b) An energy band diagram of a double-barrier junction under the resonance conditions. B1 is the tunneling gap, and B2 is thin oxide. (c) (dI/dV) spectra of C_{60} on p-type Si substrates with a boron concentration of 8×10^{14} cm^{-3} (curve 1), 4×10^{15} cm^{-3}(curve 2), 3×10^{18} cm^{-3}(curve 3), and without C_{60}. (d) RET voltage as a function of the Si Fermi energy $(E_F - E_i)$ from measurements (symbols) and 3D numerical calculations for oxide thickness of 0.3 nm (broken line) and 0.7 nm (solid line) according to Eq. (13) and Reference [41].

The measured RET voltage obtained for uniformly doped Si wafers with different dopant concentrations is shown in **Figure 4(d)**. The data are well reproduced by the numerical calculations according to Eq. (13) where STM probe emitter was modeled as a cone with a

hemispherical end and a radius of curvature of 10 nm, and Z_0 = 1 nm, d_{C60} = 1 nm , and d_{ox} = 0.3 nm, Φ_M = 4.5 eV for W(111) probes and E_A = 2.6 eV. The good agreement between the calculated RET voltage and the experimental data for uniform-doped wafers verifies the calibration relationship for Si [41, 63].

The spatial resolution of the method is restricted to the size of the *marker* molecule and to the electric field penetration length. It has been demonstrated by the (dI/dV) mapping that the RET peaks are localized within the C_{60} core (~1 nm) due to their origin in resonant tunneling mediated by one lowest unoccupied molecular orbital (LUMO+1) of C_{60} [41]. Since the LUMO +1 was localized at the pentagonal rings [65] and C_{60} molecule rotates at room temperature, the observed peak intensity represents the orientation-averaged orbital conductance of C_{60}. The estimate of the penetration depth is a Debye length of ~1.5 nm for *p*-Si under large positive bias, though the length depends on the dopant concentration for n-Si [41, 63].

4.3. A dual-imaging method

STM technique is limited to conductive surfaces and is inapplicable to the imaging of novel device structures, including insulator surfaces such as silicon-on-insulator (SOI) devices. Strong interest to such measurements is stimulated by the fact that discrete dopant distribution enables attractive applications such as quantum computing [67] and single-electron devices [68]. Therefore, a dual-imaging method was developed to enable simultaneous measurements of electric current and interaction force acting on the scanning probe. It was achieved by attaching an STM metal tip to a special force sensor [67–76].

Figure 5 shows the experimental setup for the simultaneous measurement of tunneling current (I_{tun}) and force between the metal probe tip and the Si surface. In our technique, the interaction force gradient between the metal probe tip and the surface was detected as a shift in the resonance frequency (Δf) of a quartz length extension resonator (qLER) which vibrated at ~1 MHz (Q factor ~50,000) with an amplitude of 0.05–0.3 nm [67–70]. The probe tips were made of a tungsten wire with a diameter of 10 μm. The wire was attached to the quartz resonator and sharpened by the focused ion beam technique (FIB). Typically, the probe tips had a diameter of Ø30 nm and the aspect ratio of more than 10, resulting in small stray capacitance. Detection of the frequency shift by electric means makes such sensors suitable for measurements in ultra-high vacuum environment and at different temperature, which are often required in nanomaterial and nanoscale device research.

The advantages of our multimode scanning probe microscopy (MSPM) system are

- tunneling current and forces acting on the probe tip are measured *simultaneously* at a mean probe-sample gap of about 1 nm in constant current (CC) or constant force (CF) operation modes;
- small vibration amplitude (0.1–0.2 nm) enables us to drastically reduce the probe-sample gap, leading to better *spatial resolution*;
- the *sensitivity* to electrostatic forces is increased at an optimal gap;

- the force detection is performed in a *noncontact* manner, which is suitable for measurements of solid crystals and thin films.

In the CC mode, a force gradient map is measured while the mean gap (Z_0) maintains a set-point tunneling current. Typically, the measurement condition corresponds to a gap of approximately 1 nm, as estimated from the distance dependence of the tunneling current [72]. The spatial variation of the frequency shift (Δf) reflects variations in the interaction force caused by charge carriers, impurity charges, and surface imperfections as illustrated in **Figure 5(b)**. When a donor is present in proximity to the STM tip, the attractive force acting on the tip increases owing to Coulomb interaction between the donor charge and the image charge induced in the STM tip, leading to measurable change in the Δf value [75, 76]. The interaction strength depends on the depth of the donor location and the electrostatic screening by mobile carriers. Experimentally, lateral extent of 5–10 nm and a detection depth of ~1 nm have been reported for phosphorus and boron atoms in Si [32, 33, 76]. Change in the interaction force on grains with different work function was employed for recognizing crystal orientation of sub-10-nm-size grains in nano-crystalline TiN films [77].

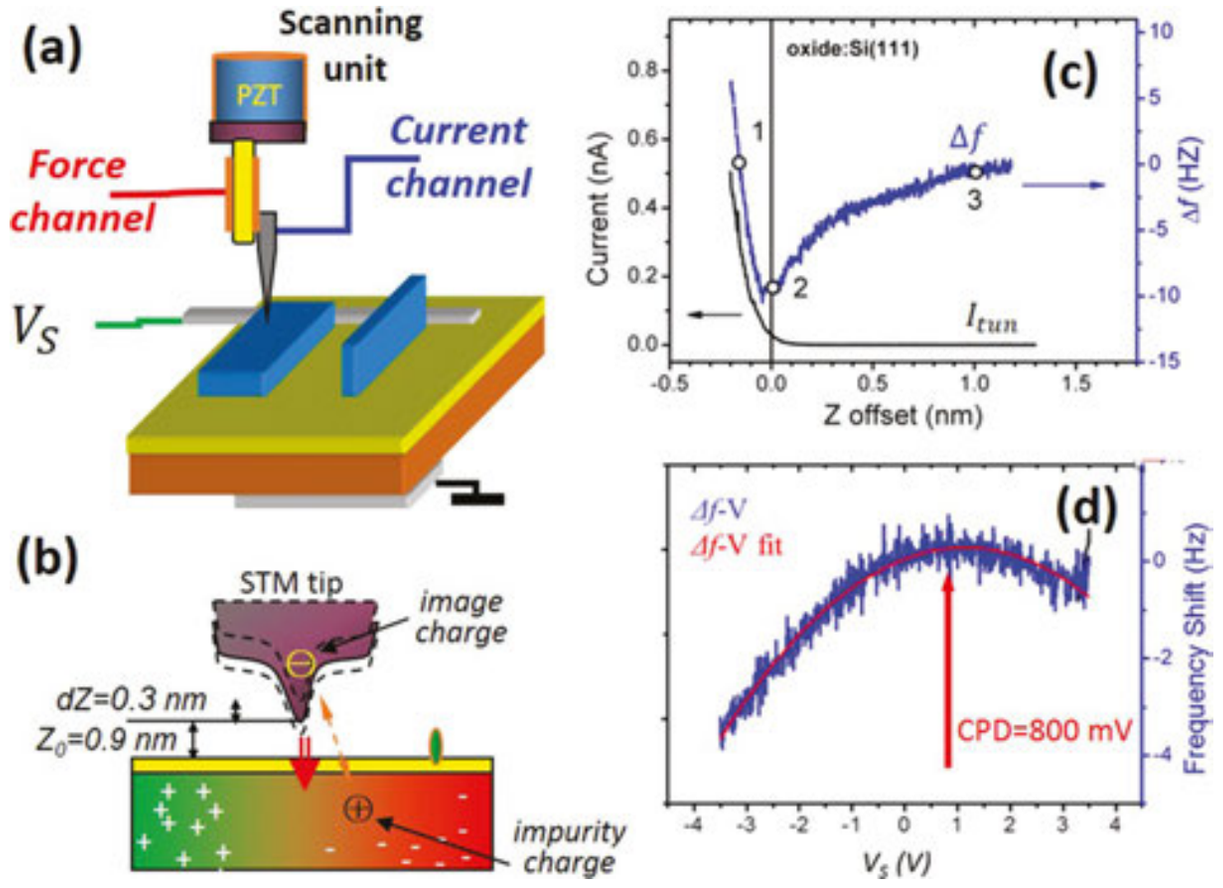

Figure 5. Dual-imaging method. (a) A measurement setup. (b) A sketch of interaction force acting on a vibrating STM probe. (c) (I_{tun}-Z) and (Δf-Z) spectra showing ranges of repulsive interaction (1–2) and attractive Coulomb interaction (2–3) for an oxide-passivated Si(111) surface (a set-point: 30 pA, 2.0 V). (d) A measured (Δf-V_S) spectrum at position 3(blue curve), and a result of fitting to Eq. (14) (red curve).

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In the CF mode, a tunneling current (I_{tun}) map is measured while the mean gap (Z_0) is maintained at a constant frequency shift. There are two ranges in distance dependences of I_{tun} *and* Δf as indicated in **Figure 5(c)** for an oxide-passivated Si(111) surface. At short distances (range 1–2), repulsive interaction dominates, and current exponentially grows when the STM tip approaches the surface. At longer distances (range 2–3), the electrostatic Coulomb interaction dominates. There is an optimal distance indicated as position 2 in **Figure 5(c)** where the sensitivity to electrostatic force is maximum [72]. At this distance, the ($\Delta f - V_S$) spectrum has the largest curvature.

Under the applied voltage V_S, the electrostatic force gradient between the probe tip and the sample is expressed according to the theory in References [73, 78] for small vibration amplitude

$$\Delta f \propto \frac{\partial F}{\partial z} = -\frac{1}{2}\left(V_S - CPD\right)^2 \cdot \frac{\partial^2 C}{\partial z^2}, \tag{14}$$

where C is the effective tip-sample capacitance. CPD, the contact potential difference, refers to the difference between the work function of the metal probe (Φ_M) and the Fermi energy of the underlying Si (E_F), and is given by

$$CPD = \frac{1}{q}\left(E_F - \Phi_M\right), \tag{15}$$

where q is the elementary charge. A local value of the CPD voltage, which is determined by local charge concentration in the underlying Si, can be obtained by fitting of the spectrum to Eq. (14). In the example in **Figure 5(d)**, a CPD voltage of +0.8 V was obtained for an oxidized p-Si(111) surface. The CPD voltage mapping was employed in 2D analysis of the built-in potential in small Si MOSFET devices [79] and p-n junctions [72] showing the attainable spatial resolution better than 3 nm. Particular applications of the CF mode also include analysis of impurity distribution profiles from I_{tun} maps measured at different bias voltage [80], non-uniform distribution of photocarrier in Si stripes [81], and nanoscale conductance switching in phase-change GeSbTe thin films [82].

5. Application examples

5.1. Channel length in small MOSFET

For STM measurements, cross-sections of Si MOSFETs were prepared by ultra-fine polishing to expose (110) surfaces and were passivated by ultra-thin oxide layer as described in Section 2.2. Si *n*-type MOSFET with nominal gate lengths (L_G) in the range of 20–150 nm were fabricated according to a process described in Reference [83]. The measurements were done with W(111) crystal probes in an ultrahigh vacuum (~4 × 10^{-9} Pa) at room temperature.

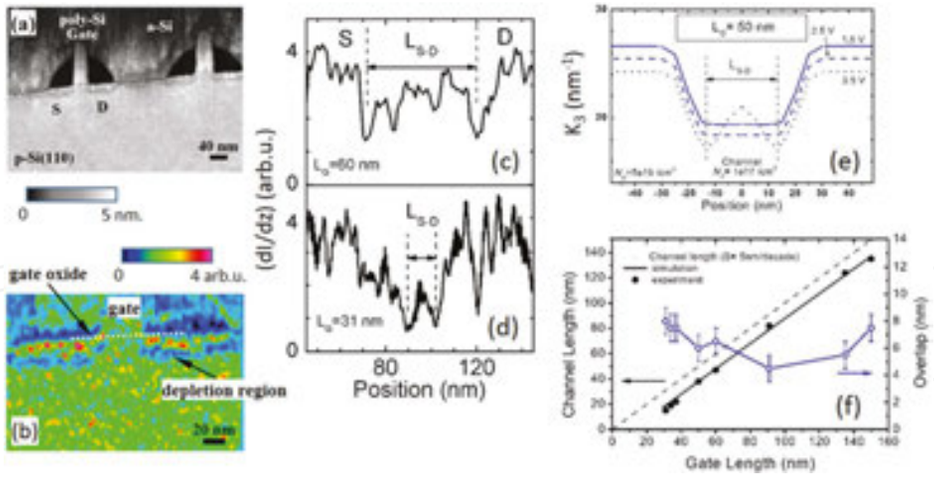

Figure 6. (a) Topographic image of a cross-section containing two small Si MOSFET devices. (b) A (dI/dZ) map of a device with a gate length of 31 nm (a set-point: 230 pA, 3.4 V, dz = 20 pm). (c)–(d) Line profiles measured at 12 nm depth beneath the gate electrodes showing the electric channel length (L_{S-D}). (e) Profiles calculated by Eq. (12) for expected impurity distribution. (f) Measured electric channel length (symbols) as a function of gate length. Line is the calculation result.

Topographic image of two small MOSFET is shown in **Figure 6(a)**, where the gate electrodes are surrounded by two black cavities produced by sidewall oxide etching during the surface preparation. The source/drain (S/D) extensions on the left- and right-hand sides of the gate electrode are seen as bright stripes in the (dI/dZ) map in **Figure 6(b)**. Depletion regions separate the S/D extensions from the p-type channel beneath the gate electrode and the Si bulk. The extension depth is ~18 nm as measured from the gate oxide. The electric channel length (L_{S-D}) was determined as the distance between 2 minima in (dI/dZ) line profiles measured at a depth of 12 nm beneath the gate oxide as indicated in **Figure 6(c, d)**. Calculated profiles of the K_3 factor in **Figure 6(e)** reproduce the measured (dI/dZ) profiles, confirming that each minimum in (dI/dZ) signal represents the position of the electric p-n junction. L_G was determined from STM topographs. Results summarized in **Figure 6(f)** give an overlap value of 6 ± 1 nm, which is in excellent agreement with a transverse straggle of 7 nm for an implanted ion energy of 25 keV. An accuracy of the channel measurements was about 1 nm at 3.4 V, while the measurements were affected by random positions of individual ionized dopant atoms in the extension regions.

5.2. Super-junction devices fabricated by the channeling ion implantation

The C_{60}-assisted probing technique has been actually applied to quantitative analysis of charge carrier profiles on cross-sections of power MOSFET, where the precise control over the doping profile is essential to obtain low ON-state resistance and high breakdown voltage [39, 40]. **Figure 7(a)** depicts a schematic structure of a super-junction power MOSFET. Two *p*-type islands were formed by multiple boron ion implantations into the low-doped *n*-type epitaxial layer with a carrier density of ~1×10^{16} cm^3. In **Figure 7(b)**, we clearly see that two p-type islands are separately formed with the same peak concentrations, confirming the anticipated dopant concentration. Moreover, the experimental data revealed an extension of island 1 beyond the

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expected depth, which is attributed to a scatter-less travel of boron ions through Si crystal at high implantation energy, the ion channeling effect[84].

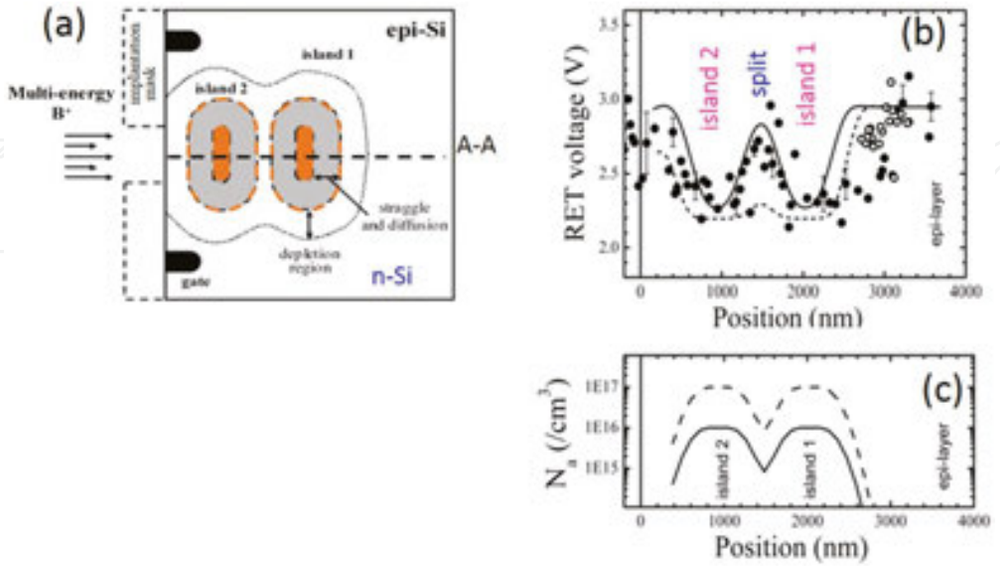

Figure 7. (a) Schematic structure of a super-junction device showing two p-Si islands made by boron ion implantation. (b) Depth profiles of the RET voltage along center of the device: measured data (symbols) taken with 20-nm steps. Profiles (lines) were calculated for the two boron density profiles shown in (c). Reproduced with the permission from Reference [39].

5.3. Length-dependent resistivity of Si nanowires

The ability of the dual-imaging method for characterization of modern silicon-on-insulator (SOI) devices is illustrated by analysis of the structure and electric conductance of SOI nanowires (NW) with different surface passivation. Note that the NW is the promising structure for sub-10-nm MOSFETs and for such functional devices as chemical sensors. **Figure 8** shows high-resolution measurements of a Si NW with a cross-section area of 20 × 20 nm^2 acquired at a set point of Δf = 0.6 Hz, dz = 95 pm, V_S = − 1.5 V. We see in **Figure 8(c)** the current gradually decreases in the NW interior with the distance from the Si pad owing to the dependence of the NW resistivity on its length. We note that an apparent NW width in the current map is about 2-fold of that in the topograph. As the NW is protruded above the buried oxide (BOX) by 20 nm, a side surface of the sharp tip touches the NW as illustrated in the insert of **Figure 8(c)**, and this results in a so-called "sidewall" current outside the Si NW body. The current value and fluctuations were reduced for the NW passivated with an ultrathin oxide layer compared to the hydrogen passivation. The tunneling current decreased within a distance of ~300 nm from the Si pad electrode for both types of surface termination. At the negative voltage, the tunneling current is defined by electrons traveling from large Si pad through the SOI nanowire, and the current value is determined by resistivity of the NW volume and the surface conduction. The macroscopic conduction model including the conductance contributions of the nanowire volume and the surface states confirmed the length-dependent conductance of thin Si nanowires [85].

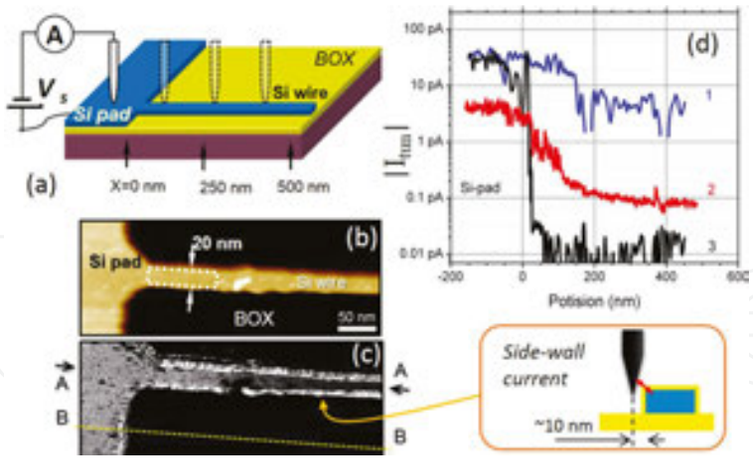

Figure 8. (a) An experiment setup. (b) Topographic image of silicon-on-insulator nanowire with a cross-section of 20 × 20 nm^2, and (c) corresponding current map acquired at -1.5 V and Δf = 0.6 Hz, dz = 95 pm. (d) Current profiles along A-A line for Si nanowires after hydrogen-passivation (curve 1), oxide passivation (curve 2), and along B-B line (curve 3). Adopted from Reference [85] (Copyright 2013 Trans. Mat. Res. Soc. Japan).

5.4. Wavelength-dependent photocarrier distribution across strained Si stripes

Photo-carrier generation in semiconductors is a fundamental process utilized in solar cells and photo-detectors. For reduced size of modern detectors, the role of structural elements in carrier accumulation and transport has been increasing [86]. In particular, photocarrier distribution on textured surfaces of Si can be a factor to improve the efficiency of solar cells. Analysis of spatial distribution of photocurrent (PC) in strained Si stripes under tilted illumination gives an insight into photocarrier behavior near the stripe edges with an effective spatial resolution of ~10 nm [81].

Figure 9 shows the sample structure and the measurement setup, where inhomogeneous light intensity profile was created under tilted (50° off-normal) illumination and different light wavelength (λ). Strained Si stripes of 50–1000 nm in width and 300 nm in height were fabricated on Si(001) wafer, and separated by SiO_2. The stripe surface was passivated by an ultrathin oxide as described in Section 2.2. The light intensity was mechanically modulated at frequency of ~3 kHz, and the PC signal was measured by a lock-in unit. Topographs and PC maps were measured by the dual-imaging method where the tip-sample gap was set by a set-point of Δf = 1.2 Hz, dz = 130 pm, and V_S = − 0.8 V, using the CF mode.

Topographic image in **Figure 9(b)** shows uniform surface of the Si stripe. The PC signal was not uniform, and large at a distance of ~50 nm from the stripe edge on the light illumination side, when stripes were illuminated with laser light and an intensity of 12 mW/cm^2 as seen in **Figure 9(c)**. Large PC signal at stripe edges was observed irrespective of the scanning directions, when light with λ = 405 and 364 nm was used as seen in line profiles in **Figure 9**(**d**, **e**). In contrast, illumination with red light (λ = 675 nm) produced uniform PC distribution. As the absorption depth in Si is ~11 nm for λ = 364 nm, ~130 nm for λ = 405 nm, and ~4000 nm for λ = 675 nm [87], the respective illumination produces different light intensity profiles. Calcu-

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lated PC profiles in **Figure 9(f)** reproduced the observed PC distributions when a rectangular bar geometry, non-coherent light, and a photocarrier diffusion length of 100 nm were used [81].

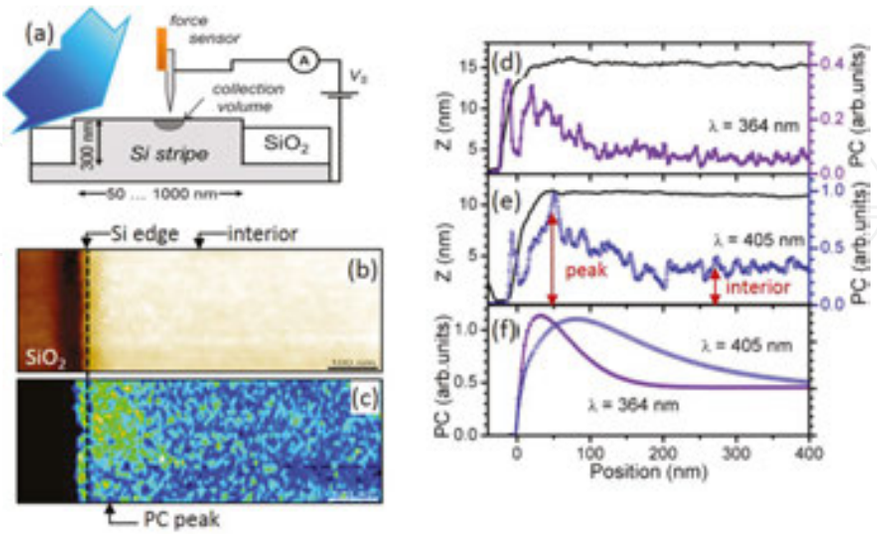

Figure 9. (a) Photocurrent (PC) measurement setup. (b) A topograph and (c) corresponding PC map of a Si stripe under illumination with λ = 405 nm. (d)–(e) Measured line profiles of height (black lines) and PC (dotted lines) across the stripe edge under tilted illumination for two wavelengths (λ). (a set-point: Δf = 1.2 Hz, dZ = 130 pm, V_S = − 0.8 V). (f) PC line profiles calculated for a rectangular bar exposed to light at top and side surfaces. Adopted from Reference [81] (Copyright 2012 The Japan Society of Applied Physics).

We note that the relative intensity of a PC peak at a position of ~30 nm for λ = 364 nm is ~3.2-fold the signal in the stripe interior. Enhancement of light intensity by ~3.5-fold at strained Si stripe edges has been reported for λ = 364 nm [88, 89]. The enhancement mechanism may be related to increased photocarrier generation owing to interference of coherent laser light [81], narrowing of the Si energy gap under stress [90] or increase in the tunneling probability through electromagnetic field coupling to the sharp STM tip [91].

6. Simulations of tunneling current spectra

STM has the capability to 2D impurity profiling by employing advanced STM methods as shown above. Although, accurate analysis of charge carrier distributions in actual 2D and 3D device structures has been a substantial challenge. STM tunneling current is a complex function of structural, material, and electronic parameters of the system consisting of a 3D probe tip and a semiconductor. On the basis of fundamental theory, there have been theoretical discussions of 1D and 2D treatments for the STM junction geometry. A 3D numerical simulator has been reported that solves the 3D potential distribution of the sample STM probe system and calculates the tunneling current, so-called *the potential-based model* [23, 92, 93]. However, to describe the precise physics of STM measurements, the charge carrier flow in the sample must be included, as evidenced by the NW measurements in **Figure 8**. Recently, new model evolves solving the charge carrier transport between a probe tip and a sample consistently

with the current continuity equation, so-called *the current-continuity model*. The current-continuity model accounts for charge carrier transport between states in an STM probe and the conduction and the valence band of Si and was implemented on the basis of a technology computer-aided design (TCAD) semiconductor device simulator code [94]. It is a significant advancement in the field.

An analysis based on the current-continuity model has been applied successfully to extracting impurity distribution profiles in a MOSFET from experimental current maps measured by the dual-imaging method [80], and for evaluating photocarrier dynamics in Si nanowires with a cross-section of 10 × 10 nm^2 [95].

The remaining challenge is to include the effect of single impurity scattering on charge carrier transport in nanoscale devices. The impurity scattering for a thin semiconductor wire has been solved using the 3D Green function approach and the numerical Monte-Carlo method [96]. An atomistic view into an impurity atom appearance in STM images has been elaborated within the framework of a self-consistent-charge density functional tight-binding method (SCCDFTB), for example, see [97, 98].

7. Conclusion

Advanced STM-based methods for 2D analysis of charge carrier distributions in semiconductor devices with high spatial resolution represent the substantial development of scanning probe microscopy. The described methods rely on detection and analysis of tunneling current which is strongly localized within an atomic dimension. This leads to significant improvement in the sensitivity and spatial resolution for measuring local electric characteristics of Si devices and nanowires, when effects of surface states are suppressed by adequate surface treatment.

The gap modulation method can attain an ultimate spatial resolution comparable to that of STM topographic images in p-n junction regions, and can detect individual charged impurity atoms along the surface at a depth of few nanometers. Quantitative evaluation of charge distributions can be derived by comparing experimental data and simulations of the underlying charge concentration. The accuracy relies on the ability of the simulation to account for quantum phenomena, and further development of simulations based on the current-continuity model will be essential.

The capability of the molecule-assisted probing method has been demonstrated with the use of C_{60} molecules. A spatial resolution of ~1 nm is determined by the size of the molecule. However, the C_{60} film on oxidized Si surfaces leaves ~20% uncovered areas. The coverage can be increased by the use of chemically modified C_{60} or other small molecules those formed a monomolecular-thick film on SiO_2 surface. For high conductance of the tunnel gap, another transport mechanism, the single electron tunneling [66], becomes dominant and obscures the RET voltage measurements. Thus, optimization of the gap width is required.

The presented methods can be used for measuring on rough surfaces, but careful data analysis should be performed to discard "artifacts." In the gap modulation method, the tip vibration

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amplitude (*dz*) varies with tilt angle of the underlying surface, causing changes in the (dI/dZ) signal. In the dual-imaging method, large "sidewall" current such as shown in **Figure 8** must be considered in data analysis. Also, atomically ordered surfaces can be obtained by cleavage, yet, to attain ultimate spatial resolution, STM measurements in well-controlled environment such as in an ultrahigh vacuum are necessary, where we can avoid undesirable effects caused by absorption of charged particles and molecules from air.

To summarize, specific features of the presented 2D STM-based methods are (a) noncontact, stress-free measurements allowing analysis of delicate sample structures; (b) high spatial sensitivity to electrostatic field, which is substantial advancement in comparison with scanning Kelvin probe microscopy; (c) the ability to study nanoscale structures with a lateral size of 20 nm and below, which are inaccessible by other techniques.

Further applications of the advanced STM methods will contribute to high-spatial resolution analysis of modern sub-100-nm electronic devices, functional nanowire devices, and novel devices incorporating two-dimensional materials such as graphene and topological superlattices. It will advance our understanding of charge carrier transport at nanoscale and encourage inventing novel energy-efficient devices.

8. Appendix A

The tunneling current is described as a periodic function as

$$I_{tun}(t) = I_0 + dI \cdot \sin \omega t = I_0 \cdot (1 + K_3 \cdot dz \cdot \sin \omega t), \tag{A1}$$

The mean tunneling current is given in terms of the thermionic emission approximation including the vacuum tunneling term according to Reference [99] as

$$I_0 = A_e^* T^2 \cdot \exp\left(-\alpha \sqrt{BH} \cdot Z_0\right) \cdot \exp\left(-\beta V_{bb}\right) \cdot \left[\exp\left(\beta V_{gap}\right) - 1\right], \tag{A2}$$

For $dz \ll Z_0$, the factor K_3 is derived considering only linear terms of dz and $d\psi$, and is given by

$$K_3 = \alpha \sqrt{BH} - \left(\frac{\alpha Z_0}{4\sqrt{BH}} + \beta\right) \cdot \frac{|Q_{SS}|}{\epsilon_0}, \tag{A3}$$

The area charge concentration at the Si surface (Q_{SS}) is obtained by solving the Poisson equation. An analytic solution for a 1D abrupt junction is given by [47]

$$Q_{SS} = -\frac{\in_{Si}}{\beta \cdot \Lambda} \cdot G(V_{bb}), \tag{A4}$$

$$G(y) = \left[\left(e^{-\beta y} + \beta y - 1 \right) + \frac{n}{p_0} \left(e^{\beta y} - \beta y - 1 \right) \right]^{1/2} \geq 0, \tag{A5}$$

$$\Lambda = \sqrt{\frac{\epsilon_{Si}}{\beta Q_N}}, \tag{A6}$$

Λ is the extrinsic Debye length, and volume densities of positive (p_0) and negative (n) charge are in the Si bulk. The factor $\beta = 1/k_B T$, and k_B is the Boltzman constant, T is temperature.

For 3D structures, a charge concentration at the semiconductor surface (Q_{SS}) is obtained by numerically solving the Poisson equation.

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