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Chapter 3

Impact of Dielectric Formation and Processing Techniques on the Operation of 4H-SiC MOSFETs

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Additional information is available at the end of the chapter

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Abstract

The mobility of carriers in the channel of silicon carbide is significantly lower than in equivalent silicon devices. This results in a significant increase in on-state resistance in comparison to theoretical predictions and is hindering the uptake of silicon carbide technology in commercial circuits. The density of interface traps at the interface between silicon carbide and the dielectric film is higher and this is often considered to be the primary reason for the low mobility. In this work, we show that the mobility is dominated by the surface roughness of the silicon carbide, especially when the transistor is operating in the strong inversion regime, by careful examination of the characteristics of lateral transistors designed to form complimentary MOS functions.

Keywords: Surface roughness, mobility, complementary metal–oxide semiconductor, flat band, 1/*f* noise

1. Introduction

The main objective of this study is to aid in the advancement and commercialisation of a CMOS process to enable the production of signal-level 4H-SiC MOSFETs for high-temperature digital and analog applications. Therefore, we report on the electrical characterisation and performance of 4H-SiC n- and p-channel MOSFETs that have been fabricated using different, commercially relevant dielectric process treatments. The samples labelled as HV06, CR25 and CR27 were fabricated using the process conditions detailed in Table 1. The aim of this work is to establish which oxidation process technique provides the best characteristics for a complementary CMOS process.

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2. Overview of the theoretical MOSFET

The metal–oxide semiconductor field-effect transistor (MOSFET) is one of the most important devices for integrated circuits in microprocessors and semiconductor memories, as well as being a very important power device. Due to this, it is becoming increasingly important to understand and advance the characteristics of 4H-SiC MOSFETs for both power device applications and signal-level devices. MOSFETs have several attractive features, which make them ideal for use in analog switching, high-input-impedance amplifiers, microwave amplifiers and digital integrated circuits.

The features include the following:

1. Higher input impedance than bipolar transistors, which allows the input impedance to be more readily matched to the standard microwave system.
2. Negative temperature coefficient at high current levels – more uniform temperature distribution over the device area and prevents the FET from thermal runaway or second breakdown that can occur in the bipolar transistors.
3. The device is thermally stable, even when the active area is large or when many devices are connected in parallel.
4. FETs do not suffer from minority carrier storage as there is no forward-biased p–n junction and consequently have higher large-signal switching speeds.

The MOSFET is usually referred to as a majority carrier or unipolar device because the current in a MOSFET is predominantly transported by carriers of one polarity. As shown in Figure 1, a MOSFET is a four-terminal device made up of a source, drain, gate and substrate or body. Figure 1 shows an n-channel MOSFET, which is made up of a p-type substrate into which two n+ regions are formed, the source and drain and a gate electrode which is usually made of doped polysilicon or metal and is separated from the substrate by a thin insulating film known as the gate dielectric.

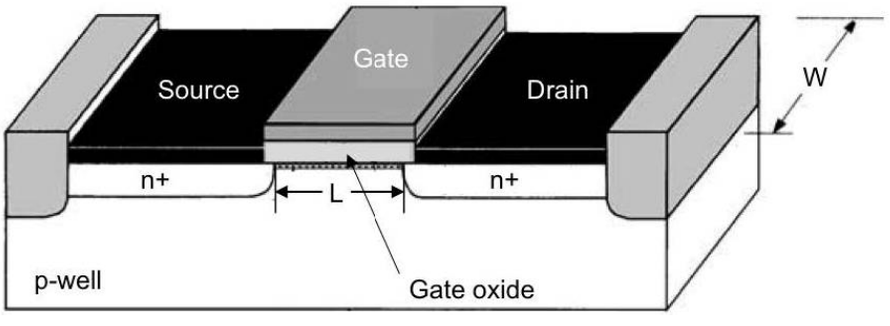


Figure 1. Schematic representation of a simple n-MOSFET

When a low voltage is applied to the gate electrode that is insufficient to form an inversion layer at the surface, there is no conduction in the channel, which corresponds to two p–n

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junctions situated back to back. This results in a high resistance and electrical isolation between the source and drain contacts. If a sufficiently large bias is applied to the gate electrode, a surface inversion layer will be formed between the source and drain, which will form a conductive channel through which a current can flow. The conductance of the channel can be modulated by varying the voltage applied to the gate electrode. Conduction in n-channel devices is based on the flow of electrons, and the channel becomes more conductive with increasing positive bias on the gate, whilst p-channel devices are controlled by hole conduction and are more conductive with a more negative gate bias. Enhancement-mode (or normally off) devices have a low transconductance at zero gate bias and require an applied gate voltage to form a conductive channel. Their counterpart, depletion-mode (or normally on) devices, are conductive when a zero bias is applied to the gate of the device, and a gate voltage must be applied to turn the channel off. Devices can either have a surface inversion channel or a buried channel. Buried channel devices are based on bulk conduction and are, therefore, free of surface effects such as scattering and surface defects resulting in better carrier mobility. The physical distance between the gate and the channel is larger and also dependent on gate bias, leading to lower and variable transconductance.

In a long-channel MOSFET, at low drain voltage and for a given gate voltage, the drain current is given by

$$I_{DS} = \frac{W}{L} q \mu_{inv} \left| Q_{inv} \right| V_{DS} \tag{1}$$

where W and L are the gate width and length, q is the electron charge, μ_{inv} the average mobility of the carriers in the inversion layer, V_{DS} the drain voltage and Q_{inv} the average charge in the inversion layer.

The field effect mobility μ_{FE} is defined as

$$\mu_{FE} = \frac{L}{WC_i V_{DS}} \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \tag{2}$$

where C_i is the insulator capacitance per unit area and V_{GS} is the gate voltage.

In 4H-SiC MOSFETs, the values of the field effect mobility extracted from the V_{GS} –I_{DS} characteristics will not correspond to the true inversion mobility due to the large density of interface charge. A knowledge of Q_{inv} as a function of V_{GS}, which can be extracted from the measured V_{GS} –I_{DS} characteristics, can allow the immobile interface charge to be calculated, which includes contributions from both Q_f and Q_{it}. A change in gate voltage δV_{GS} results in a change in Q_{it} and a change in δQ_{inv} in the inversion layer as the surface Fermi level moves away from the intrinsic level towards the conduction band edge [1]. This can be summarised through the use of equation 3:

$$\delta V_{GS} = -\frac{q}{C_i}\left(\delta Q_{it} + \delta Q_{inv}\right) \tag{3}$$

By combining equations 2 and 3, an expression that relates the experimental field effect mobility and the inversion carrier mobility can be derived [2]:

$$\mu_{FE} = \mu_{FE}\frac{\left[1 + \frac{Q_{inv}}{\mu_{inv}}\frac{\delta\mu_{inv}}{\delta Q_{inv}}\right]}{1 + \frac{\delta Q_{it}}{\delta Q_{inv}}} \tag{4}$$

3. Carrier mobility and scattering mechanisms in 4H-SiC

The conductivity (σ) of a semiconductor can be varied by the introduction of n- or p-type dopants and can be represented by equation 5:

$$\sigma = qn\mu \tag{5}$$

where μ is the carrier mobility, q the charge of an electron and n the number of carriers in the material.

The carrier mobility is principally how quickly an electron or hole can move through a semiconductor under the influence of an applied electric field and is affected by the frequency of collisions with lattice defects and impurities. The probability of scattering is inversely proportional to the carrier mean free time and the mobility. A carrier moving through a semiconductor crystal can be scattered by a vibration of the lattice, which increases for high temperatures when the thermal agitation of the lattice becomes higher. Scattering can also be due to lattice defects (e.g. ionised impurities) and is prominent at low temperatures since atoms are less thermally agitated and the thermal motion of the carriers is also slower. Higher scattering arises because a slow moving carrier is likely to be scattered more significantly by an interaction with a charged ion than a carrier with a larger velocity. If the carrier mobility in a material is reduced, the conductivity of the material will reduce and hence the resistivity will increase and channel current will reduce. As it is widely known that 4H-SiC MOSFETs exhibit low channel mobility and hence low current, it is of great importance to analyse the mechanisms that are contributing to the reduced channel mobility.

As previously reported [3-5], the total inversion carrier mobility in 4H-SiC MOSFETs can be described by the sum of four mobility terms using Matthiessen's rule which is often incorporated in simulation tools, such as the Synopsys suite by means of the Lombardi mobility model [6,7]:

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \tag{6}$$

As previously stated, the measured field effect mobility will not correspond to the true inversion mobility due to the presence of interface trapped charges. However, the main interest in silicon carbide technology is in the development of devices with higher functionality, and so the experimental device characteristics of the modelled mobility mechanisms will be equated to the field effect mobility using equation 7. Therefore, each of the scattering mechanisms considered here (μ_{AC}, μ_{SR} and μ_C) will result in a mobility which is lower than the value of each that would combine to form the true inversion mobility:

$$\mu_{FE} \propto \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right] \tag{7}$$

whereμ_B is the carrier mobility in the bulk semiconductor, μ_{AC} the acoustic phonon mobility, μ_{SR} the surface roughness mobility and μ_C the mobility related to carrier scattering at trapped charge at the silicon carbide–oxide interface.

At low electric fields, the carrier mobility in a semiconductor is a function of the temperature and the total doping concentration, which is referred to as the bulk or low-field mobility, μ_B. To represent this phenomena, an empirical model was developed by Caughey and Thomas which is described through the use of equation 8 [8, 9]:

$$\mu_B = \frac{\mu_{max}\left(\frac{300}{T}\right)^{\alpha} - \mu_{min}}{1 + \left(\frac{D}{N_{ref}}\right)^{\beta}} \tag{8}$$

where N_{ref}, μ_{min}, μ_{max}, α and β are fitting parameters, T the temperature and D the total doping concentration.

The second term in equation 7 is the acoustic phonon mobility, μ_{AC}. Both surface phonon and bulk phonon scattering have been modelled previously [10-12]. Each shows a temperature dependence and both surface and bulk phonon scatterings increase with an increase in temperature. Previous research has indicated that phonon scattering has a strong effect on surface mobility in SiC MOSFETs at high gate biases and high temperatures [13], and Potbhare et al. showed that surface phonon mobility does not play an important role at temperatures below 200°C [14]. The carrier mobility related to phonon scattering can be determined using equation 9:

$$\mu_{AC} = \frac{B}{E} + \frac{CN_A^{\alpha 1}}{TE^{\frac{1}{3}}} \tag{9}$$

where B and C are fitting parameters, E the perpendicular electric field, N_A the total doping concentration, T the temperature and $\alpha 1$ a factor that indicates the dependency of the mobility term μ_{AC} on the impurity concentration.

Surface roughness scattering is due to the scattering of mobile carriers by imperfections in the SiC surface and is known to cause severe degradation of the surface mobility at high electric fields [8, 15, 16]. The carrier mobility determined from surface roughness scattering may be calculated using equation 10:

$$\mu_{SR} = \frac{D_1}{E^{\gamma 1}} \tag{10}$$

where E is the perpendicular electric field and D_1 and $\gamma 1$ are fitting parameters.

Coulomb scattering is a result of carrier interactions with ionised impurities, which are most commonly a product of interface traps at the semiconductor–dielectric interface. Coulomb scattering is believed to dominate carrier mobility at low electric fields and is calculated using equation 11 [4]:

$$\mu_C = NT^{\alpha 2} \frac{Q_{inv}^{\beta 2}}{Q_{trap}} \tag{11}$$

where Q_{inv} is the inversion charge per unit area, $\beta 2$ a fitting parameter, Q_{trap} the trapped charge per unit area at the silicon carbide–oxide interface and T the temperature. For the analysis reported here, the exact values of Q_{trap} and $\beta 2$ were unknown, and so a simplified formula was derived that has the same functional form but could be fitted to the measure MOSFET field effect mobility characteristics [17], which is given in equation 12:

$$\mu_C = \left(E - \lambda\right)^{\Phi} \tag{12}$$

where E is the perpendicular electric field, λ the electric field offset at which the mobility becomes nonzero and Φ a fitting parameter which describes the gradient of the increasing mobility.

Figure 2 shows a schematic plot of the contributions of the three scattering mechanisms that have been discussed here: μ_{AC}, μ_{SR} and μ_C. For MOSFETs fabricated using 4H-SiC, the bulk mobility contribution to equation 7 term (μ_B) is far higher than the other scattering mechanisms,

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resulting in a negligible impact on the field effect mobility characteristics of the devices. For this reason, $\mu_B$is omitted from further analysis and is not included in Figure 2. As shown in Figure 2, Coulomb scattering dominates the field effect mobility under low electric fields, with surface roughness scattering dominating under high electric fields as carriers are strongly attracted to the semiconductor surface under high applied biases and therefore have more interactions with the surface.

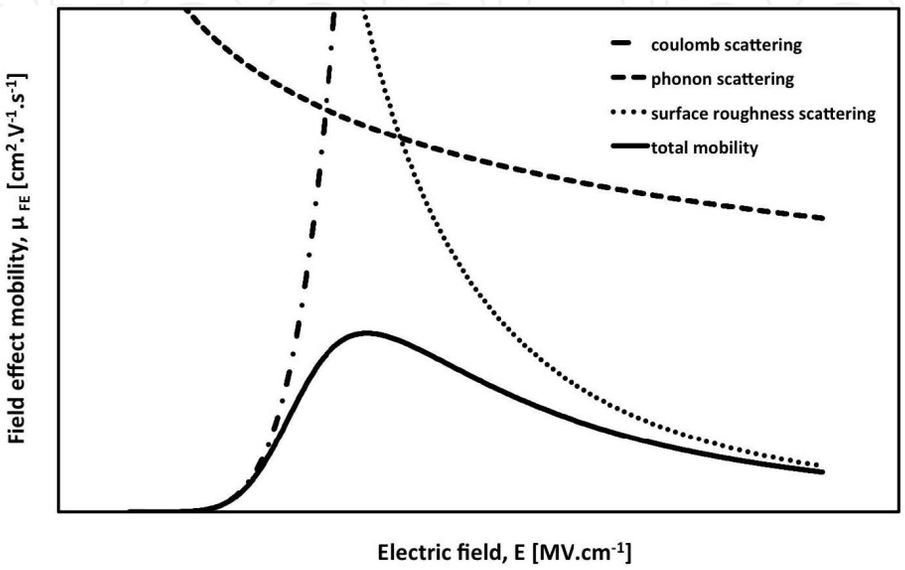


Figure 2. Schematic representation of the field effect mobility in an n-type MOSFET channel

4. Current status of the technology

The current status of MOSFET technology is still plagued by low channel mobility and oxide reliability issues due to issues with the 4H-SiC/dielectric interface, which is believed to be due to an unoptimised dielectric formation and post-oxidation anneal procedure. There has been a significant amount of research into the effects of varying the post-oxidation anneal conditions, including the use of hydrogen, oxygen, nitrogen and phosphorus anneal environments, which have previously been used to passivate interface traps in silicon technology. This has led to advances in the capabilities of the technology, and MOSFET field effect mobilities of over $100\ cm^2 \cdot V^{-1} \cdot s^{-1}$ have been reported in n-channel MOSFETs formed in Al-implanted regions, after performing a post deposition anneal in $POCl_3$ [18].

5. Fabrication techniques and process variations

Complementary metal–oxide semiconductor (CMOS) devices fabricated using the three gate dielectrics summarised in Table 1 were examined using electrical characterisation techniques.

The remaining process steps utilised in their fabrication were identical. The main aim of this investigation is to highlight the benefits and potential issues of each processing technique on the electrical performance of the devices under test.

The CMOS test structures reported here were fabricated on a 100 mm, Si face, 4° off axis, 4H SiC n^+ wafer with a doped epitaxial layer. N- and p-type regions and the source and drain regions were formed by ion implantation. The implants were annealed at high temperature with the surface protected by a carbon cap. A thick field oxide and a thin gate dielectric region were then formed and doped polysilicon gate electrodes. Nickel-based contacts were then formed on the doped regions and a refractory metal interconnect was deposited and patterned. Next, a thin nickel top layer was applied to protect the pads from oxidation during probe testing at elevated temperatures. Finally, an oxide layer was deposited for final passivation and scratch protection, and openings were made for bond pads. A schematic of the device cross section is shown in Figure 3.

Sample	Initial process	Dielectric	Post-oxidation anneal
HV06		Dry oxidation at 1200 C	O_2 950 C N_2 1200 C
CR25	Dry oxidation at 1200C with phosphorous anneal and strip	Deposited undoped oxide	H_2O 875 C N_2 1100 C
CR27		Dry oxidation stub oxide Deposited phosphorous doped	Steam 950 C

Table 1. Summary of the dielectric process conditions

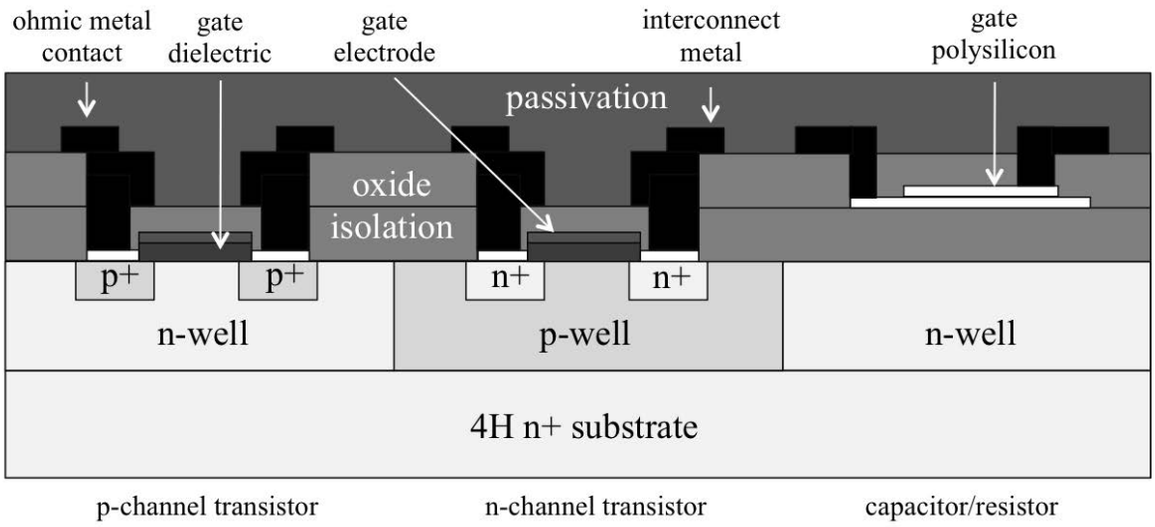


Figure 3. Schematic cross section of the completed transistor structures

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6. Temperature-dependent electrical characteristics of 4H-SiC MOSFETs

In the following subsections, the current-voltage characteristics are extracted and explored for the three different dielectric samples (HV06, CR25 and CR27) on both n-channel and p-channel 4H-SiC MOSFETs. This involved the extraction of the field effect mobility μ_{FE}, subthreshold slope (*SS*) and threshold voltage V_{TH} from the measured V_{GS} –I_{DS} characteristics across a temperature range of 298 K to 498 K with 50 K increments in order to understand the effect of the dielectric processing treatment on the MOSFET characteristics. The extracted field effect mobility for each of the samples is also fitted to the theoretical model for mobility using equation 6 in order to predict the mobility-limiting mechanisms for each of the MOSFETs and the impact of temperature on the mobility-limiting mechanisms involved. All of the electrical characteristics discussed in this chapter were extracted using a Keithley 4200 SCS Parameter Analyser.

7. Temperature-dependent electrical characteristics of n-channel 4H-SiC MOSFETs

The data shown in Figures 4, 5 and 6 show the V_{GS} –I_{DS} and V_{GS} -$log(I_{DS})$ characteristics for a typical 400x1.5 μm n-channel MOSFET for HV06, CR25 and CR27, respectively, measured from 298 K to 498 K. The drain bias in each of the measurements was 500 mV. Each of the samples shows a similar trend and there is an increase in drain current, a reduction in threshold voltage and a change in the subthreshold slope with increasing temperature. The data for HV06 in Figure 4 shows a much higher off-state leakage current, with subthreshold drain currents consistently around 0.1 nA, whereas the data for both CR25 (Figure 5) and CR27 (Figure 6) show reverse leakage current of approximately 1 pA. The off-state conduction could be due to counter doping in the channel region, which could be a product of the threshold-adjust implant [19]. This counter doping could have also been increased as an unwanted effect during the 1200 C to the N_2O post-oxidation anneal that was performed on the dielectric as described in Table 1.

The increase in current with temperature observed in Figures 4.a, 5.a and 6.a for the three samples is due to the decrease of occupied interface traps with an increasing temperature, which is an agreement with the density of interface traps data extracted from capacitor test structures fabricated monolithically with the MOSFETs. As the density of interface traps decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the channel. This finding also supports previous work conducted in the field [14].

The observed reduction in threshold voltage with temperature is also evident for each of the transistors across the temperature range and values extracted using linear interpolation of the I_{DS} –V_{GS} characteristics are summarised in Figure 7. The threshold voltage can be calculated using equation 13:

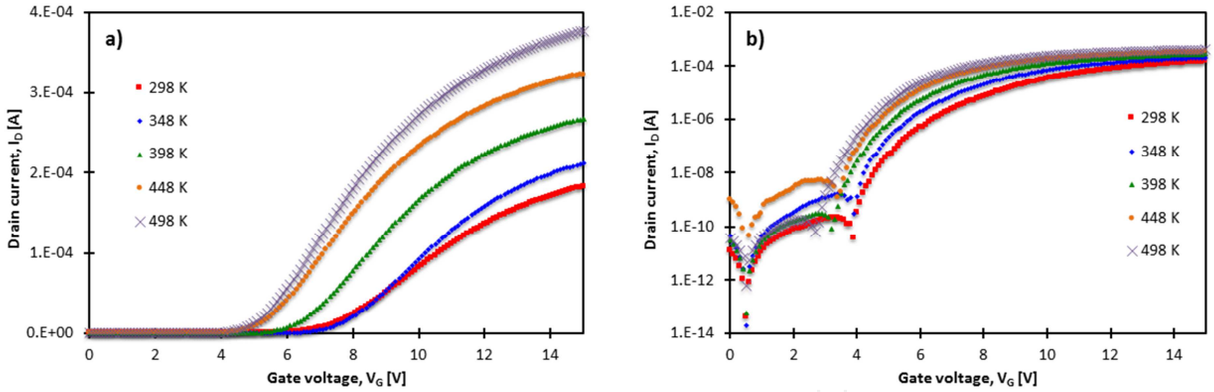


Figure 4. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process HV06

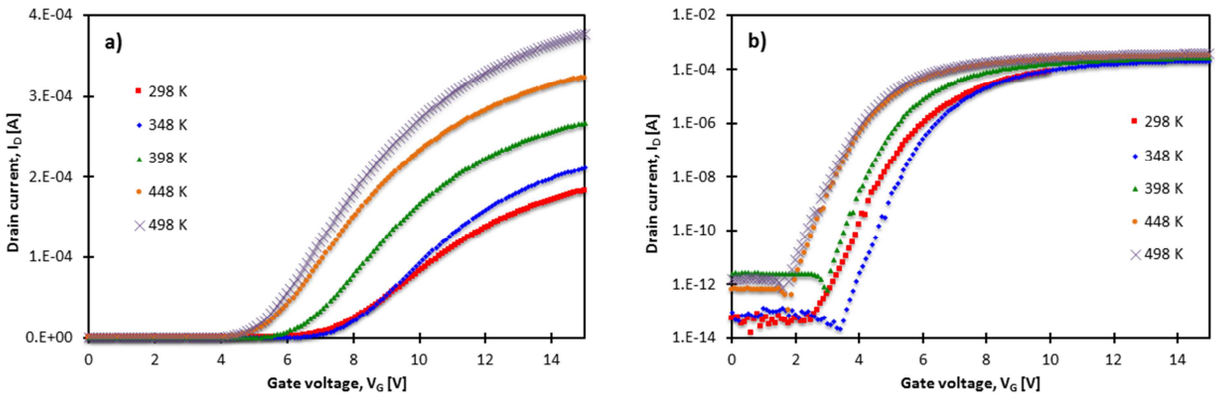


Figure 5. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process CR25

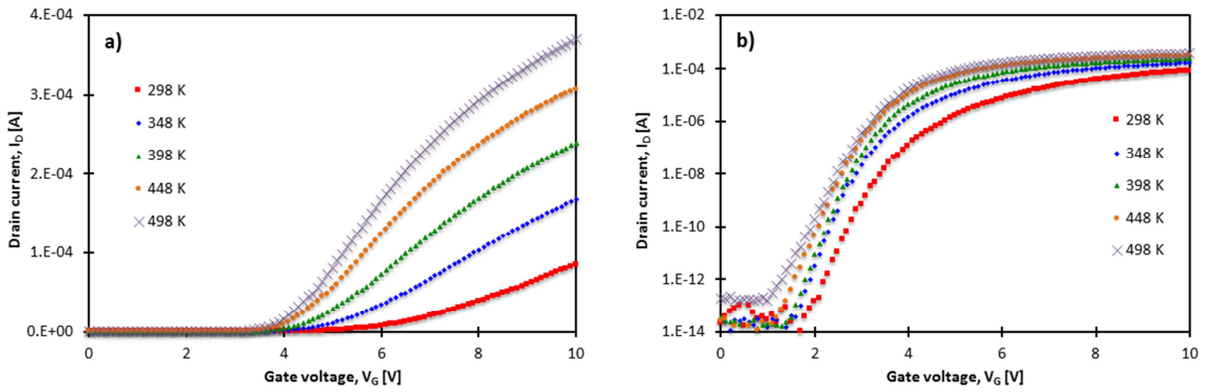


Figure 6. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process CR27

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$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_o \varepsilon_s q N_A 2\phi_B}}{C_i} \tag{13}$$

The observed shift in threshold voltage with temperature is due to the reduction in the surface band bending required for inversion, which is due to the increase in intrinsic carrier concentration and the decrease in band gap energy with an increase in temperature as described previously [20].

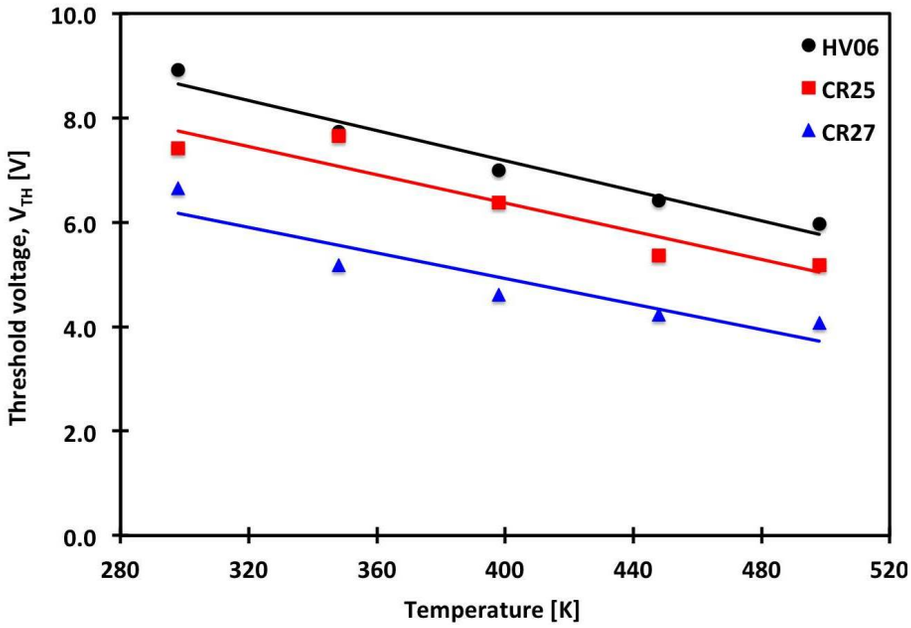


Figure 7. Variation of MOSFET threshold voltage with temperature

However, a change at the interface and within the depletion layer can also act to modify the gate voltage as V_{FB} is dependent on the amount of charge trapped at the silicon carbide–oxide interface, as shown by equation 14:

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{it}}{C_i} \tag{14}$$

where ϕ_{ms} is the metal–semiconductor work function difference.

The data in Figure 8 shows the variation in subthreshold slope (*SS*) as a function of temperature for each of the dielectrics studies. As shown by the data, both HV06 and CR27 show an increase in *SS* with temperature, whereas CR25 shows a decrease in *SS*. An increase in the subthreshold slope with increasing temperature is expected, as *SS* is proportional to kT/q. The decrease of *SS* with temperature that is witnessed for CR25 suggests that there is a change in the interface

trapped charge at the semiconductor dielectric interface as subthreshold slope is also dependent on the interface trap capacitance (C_{it}) as detailed in equation 15:

$$SS = ln(10)\left(\frac{kT}{q}\right)\left(\frac{C_i + C_D + C_{it}}{C_i}\right) \tag{15}$$

where C_D is equal to the capacitance of the depletion region in the semiconductor formed under the oxide layer [21].

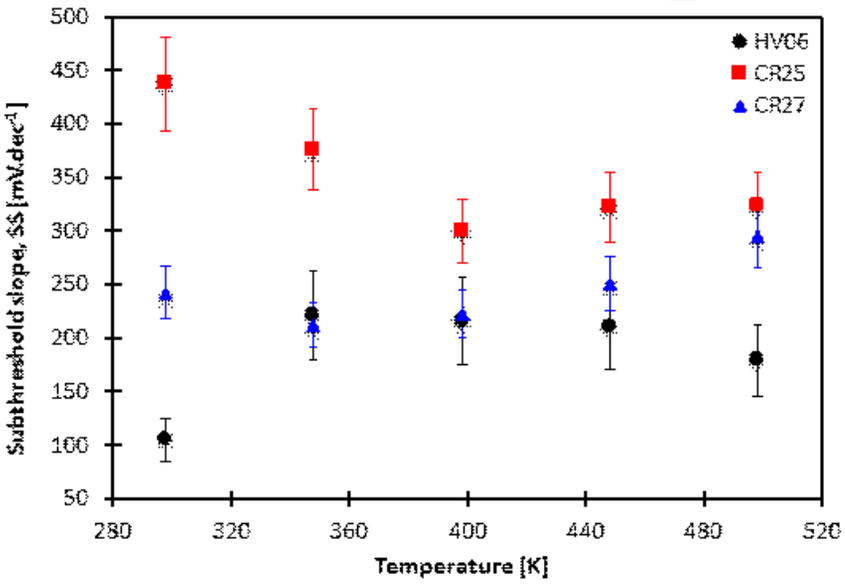


Figure 8. Variation of extracted subthreshold slope with temperature, for 400x1.5 μm n-channel MOSFETs

This observed in subthreshold slope with temperature is in agreement with the change in interface trap density with temperature that was witnessed in capacitor test structures for both the CR25 n-type and p-type MIS capacitors that were analysed using Terman analysis. This change is most likely due to the change in D_{it} with temperature, which was observed at both the conduction band and valence band edges in the semiconductor for both the n-type and p-type CR25 MIS capacitors, respectively. The data in Figure 9 shows a plot of D_{it} as a function of temperature as extracted from the subthreshold slope of each of the MOSFET devices using equation 15. As can be observed from the data, the change in D_{it} for CR25 is significantly higher than that observed in either HV06 or CR27, decreasing from 3×10^{12} to 1.5×10^{12} cm^{-2} eV^{-1} between 298 and 498 K.

The data in Figures 10(a), 11(a) and 12(a) show the variation in field effect mobility with electric field (μ_{FE} *-E)* for a 400×1.5μm n-channel MOSFET measured between 298 and 498 K taken from samples HV06, CR25 and CR27, respectively. The field effect mobility was extracted from the V_{GS} –I_{DS} data sets shown in Figures 4(a), 5(a) and 6(a) by means of equation 2. All data sets exhibit a similar trend, with increasing maximum field effect mobility with increasing

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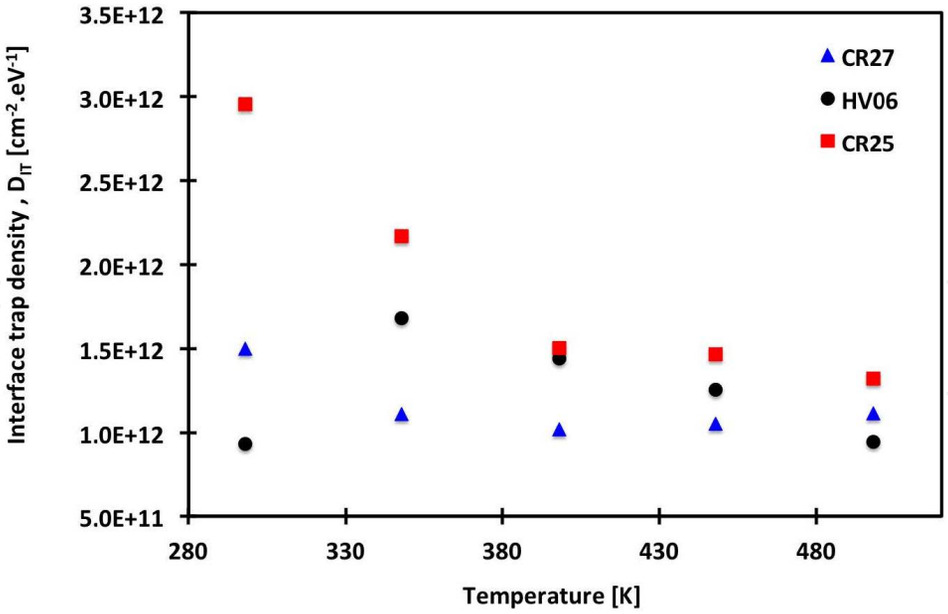


Figure 9. Variation of extracted interface trap density (D_{it}) from the subthreshold slope of 400x1.5 μm n-channel MOSFETs

temperature. The data in Figure 12(a) for sample CR27 shows the highest field effect mobility across the temperature range out of the three samples as supported by the data in Figure 16, which shows the peak field effect mobility of each device against temperature.

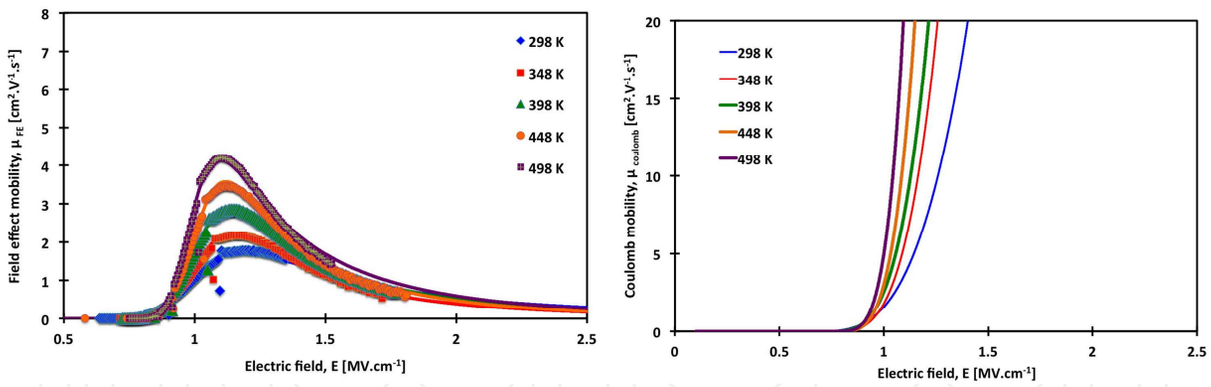


Figure 10. (a) μ_{FE} -E and (b)μ_C-E characteristics of 400x1.5 μm HV06 n-channel MOSFET at different temperatures

Figures 10(b),11(b) and 12(b) show the Coulomb mobility values that were fitted to the measured characteristics using equation 11. As shown by the data, all of the devices show an increase in Coulomb mobility with increasing temperature, which suggests that the effect of Coulomb scattering reduces with an increase in temperature. The data sets also show that the electric field at which the mobility increases from zero (the λ parameter in equation 12) does not show a significant variation with temperature; however, the Φ term used to describe the change in mobility with electric field does, especially for the HV06 data.

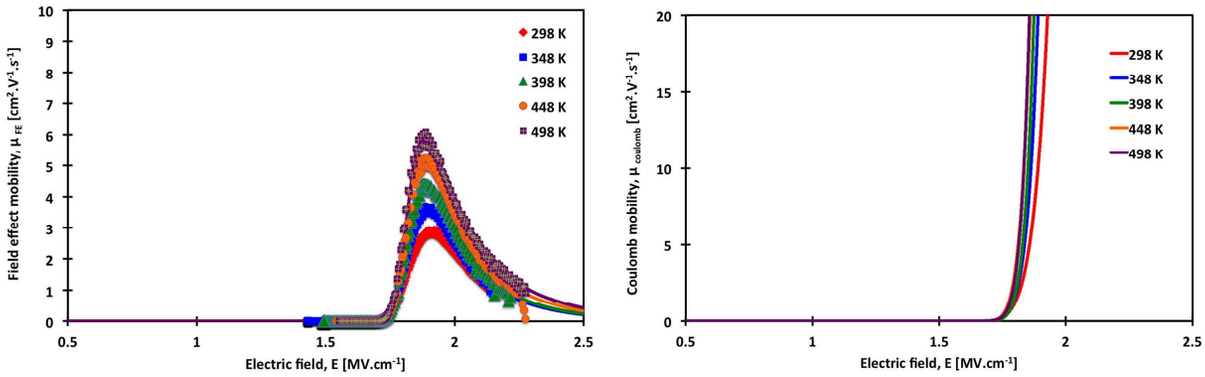


Figure 11. (a) μ_{FE} -E and (b) μ_C -E characteristics of 400x1.5 μm CR25 n-channel MOSFET at different temperatures

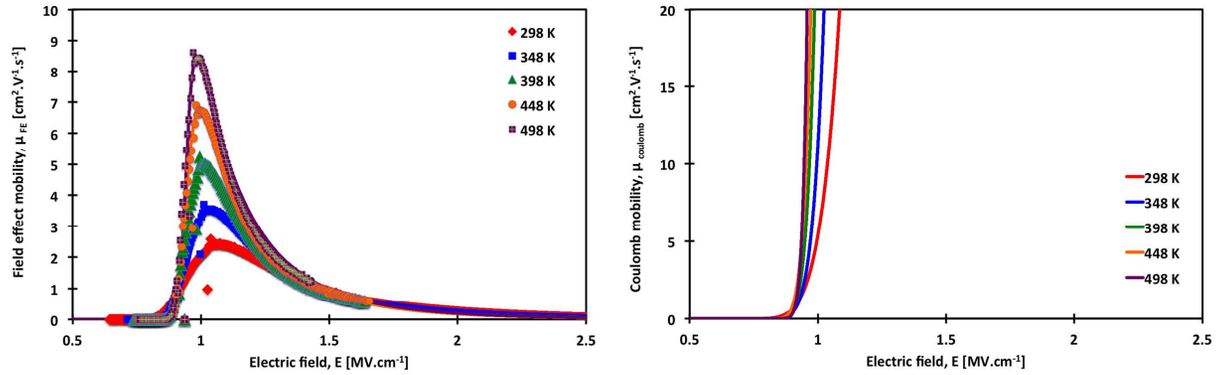


Figure 12. (a) μ_{FE} -E and (b)μ_C-E characteristics of 400x1.5 μm CR27 n-channel MOSFET at different temperatures

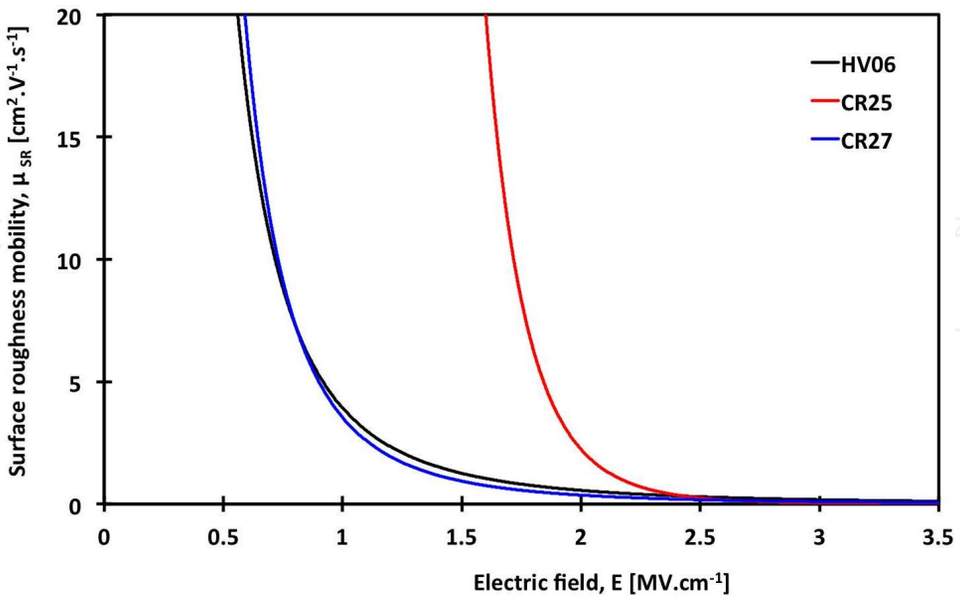


Figure 13. Surface roughness mobility (μ_{SR}) as a function of electric field for 400×1.5 μm n-channel MOSFETs at 298 K

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At high electric fields, the extracted values of μ_{FE} for each of the devices is severely limited by surface roughness scattering as shown by the data in Figures 10(a), 11(a) and 12(a). The data in Figure 13 shows the extracted μ_{SR} as a function of electric field for each of the samples at 298 K. This clearly identifies that the observed surface roughness mobility varies dependent on the dielectric under investigation. HV06 and CR27 show the lowest surface roughness mobility, which suggests that surface roughness scattering is higher within those devices. CR25 shows the highest surface roughness mobility, which suggests that the process techniques used in the fabrication of this sample produce the highest quality dielectric-semiconductor interface out of the 3 samples investigated. The data in Figures 14(a), 14(b) and 14(c) show the values of μ_{SR} fitted to each of the extracted MOSFET μ_{FE} characteristics between 298 and 498 K. The negligible temperature dependence observed in the high field regime for all three of the devices supports previously reported observations on 4H-SiC MOSFETs and shows that the experimental μ_{SR} has the same functional form as equation 10.

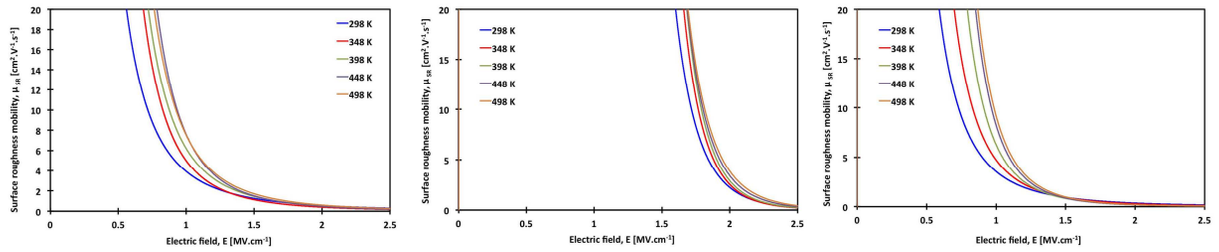


Figure 14. μ_{SR} -E characteristics of a 400×1.5 μm n-channel MOSFET from (a) HV06, (b) CR25 and (c) CR27 samples

The data shown in Figure 15 shows the theoretical acoustic phonon mobility (μ_{AC}) fitted to each sample using equation 9. The values of the fitting parameters were identical for each of the samples studied, for both n-channel and p-channel devices, and were based on values reported in the literature [5, 8]. The value of B is 1.0×10^6 cm s^{-1}, C is 3.23×10^6 K cm s^{-1} and α is 0.0284. As shown by the data in Figure 15, the modelled acoustic phonon mobility is consistently above 150 cm^2 V^{-1} s^{-1} across the entire investigated electric field and temperature range. As this is significantly higher than both μ_{SR} and μ_C, it has a negligible effect on the experimentally measured field effect mobility in each of the devices. The experimentally determined characteristics are consistently dominated at low and high electric fields by Coulomb and surface roughness scattering, respectively, as shown by the data in Figures 10(a), 11(a), 12(a) and 14.

The data in Figure 16 shows the variation in the peak field effect mobility with temperature for the three dielectrics studies. It is apparent that sample HV06 consistently shows the lowest channel mobility, whilst CR27 shows the most significant variation with temperature, giving the highest mobility at temperatures above 350 K. The main limiting factor that is witnessed across all of the samples is that of severely low surface roughness mobility, which acts to dominate the device mobility characteristics from electric fields above 1 MV cm^{-1}. The extracted surface roughness mobility reported here for all three dielectric processes is approximately an order of magnitude lower than other 4H-SiC MOSFETs that have previously been reported,

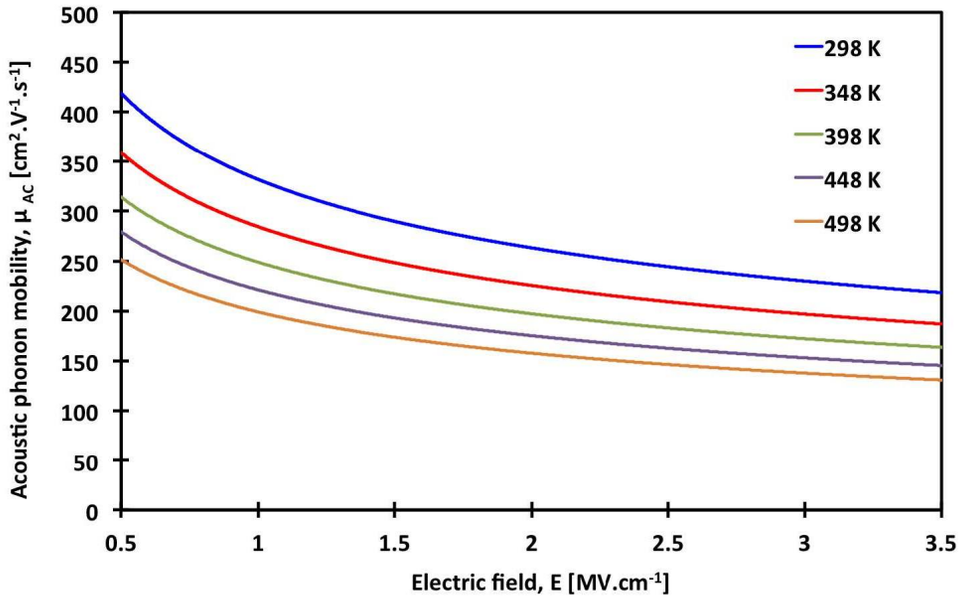


Figure 15. Predicted μ_{AC} -E characteristics of a 400×1.5 μm n-channel MOSFET

which showed field effect mobility of consistently over 20 $cm^2\ V^{-1}\ s^{-1}$ at high electric fields [8, 22-25].

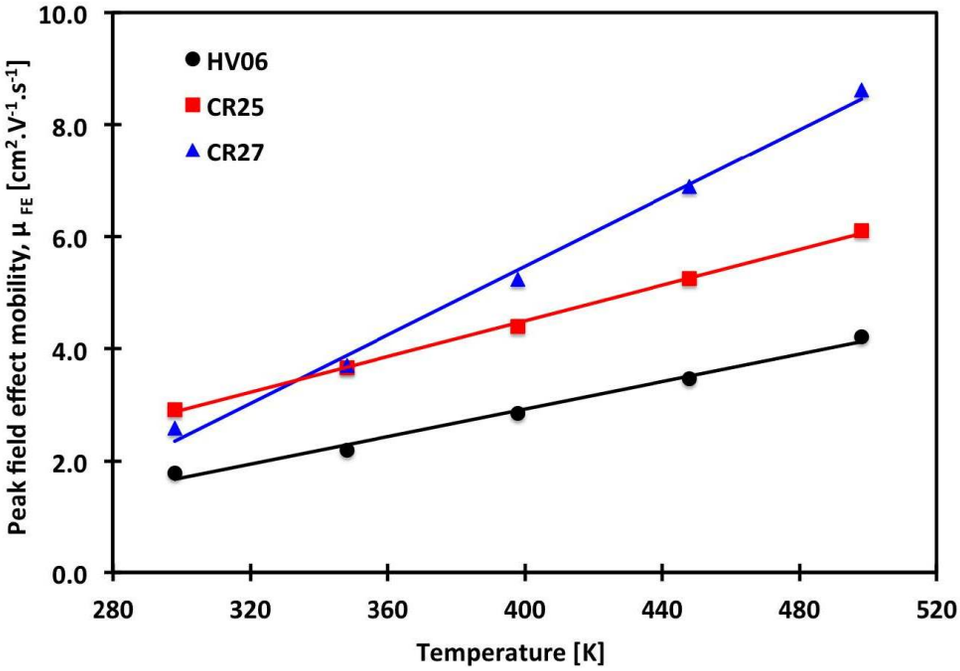


Figure 16. Variation of peak field effect mobility (μ_{FE}) with temperature for a 400×1.5 μm n-channel MOSFET

The data in Table 2 shows the fitting parameters used to generate the mobility plots for the n-channel FETs reported here.

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HV06	Acoustic phonon		Surface roughness		Coulomb
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^{7}	3.2×10^{6}	3.0×10^{17}	2.81	3.20
348	1×10^{7}	3.2×10^{6}	5.0×10^{22}	3.67	3.40
398	1×10^{7}	3.2×10^{6}	1.9×10^{22}	3.58	3.58
448	1×10^{7}	3.2×10^{6}	7.4×10^{24}	4.00	3.70
498	1×10^{7}	3.2×10^{6}	5.8×10^{22}	3.65	4.28
CR25	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^{7}	3.2×10^{6}	2.3×10^{62}	9.84	5.88
348	1×10^{7}	3.2×10^{6}	2.5×10^{70}	11.1	7.00
398	1×10^{7}	3.2×10^{6}	9.3×10^{70}	11.2	7.92
448	1×10^{7}	3.2×10^{6}	8.8×10^{65}	10.4	6.32
498	1×10^{7}	3.2×10^{6}	4.1×10^{62}	9.84	8.23
CR27	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^{7}	3.2×10^{6}	1.9×10^{20}	3.29	5.11
348	1×10^{7}	3.2×10^{6}	6.1×10^{24}	4.02	5.65
398	1×10^{7}	3.2×10^{6}	5.8×10^{30}	4.99	6.42
448	1×10^{7}	3.2×10^{6}	1.5×10^{34}	5.54	6.23
498	1×10^{7}	3.2×10^{6}	1.3×10^{34}	5.53	8.98

Table 2. Fitting parameters to the mobility models used to describe the behaviour of n-channel MOSFET structures

8. Temperature-dependent electrical characteristics of p-channel 4H-SiC MOSFETs

The data in Figures 17, 18 and 19 show the V_{GS} –I_{DS} and V_{GS} -$log(I_{DS})$ characteristics for a 1600×1.5 μm p-channel MOSFET from the HV06 sample and an 8000×1.5 μm CR25 and CR27 p-channel MOSFET, respectively, measured from 298 to 498 K. The drain bias in each of the measurements was 500 mV. The data for each of the samples exhibits a similar trend, showing an increase in drain current with increasing temperature, a change in threshold voltage and a change in the subthreshold slope across the measured temperature range. In contrast to the n-channel data shown in Figures 4(b), 5(b) and 6(b), all p-channel samples exhibit a very low reverse leakage current of below 1 pA as shown in Figures 17(b), 18(b) and 19(b).

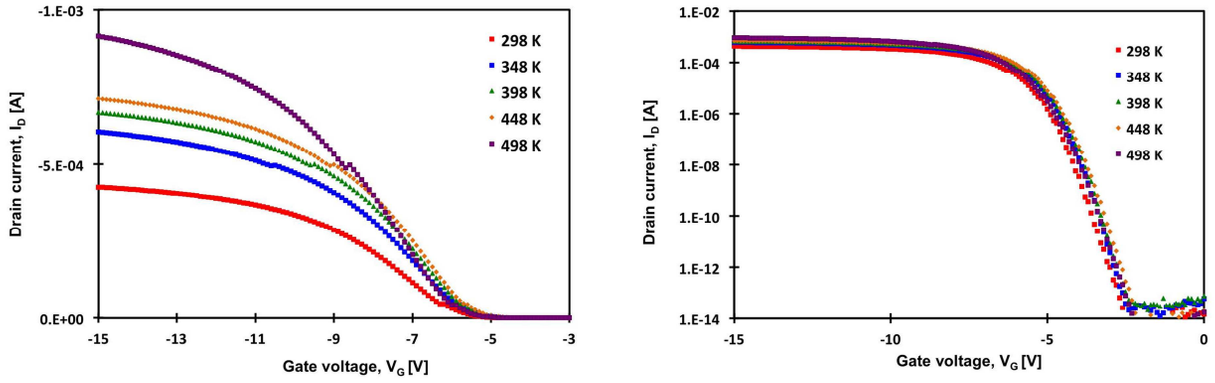


Figure 17. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 1600×1.5 μm p-channel MOSFET from sample HV06

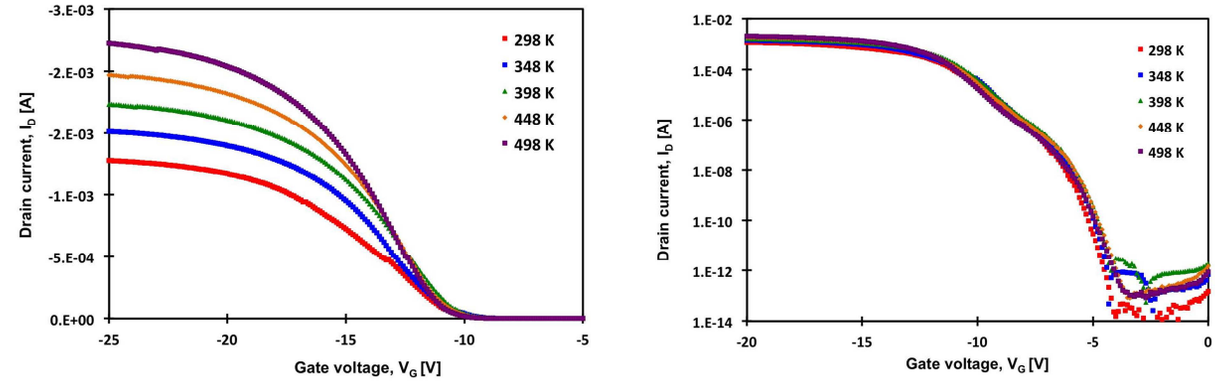


Figure 18. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR25

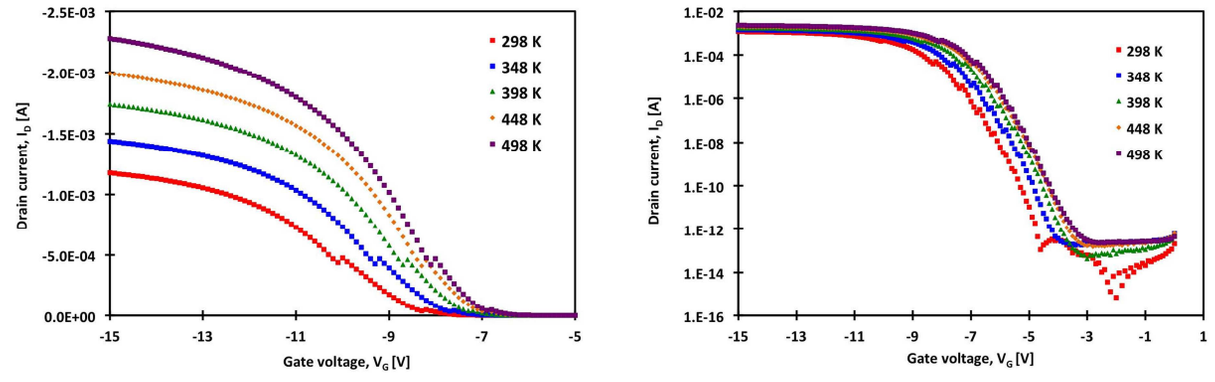


Figure 19. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR27

The change in threshold voltage with temperature is also shown for each of the transistors across the temperature range by the data in Figure 20. The threshold voltage of a MOSFET can be calculated using equation 13 [21], and as with the n-channel devices, CR27 shows a reduction (i.e. becoming closer to zero) in V_{TH} with increasing temperature due to the reduction

in the surface band bending required for inversion. This observation is identical to that observed in the n-channel data and is due to the increase in intrinsic carrier concentration and the decrease in band gap energy with increasing temperature. The data for HV06 shows a minimal change in V_{TH} with increasing temperature. However, in contrast, the data for CR25 shows an increase in V_{TH} with temperature. This could be due to a change in the interfacial charge or a change in the charge within the depletion layer, which can also act to modify the gate voltage as V_{FB} is dependent on the charge trapped at the silicon carbide–oxide interface. This is likely to be due to the increase in D_{it} with temperature that was witnessed in monolithically fabricated MOS capacitor structures and the effects of mobile oxide charge present within the dielectric.

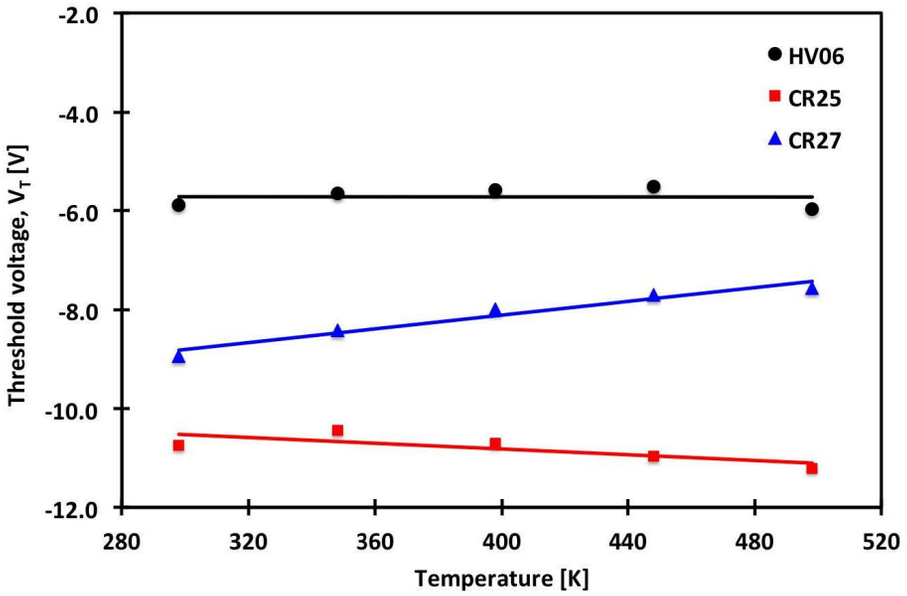


Figure 20. Threshold voltage as a function of temperature for 1.5 μm gate length p-channel MOSFETs

The increase in current with temperature that can be observed from the data shown in Figures 17(a), 18(a) and 19(a) for the three dielectrics studied is due to the decrease of occupied interface traps with an increase in temperature, which is an agreement with D_{it} values extracted from capacitor-based test structures fabricated monolithically with the MOSFETs. As the density of interface traps (D_{it}) decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the MOSFET channel, as observed in previous reports in the literature [14].

The data in Figure 21 shows the variation in subthreshold slope (SS) with temperature for each of the samples. As shown, all three samples show an increase in SS with temperature. An increase in SS with temperature is expected, since SS is proportional to kT/q. The variation in SS with temperature is also influenced by the density of interface trapped charge (D_{it}) at the silicon carbide–oxide interface as SS is also dependent on the interface trap capacitance (C_{it}) as outlined in equation 14. This is in agreement with the trend witnessed for the equivalent n-channel MOSFET samples with the exception of sample CR25. The n-channel equivalent

sample for CR25 showed a decrease in *SS* with temperature, whereas the p-channel device exhibits an increase in *SS* for increasing temperature, and the observed change is much smaller than that of the n-channel device. This is related to the experimentally measured variation in D_{it} over the measured temperature range on monolithically fabricated capacitor test structures.

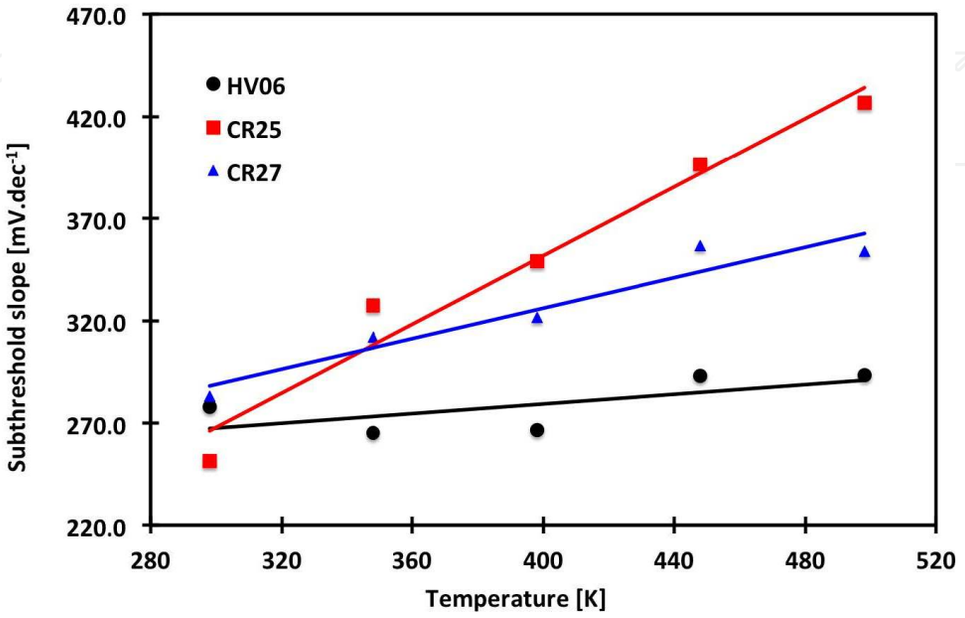


Figure 21. Subthreshold slope as a function of temperature for 1.5 µm gate length p-channel MOSFETs

The data shown in Figures 22, 23 and 24 show the variation of μ_{FE} -*E* and the μ_C -*E* characteristics for the 1.5 µm gate length p-channel MOSFETs on HV06 and CR25 and CR27, respectively, measured from 298 to 498 K. The data sets for all three dielectrics show evidence of an increase in field effect mobility with increasing temperature, and the data for CR27 in Figure 24 shows the highest field effect mobility out of the three samples across the temperature range studied.

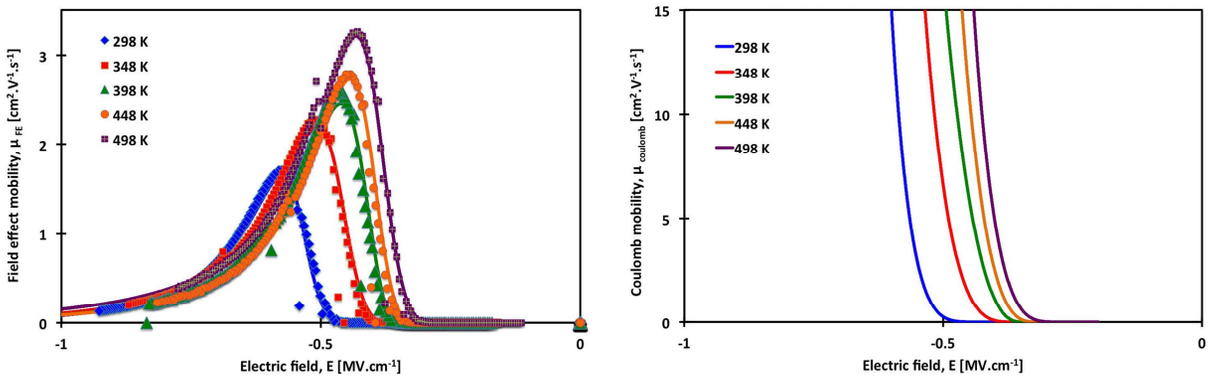


Figure 22. (a) μ_{FE} -E and (b) μ_C -E characteristics of a 1600×1.5 µm p-channel MOSFET from sample HV06

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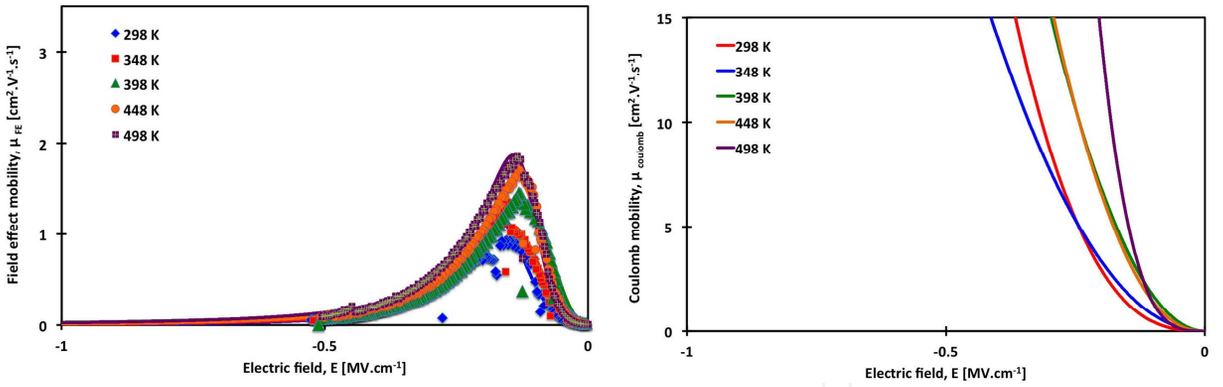


Figure 23. (a) μ_{FE} -E and (b) μ_C -E characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR25

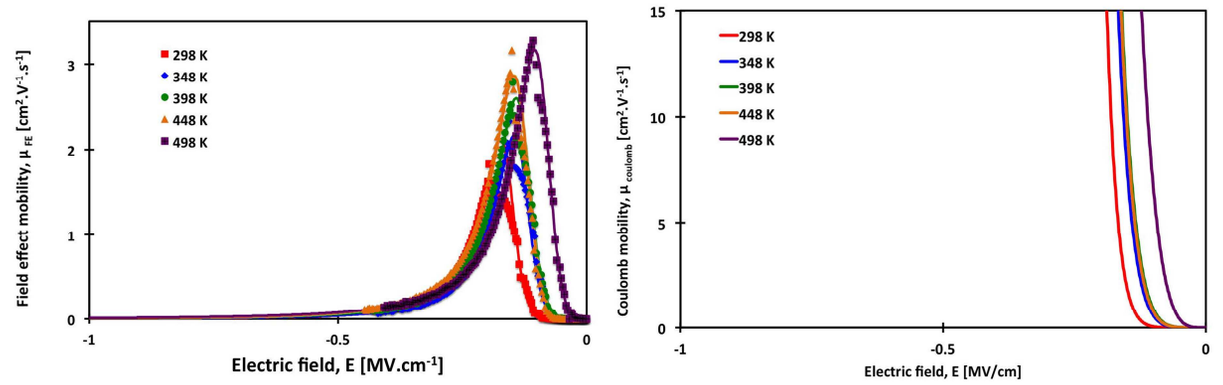


Figure 24. (a) μ_{FE} -E and (b) μ_C -E characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR27

The data in Figures 22, 23 and 24 show the μ_{FE} -*E* and μ_C -E characteristics for 1.5 μm p-channel MOSFETs on HV06, CR25 and CR27 extracted from experimental V_{GS} –I_{DS} measurements taken at temperatures between 298 and 498 K that are shown in Figures 17, 18 and 19 using equation 2. All devices studied exhibit a similar trend and show an increase in field effect mobility with increasing temperature. The field effect mobility data for CR27 shown in Figure 24 demonstrates the highest field effect mobility across the temperature range out of the three samples, as supported by the data shown in Figure 25, which shows the peak field effect mobility of each device against temperature.

The data in Figures 22(b), 23(b) and 24(b) show the Coulomb mobility mechanism that was fitted to the measured characteristics using equation 11. As shown by the data in the figures, all of the devices (HV06, CR25 and CR27) show an increase in mobility with increasing temperature, which suggests that the effect of Coulomb scattering reduces with increasing temperature due to the reduction of interface trapping effects with increasing temperature. The same phenomenon was also witnessed in the equivalent n-channel MOSFETs, which suggest that the dominant mobility mechanisms are dominated by the processing of the gate dielectric for both the n- and p-channel devices.

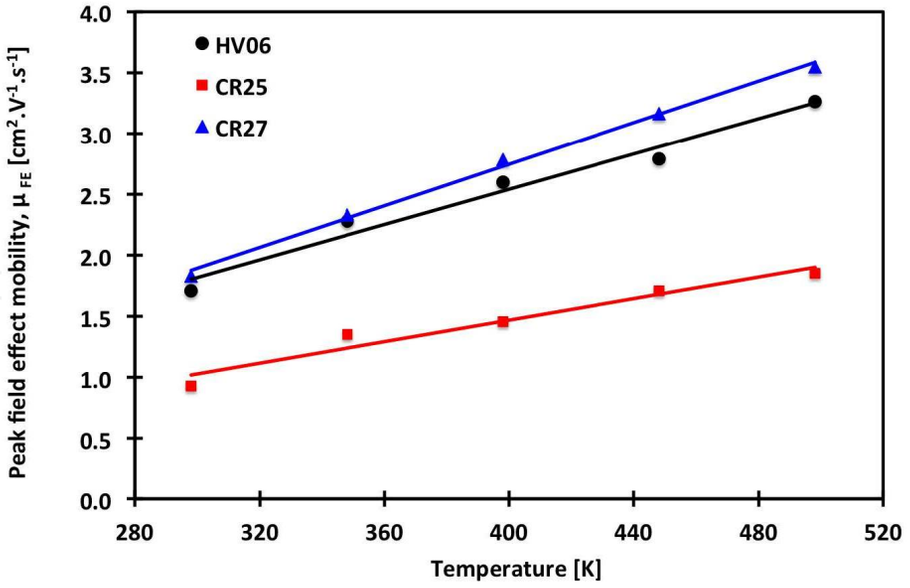


Figure 25. Peak field effect mobility (μ_{FE}) as a function of temperature for 1.5 μm gate length p-channel MOSFETs

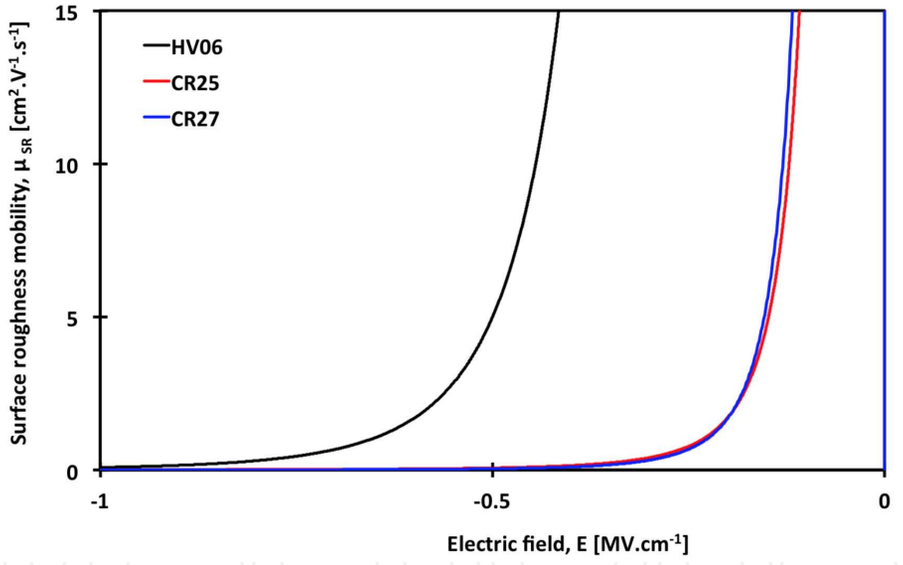


Figure 26. μ_{SR} -E characteristics of a 1600 x 1.5 μm HV06 and an 8000 x 1.5 μm CR25 and CR27 p-channel MOSFET at 298 K

At high electric fields, the extracted μ_{FE} for each of the devices is limited by surface roughness scattering as shown by the data in Figures 26 and 27, where the predicted μ_{SR} mobility fits to each of the extracted MOSFET μ_{FE} characteristics between 298 and 498 K. A negligible temperature dependence is exhibited by all three devices, which supports previous analysis performed on 4H-SiC MOSFETs and shows that the experimentally extracted μ_{SR} characteristics have the same functional form as expressed in equation 10 [5]. The data in Figure 26 shows the variation of the fitted surface roughness (μ_{SR}) as a function of electric field for each of the

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samples as 298 K. The data clearly identifies that the surface roughness mobility is different for each of the dielectrics under investigation. HV06 shows the highest surface roughness mobility, which suggests that surface roughness scattering is lower within the device and produces the highest quality dielectric–semiconductor interface out of the three samples investigated. The data for samples CR25 and CR27 show an almost identical surface roughness mobility across the measured electric field range, which suggests that the process techniques used in the fabrication of those samples produce a very similar quality of interface. However, all of the devices show very low field effect mobility at high electric fields, which is lower than recently reported values for 4H-SiC devices, such as those summarised in Table 4.

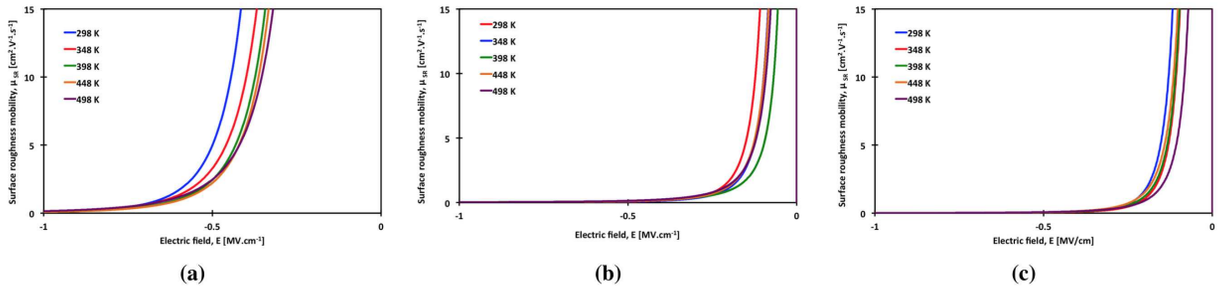


Figure 27. μ_{SR} -E characteristics of a 1600 x 1.5 μm (a) HV06 and an 8000 x 1.5 μm (b) CR25 and (c) CR27 p-channel MOSFET from 298 to 498 K

The data in Table 3 shows the fitting parameters used to generate the mobility plots for the p-channel FETs reported here.

This indicates that there is something common to all three dielectric processes that consistently act to reduce the surface roughness mobility. This could be due to the topography of the 4H-SiC epitaxial layer that was used for the fabrication of the devices or could potentially be a contribution of surface damage due to the ion implantation doping or the post-implantation anneal process that was used to form the n-type regions that are employed across all of the p-channel devices. In order to establish if this is the true cause, an investigation of the surface morphology using a technique such as atomic force microscopy is required, with measurements performed after the implantation and anneal process to measure the surface roughness, which could then be correlated to the measured electrical characteristics of the devices. A limited amount of data is available from a similar study conducted on n-channel 4H-SiC MOSFETs to establish the impact of the morphological and electrical properties of the SiO_2–4H-SiC interface on the mobility behaviour of 4H-SiC MOSFETs. The results indicated that a higher mobility can be observed in devices with a larger root-mean-square (RMS) roughness of the channel surface, possibly due to lower values of D_{it} associated to faceted surface morphologies [26]. However, this limited data contradicts observations made on other semiconductor systems, such as silicon and silicon-germanium. However, in the case of silicon carbide, evidence indicates a strong dependence between carrier mobility and the crystal surface from which the device is fabricated [27].

HV06	Acoustic phonon		Surface roughness		Coulomb
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	3.7×10^{34}	5.9	5.0
348	1×10^6	3.2×10^6	7.2×10^{28}	5.0	3.7
398	1×10^6	3.2×10^6	6.2×10^{27}	4.8	2.6
448	1×10^6	3.2×10^6	1.5×10^{27}	4.7	3.3
498	1×10^6	3.2×10^6	2.5×10^{23}	4.0	4.1
CR25	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	1.2×10^{19}	3.6	2.7
348	1×10^6	3.2×10^6	8.3×10^{15}	3.0	2.1
398	1×10^6	3.2×10^6	3.2×10^{11}	2.2	2.0
448	1×10^6	3.2×10^6	1.1×10^{15}	2.8	2.1
498	1×10^6	3.2×10^6	2.4×10^{13}	2.5	3.4
CR27	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	10.0×10^{21}	4.1	9.1
348	1×10^6	3.2×10^6	1.2×10^{19}	3.6	6.4
398	1×10^6	3.2×10^6	2.2×10^{18}	3.4	6.0
448	1×10^6	3.2×10^6	1.4×10^{18}	3.4	6.2
498	1×10^6	3.2×10^6	1.9×10^{14}	2.7	4.1

Table 3. Fitting parameters to the mobility models used to describe the behaviour of p-channel MOSFET structures

The data in Figure 28 shows the predicted values for the mobility limited by acoustic phonon scattering (μ_{AC}) based on equation 9. The parameters used to generate the values for μ_{AC} are identical to those used in the n-channel devices reported in a previous section and have been taken from the literature [5,8]; B is 1.0×10^6 cm s^{-1}, C is 3.23×10^6 K cm s^{-1} and α is 0.0284. As shown by the data in Figure 28, the modelled acoustic phonon mobility is consistently above 150 cm^2 V^{-1} s^{-1} for electric fields below 3.5MV cm^{-1} for the temperature range studied. Because the predicted mobility is significantly higher than both μ_{SR} and μ_C, the field effect mobility of a p-channel MOSFET is not determined by a contribution from acoustic phonon scattering. As observed with the n-channel data, the characteristics are consistently dominated at low and high electric fields by Coulomb and surface roughness scattering as shown by the data in Figures 22(b), 23(b), 24(b) and 27.

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Ref	Device	Gate dielectric	Gate dimensions (W×L μm)	Peak μ_{FE} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	V_T (V)	T_{ox} (nm)	D_{it} ($cm^{-2} \cdot eV^{-1}$)
28	n-FET	SiO_2 (pyro)	10×150	6.2	5.8	47	7.1×1011
		SiO_2 (pyro + NO)		30.4	2.7	51	1.3×1011
29	n-FET	SiO_2 (dry)	120×400	4	5		
		SiO_2 (dry +NO)		30			
30	n-FET	SiO_2 (dry + NO)	320×40	34		125	
31	n-FET	SiO_2 ($POCl_3$ POA)	30×200	89	0	56	9×10^{10}
32	n-FET	SiO_2 ($POCl_3$ PDA)		108		45	5×10^{11}
33	n-FET	SiO_2 (P_2O_5 POA)	150×290	72			3×10^{11}
34	n-FET	SiO_2 (N_2O POA)	150×290	55			3×10^{11}
35	n-FET	SiO_2 (N_2O PDA)	40×16	40		30	7.2×10^{11}
36	n-FET	SiO_2 (N_2O POA)	140×50	49		54	
37	n-FET	SiO2 (NO)	200×200	31	1.6	65	
		SiO_2 (2hr N plasma)		22	1.6	50	
		SiO_2 (4hr N plasma)		34	2.0	48	
38	n-FET	SiO_2 with Na contam	400×400	90	5		
39	p-FET	SiO_2 (pyro)	10×150	5.5	-8.5	47	8.9×1011
		SiO_2 (pyro + NO)		5.6	-6.4	51	1.3×1011
40	p-FET	SiO_2 (N_2O)	100×200	10		47	1×10^{12}
41	p-FET	SiO_2 (pyro+wet+Ar)	100×150	15.6	-4.2	45	2×10^{12}
42	p-FET	SiO_2 (N_2O)	4×150	5	-6	38	1×10^{12}

Table 4. Comparison of 4H-SiC MOSFET characteristics

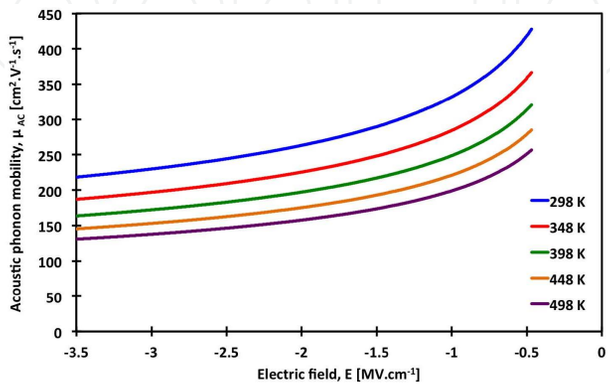


Figure 28. μ_{AC} -E characteristics for a 1.5 μm gate length p-channel MOSFET

9. Impact of gate dielectric on the 1/*f* noise characteristics of 4H-SiC MOSFETs

Low-frequency noise (1/*f* noise) measurements are used to study impurities and defects in semiconductor devices. The technique is useful to investigate device quality and reliability issues as well as the examination of the density of interface states in MOS devices. Whilst 1/*f* noise dominates the low frequency region (up to 100 kHz), it can be up converted into a high-frequency component affecting the phase noise characteristics of devices used for RF applications [43] as well as degrading the signal-to-noise ratio in analog circuitry. Very few studies of the 1/*f* noise in 4H-SiC have been explored to date [44 - 46]. Here, low-frequency noise is used to investigate how the gate dielectric influences the interface trap density and hence the characteristics of the 4H-SiC MOSFETs. The aim is to determine the impact of the interface quality and resulting noise characteristics on the device performance.

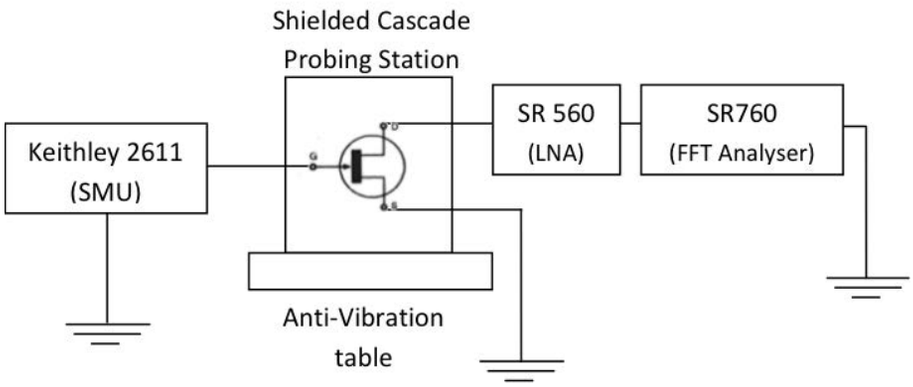


Figure 29. Schematic diagram of the low-frequency noise measurement set-up

The low-frequency noise measurements were conducted using a Stanford Research 760 FFT at 298 K, and the current-voltage characteristics that were used to normalise the characteristics were conducted on a Keithley 4200 SCS semiconductor analyser. A schematic of the measurement set-up is shown in Figure 29.

The normalised 1/*f* noise characteristics and the normalised noise power spectral density (NNPSD) for each of the dielectrics on the n-channel MOSFETs are shown in Figures 30, 31 and 32 for HV06, CR25 and CR27, respectively. The data in Figures 30(a), 31(a) and 32(a) show a plot of the NNPSD against frequency for varying V_{GS} for each of the n-channel MOSFETs studied. The data shows that each of the devices shows a similar trend, with the NNPSD decreasing with increasing gate bias, and this indicates that 1/*f* noise is higher at low gate biases (during weak inversion) and reduces at higher gate biases (at strong inversion).

Figures 30(b), 31(b) and 32(b) show the variation of normalised noise power spectrum (NNPSD) at 10 Hz as a function of V_{GS} and I_{DS} for each of the devices studied here. The trends observed in the data for each of the devices suggest that mobility fluctuations are the main contributor to the noise characteristics [47]. During weak inversion, the I_{DS} –*NNPSD* characteristics show a linear trend as shown by the data in Figure 30 (a), which suggests that carrier

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mobility fluctuations dominate the noise spectra, whereas during strong inversion and increased current levels, the dependency exhibits a different trend. This suggests that during weak inversion, the noise characteristics are dominated by carrier mobility fluctuations as a consequence or charge trapping at the interface due to Coulomb scattering as discussed in a previous section, which can be described by the McWhorter model [48]. During strong inversion, the noise characteristics reduce significantly due to the reduction in the effect of Coulomb scattering. The trends are also consistent with those reported by Rumyantsev et al. who examined the low-frequency noise characteristics of n-channel 4H-SiC with varying annealing treatments in NO [46].

CR27 exhibits the lowest noise characteristics of the three samples, which suggests that CR27 has the highest quality interface as there is a very low noise contribution from carrier mobility fluctuations at the interface, which suggests that the oxide also has the lowest trap density in the oxide out of the three dielectric samples. This is also in agreement with the findings of the D_{it} values extracted from the subthreshold slope data for CR27 that was presented in Figure 9.

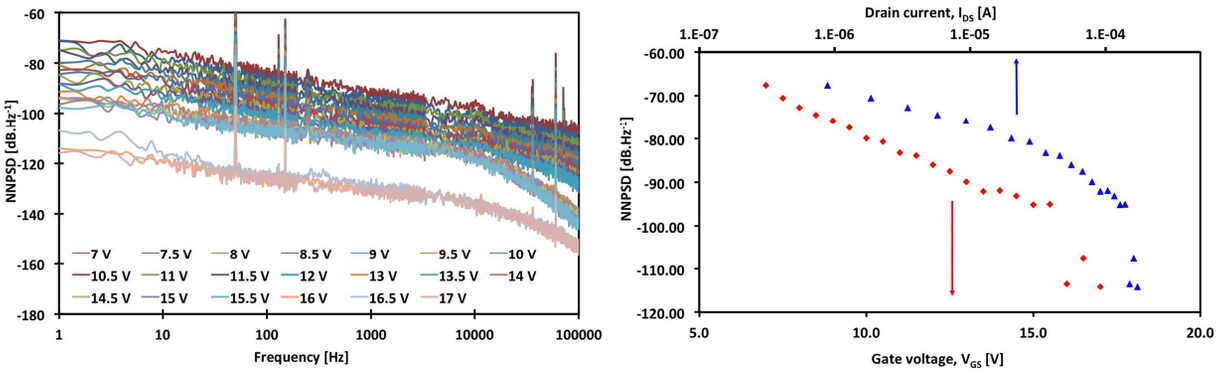


Figure 30. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with HV06 dielectric

In general, the frequency dependence of the NNPSD is described by equation 16:

$$NNPSD = \frac{\beta}{f^{\alpha}} \tag{16}$$

where α and β are fitting parameters. The frequency exponent (α) describes how much the trend deviates from a pure f^{-1} behaviour. The data in Figure 33 shows the variation of this frequency exponent, α, as a function of gate overdrive (V_{GS} -V_{TH}) for each of the n-channel MOSFETs, HV06, CR25 and CR27, respectively. As shown by the data, all three devices have consistently deviated from the common low-frequency noise exponent (α=1), and α values of between 0.5 and 1 have been extracted across the measured voltage range. According to theory, the frequency exponent deviates from 1 if the trap density is not uniform in depth, and because the extracted values of α<1, this suggests that the trap density is higher close to the silicon carbide–oxide interface and reduces further into the oxide [49].

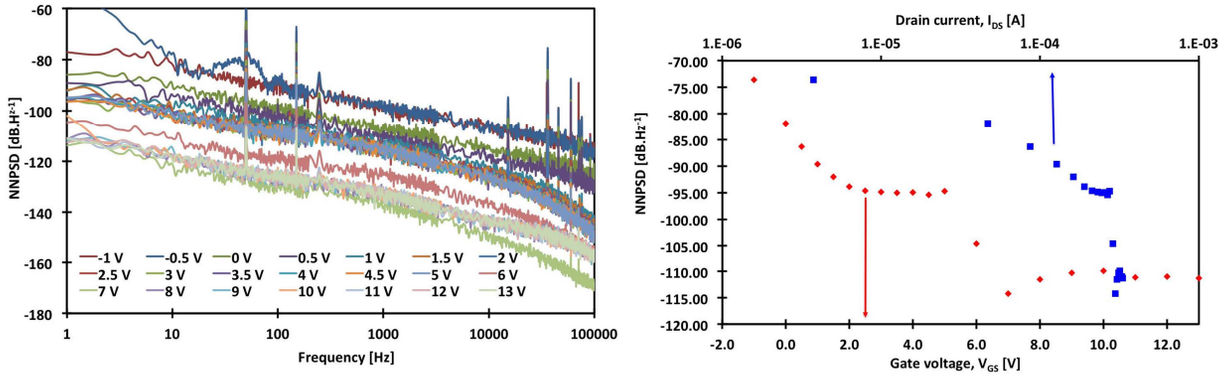


Figure 31. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with CR25 dielectric

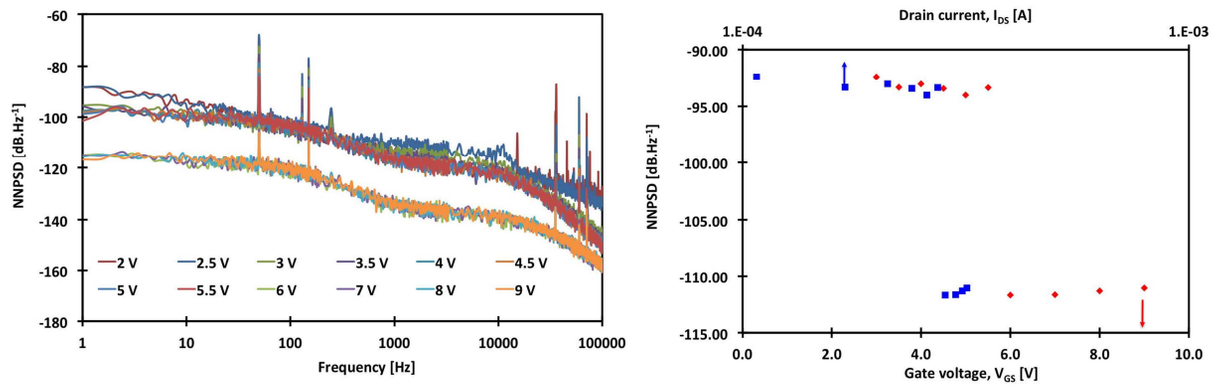


Figure 32. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with CR27 dielectric

The 1/*f* noise characteristics for each of the dielectrics on the p-channel MOSFETs are shown in Figures 34, 35 and 36 for HV06, CR25 and CR27, respectively. The data in Figures 34(a), 35(a) and 36(a) show a plot of the NNSPD against frequency for varying (V_{GS}) for each of the p-channel MOSFETs, HV06, CR25 and CR27, respectively. Both HV06 and CR25 exhibit a similar characteristic and suggest that 1/*f* noise is higher at low gate biases (during weak inversion) and reduces at higher gate biases (at strong inversion) as shown by the data in Figures 34(a) and 35(a). However, the data for sample CR27 shown in Figure 36(a) shows that NNSPD increases slightly with increasing gate bias for sample CR27; however, the noise level is substantially lower than the noise level in both HV06 and CR25. A plot of the normalised noise spectrum power density (NNSPD) at 10 Hz against V_{GS} and I_{DS} is shown for each of the devices in Figures 34(b), 35(b) and 36(b).

As with the n-channel devices, CR27 exhibits the lowest noise characteristics of the three p-channel samples, supporting the hypothesis that the quality of the silicon carbide–oxide interface is highest in this sample.

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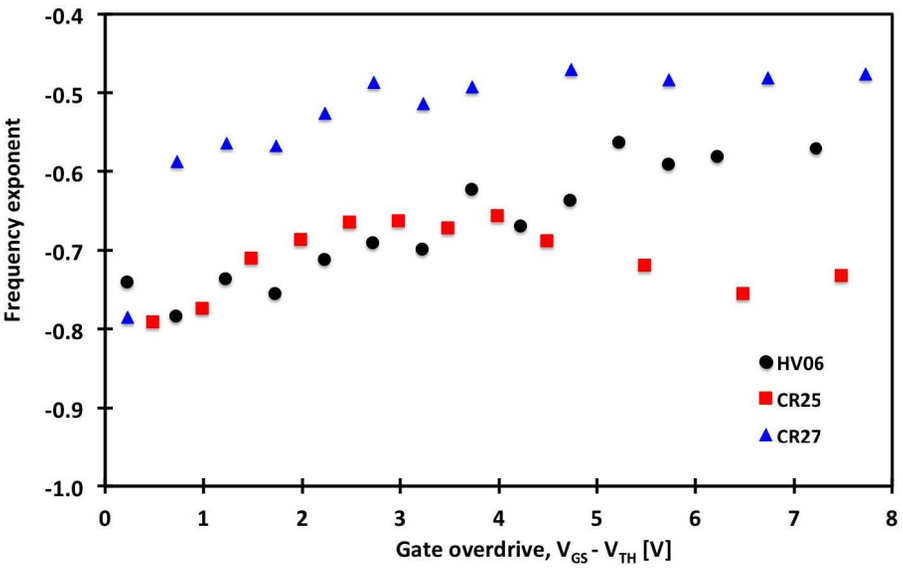


Figure 33. Variation of the frequency exponent as a function of gate overdrive for 400×1.5 μm n-channel MOSFETs

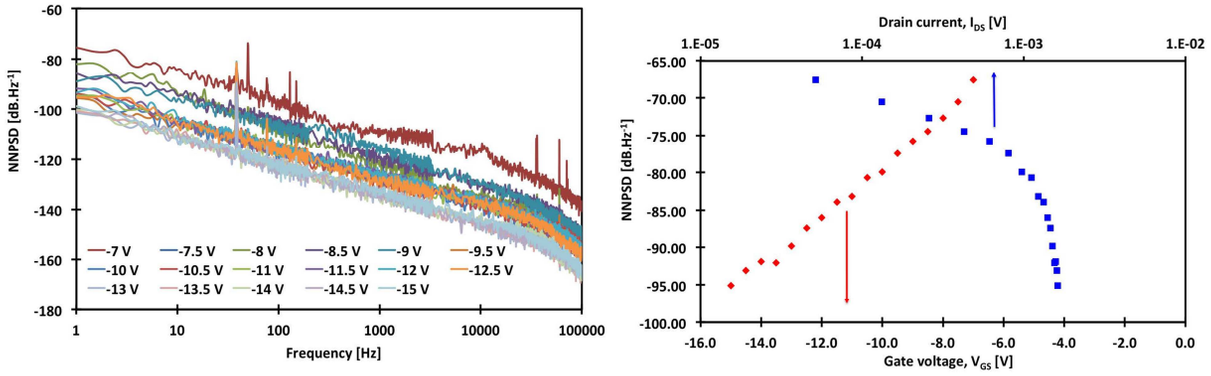


Figure 34. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with HV06 dielectric

The data in Figure 37 shows the variation of the frequency exponent as a function of gate overdrive (V_{GS} –V_{TH}) for each of the p-channel MOSFETs. The frequency exponent (α) was extracted from the data in Figures 34(a), 35(a) and 36(a) based on equation 16. The data for all three devices show consistent deviation from the common low-frequency noise exponent (α=*1*), and values between 1 and 2 have been extracted across the measured voltage range. In contrast to data for the n-channel devices shown in Figure 33, the α values for the p-channel devices are all greater than 1. This indicates that in the case of the p-channel devices, the trap density is lower at the silicon carbide–oxide interface than in the bulk of the oxide and increases further into the oxide [49], similar to reported values for nitrided gate oxides in SOI MOSFETs [50].

The contrast between the distribution of the trapping states extracted from the 1/*f* noise data suggests that optimisation of the dielectric process steps for CMOS structures with monolith-

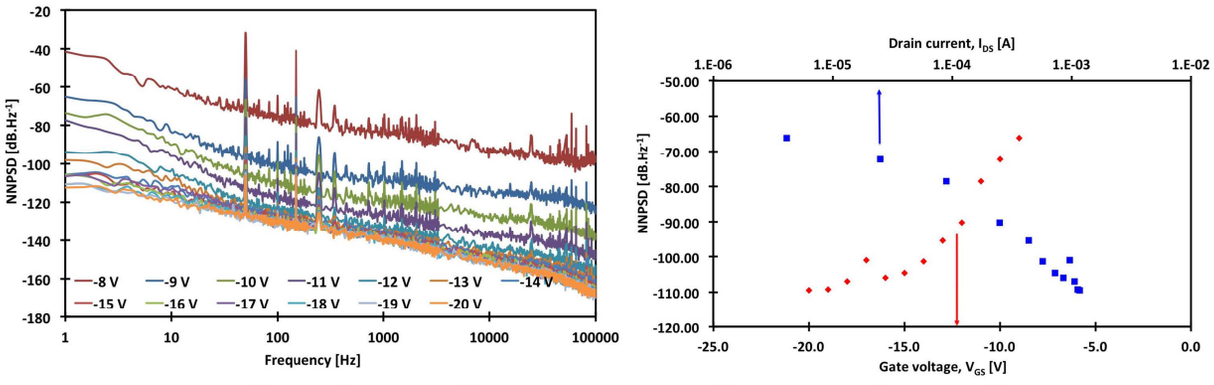


Figure 35. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with CR25 dielectric

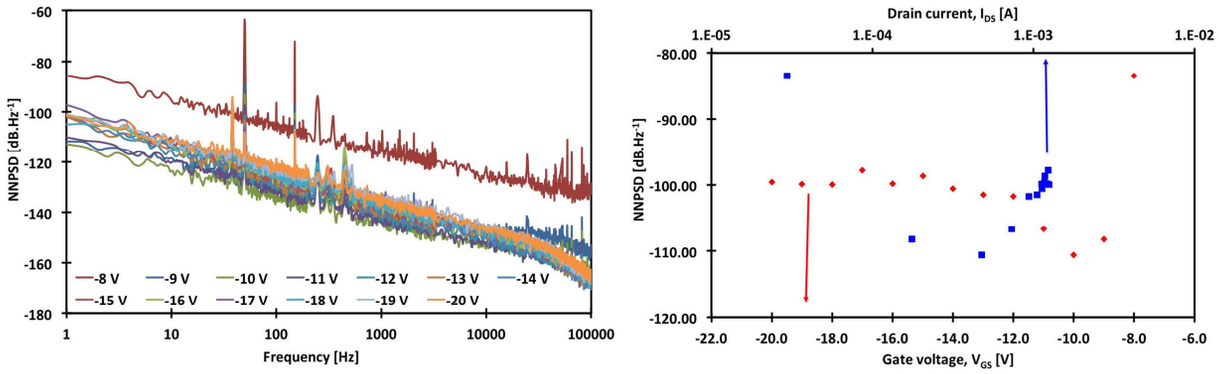


Figure 36. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with CR27 dielectric

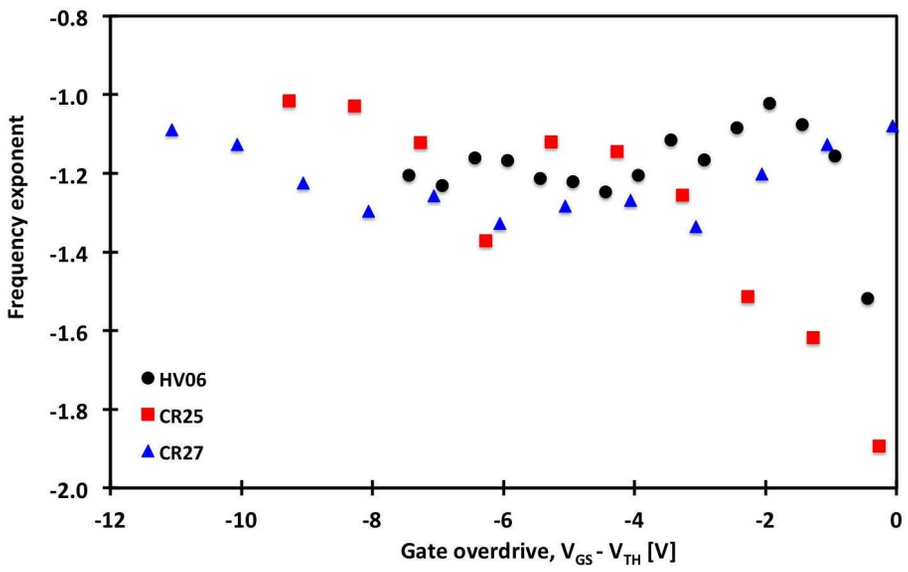


Figure 37. Variation of the frequency exponent as a function of gate overdrive for 8000×1.5μm p-channel MOSFETs

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ically fabricated n- and p-channel devices is more complex than the purely n-channel devices common in power electronic applications. The variation in depth of the highest trap density within the dielectric layer suggests that the electron interact with traps in the oxide close to the interface, whereas, holes interact with traps at deeper energy levels within the oxide.

10. Summary

The focus of this chapter was on the investigation of the electrical characteristics and device performance parameters of the 4H-SiC n- and p-channel MOSFETs that had undergone a range of dielectric process treatments to establish the suitability of conventional oxidation and deposited dielectrics for the realisation of complementary metal–oxide semiconductor circuits. The investigation into the temperature-dependent electrical characteristics of the devices demonstrated that all of the devices showed similar characteristics across the measured temperature range including an increase in I_{DS}, a reduction in V_{TH}, a reduction in D_{it} and, therefore, an increase in μ_{FE} with increasing temperature. This demonstrated that as temperature increases, there is a reduction of interface trapping effects, and therefore, Coulomb scattering reduces causing the device mobility and current to increase.

The CR27 samples for both n- and p-channel MOSFETs exhibit the highest field effect mobility characteristics, suggesting that a thin thermally grown oxide provides improved interfacial characteristics. This was further validated by the 1/*f* noise characteristics of the CR27 MOSFETs, which exhibited the lowest 1/*f* noise characteristics out of the three dielectrics at 298 K.

All three dielectrics in both the n- and p-channel devices showed severely high mobility limiting surface roughness scattering during strong inversion and high electric fields, which suggests that a process parameter – which is consistent amongst all three dielectrics and both the n- and p-channel devices – is causing high surface roughness in the channel, which is acting to degrade the channel mobility. In order to improve the device characteristics, a major focus should be given to increasing the surface roughness mobility of the samples. There is a strong trend across all of the examined samples of extremely low surface roughness mobility from applied electric fields of 1 MV cm^{-1} onwards, which is consistent across all of the processed samples and much lower than other reported devices. This is also consistent between the n- and p-channel devices, which suggests that it is inherent in the process technique used in both devices. This suggests that process contributions that are acting to degrade the surface roughness mobility of the devices is a major factor which is consistent across all of the samples. This suggests that the severely low μ_{SR} is not a contribution of the dielectric processing steps but could be a product of the ion implantation or the post-implantation anneal process.

An investigation into the 1/*f* noise characteristics of each of the MOSFET samples between 1 Hz and 100 kHz showed that in the n-channel MOSFETs, the oxide trap density was higher close to the interface, whereas, in the p-channel MOSFETs, the trap density was consistently higher further away from the silicon carbide–oxide interface consistently across all three dielectrics. The investigation also highlighted that in weak inversion, the 1/*f* noise characteristic of all of the devices is dominated by mobility fluctuations due to charge trapping at the

interface as a consequence of Coulomb scattering, which can be described by the McWhorter low-frequency noise model.

Finally, an investigation into the impact of the threshold voltage-adjust ion implantation procedure on the device characteristics was investigated for the CR27 n-channel MOSFETs. The findings showed that the increasing nitrogen dose was successful in acting to reduce the device threshold voltage; however, the nitrogen implant within the p-well also acts to improve the low electric field mobility characteristics of the n-channel 4H-SiC MOSFETs as an increased dose of nitrogen during the implant acts to reduce the effects of Coulomb scattering and therefore increase Coulomb mobility.

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