Chapter 10

Recent Developments on Silicon Based Solar Cell Technologies and their Industrial Applications

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1. Introduction

Solar energy is one of the most important alternative energy resources to the traditional fossil fuel energy. Since solar energy merely utilizes the solar radiation lights inducted from the sun, which are endless and available periodically to the earth planet, it is considered a renewable energy. It does not depend on the geographic location of the specific sources and is available everywhere in all countries in the planet. Since solar energy is completely natural, it is also considered a clean energy source. It does not disrupt the environment or create a threat to our eco-systems the way fossil fuel and some other energy sources might. It does not cause greenhouse gases, air or water pollution. With the development of solar technology in the past decades, solar energy becomes an economically affordable energy source and attracts more and more countries to include it in their national strategy for development.

There are several applications utilizing the solar energy, among which the photon thermal utilization and photovoltaic (PV) application are the most common applications. Photon thermal system generally converts the sunlight energy to thermal energy by collecting heats to the medium distributed within a structure or a district heating network. PV system is using the so called photovoltaic effect to convert sunlight energy into electricity. The energy conversion efficiency of a typical photon thermal system is around 28% while a typical PV system is around 18% in the current market. The utilization of photon thermal system normally requires complicate configuration in the system integration and is limited by the thermal consumption. PV system generating electricity can be used for direct residential and industrial utilization whose consumption is unlimited. Both photon thermal system and PV system require the conversion device to be positioned in the sunlight receiving surface, which is limited by the area of rooftop or land. Higher conversion efficiency of solar system is pursued in the market balancing the investment and the return.

In a PV system, the solar cells exercise the photovoltaic effect and determine the conversion efficiency of the whole system. Traditionally, semiconductor materials in the solar cell are doped to form P-N structure as an internal electric field. Among plenty of the semiconductor materials, silicon has a development history up to 50 years. The p-type (positive) silicon has the tendency to give up electrons and acquire holes while the n-type (negative) silicon accepts electrons. When sunlight hits the solar cell, the photons in light excite some of the electrons in silicon to become electron-hole (negative-positive) pairs. Under the internal electric field established in the P-N structure, these pairs are induced to separate. As a consequence, the electrons move to the negative electrode while the holes move to the positive electrode. If a conducting wire connects the negative electrode, the load and the positive electrode in series to form a circuit, an electric current is generated to supply the external load as a result. This is how the PV effect works in a solar cell.

Solar cells are assembled together to form solar modules, which can be arranged into arrays to form a so-called PV system that is large enough to function as a power station for industrial, commercial, and residential use. Through PV effect, the solar cells capture sunlight and turn it into direct current (DC) electricity. For off-grid PV system, the DC can be immediately used for the DC loads or the DC can be directed to an inverter, which converts DC into alternating current (AC) that is suitable for conventional electric appliances. In the off-grid system, the excess energy generated from the PV modules is usually stored in energy storage unit such as capacitors or batteries, controlled by charge controller, for use at night when there is no sunlight or when a larger energy consumption than generation is loaded. An optional backup power, such as diesel generator, can be installed if electricity from the energy storage unit runs out. For grid-tied system, DC electricity generated from the solar cells is converted into AC to be used on-site or stored for backup if the PV system includes energy storage unit. When there is more demand, power can be drawn from the tied grid. Excess supply of electricity from the PV modules can also be fed back into the grid after tuning the phases and frequency. This process of drawing and/or feeding electricity to the tied grid can be monitored by the solar production meter and the export/import meter.

Among all the components in a PV system, the solar cell that converts sunlight to electrical energy is considered to be the most critical device. Solar cell technology is thus deemed to be the most important sector in the solar industry for several decades. Increasing the conversion efficiency and reducing the cost of silicon based solar cells are the two mainstream trends in recent years. This paper attempts to briefly overview the developments in the fields of solar cell silicon materials, the emerging solar cell device architectures and the corresponding immerging silicon based solar cell manufacturing processes, especially from an industrial application point of view.

2. Traditional silicon material, cell structure and processes for silicon based solar cell

Silicon and some other semiconductor materials are the basic materials of solar energy. Today, about 90% of solar cells that installed globally are made from silicon. There are generally two

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types of this semiconductor: monocrystalline (also called single crystal) silicon and multicrystalline silicon. Multicrystalline silicon is composed of a number of smaller silicon crystals.

Figure 1 shows a traditional manufacturing process from raw silicon (polycrystalline silicon) to final solar modules (also called solar panel) [1]. At first step, silica goes through carbothermic reduction process and forms the metallurgical grade silicon at a purity level of 2N-3N.The metallurgical grade silicon is then refined and subjected to the casting scratch process to become polysilicon raw materials at a purity level of around 6N. For growing the silicon crystals, polysilicon material is then introduced into two different production process for mono-crystalline silicon and multi-crystalline silicon production: monocrystalline silicon are generally produced with the Czochralski (CZ) method and multicrystalline silicon are commonly made with directional solidification methods (also called the brick casting method). The monocrystalline silicon ingot is then sliced into wafers. As for the multicrystalline silicon, the silicon brick is first diced into bars and then sliced into wafers [2]. The multiple crystals create boundaries for electrons resulting in less efficiency comparing to monocrystalline silicon. The difference in cell conversion efficiency between these two type silicon solar cell modules is typically 1.5-2% [2]. However, multicrystalline silicon can be produced at a lower cost than the mono-crystalline and it is used most in the solar industry. For traditional silicon based solar cells, the dopant in silicon is p-type (boron).

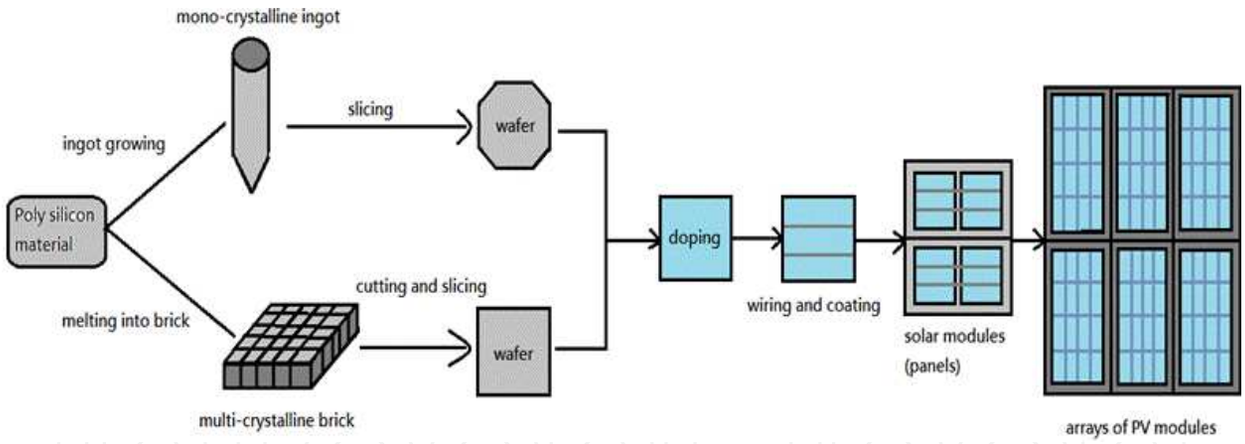

Figure 1. Traditional manufacturing process from raw polysilicon to the final solar module [2]

Compared to monocrystalline silicon, the surface of multicrystalline silicon wafer is more difficult to be passivated due to the existence of grain boundaries and the various grain crystallization orientations, which typically results in about 0.5% conversion efficiency loss. The crystallization defects in the bulk of multicrystalline silicon, such as grain boundaries and metal impurity contaminations, generate the carrier recombination centers and hence degrade the conversion efficiency further [3, 4]. However, ascribed to the low cost of crystallization, multicrystalline silicon wafers have gained more than 40% market share in the global solar market. The monocrystalline silicon wafer is popular especially in the rooftop applications due to its higher cell conversion efficiency per unit covering rooftop area.

Screen printing technology mainstreams the manufacturing processes for traditional silicon based solar cell. Figure 2 shows a structure and fabrication flow for a conventional screen printed solar cell [5]. Generally, the major processes in the common industrial screen printing technology include six core steps: texturing and surface cleaning, phosphorous doping diffusion to generate p-n junction, coating antireflection layer on the front side, printing aluminum paste on rear to form back side field (for metal impurity gettering, light reflection and rear passivation) and silver pastes on both sides, firing the printed pastes to form contacts to front emitter and rear base and isolating the emitter and base on cell edges. There are quite a few review papers covering the detailed description of the screen printing technology [6, 7].

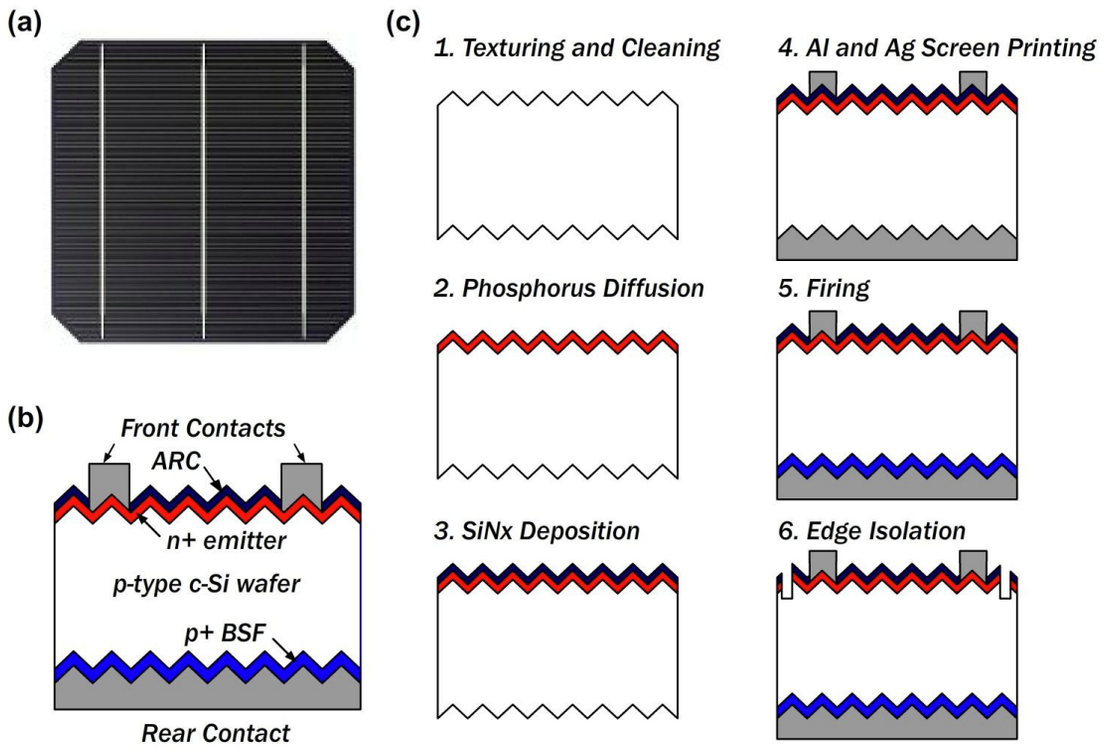

Figure 2. A structure and fabrication flow for a conventional screen printed solar cell. (a) A photo of a typical solar cell on a monocrystalline Si wafer. (b) Schematic diagram of the cross section of screen printed solar cell. (c) six core process flow steps which are used in manufacturing of basic screen printed cells. [5]

3. New developing silicon crystals and their challenges to the traditional silicon based solar cell processes

When the solar market demand shifts to the high efficiency side, to low down the preparation cost of material and improve the degradation resulted from the intrinsic and external defects are widely pursued in the silicon manufacturing industry. New silicon materials, such as cast-mono silicon, large-sized grain multicrystalline silicon and ultra-thin crystalline silicon are the representative silicon materials under development. Moreover, the n-type silicon material also

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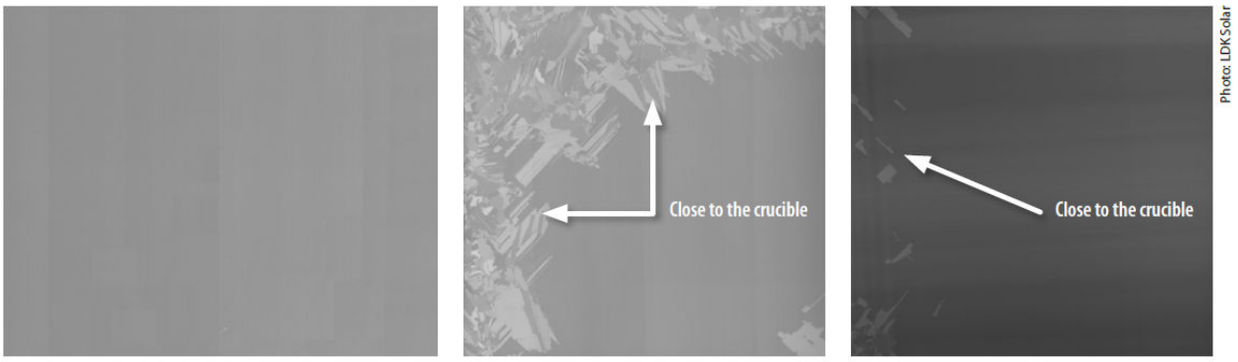

Figure 3. Image of silicon wafers with different categories of quasi-mono wafer sliced from the same ingot [8].

shows its growing tendency to be adopted as the solar cell substrate. Additionally, one shall note that recent market demands in the distributing PV system increases the market share of cells made from monocrystalline silicon steadily.

3.1. Quasi-monocrystalline silicon

The directional solidification method (also called casting method) was used to grow single crystals. The directional solidification system (DSS) furnace used for multicrystalline silicon production was originated from the heat exchange method (HEM) furnace for single crystals of sapphire. The growth of single crystal silicon with the directional solidification (or casting) method and the application of the resulting mono (or quasi-mono) silicon wafers for solar cells was also carried out by numerous researchers since 1987, implemented in large scale pilot application since 2006 and attracted the interests from industrial applications since 2011 [8]. Quasi-monocrystalline silicon is casted with the common crystal growth furnaces for multi-crystalline silicon. There are two casting approaches for obtaining the quasi-mono-crystalline silicon ingots, one is cast with the pre-grown seeds (cast-on-seed) and the other is to cast the ingot without seeding (seedless casting).

Casting ingot with seeds has been successfully commercialized. The major difference in the cast-on-seed process of growing the quasi-monocrystalline silicon ingots, compared to the growth process of multicrystalline silicon ingots, is that a layer of monocrystalline silicon seeds are employed on the surface of the bottom side of the crucible [9]. These seeds are usually sliced from the monocrystalline silicon ingot grown with the CZ method. Silicon feedstock and dopants are then loaded on top of the seed. In the process of melting, the silicon feedstock is controlled to start the melting from the top so that the seeds will not be completely melted. In the process of solidification, the silicon melt starts to nucleate on the remaining seeds and the grown crystal follows the orientation of the seeds and gradually form a large ingot consisting of crystals with some sections having multiple grains, especially in the areas close to the crucible and between the seeds. As a result, the ingot is with large single crystalline grains present in the center while plenty of small-sized grain exists in the edge regions of the same ingot. Figure 3 shows the image of silicon wafers with different categories of quasi-mono wafer sliced from the same ingot. [8]

Quasi-mono crystalline silicon can also be obtained without the pre-arranged CZ seeds. However, the challenges rely on a more precise control of the temperature distribution gradient in the silicon liquid as well as the solidification speed of the crystal ingot. In principle, a smoother temperature distribution gradient as well as a slower but steady solidification speed is beneficial for coarsening the grain sizes and in turn reduces the grain boundaries in the casted ingot, which can form the large grain multicrystalline crystal and eventually form quasi-mono crystal if the nucleation sites during solidification process are controlled ideally. Using such approaches to obtain quasi-mono crystal is still under early stage of development whereas using the principle to grow the large grain multicrystalline silicon has been adopted in practice. The electrical behavior of multicrystalline silicon is shown to be influenced by the properties of the grain boundaries, the study of the grain boundaries is very important for improving the efficiency of multicrystalline silicon solar cells over decades. Improving the thermal filed control through some simple retrofits on the traditional casting furnaces can form a multicrytalline silicon ingot with the large grains sizing up to 120-220mm. In such ingot, the amount of grain boundaries are greatly reduced compared to the common multicrystalline silicon ingot whose grain sizes are typically few millimeters [10].

Compared to the CZ monocrystalline, the small angle sub-grain boundaries originating from the gap of the seeds can be observed from the centered quasi-monocrystalline silicon, which increases the recombination of carriers. Nevertheless, the oxygen content of quasi-mono is less than that of mono-crystalline silicon, which reduces the effect of light induced degradation of quasi-mono solar cells. In such a way, the cell efficiency made from quasi-mono wafers with large percentage of quasi-mono grain is comparable to the mono wafers. However, for the quasi-mono wafer with low percentage of quasi-mono grains, the dislocation density, the concentration of oxygen and carbon, and the impurity made the efficiency obviously lower than that of a high percentage of large quasi-mono grains. The properties of the silicon wafers sliced from the edge regions of quasi-mono crystalline ingot are closed to the common multicrystalline silicon wafers. Typically, if the efficiency of a mono silicon cell is 18.5%, the efficiency of a quasi-mono silicon solar cell with a high large single grain percentage can reach about 17.5 to 18.2%. But for low single grain percentage quasi-mono silicon solar cells, the efficiency can be as low as about 16.6 to 17.0%. [8]

The major challenge that quasi-monocrytalline silicon materials brought to the common solar cell processing is mainly the texturing compatibility. In general, for different percentages of large grains of the quasi-mono wafer, different texturing processes should be selected, so as to minimize the textured surface reflectivity and in turn maximize the solar cell conversion efficiency. Typically, the alkali texturing process can be applied to the quasi-mono wafers with mono grain or large percentage of mono grain, so that the light reflection on the solar cell surface can be greatly reduced. For the large quasi-mono grain, alkali texturing can form an inverted pyramid texture surface, similar as the mono crystalline wafers, and improve the efficiency of the solar cell. But due to the anisotropic etching of alkaline, the pyramids that form on the other grains with an orientation different from that of the large quasi-mono grain will have a different structure and orientation. This area has a different reflectivity for the induced light and exhibits different colors from that of the large quasi-mono grain. For a quasi-

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mono wafer with low percentage of large quasi-mono grains, acid texturing can be applied similar to that for multi silicon wafers [10]. Some compensated texturing processes comprising multiple-step alkaline and acid texturing as well as adopting specific additives in the wet-chemical solutions are also developed [11].

3.2. N type silicon

The very first solar cell, fabricated in 1954 in the Bell Labs, was made of a monocrystalline n-type Si wafer. However, the main industrial application of solar cell was for space applications like satellites until the 1980s. Because the p-type silicon was proved to be less sensitive to the degradation caused by exposure to cosmic rays, such as high-energy particles (protons and electrons), all industrial solar cell development was based on p-type silicon for decades. Since past decade, n-type (mainly phosphorus-doped) silicon material and related cell processes for the territorial application starts to attract a lot of attentions from the scientific researchers.

Compared to standard p-type (boron-doped) silicon solar cells, n-type silicon solar cells feature two important advantages. In one aspect, n-type silicon does not suffer from light induced degradation caused by the simultaneous presence of boron and oxygen (B-O pairs) in the wafers, a phenomenon that in standard p-type silicon solar cells leads to a reduction of the module power output by usually 2-3% within the first few weeks of installation. In another aspect, n-type silicon wafers are less sensitive to metal impurities that are usually present in the silicon feedstock and less effort has to be made to obtain n-type silicon wafers with a high electronic quality. In addition, the performance at low light intensities is predicted to be higher for n-type solar cells, as the lifetime increases in contrary to p-type cells [12], thus enabling an increased power output averaged over the year. As a consequence, n-type silicon wafers featuring high solar cell efficiency potential can be produced more cost effectively than the high quality p-type silicon wafers.

Although the n-type silicon has not yet been studied exhaustively, the industrial applications of n-type silicon have been pushed by the market. Very high quality monocrystalline n-type ingot can be pulled via CZ pulling method and the n-type wafers featuring a high diffusion length of the charge carriers can be manufactured in a routine industrial process used for p-type silicon. However, the challenge of n-type (phosphorus-doped) silicon material is, compared to the standard p-type (boron-doped) silicon, the poor homogeneity of the electrical properties throughout the height of the silicon ingot ascribed to the low segregation coefficient of phosphorus (0.35) compared to boron (0.8) dopant in the silicon liquid during solidification [13]. For instance, for boron doping, a range between 1-3 ohm.cm can be easily maintained throughout the height of whole ingot, while in the case of phosphorus doping, this range increases to 3-12 ohm.cm or more. As standard solar cell concepts require a narrow resistivity distribution to allow stable efficiencies for mass wafers from same ingot, the large variation of the resistivity of n-type silicon ingot decreases the yield for solar cell production thus increasing overall production costs. One solution is to develop new solar cell structures that are less sensitive to the base resistivity; however, a more feasible solution is the application of ingot growth techniques based on the continuous feeding of Si feedstock. Such continuous CZ-

pulling technologies can result in a better homogeneous and higher quality electrical properties distribution in the n-type silicon ingot and are currently under development.

The adoption of n-type silicon as the solar cell substrate also brings several challenges to the industrial processes established for traditional p-type solar cell. There are quite a lot of academic and industrial groups working on developing the n type cell technologies in various manufacturing processes, among which the aluminium rear emitter, passivation for p+surface and the metallization are three of the key fields. However, besides the improvements in solar cell technology, it is also necessary to advance the modules, in order not to lose the benefit of the enhanced performance of the cells. The most important topics besides material savings are the improvement or replacement of the absorbing EVA by silicones and the replacement of soldering by gluing techniques which will not be discussed herein.

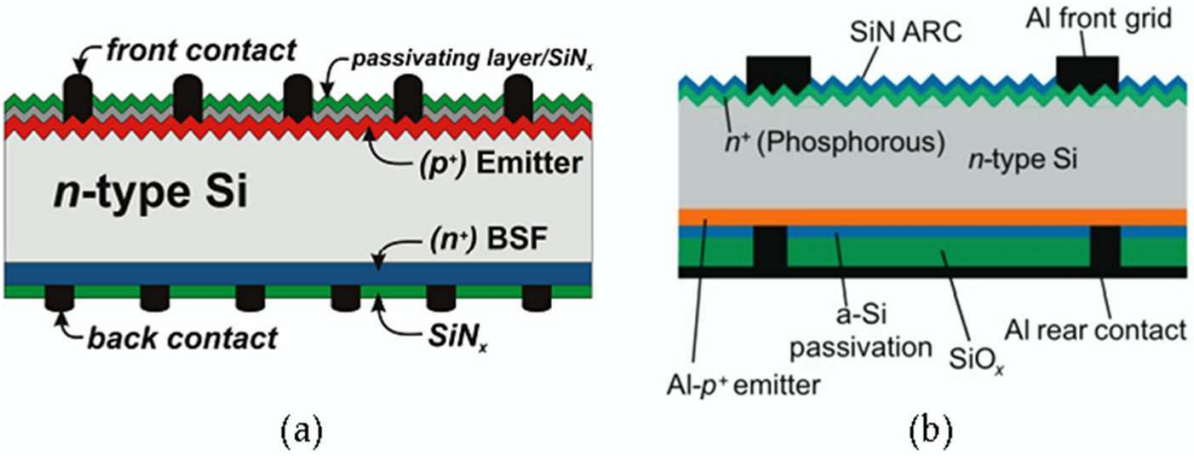

Figure 4. Two schematic cross-section of typical concept of n-type silicon based solar cells. (a) a fabricated n-type solar cells with front emitter [14]. (b) with screen printed rear Al-p+ emitter, full-area metalized a-Si passivated emitter and with local point contacts [15].

The most essential process for good processing of advanced n-type solar cells is the creation of a homogeneous and adapted p+ emitter. Figure 4 shows a typical n-type solar cell. [15] The rear p+ emitter is usually generated by the recrystallization process forming an Al-doped region [16]. In the more advanced solar cell structures, such as HIT concept, a boron-doped emitter is formed by the growth of an amorphous, boron-doped thin layer. Intrinsic and doped amorphous silicon layers are deposited at low temperatures on the front for the emitter (silane and diborane) and on the rear for back surface field creation (silane and phosphine) [17]. In such process, the cleanliness of the surface before amorphous silicon layer depositions is extremely important and several wet chemical processes are developed, for example, Piranha cleaning of H_2O_2/H_2SO_4 and HF/O_3 cleaning. Low temperature (<200°C) screen printing pastes also has to be used for such process since these layers are not stable against high temperatures above 300-400°C. Furthermore, boron-doped emitter for n-type silicon can be also realized by

the high temperature tube diffusion process using boron containing dopants as well as by ion implantation followed by thermal recrystallization anneal process [18].

However, the silicon nitride (SiN_x) layer formed by plasma enhanced chemical vapor deposition (PECVD) that widely used for passivating the n+surface of p-type silicon not only has no passivating effect but even deteriorates the surface passivation with respect to an unpassivated surface for boron-doped p+ emitter of a n-type cell. The efficient passivation material for n-type silicon includes, a stack consisted of a thin thermal SiO_2 (formed by anneal processing at a short process time and a low temperature), a PECVD SiNx layer and an aluminum oxide (Al_2O_3) layer deposited either by atomic layer deposition technology or PECVD. A stack of boron silicate glass (BSG) and PECVD SiN_x is also proposed [19]. Such stack has the advantage that no additional equipment is needed as the BSG is already formed during the formation of the boron emitter and the SiN_x requires only standard PECVD equipment as used in p-type cell production lines.

The classical screen printing process can be applied for n-type cell, however, the pastes have to be modified. As low temperature firing is preferred for the n-type cell and p+ surfaces have to be contacted, a simple Ag paste for p-type cell is not suitable. A silver aluminium (AgAl) paste is used and optimized. The aluminium (Al) in the paste allows a good contact resistance, reduces conductivity strongly and limits the open circuit voltage due to penetration into the space charge region, a substitute of Al in the paste is seeking. Additionally, other screen printed products such as diffusion pastes, diffusion barriers, etching and isolation pastes are gaining more and more importance for advanced cell concepts [18]. Furthermore, the tabbing of Al ribbons to interconnect neighbouring solar cells shall be more careful for n-type cell because the devices will be shunted completed if the AgAl emitter contacts contact the n-type base directly [16].

3.3. Kerfless ultra-thin crystalline silicon

In the 1980s, silicon based solar cells are made on crystalline silicon wafers with typically 400 micron thick, where the silicon material cost corresponds to a large fraction of the total cost of a final solar module. The wafers thickness has been significantly decreased from 400 micron to 200 micron while the cell's surface has increased from 100 cm^2 to 240 cm^2 between 1990 and 2006 [20]. Advanced solar cells were fabricated on wafers as thin as 140 um, resulting to efficiencies higher than 20% in 2006 [21]. Current silicon wafer thickness used for traditional silicon based solar cell is in the 150 micron range.

The development work on the ultra-thin silicon substrate was stimulated by the very high price of raw polysilicon materials. In 2008, the cost of silicon wafer accounted for more than 30% of a PV module cost with approximately 60% of the wafer cost coming from ingot growth and wafering. Additionally, the silicon wafer manufacturing consumed the major fraction of energies used to produce PV modules thus in turn increases the energy payback time. However, the price of polysilicon reduced from $400/kg in 2008 to a price as low as $30/kg in 2013 with the rapid expansion of manufacturing capacity primarily in China and Korea since 2010. Therefore, the advantages of kerfless approaches for reducing the silicon material cost were leveled to a big extent while most manufacturers have failed to scale their technologies

and compete with competitors who produce the substrates based on traditional ingot casting and wire sawing. Nevertheless, the use of thin substrate for reducing the consumption of silicon is till of interest for manufacturing high efficiency solar cells based on n-type CZ silicon presently because the n-type silicon material can be up to three times more expensive than the p-type material. However, the cost of n-type wafers may drop as the industry already shows a trend to shift towards n-type technology and some developing advanced ingot growing technologies, such as continuous CZ and magnetic CZ, will be available to a larger number of manufacturers in the near future.

Thinning the wafer can be beneficial for two reasons: reduce the consumption of expensive silicon and gain a higher open circuit voltage in the cell. Instead of wire sawing, lifting off thin wafers from a crystalline substrate could potentially reduce crystalline silicon material lost to kerf, which is usually 120-180 micron thick. Epitaxial growth the crystalline silicon could also potentially provide cost reduction since in this approach the substrates are obtained directly from silane bypassing the growth of polysilicon and pulling CZ silicon ingots. The challenge to produce ultra-thin crystalline silicon solar cells consists of three major tasks: the growth of a high quality large-grained crystalline silicon layer on inexpensive substrate, the incorporation of some light trapping scheme to compensate for the weak near-infrared absorption of crystalline silicon and effective passivation of grain boundaries and surfaces.

In the material preparation level, various approaches to manufacturing the kerfless ultra-thin silicon wafers are developed, among which the two main technologies are ion implantation followed by cleaving [22] and epitaxial growth followed by a lift off [23]. Several lifting off process are developed, including epitaxial growth of silicon film on dissolvable CaF_2 to fabricate the textured monocrystalline silicon film [24, 25], epitaxial growth of silicon on a preformed porous silicon layer as the lifting-off buffer layer [26] and the so-called perforated silicon process [27].

In the solar cell level, two critical requirements in achieving high efficiency on the ultra-thin silicon wafer are advance IR light trapping and very good surface passivation [28]. Light trapping in the ultra-thin monocrystalline silicon cells is important because the optical path length of the IR photons may reach the cell substrate several hundreds of microns. These photons may escape the device after multiple internal reflections through the front surface, thus reducing generation current. Very good surface passivation is also important since the contribution of surface recombination in overall recombination losses increases in the ultra-thin silicon cells and the moderately passivated surfaces may pull the efficiency down.

The basic idea of producing kerfless ultrathin crystalline silicon is to eliminate saws, furnaces, and cell finishing equipment as well as slurry and thick wafers. An ion implant machine is also proposed to replace the diffusion equipment in the commercial production chain. However, whether the new process fits seamlessly into the production flow with little impact on the wafer handling, interconnection, packaging and reliability have not been proven at a full production level. Therefore, developing a new wafer technology and integrating it into an existing process chain remains an enormous challenge [29].

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4. Immerging architectures of high efficiency silicon based solar cells and their realization processes

Solar cell is an energy conversion device using the photovoltaic effect, which is basically a device separating the electron and hole in a semiconductor material and typically a p-n junction. However, the modern silicon based solar cell is not a device consisting of a single p-n junction as it was born any more. Thanks to the well-established semiconductor manufacturing technology, wet chemical processing, low cost thin film coating, chemical lithography as well as the laser patterning technologies keep attracting the attentions from of the solar industry globally. Surface structure optimization and better surface passivation both on the light induction front side and the rear side are developed in the past years. The deeper understanding of the device physics and specific material properties, solar cell architectures become more and more complicated. PERC/PERL, MWT/EWT, PHASHA, IBC and SHJ/HIT type solar cells structures are under development in the industry, which would increases the solar conversion efficiency gradually in the next few years.

4.1. Front emitter optimization: selective emitter

As it is shown in Figure 2(b), the most commonly used silicon based solar cell architecture is a planar diode structure, where a thin layer of heavily doped silicon (often called emitter, typically n+) is present at the front surface of a moderately doped wafer of the opposite type (often called base, typically p-type). The emitter area is the region that emits or injects most of the charge carriers under dark operation. In the current standard solar cell manufacturing process, the emitter is formed by in-diffusion at high temperature of an n-type dopant (typically phosphorous) into the surface region of a p-type wafer (typically doped with boron). Besides diffusion, the emitter can also be formed by exploiting ion implantation and/or epitaxy technologies.

A good emitter shall efficiently collect the photo-generated carriers in the emitter region, induce a low-loss lateral transport of the majority carriers from the location where they are collected to the nearby metal contacted region and maximize the output voltage with an optimum doping concentration [30]. In industrial practice, the best emitter is a very thin but heavy doped layer. In the very thin emitter, the photon-generated carriers can be collected from the depletion region as well as the moderately doped base underneath the emitter. The extremely high doping concentration at the surface reduces the contract resistance meanwhile act as a sink for metallic impurity gettering [31]. However, the further optimization of the homogeneous emitter approach requires the development of the printable pastes that can contact the emitters with higher sheet resistance which is a challenge to the front silver paste suppliers. A typical doping of 50 ohm/square on the front side of today's industrial type solar cells is therefore a compromise between the emitter performance and sufficiently low contact resistance.

Selective emitter is developed to overcome the above compromise. The selective emitter structure is normally formed by heavily doped the regions underneath the contact grid and by lightly doped in the light illuminated area at the same time. Figure 5 shows a selective

emitter that is a heavily doped region placed directly under the metal line [32]. Such selective doping regime leads to a reduced contact resistance and lower Auger-and SRH recombination and therefore results in an improved blue response and a higher open circuit voltage. Several selective emitter technologies have been developed in the past few years. Among which, the etch-back emitter, inline selective emitter, laser doping and doped silicon ink are successfully commercialized in industrial mass production.

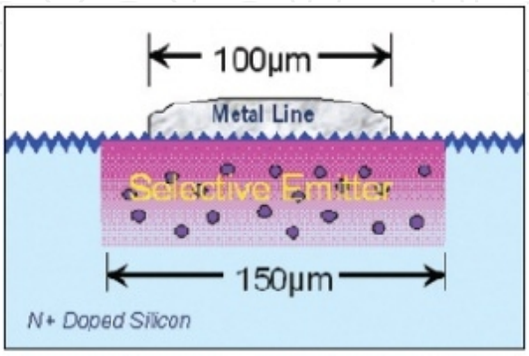

Figure 5. The selective emitter is a heavily-doped region placed directly under the metal line [32].

The etch-back process can be realized with highly homogeneous doping on large area wafers and followed by removing the porous silicon in a wet-chemical solution. The etch-back process in combination with a masking step is an industrially feasible scheme to form a selective emitter structure on p-type wafers. By changing the initial $POCl_3$ diffusion to 20 ohm/square and etching back to 95 ohm/square, a maximum efficiency of a selective emitter solar cell was measured to 19.0% [33].

An inline diffusion process can be realized by coating the wafer surfaces with a defined amount of phosphorus containing dopant with a doper before being laterally transported through a conveyor belt furnace in a controlled ambient at standard pressures. Applying inline selective emitter concept, an increase in open circuit voltage by 18.6 mV and an increase in short circuit current by 1.2 mA/cm^2 were obtained followed by an average efficiency gain of 1.4% and a fill factor improvement by 1.3% compared to homogeneous inline emitters [34].

A laser doping process can be realized by scanning the surface of lightly doped wafers so as to melt the wafer surface locally and enables the fast incorporation of phosphorus atoms from the PSG-layer to form a highly doped selective emitter by recrystallisation. Such process can generate an emitter as thin as 800nm within a few hundred nanoseconds and the emitter will not incorporate any grain boundaries and dislocations. An efficiency gain of 0.5% absolute is reported by adopting such laser doping process [35].

A silicon ink doping process to generate the selective emitter is also commercialised. Such process can be realized by printing the highly doped silicon nano-particles onto the silicon wafer surface prior to the common phosphorous diffusion. The ink is printed only in the areas where the screen-printed front contact is located afterwards. During the following doping diffusion step, a lightly doped emitter (for example 80-100 ohm/square) is realized in the

uncovered areas whereas a highly doped areas (for example 30-50 ohm/square) is formed and serves for electrode contacting [36].

4.2. Wafer surface passivation: dielectric materials

Coating a cost-effective antireflection layer is an important step during silicon-based solar cell fabrication. Ideally, the coating should not only reduce optical losses but simultaneously provide a reasonable degree of surface passivation and, for multicrystalline silicon material, a hydrogen passivation of bulk defects and /or grain boundaries. Thermal SiO_2 is one of the obvious candidates for the surface passivation of both n-and p-type silicon of arbitrary doping level and is used in the record-efficiency passivated emitter and the rear locally diffused (PERL) crystalline silicon solar cell [37]. However, the use of a high quality thermal oxide would lead to a high cost of ownership, and the high oxidation temperature may degrade the crystalline silicon bulk quality. Many alternatives based on low-temperature processes therefore receive currently strong research interest, including PECVD, rapid thermal oxidation and electro-chemical oxidation [38] Meanwhile, alternative novel dielectric materials, such as SiN_x, SiC_x, SiON and Al_2O_3 are being investigated [39].

SiN_x fabricated by PECVD is increasingly used in industry as it offers the possibility to fabricate a surface and bulk passivating antireflection coating at low temperature (≤450°C) and becomes the most promising candidate for p-type silicon wafers [40]. Recently, eexcellent surface passivation of silicon wafers has been achieved by about 30 nm thick Al_2O_3 layer prepared by plasma-assisted atomic layer deposition (ALD), yielding effective surface recombination velocities of 2 and 13 cm/s on low resistivity n-and p-type silicon, respectively. These results are comparable to the solar cells employing thermal oxide as used in record-efficiency solar cells [39]. Al_2O_3 layer also demonstrated a better UV stability than thermal SiO_2 with the surface passivation improving during UV irradiation [41].

Bi-layer antireflection coatings on the front side have significant advantages over single-layer antireflection coatings due to their broad-range coverage of the solar spectrum. For example, a solar cell with 60 nm / 20 nm SiN_X:H double stack coatings has 17.8% efficiency, while that with a 80 nm SiNX:H single coating has merely 17.2% efficiency. The improvement of the efficiency is due to the effect of better passivation and better antireflection of the stack of antireflection bilayer coating. The double stack antireflection coating is also stable against external stress, which is beneficial for the fabrication of solar module. [42] Bi-layer schemes with different dielectric materials, like SiO_2 capped with SiN_x, have also been explored [43].

Recently, the dielectric rear side passivation of crystalline silicon solar cells has expanded from small lab-scale cells to industrial production. One major advantage of using dielectric passivation instead of a full area Al back surface field is the substantial gain in short circuit current density. A major contribution of this gain stems from the enhanced reflectivity of the rear side of 90-95% at 1000 nm compared to 65% common for fully Al alloyed rear sides in the solar spectrum [44].

Figure 6 depicts the working principle of the solar cell with a rear passivation coating layer [45]. The introduction of backside passivation increases cell efficiency in two ways. Firstly, the

backside passivation layer reflects light that has travelled through the cell without generating electrons and reached the backside. The reflected light will pass through the cell a second time generating additional current. Secondly, the layer passivates the crystal matrix defects associated with the back surface of the silicon wafer better than a conventional cell. As a consequence, the electrons generated near the backside of the cell are less likely to be captured and lost. They will have a higher probability of reaching the interface between the base and emitter contributing to the current of the cell improving the cell output voltage. Since blue light will generate more electrons near the front of the cell whereas red light will generate electrons at the back of the cell or even pass the wafer without generating electrons, backside passivation increases the sensitivity of the cell to infrared light with a wavelength of between 1000 and 1180 nm. This additional sensitivity will result in an increased current and in the efficiency of the solar cell.

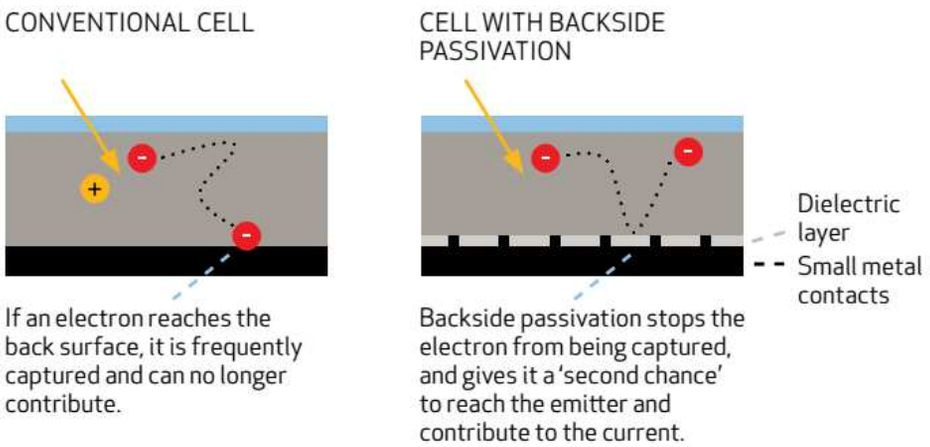

Figure 6. Backside passivation prevents electrons from being captured by the rear surface, resulting in an increased current and voltage of the cell. [45]

Most development efforts are geared towards an evolutionary approach, where the prevailing metallization by means of screen printing and co-firing of thick film paste is retained and the deposition and structuring of the dielectrics is merely added into an already established process [46]. In industrial practise, laser ablation of the dielectric layer for opening the contact channels has been employed on the rear side before printing AgAl paste for contacting the base while some innovative firing through pastes without opening the dielectric layer are also under development.

4.3. Cell structure innovation: Advanced architectures

High efficiency solar cell technologies that can replace screen printed cells in large volume manufacturing in the next 5-10 years are under development. The mainstream high efficiency technologies are passivated emitter and rear cell structure (PERC) or PERL solar cell, metal warp through (MWT) or emitter warp through (EWT) solar cell, bifacial cell with passivated

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diffusion at the rear (PASHA cell), interdigitated back contact (IBC) solar cell and silicon hetero-junction (SHJ, also known as HIT cells which is a brand name by Panasonic) solar cell.

MWT/EWT technology has been regarded as industrially promising recently because of its high cost-effectiveness for increasing cell and module efficiency [47, 48]. In the MWT/EWT cells, the front metal grids or the front emitter will be wrapped through the laser opened via-holes to the rear side of the wafer inducing reduced shading losses, and reduced surface recombination, and as a result the cell efficiency will be improved [49]. Isolation between emitter and base region is required for MWT cells while the emitter formation on the via-holes is required for EWT cells. Figure 7 shows the cross-section structure of the MWT cells on the top and the EWT cells on the bottom, where the EWT cell is free of contact strips on the front surface [50]. On the MWT/EWT module level, the full back interconnection of the cells results in lower cell-to-module loss thanks to avoiding much of the resistive loss existing in the normal double-side interconnection of H-pattern solar cells with tabs [51]. MWT techniques can be used for commercial solar cells mainly focus on the p-type solar cells as well as n-type materials [52] and is successfully put into mass production.

The structures of the solar cells representing other four main high efficiency technologies are illustrated in Figure 8 [5]. In PERC cells (device a), the efficiency improvement is mainly due to the increase of open circuit voltage which is achieved by replacing a continuous Al BSF with the dielectric passivation layer having the local Al BSF [37]. Additionally, the front surface usually has a higher sheet resistance emitter, with or without higher doping underneath metal contacts (selective emitter), which is usually passivated by thermal SiO_2 and/or AlO_x layers.

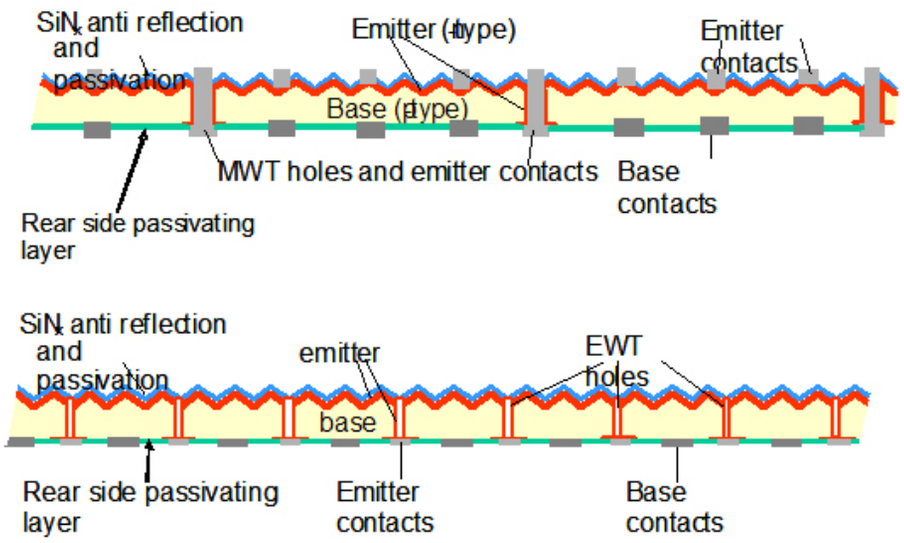

Figure 7. Cross-section structure of the MWT cells (top) and the EWT cells (bottom) [50]

One modification of PERC cell design is the PERL cell concept, where the rear local contacts are additionally passivated by p+ boron diffusion. Instead of annealing of the printed or evaporated Al on the rear side, the rear base contact can also be formed by laser firing. Alternatively, the entire rear surface may have additional boron doping formed either by

diffusion or implantation which may or may not be passivated by dielectric [5]. Such cell structure concepts are currently incorporated in the conventional p-type cells and have been developing in the campus of a large number of cell manufacturers.

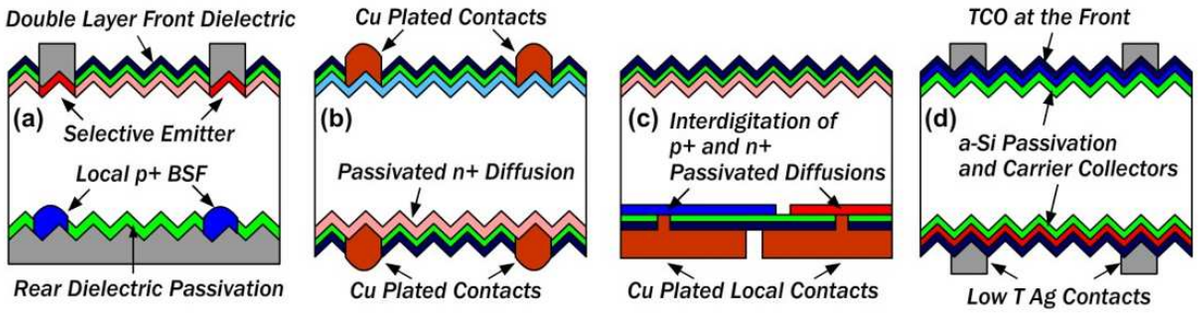

Figure 8. Structure of the solar cells representing four main high efficiency solar cell technologies: (a) PERC/PERL solar cell, (b) bifacial cell with passivated diffusion at the rear (PASHA cell), (c) interdigitated back contact (IBC) solar cell, and (d) silicon heterojunction (SHJ) solar cell. [5]

The other three advanced cell concepts are being developed mainly on the n-type CZ silicon wafers. Bifacial cells (device b) with the passivated diffused carrier collectors and either Al/Ag printed grid or Cu plated grid from both sides of the cell are being developed [53, 54]. The Cu plated metallization increases both short circuit current and filling factor by achieving very thin fingers down to 30 micron width with low resistance, showing the potential of adopting the plating technology in solar industry [55]. IBC cells (device c) utilize the concept that both carrier collectors are formed at the rear side of the cell [56]. This design avoids front metal shading losses and allows the use of thick plated Cu metallization which reduces resistance losses, a recorded efficiency with >21.5% is achieved by the module made from the advanced IBC cells [57]. However, the IBC technology induced a high number of additional manufacturing steps and the use of specialized equipment compared to the common solar cell production line. In SHJ cells, the carrier collectors are formed by depositing thin a-Si layers on both sides of the cell. A transparent conductive oxide (TCO) layer at the front surface (usually Indium Tin Oxide) serves as an antireflection coating, a contacting layer between a-Si and metal electrodes and a lateral conductivity layer. A TCO at the rear surface is usually used for making good ohmic contact and ensuring good internal reflectance of IR light. The efficiency record among large area crystalline silicon solar cells with 24.7% efficiency is reached [58]. The distinguishing feature of SHJ solar cells is due to the almost perfect surface passivation by intrinsic a-Si allowing very high open circuit voltage, which can be higher than 730 mV in commercial solar cell.

5. Conclusions

Upon reviewing of the recent technology developments on the silicon material, cell device architecture and manufacturing processing for the silicon based solar cell, this paper raises the prospective trends of solar industry driven by the global market demands.

Conclusively, pursuing the highest cost performance ratio of solar cell drives the development of the solar industry. The only measurement of a successful solar cell technology is whether the solar cell can be manufactured in a cost effective way. Restricted by the limitation of area available for installing PV system, the trend of pursing higher conversion energy efficiency does pursed steadily by the terminal users. Therefore, reducing the manufacturing process cost is the only way to survive in the solar industry.

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