

We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

6,900

Open access books available

186,000

International authors and editors

200M

Downloads

Our authors are among the

154

Countries delivered to

TOP 1%

most cited scientists

12.2%

Contributors from top 500 universities



WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com



Nanolithography

Gunasekaran Venugopal and Sang-Jae Kim

Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/55527>

1. Introduction

Nanolithography is the branch of nanotechnology concerned with the study and application of the nanofabrication of nanometer-scale structures, meaning nanopatterning with at least one lateral dimension between the size of an individual atom and approximately 100 nm. The term nanolithography is derived from the Greek words “nanos”, meaning dwarf; “lithos”, meaning rock or stone; and “graphein” meaning to write. Therefore the literal translation is “tiny writing on stone”, however nowadays one understands something different whenever this term is associated with nanotechnology. Nanolithography is used e.g. during the nanofabrication of leading-edge semiconductor integrated circuits (nanocircuitry), for nanoelectromechanical systems (NEMS) or for almost any other fundamental application across various scientific disciplines in nanoresearch.

This technology can be suitable to use in nanofabrication of various semiconducting Integrated Circuits (ICs), NEMS and for various applications in research. The modification in semiconductor chips at the nano-scale (in the range of 10^{-9} meter) is also possible. This method is contrasting to various existing nanolithographic techniques like Photolithography (Venugopal, 2011), Nanoimprint lithography (NIL), Scanning Probe Lithography (SPL), Atomic Force Microscope (AFM) nanolithography, Extreme Ultraviolet Lithography (EUVL) and X-ray Lithography.

In this chapter, the various nanolithographic fabrication techniques will be discussed in detail in which we will focus the various nano-patterning techniques/procedures suitable for device fabrication and their engineering applications. This technique is mainly used for nanofabrication. Nanofabrication is the method in which the devices can be designed and manufactured with the dimensions in nanometers [Kim, 1999; Venugopal, 2011a, 2011b, 2011c].

The conventional fabrication techniques like Focused Ion Beam (FIB) and wet etching methods are able to remove or etch the parts in the range to micron scale (Kim, 2001). However, in recent

days, patterning and etching have to be done in nanoscale for specific applications. For that nano-fabrication and nano-level manipulation are the options to choose. Nanomanipulation plays major role in the field of nanofabrication. Nanomanipulation is a technique in which some specific tools are used to manipulate the objects in nanoscale (Parikh, 2008). At present, Scanning Probe microscopic methods involved in AFM [Davis, 2003] and Scanning Tunneling Microscopy (STM) are being used to manipulate the objects in nanometer scale. Specifically, AFM is being used to move the atoms, carbon nanotubes, nanoparticles, various nano-scale objects and also to test integrated circuits. Instruments used in nanolithography include the Scanning Probe Microscope (SPM) and the AFM. The SPM allows surface viewing in fine detail without necessarily modifying it. Either the SPM or the AFM can be used to etch, write, or print on a surface in single-atom dimensions (Venugopal, 2012).

The main drawbacks in the existing lithographic techniques will be carefully analyzed in this chapter. Also the need of nano-patterning for the low-cost, high throughput surface patterning technologies will be presented in this chapter. In addition, the complete coverage of nanolithographic process which includes Introduction, Resists and Masks, Photon-based Lithography, Electron Beam Lithography, Ion Beam Lithography and emerging nanolithographic techniques will be discussed in detail. However, the alternate nanolithography techniques like Micro-contact printing, Nanoimprint Lithography, Scanned Probe Lithography, Dip-pen Lithography will also be discussed in detail in this chapter

2. Importance of micro/nano patterning

Micro/Nano patterning is a one of the miniaturization technique for patterns, especially used for electronics. Nowadays it becomes a standard in biomaterials engineering and for fundamental research on cellular biology by mean of soft lithography. It generally uses photolithography methods but many techniques have been developed. The batch fabrication of microstructures requires a low-cost, high throughput surface patterning technology.

For example, it is important to design nanodevices such as nano-transistors and nanodiodes, nanoswitches and nanologic gates, in order to design nanoscale computers with tera-scale capabilities. All living biological systems function due to molecular interactions of different subsystems. The molecular building blocks (proteins and nucleic acids, lipids and carbohydrates, DNA and RNA) can be viewed as inspiring possible strategy on how to design high-performance NEMS and MEMS that possess the properties and characteristics needed. In addition, analytical and numerical methods are available to analyze the dynamics and three-dimensional geometry, bonding, and other features of atoms and molecules. So, electromagnetic and mechanical, as well as other physical and chemical properties can be studied. Nanostructures and nanosystems can be widely used in medicine and health. Among possible applications of nanotechnology are: drug synthesis and drug delivery (the therapeutic potential will be enormously enhanced due to direct effective delivery of new types of drugs to the specified body sites), nanosurgery and nanotherapy, genome synthesis and diagnostics, nanoscale actuators and sensors (disease diagnosis and prevention), nonrejectable nanoartificial organs design and implant, and design of high-performance nanomaterials.

It is important that these technologies drastically change the fabrication and manufacturing of materials, devices, and systems via:

- higher degree of safety
- environmental competitiveness.
- improved stability and robustness
- higher degree of efficiency and capability, flexibility and integrity supportability and affordability, survivability and redundancy
- Predictable properties of nano composites and materials (e.g., light weight and high strength, thermal stability, low volume and size.

3. Classification of lithographic techniques

There are many techniques through which micro/nano patterning could be possible. They are,

- Photolithography – an conventional and classical method
 - Ion beam Lithography
- X-ray lithography
- Electron beam lithography
- Alternate Nanolithographic Techniques
 - Micro-contact printing
 - Nano-imprint lithography
 - Scanning Probe lithography

3.1. Photolithography – A conventional and classical method

Lithography consists of patterning substrate by employing the interaction of beams of photons or particles with materials. Photolithography is widely used in the integrated circuits (ICs) manufacturing. The process of IC manufacturing consists of a series of 10-20 steps or more, called mask layers where layers of materials coated with resists are patterned then transferred onto the material layer.

A photolithography system consists of a light source, a mask, and an optical projection system. Photoresists are radiation sensitive materials that usually consist of a photo-sensitive compound, a polymeric backbone, and a solvent. Resists can be classified upon their solubility after exposure into: positive resists (solubility of exposed area increases) and negative resists (solubility of exposed area decreases). Fig. 1 shows the schematic of lithographic process in order to make the pattern on the desired substrate.

3.1.1. Patterning graphene device using photolithography

As mechanically exfoliated graphene sheets are in a mesoscopic scale, a lithographic technique is required to make metallic contacts on the sheet. Highly oriented pyrolytic graphite (HOPG) was used as the source material for graphene fabrication. Graphene flakes were mechanically transferred onto a highly doped silicon wafer. The graphene flakes for device fabrication were chosen by color and contrast method. p-type silicon wafers (100) with a boron doping concentration of $N_A = 10^{15} \text{ cm}^{-3}$ can be used in which SiO_2 was thermally oxidized with the thickness of $t_{\text{ox}} = 300 \text{ nm}$. The substrate, p +Si (resistivity 1-30 $\Omega \text{ cm}$), serves as a back-gate for the FET. To keep the disorder level comparable, standard RCA cleaning process followed by acetone and isopropyl alcohol to clean the Si/SiO₂ wafers.

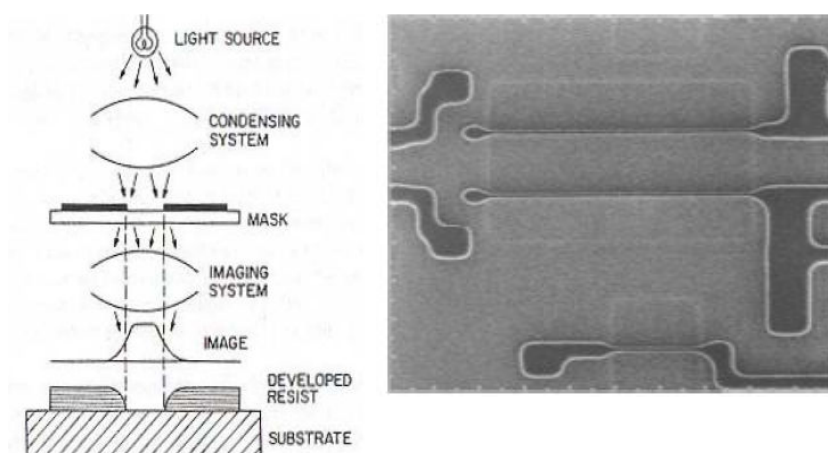


Figure 1. Schematic of photolithographic process. A pattern has been made on the substrate. (Scale bar is not mentioned)

Photo-lithography method can be used in this work to make electrode pattern. Details about the lithography process is discussed below. Figure 2 shows the mask aligner system.



Figure 2. Mask aligner system (MDA-400 M) for lithography pattern fabrication

The various stages of this lithography process or the procedures to be followed for lithographic pattern which are given below:

Stage -1: Wafer or substrate cleaning:

- Use clouse in the entire experiment
- Use Iso-propyl alcohol to clean wafer/substrate
- Use DI water to clean
- Use tissue paper and Air - drying to remove the water particles from the surface of wafer (both side).

Stage – 2: Spin coating of Photo-resist:

- The cleaned wafer to be put in spin coater and start creating vacuum
- Set spin coating rpm and time, using timer 1 and 2. (see the optimized parameter table)
- Put photo resist at the center of the cleaned wafer and spin coat.

Stage – 3: Baking the wafer

Put the spin coated wafer in the hot plate which is in 60° C for 150 sec and then remove wafer from the hot plate and do air cooling (only for back side of wafer)

Stage – 4: UV Exposure

Check and ensure the initial machine set up parameters is done carefully.

- Put the wafer on the substrate stage properly and press substrate Vac. button
- Put the mask in mask- holder and press Mask Vac. button on
- Mount the mask- holder over the substrate stage.
- Use Micrometer handle to bring the substrate stage and mask holder to touch each other. (no gap should be maintained between them). Be careful while doing this process.
- Press Vacuum contact button
- Then wait for 20 sec.
- Turn Align and Exposure knob one by one carefully.
- Now the aligner system will start working and comes to its position.
- Set the expose time by using timer (standard 2.5 sec)
- Now press Exposure button.
- After exposing UV light, turn off align and exposure knob.

Stage – 5: Removal of wafer

- Now put off Vacuum contact button

- Then bring down the stage by using Micrometer handle
- Remove mask holder carefully
- Then press substrate vac. button off and remove wafer from the wafer stage.

Stage – 6: Developing process

The UV-exposed wafer to be put in developer solvent [standard developer solution AZ 300 MIF used]. Slow soaking has to be performed with respect to user need and process. In this process, the UV-unexposed parts (in case of positive PR) the photo-resist will be dissolved in the developer solution and show clear electrode pattern fabricated via mask. Then put the wafer in DI water bath for 1 min and do air- drying to clean the wafer thoroughly.

Stage – 7: Pattern Analysis

After developing,

- Put the developed wafer again in wafer stage and press substrate Vac. Button
- Use CCD camera -module’s adjusting knobs in order to check the developed pattern.

Sample	Spin coating		Prebake		Expose UV with Mask	Developing time	Remarks
1	300 rpm	2200 rpm	60°C	150 sec	55 sec	2 sec	Excellent 4-probe Pattern obtained
	6sec	40 sec					
	(timer 1)	(timer 2)					

Table 1. Optimized condition for Lithographic Process in MDA-400M Mask Aligner (using AZ 5214 positive photo-resist)

The schematic of the detailed lithographic process is presented in Figure.3 (a-e).

After completing the experiment: Mask cleaning to be done

Mask cleaning after exposure is important in the lithographic pattern process. Hence, the defects deposited in mask can be avoided during next experiment time. To clean the mask, the following things to be followed:

- rinse the mask with acetone
- rinse the Mask with IPA
- Dry the Mask using the N₂ gun

The Lithographic process was followed which was described in the above section 2.4. The positive photo-resist (AZ 5214) was spin-coated over the graphene flakes on the substrate. By using photolithography (Mask Aligner MDA- 400M; MIDAS), the graphene flakes were patterned through Cr mask for electrode formation. Then the gold (99.99 %) electrodes of 100 nm- thick were formed through thermal evaporation technique and structured by lift-off using acetone. A metal contact was made to the substrate as the back-gate contact. After lift-off

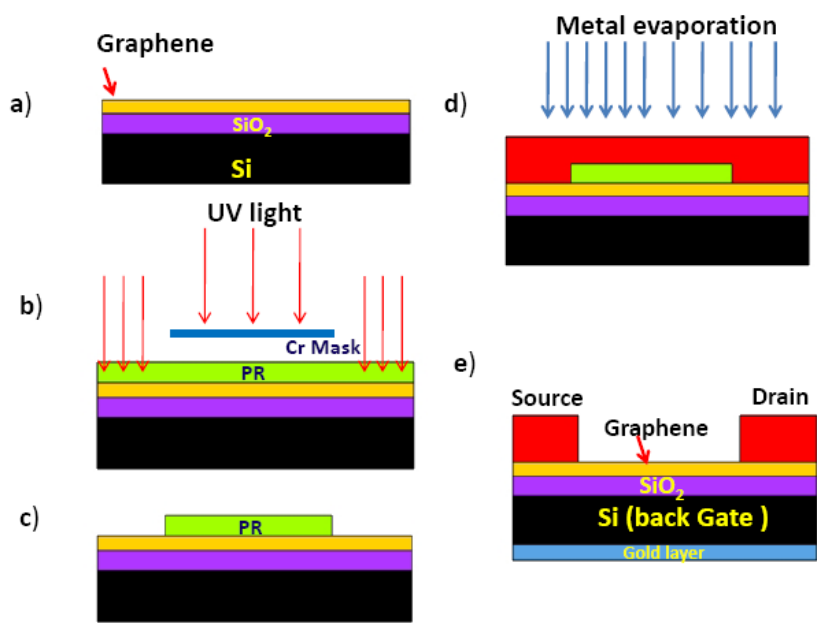


Figure 3. Photolithographic process of electrode patterning on graphene. (a) Graphene flake on Si/SiO₂ substrate (b) Photoresist is spin-coated over the graphene flake and UV light illuminated through Cr mask. (c) the pattern after developing process (d) gold (Au) evaporation through thermal evaporation technique (e) after lift-off process, the device with source and drain electrode structure with back-gate configuration. (Venugopal, 2011).

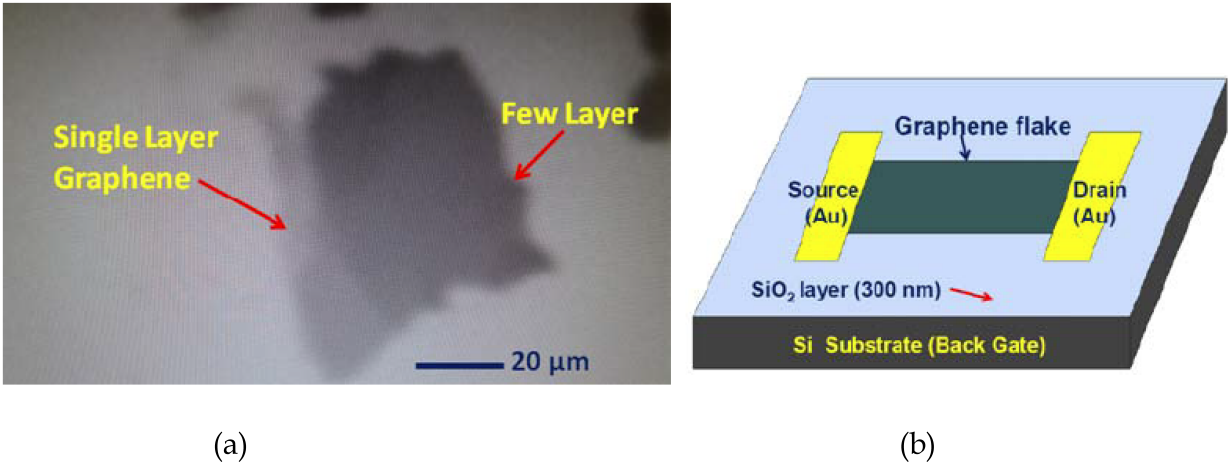


Figure 4. (a) An optical image of single layer graphene is shown. Single and few layer graphene flakes are clearly seen. (b) Schematic of graphene device with electrode pattern.

process, the device was annealed at 200° C in Ar/H₂ atmosphere for 45 min to improve the adhesion with graphene flake as well as to avoid contaminants. After the lithography, metallic Au/Al electrodes are deposited by using thermal evaporation system. Then lift-off process is carried out (using acetone) to get the final pattern for device characterization. If necessary, graphene can be etched to a desired shape by the oxygen plasma ashing with negative or positive electron-beam resist stencils, which were not followed here.

3.2. Ion beam lithography

In this section, ion beam based patterning technique is discussed. For example Focused Ion Beam (FIB) based three dimensional etching method is followed for patterning micro/nano devices (Seliger, 1979).

3.2.1. Focused ion beam 3-D fabrication technique

Miniaturization is the central theme in modern fabrication technology. Many of the components used in modern products are becoming smaller and smaller. Here, the focused ion beam (FIB) direct milling technique will be discussed with the focus on fabricating devices at the micrometer to nano-scale level. Because of the very short wavelength and very large energy density, the FIB has the ability for direct fabrication of structures that have feature sizes at or below $1\text{ }\mu\text{m}$. As a result, the FIB has recently become a popular candidate in making high-quality microdevices or high-precision microstructures (Kim, 2008).

The FIB has been a powerful tool in the semiconductor industry mainly for mask repairing, device modification, failure analysis and integrated circuit debugging. Two basic working modes, ion beam direct write and ion beam projection, have been developed for these applications. The ion beam direct write process, also known as FIB milling (FIBM), is the process of transferring patterns by direct impingement of the ion beam on the substrate. It is a large collection of microfabrication techniques that removes materials from a substrate and has been successfully used for fabricating various three-dimensional (3D) micro structures and devices from a wide range of materials. For the ion beam projection process, a collimated beam of ions passes through a stencil mask and the reduced image of the mask is projected onto the substrate underneath. The ion beam projection process is also known as focused ion beam lithography (FIBL) and can serve as an alternative to conventional optical lithography (Kim, 1999).

For example, to develop the graphite stacked-junctions, planar-type nanostructures, a high-resolution FIB instrument (SII SMI-2050) can be used. The photo-image of FIB unit and the schematic of FIB functions are presented in Figure. 5.

The 3-D etching technique can be followed by tilting the substrate stage up to 90° automatically for etching thin graphite flake. It has freedom to tilt the substrate stage up to 60° and rotate up to 360° . The steps of the fabrication process using a FIB etching are shown in Figure. 6 (a–d). The clear axes of the FIB process configurations with in-plane (x–y) and vertical axes (as z direction) are indicated in an axis diagram in Figure. 6(b). The in-plane area was defined by tilting the sample stage by 30° anticlockwise with respect to the ion beam and milling along the *ab*-plane. The in-plane etching process is shown in Figure. 6(a)–(c). The out of plane or the *c*-axis plane was fabricated by rotating the sample stage by an angle of 180° , then tilting by 60° anticlockwise with respect to the ion beam, and milling along the *c*-axis direction (Saini, 2010). The schematic diagram of the fabrication process for the side-plane is shown in Figure. 6(d).

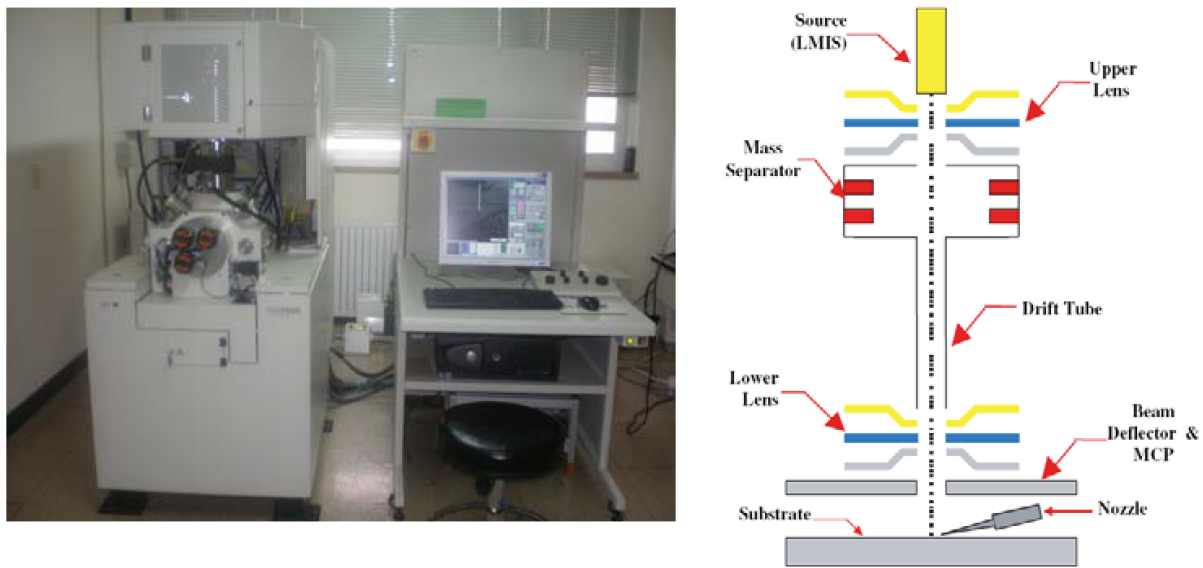


Figure 5. The photograph image of FIB unit and schematic of FIB machine

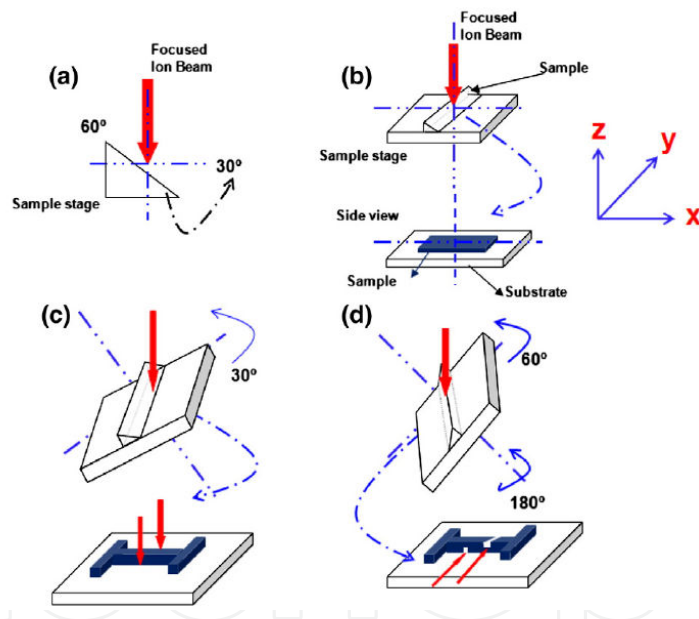


Figure 6. Nanoscale stack fabrication process using focused ion beam 3D etching method. (a) Scheme of the inclined plane has an angle of 60° with ion beam (where we mount sample). (b) The initial orientation of sample and sample stage. (c) Sample stage tilted by 30° anticlockwise with respect to ion beam and milling along *ab*-plane. (d) The sample stage rotated by an angle of 180° and also tilted by 60° anticlockwise with respect to ion beam and milled along the *c*-axis. (Venugopal, 2011d)

By varying the stack height length and in-plane area, the various sizes of stacked-junctions can be fabricated on the graphite layer. The number of elementary junctions in the stack will vary depends on the height of the junction. If junction height is more, the more number of elementary junctions exists which provide larger more resistance in *c*-axis characteristics.

3.3. X-ray lithography

This lithography processes involve the category of nanolithographic techniques, through which transistors with smaller features can be patterned. It uses X-rays to transfer a geometric pattern from a mask to a light-sensitive chemical photoresist, or simply "resist," on the substrate. A series of chemical treatments then engraves the produced pattern into the material underneath the photoresist.

X-ray lithography can be extended to an optical resolution of 15 nm by using the short wavelengths of 1 nm for the illumination. This is implemented by the proximity printing approach. The technique is developed to the extent of batch processing. The extension of the method relies on Near Field X-rays in Fresnel diffraction: a clear mask feature is "demagnified" by proximity to a wafer that is set near to a "Critical Condition". This Condition determines the mask-to-wafer Gap and depends on both the size of the clear mask feature and on the wavelength. The method is simple because it requires no lenses. This technique originated as a candidate for next-generation lithography for the semiconductor industry, with batches of microprocessors successfully produced. Having short wavelengths (below 1 nm), X-rays overcome the diffraction limits of optical lithography, allowing smaller feature sizes. If the X-ray source isn't collimated, as with a synchrotron radiation, elementary collimating mirrors or diffractive lenses are used in the place of the refractive lenses used in optics. Fig. 7 illustrate the process of X-ray lithography.

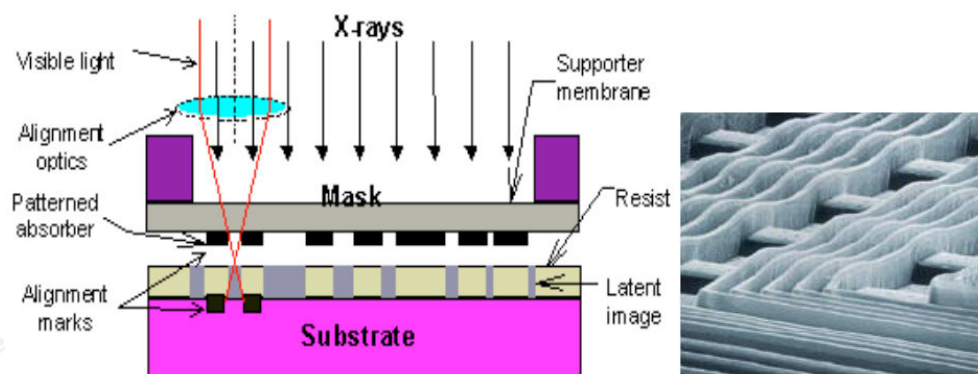


Figure 7. (a) Schematic process of X-ray lithography. (b) structure produced with X-ray lithography (Courtesy Source : SAL, Inc.). (Scale bar is not mentioned)

The X-rays illuminate a mask placed in proximity of a resist-coated wafer. The X-rays are broadband, typically from a compact synchrotron radiation source, allowing rapid exposure. Deep X-ray lithography (DXRL) uses yet shorter wavelengths on the order of 0.1 nm and modified procedures such as the LIGA process, to fabricate deep and even three-dimensional structures. X-rays usually generate secondary electrons as in the cases of extreme ultraviolet lithography and electron beam lithography. While the fine pattern definition is due principally to secondaries from Auger electrons with a short path length, the primary electrons will sensitize the resist over a larger region than the X-ray exposure.

3.3.1. Advantages of X-ray lithography

There are several advantages in X-ray lithography.

1. Resolves diffraction issues
2. Shorter wavelengths (0.1 - 10 nm) can be used
3. Smaller features can be patterned

3.3.2. Disadvantages of X-ray Lithography

The following are the disadvantages of X-ray Lithography

1. Usage of X-ray masks
2. Deformation during the process
3. Vibrations during the process
4. Time consuming process

3.4. E-beam lithography

Electron Beam Lithography uses a tightly focussed beam of electrons scanned over the surface of a substrate. Typically, electron beam lithography with ultra high resolution (UHR) is used at the very beginning of a multiple technique and a multiple step process in a top down approach in order to transfer the nanostructure into the substrate or subsequently build up a device in a layer by layer fashion.

3.4.1. E-beam applications

This E-beam lithographic technique is mainly having following advantages in research field:

1. Research and Development
2. Advanced processing techniques
3. Future processing equipment
4. Can convert SEM to be used as an EBL machine
5. Minimum resolution is slightly larger
6. Used with photolithography and X-ray lithography to create next generation devices.

For nanolithography with ultra high resolution down to sub10nm feature sizes, complete dedicated e-beam writer systems or converted scanning electron microscopes (SEM) can be used. With the help of a design editor and a pattern generator, the electron beam is guided over the substrate surface, which is covered with electron beam sensitive resist such as PMMA, in order to generate a resist mask which then can be further used for nanopattern transfer. The steps of e-beam lithography is given in Fig. 8.

a. Resist Preparation

In this Process, the PMMA solution is spin coated onto the sample and baked to harden the film and remove any remaining solvent.

b. Exposure

Selected areas of sample are exposed to a beam of high energy electrons

c. Development

Sample is immersed in developer solution to selectively remove resist from the exposed area.

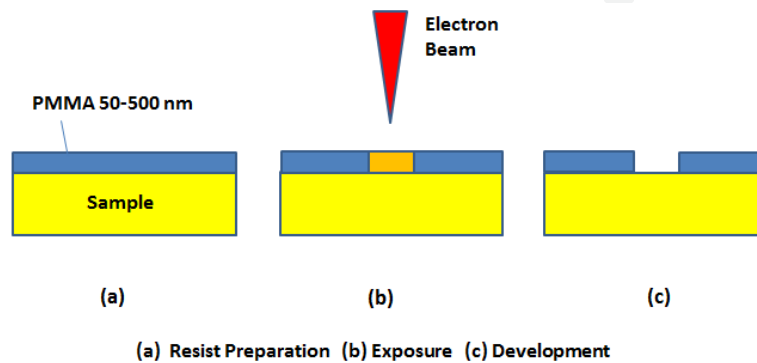


Figure 8. Schematic process of e-beam lithography. (a) Resist Preparation (b) Exposure (c) Development

3.4.2. E-beam lithography advantages

1. The resolution is not limited by diffraction; minimum feature is written on the nanoscale.
2. Can write smaller features than X-ray lithography and photolithography
3. Pattern is written directly to the wafer.
4. Used to develop specialized devices and prototype devices
5. Fast turn-around time
6. This employs a beam of electron instead of photons

3.4.3. E-Beam Lithography Disadvantages

1. Not an efficient process for industrial processing
2. Takes multiple hours to pattern entire wafer
3. Machines are costly
4. Greater than 5 million dollars
5. System is more complex than photolithography system

6. Scattering and over exposure result in minimum feature being larger
7. Slow throughput

3.5. Alternate nanolithographic techniques

3.5.1. Micro-contact printing (soft lithography)

This is known as soft lithography that usually uses the relief patterns on a PDMS (polydimethylsiloxane) stamp in order to form patterns of self-assembled monolayers (SAMs) of ink on the surface of a substrate through conformal contact. This technique has wide range of application in cell biology, microelectronics, surface chemistry, micromachining, Patterning cells, patterning DNA and Patterning protein.

Figure 9 represents the process of Micro-contact printing. This process involves the application of ink to stamp, application of stamp to surface, removal of stamp and residues rinsed off

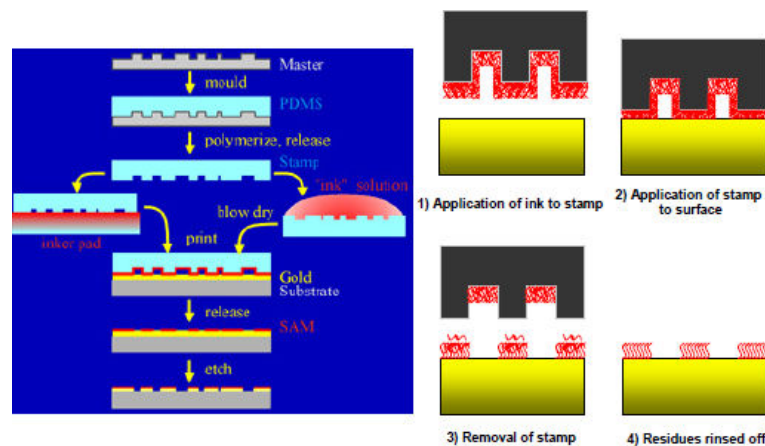


Figure 9. Schematic of the Micro-contact printing process (Courtesy: IBM Zurich)

Advantages of Micro-contact printing:

1. Very simple and easy pattern procedures to create micro-scale features
2. This can be done in a traditional laboratory environment. No need clean room facility
3. Using single master, multiple stamps can be made
4. Reliability of individual stamps which can be used for many times.
5. It is a cheaper method.

Limitation in Micro-contact Printing:

1. Diffusion of ink from PDMS stamp to surface during patterning
2. Shrinking of stamp is one of main problem in which stamp can eventually shrink in size resulting difference in desired dimensions of the substrate patterning

- 3. Contamination of substrate
- 4. Stamp deformation

3.5.2. Nano-imprint lithography

Nanoimprint lithography (NIL) is an emerging process that can produce sub-10nm features. It is a simple process that uses a mould to emboss the resist with the required pattern. After embossing the resist, compressed resist material is removed using anisotropic etching and the substrate exposed. It can produce features at extremely small resolutions that cover a large area with a high throughput and relatively low cost, which is main advantage of this technique. It can be adapted to transfer all components needed to create a thin film transistor on a plastic substrate. It involves pressing and heating a thin film between a patterned template and a substrate. Upon heating, the patterned film adheres only to the substrate [ref Fig. 10]. This has high throughput and is relatively inexpensive compared to developing extreme deep UV lithography for commercial viability. It is also flexible enough to be used at chip level with several layers or at the wafer level when single layer is required. It can give resolutions lower than 10nm with high throughput at low cost. One of the current barriers to production at these resolutions is the development of mould. It can be used for fabricating nanoscale photo-detectors, silicon quantum-dot, quantum wire and ring transistors (Chou, S.Y. 1996)

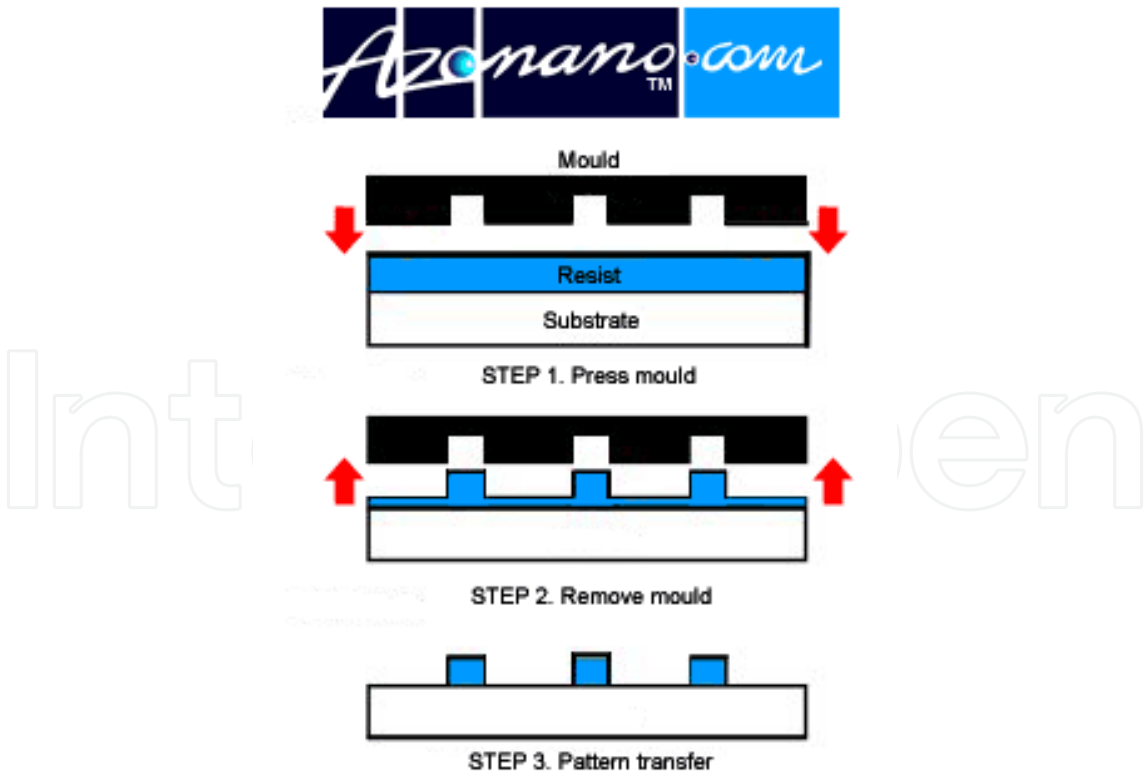


Figure 10. Schematic diagram of the steps involved in the nanoimprint lithographic process [Courtesy: Source: AZo-Nano]

Applications of Nanoimprint lithography

1. It can be used to make optical, photonic, electrical and biological devices.
2. Advances in mould manufacturing will have wide application of NIL in smaller devices.

3.5.3. Scanning Probe Lithography (SPL)

SPL is an emerging area of research in which the scanning tunneling microscope (STM) or the atomic force microscope (AFM) is used to pattern nanometer-scale features. The patterning methods include mechanical patterning such as scratching or nano-indentation, or local heating with sharp tip (Dagata, 1995). When a voltage bias is applied between a sharp probe tip and a sample, an intense electric field is generated in the vicinity of the tip (Ref. Fig. 11).

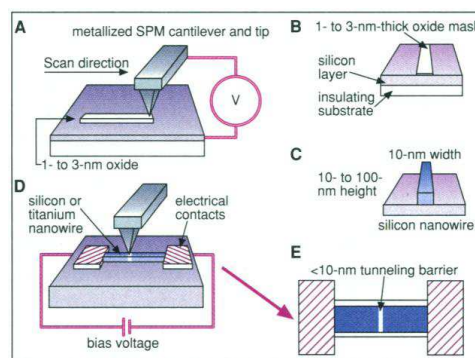


Figure 11. Schematic diagram of the Scanning probe lithography. Electrical bias between a conducting tip and a substrate induces a highly localized enhanced oxidation [Courtesy Source: Dagata et al, *Science*, Vol.270, pp.1625-1626, 1995]

Advantages:

1. This process can make nanopatterns without optical apparatus.
2. It can control deposited material by hydrophobicity of the surface.
3. This process can make arbitrary patterns by controlling the trajectory of AFM tip.
4. This process involves small scan area, Low throughput.
5. By using this technique, it is possible to make nanowire, SET, etc.. By using an organic solvent, the organic material can be deposited on the surface.

SPL method is a recognized as a lithographic tool in the deep sub-micron regime, as it is compatible with standard semiconductor processing. There are four main factors which dictate the viability of SPL as a known patterning method for the semiconductor industry. They are

1. Throughput (wafers/hour)
2. Resolution
3. Alignment accuracy

4. Reliability

Scanning probe lithography involves a set of lithographic techniques, in which a microscopic or nanoscopic stylus is moved mechanically across a surface to form a pattern. In this method, another technique describes a SPL technique which is known as Dip Pen Nanolithography.

Dip Pen Nanolithography - in this process, the patterning is done by directly transferring chemical species to the surface. We can call this process as constructive process.

3.5.3.1. Dip Pen Nanolithography (DPN)

Dip Pen Nanolithography (DPN) is known as a soft-lithography technique that uses an AFM scanning probe tip to draw nanostructures. In this process, a probe tip is coated with liquid ink, which then flows onto the surface to make patterns wherever the tip makes contact. This kind of directwrite technique provides high-resolution patterning capabilities for a number of molecular and biomolecular “inks” on a variety of substrates. Substrates are the base material that the images are printed on. Some of the applications of the DPN technique include sol gel templates that are used to prepare nanotubes and nanowires, and protein nanoarrays to detect the amount of proteins in biological samples such as blood. (Ref. Fig. 12).

This process was first developed by Professor Chad Mirkin at Northwestern University Nanotechnology Institute for depositing thin organic films in patterns with feature sizes of around 10 nm (about 20 times better than the best optical lithography) (Mirkin, 1999).

In DPN technology, the ink on a sharp object is transported to a paper substrate via capillary forces. The capillary transport of molecules from the AFM tip to the solid substrate is used in DPN to directly “write” pattern consisting of a relatively small collection of molecules in nanometer dimensions. An AFM tip is used to write alkanethiols with 30-nm line width resolution on a gold thin film in a manner analogous to that of a dip pen. Molecules are delivered from the AFM tip to a solid substrate of interest via capillary transport, making DPN a potentially useful tool for creating and functionalizing nanoscale devices (Mirkin, 1999).

Several factors decide the resolution of DPN:

1. The grain size of the substrate affects DPN resolution much as the texture of paper controls the resolution of conventional writing.
2. The tip-substrate contact time and thus the scan speed influence DPN resolution.
3. Chemisorption and self-assembly of the molecules can be used to limit the diffusion of the molecules after deposition.
4. Relative humidity seems to affect the resolution of the lithographic process by controlling the rate of ODT transport from the tip to the substrate. The size of the water meniscus that bridges the tip and substrate depends on relative humidity. For example, the 30-nm wide line required 5 min to generate in a 34% relative humidity environment, whereas the 100-nm line required 1.5 min to generate in a 42% relative humidity environment.

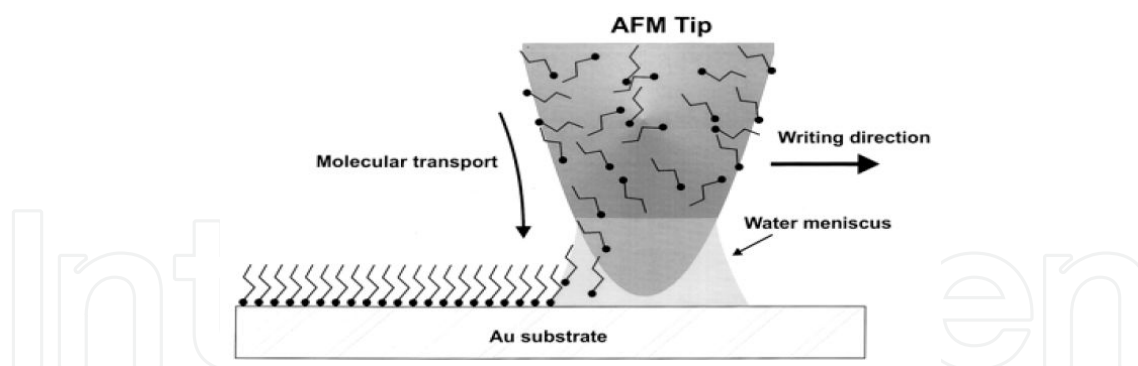


Figure 12. Schematic representation of DPN. A water meniscus forms between the AFM tip coated with ODT and the Au substrate. The size of the meniscus, which is controlled by relative humidity, affects the ODT transport rate, the effective tip-substrate contact area and DPN resolution. [Courtesy: C.A. Mirkin, et al, Science 283, 661, 1999]

3.5.3.2. DPN application on semiconductor surfaces

Dip-Pen Nanolithography can not only apply to gold surface using alkyl or aryl thiols as inks, but also to semiconductor surfaces, such as silicon and gallium arsenide. Hexamethyldisilazane (HMDS) is used as the ink to pattern and modify (polarity) the surface of semiconductors. Lateral force microscopy (LFM) can be used to differentiate between oxidized semiconductor surfaces and patterned areas with the deposited monolayers of HMDS. The choice of the silazane ink is a critical component of the process since the traditional adsorbates such as trichlorosilanes are incompatible with the water meniscus and polymerize during ink deposition. This work provides insight into additional factors, such as temperature and adsorbate reactivity, that control the rate of the DPN process and paves the way for researchers to interface organic and biological structures generated via DPN with electronically important semiconductor substrates (Ivanisevic, 2001).

3.5.3.3. DPN application on magnetic materials: Approach to high density recording and storage

Over the past decade, there has been considerable interest in methods for synthesizing and patterning nanoscale magnetic materials. These nanomaterials show novel size-dependent properties, are potentially useful for high-density recording. Two of the main challenges in this field are: (a) site-and shape-specific patterning of hard magnetic nanostructure on the sub-100 nm scale; (b) ability to reliably and reproducibly read/write such minute features. The conventional top-down approach in recording media is plagued by the difficulties of etching and patterning novel hard magnetic systems, especially as the individual recording elements approach the super paramagnetic limit at room temperature operations. DPN can be used as a direct-write method for fabricating "hard" magnetic barium hexaferrite, $\text{BaFe}_{12}\text{O}_{19}$ (BaFe), nanostructures. This method utilizes a conventional atomic force microscope tip, coated with the BaFe precursor solution, to generate patterns that can be post-treated at elevated temperature to generate magnetic features consisting of barium ferrite in its hexagonal magnetoplumbite (M-type) structure. Features ranging from several hundred nm down to below 100 nm can be generated. (Fu, 2003).

4. Conclusion

In conclusion, the complete nanolithographic processes which include introduction, resists and masks, Photon-based lithography, electron beam lithography, ion beam lithography and emerging nanolithographic techniques like the alternate nanolithography techniques Micro-contact printing, Nanoimprint Lithography, Scanned Probe Lithography, Dip-pen Lithography were briefly discussed in this chapter. As a conclusion, the following table can presents the complete scenerio of the nanolithographic process.

	Ideal	Advanced Optical	Electron Beam	Nano Imprint
Pattern shape	Any	Any	any	Any
Resolution (nm)	Good	Good	Good	Good
Alignment (nm)	Good	Good	Good	Poor
Large & small Pattern	Yes	Yes	No	Yes
Throughput (wafers/hr)	High	High	Low	Medium
Running Cost	Low	High	Low	Medium
Initial Cost	Low	High	Medium	Low

Table 2. Comparison of results between conventional and Nanolithographic methods

Acknowledgements

The authors would like to acknowledge the supports from the National Research Foundation of Korea Grant under contract number 2011-0015829 and 2011 Jeju Sea Grant College Program funded by the Ministry of Land, Transport and Maritime Affairs (MLTM), Republic of Korea. A part of this work was carried out at the Research Instrument Center (RIC) at Jeju National University, Jeju, and Republic of Korea. Also the author (G.V) would like to thank the management of Karunya University for continuing this research through their KSTG seed money grant No. KU/Reg/D(R)/OO/12/29 dated 21.01.2012 and DST NanoMission, New Delhi.

Author details

Gunasekaran Venugopal¹ and Sang-Jae Kim²

1 Karunya University, Department of Nanosciences and Technology, Tamil Nadu, India

2 Jeju National University, Department of Mechatronics Engineering, Jeju, South Korea

References

- [1] Chou, S. Y. (1996). Nano imprint Lithography. *J. Vac. Sci. Technol. B.*, , 14, 4129.
- [2] Dagata, J A. (1995). Device Fabrication by Scanned Probe Oxidation. *Science*, , 270, 1625-1626.
- [3] Davis, R. C. (2003). Chemomechanical surface patterning and functionalization of silicon surfaces using an atomic force microscope. *Appl. Phys. Lett.*, , 82
- [4] Fu, L. (2003). Dip-Pen Patterning of magnetic materials. *Nano Lett.*, , 3, 757-760.
- [5] Ivanisevic, A. (2001). Dip-pen nanolithography on semiconductor surfaces. *J. Am. Chem. Soc.*, , 123, 7887-7889.
- [6] Kim, S. J. (1999). D intrinsic Josephson junctions using c-axis thin films and single crystals. *Supercond. Sci. Technol.*, , 12, 729-731.
- [7] Kim, S. J. (1999). Submicron Stacked-junction Fabrication from $\text{Bi}_2\text{Sr}_2\text{CaCu}_2\text{O}_{8+\delta}$ Whiskers by Focused-Ion-Beam Etching. *Appl. Phys. Lett.*, , 74(8), 1156-1158.
- [8] Kim, S. J. (2001). Fabrication and Characteristics of Submicron Tunnelling Junctions on High Tc Superconducting c-axis Thin Films and Single Crystals. *J. Appl. Phys.*, , 89(11), 7675-7677.
- [9] Kim, S. J. (2008). Development of Focused Ion Beam Machining Systems for Fabricating Three-dimensional Structures. *Jpn. J. Appl. Phys.*, , 47(6), 5120-5122.
- [10] Mirkin, C. A. (1999). Dip-pen Nanolithography. *Science*, , 283
- [11] Parikh, D. (2008). Nanoscale Pattern Definition on Nonplanar Surfaces Using Ion Beam Proximity Lithography and Conformal Plasma-Deposited Resist. *J. Microelectromech. Syst.*, , 17
- [12] Saini, S. (2010). Characterization of Submicron Sized Josephson Junction Fabricated in a $\text{Bi}_2\text{Sr}_2\text{Ca}_2\text{Cu}_3\text{O}_{10+\delta}$ (Bi-2223) Single Crystal Whisker. *J. Supercond. Nov. Magn.*, , 23, 811-813.
- [13] Seliger, R. L. (1979). High-resolution, Ion-beam Processes for Microstructure Fabrication. *J. Vac. Sci. Technol. B.*, , 16(6), 1610-1612.
- [14] Venugopal, G. (2011). Temperature dependent transfer characteristics of graphene field effect transistors fabricated using photolithography. *Curr. Appl. Phys.*, , 11, S381-S384.
- [15] Venugopal, G. (2011a). Fabrication of Nanoscale Three-dimensional Graphite Stacked-junctions by Focused-ion-beam and Observation of Anomalous Transport Characteristics. *Carbon*, , 49(8), 2766-2772.

- [16] Venugopal, G. (2011b). Temperature Dependence of Transport Anisotropy of Planar-type Graphite Nano-structures Fabricated by Focused Ion Beam. *J. Nanosci. Nanotechnol.* , 11(1), 296-300.
- [17] Venugopal, G. (2011c). Fabrication and Characteristics of Submicron Stacked-Junctions on Thin Graphite Flakes. *J.Nanosci. Nanotechnol.* , 11(2), 1405-1408.
- [18] Venugopal, G. (2011d). Investigation of electrical transport characteristics of nano-scale stacks fabricated on thin graphite layer. *Thin Solid Films.* , 519, 7095-7099.
- [19] Venugopal, G. (2012). An investigation of the electrical transport properties of graphene-oxide thin Films. *Matl. Chem. Phys.* , 132, 29-33.