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Control of Single-Hole Transition in Carbon Nanotube Transistor with Quantum Dot in Gate Insulator at Room Temperature

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1. Introduction

Flash memory has been leading player in the nonvolatile memories in recent ten years because of a small cell size and a high scalability. A gate length of a flash memory has reached to 20 nm. A number of charges also have been getting smaller. a several hundred in the 20 nm device. However, a flash memory needs high operating voltage for short write time. The high operating voltage causes low durability [1, 2], and a signal due to capacitance coupling between neighbor cells becomes larger with further miniaturization [1, 2]. Therefore, lower operating voltage and stronger capacitive coupling between a gate electrode and a charge storage compare to neighbor cells are desired.

A single walled carbon nanotube (SWNT) is a cylindrical structure with a diameter of about 1 nm [3-8]. A SWNT with a semiconductor property is very sensitive to the charge around the SWNT, because whole SWNT channel can be easily modulated by the arounded charge because of the small diameter of a SWNT. This high sensitivity can sense even a single-charge [9-14]. Therefore, many sensor applications of SWNT have been reported, e.g. bio- and gas-sensors [15-31]. Moreover, a cylindrical type memory can achieve higher electric field concentration compare to a planer type memory because of higher capacitive coupling between charge storage and a gate electrode. Therefore, the signal noise attributed to the parasitic capacitances between a neighbor cells can be reduced by this higher capacitive coupling.

In this study, we succeeded in fabricating a multifunctional quantum transistor using the particle nature and wave nature of holes in SWNT. This transistor can operate as anresonant tunneling transistor (RTT) and also as an single-hole transistor (SHT). An RTT is a device

that uses the wave nature of hole and an SHT uses the particle nature of hole in the SWNT. Both devices need tunneling barriers at both sides of the quantum island. The RTT needs strong coupling while the SHT needs weak coupling between the quantum island and the electrodes. Usually, these tunneling barriers are made from thin oxide layers, etc. Therefore, the thickness of the tunneling barriers and the coupling strength cannot normally be controlled in a given device. In the present device, however, the Schottky barriers act as the tunneling barriers between the SWNT quantum island and electrodes. Therefore, the thickness of the tunneling barriers and the coupling strength between the SWNT and electrodes can be controlled by the applied gate voltage V_G.

SWNT electron devices show hysteresis characteristics in gate voltage-drain current characteristics. The hysteresis characteristics are caused by gate-voltage-dependent charge fluctuation, e.g., adsorption of water molecules around a SWNT [32], charging into insulator layer around a SWNT [33], and charging into amorphous carbon around a SWNT [34] By eliminating these origins of the hysteresis characteristics, the number of fluctuating charges becomes small and a single-charge fluctuating around the SWNT channel can be distinguished by a SWNT multi-functional quantum transistor.

Moreover, a SWNT transistor surrounded by SiN_x /Al_2O_3 double gate insulator layers with quantum dot in the insulator layers was fabricated, demonstrating discrete threshold voltage shift resulting in discrete drain current modulation at room temperature.

2. Detection of single-charge around SWNT channel

2.1. Method

We have eliminated the three origins of the hysteresis characteristics of a SWNT field effect transistor mainly pointed out in current reports [32-35]. To burn out amorphous carbon, we annealed a SWNT at low temperature in oxidizable atmosphere [33]. To reduce the number of adsorbed atmosphere molecules, we covered the channel with a silicon dioxide layer. To reduce the number of trap sites in the insulator, we reduced channel length to 73 nm. The SWNT multi-functional quantum transistor fabricated by the process mentioned above shows almost no hysteresis characteristics in the gate voltage rage from -40 to 40 V. Moreover, an abrupt discrete switching of the source-drain current is observed in the electrical measurements of the SWNT multi-functional quantum transistor at 7.3 K. These random telegraph signals (RTS) are attributed to charge fluctuating charge traps near the SWNT multi-functional quantum transistor conduction channel. The current-switching behavior associated with the occupation of individual electron traps is demonstrated and analyzed statistically.

2.2. Sample preparations

A schematic of the sample structure is shown in Fig. 1. SWNT was prepared as follows. An n⁺-Si wafer with a thermally grown 300 nm thick oxide was used as a substrate. Layered Fe/Mo/Si (2 nm/20 nm/40 nm) catalysts were evaporated using an electron-beam evaporator

under a vacuum of 10^{-6} Pa. These layered catalysts were patterned on the substrate using the conventional photo-lithography process. SWNT was grown by thermal chemical vapor deposition (CVD) using the mixed gases of hydrogen and argon-bubbled ethanol. After the growth of the SWNT, it was purified by burning out the amorphous carbon around the SWNT in an air atmosphere at a temperature of several hundred degrees Celsius [31]. Ti (30 nm) electrodes were deposited on the patterned catalysts as the source and drain, and on the back side of the n$^+$-Si substrate for the gate, using the electron-beam evaporator under a vacuum of 10^{-6} Pa. The distance (*L*) between the source and drain was 73 nm. Thus, a back gate type multi-functional quantum transistor with an SWNT channel was fabricated that had the functions of an RTT and an SHT. The single-charge measurement was carried out with the structure that silicon dioxide layer is on the SWNT channel.
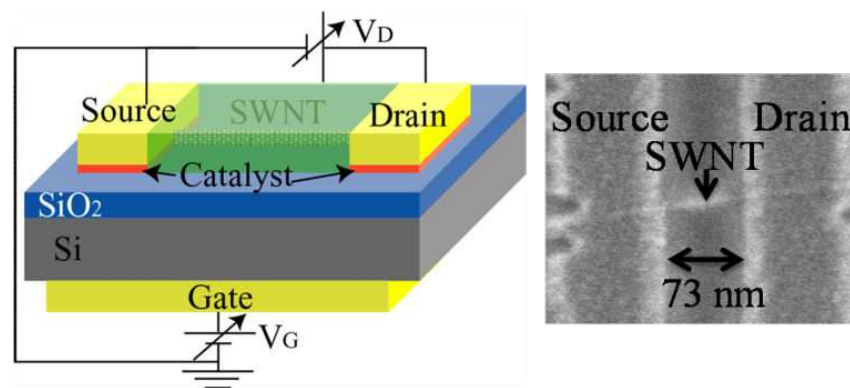

Figure 1. Schematic structure of SWNT multi-functional quantum transistor covered by silicon dioxide layer. The channel length is 73 nm. The inset shows a SEM image around the channel before silicon dioxide deposition. A few charge storages are fabricated in the SiO$_2$ layer.

2.3. Results and discussions

2.3.1. Single charge sensitivity of SWNT multi-functional quantum transistor

Figure 2 (a) shows the time dependence of the conductance of the SWNT multi-functional quantum transistor at 7.3 K with a gate bias of V_G=-25.36 V. A short sampling time of 10 ms was set in the dynamic characteristic measurements shown in Fig. 10.

The applied gate voltage was under the Fabry-Perot interference region. The SWNT multi-functional quantum transistor shows RTS, as shown in Fig. 2(a), The RTS showed three levels, n, n+1 and n+2, of the conductance shown in Fig. 2(a). At a lower applied gate voltage, current levels higher than n+2 such as n+3 and n+4 appeared. The multiple levels of RTS are attributed to charge fluctuating charge storages near the conduction channels of the SWNT multi-functional quantum transistor. Moreover, because there was a single-charge storage including multiple energy levels or were some charge storages being at almost the same distances from the conductance channel of the SWNT multi-functional quantum transistor, the RTS appeared. Figures 2(b) and (c) show histograms of the conductance levels of RTS at V_G= -25.36 V and V_G= -25.39 V, respectively. The three peaks of conductance of RTS expressed as

P_n, P_{n+1}, and P_{n+2} are shown in Figs. 2(b) and 2(c). The conductance levels of the three peaks directly correspond to the conductance levels of RTS. On the other hand, the relative heights of the peaks correspond to occupation probabilities at each conductance level of the RTS. The heights of the peaks depend on applied gate voltage. P_n decreases and P_{n+1} and P_{n+2} increase with slightly increasing applied gate voltage from V_G= -25.36 to -25.39 V, which means that the energy levels in the charge storage are modulated by applied gate voltage.
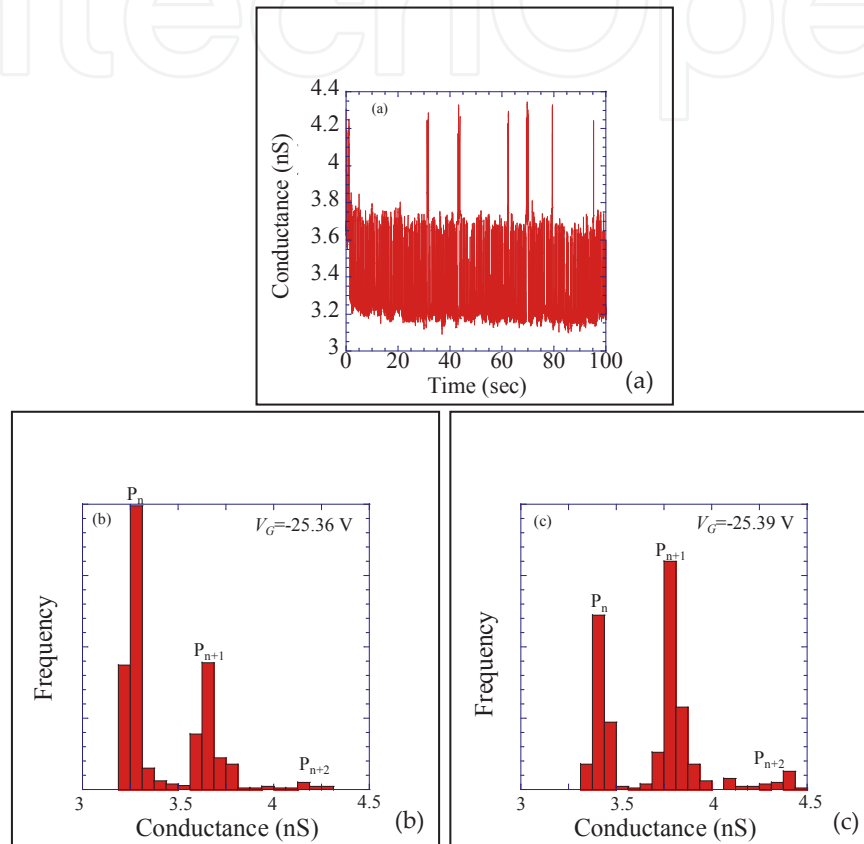

Figure 2. a) Time dependence of drain current with RTS at a gate voltage of V_G=-25.36 V. The time dependence of drain current was sampled for 100 s and the sampling time was 10 ms; (b) and (c) show histograms of the conductance levels of RTS at V_G= -25.36 and -25.39 V, respectively. $P_n$decreases and P_{n+1} and P_{n+2} increase with slightly increasing applied gate voltage from V_G= -25.36 to -25.39 V.

The gate voltage dependences of the natural log of the ratio between the m_{th} peak and the $(m+1)_{th}$ peak in the conductance histogram P_{m+1}/P_m (m= n, n+1, n+2, , n+4) are shown in Fig. 3(a). The natural log of P_{m+1}/P_m linearly depends on applied gate voltage and saturates in each V_G. Each starting point of saturation is marked by an arrow in Fig. 3(a). The charge storage energy levels are floating. Therefore, modulations of energy by V_G may be different at each charge storage. We believe that the reason why the natural log of P_{m+1}/P_m saturates at each V_G may depend on the difference in energy modulation by $V_G$at each charge storage.

The charge transition is modeled, as shown in Fig. 4(a), in which the energy barrier is between the SWNT and the charge storage.Figures 3(b)-3(e) are enlargement plots of each P_m

$_{+1}/P_m$ (m= n, n+1, n+2, , n+4).The energy differences ΔE_n between the charge storage energy level E_n and the Fermi level E_f are expressed as $\Delta E_n = E_f - E_n$, which is modulated by the applied gate voltage V_G. According to equilibrium statistical mechanics, P_{m+1}/P_m is given by

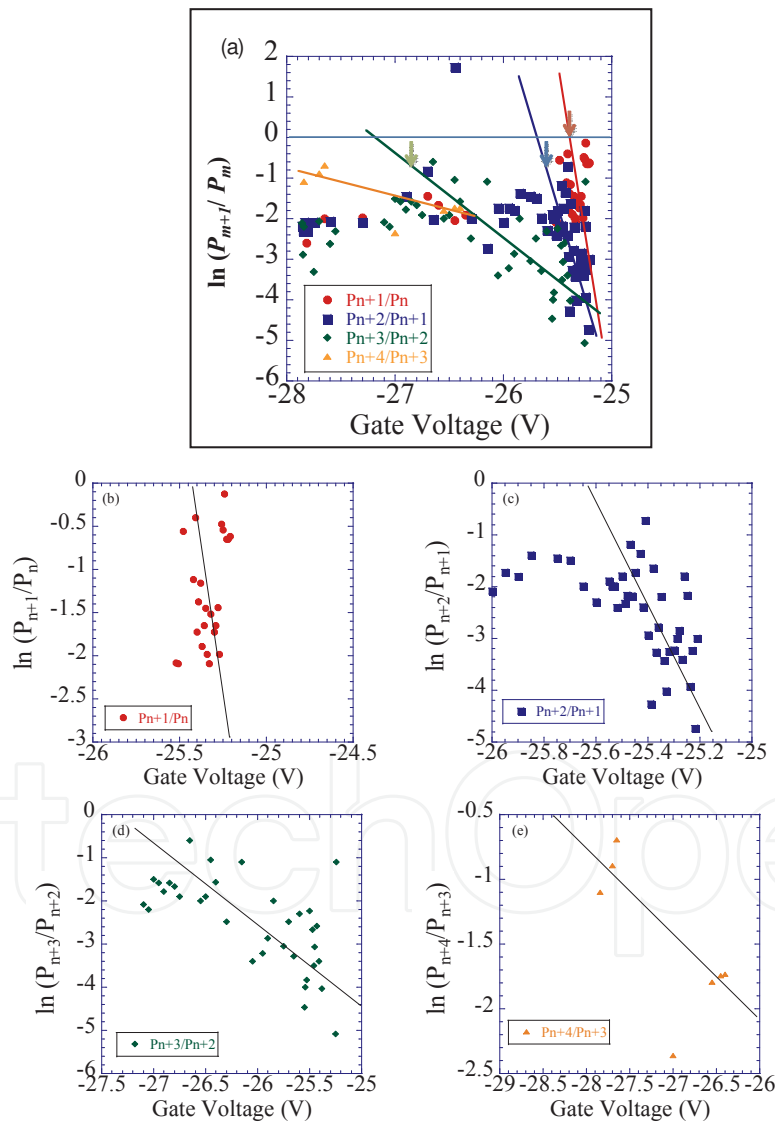$$P_{m+1}/P_m = (g_f/g_s)e^{-\beta(E_f - E_n)} = (g_f/g_s)e^{-\beta\Delta E_n} \tag{1}$$

Figure 3. a) Gate voltage dependence of the natural log of the ratio between the occupancy probabilities of the mth current levels P_{n+1}/P_n.(b)-(e) Enlargement plots of each P_{m+1}/P_m (m=n, n+1, n+2, n+4). The natural log of P_{n+1}/P_n was linearly dependent on gate voltage, the slopes of which are -10.4, -4.78, -1.47, and -0.690 V^{-1}, respectively.

where g_f and g_S are the degeneracy of the top of valence band and the charge storage, respectively [32]. g_f/g_S is assumed to be 1. β is $1/kT$. E_n includes the contributions of e electrostatic potential induced by V_G, intrinsic energy level in the storage, and Coulomb charging energy. The basis of eq. (1) is the Arrhenius equation. In this model, the height of the barrier is the energy difference between E_f and E_n. Assuming a linear dependence of ΔE_n on V_G, ΔE_n can be written as $\Delta E_n = \alpha e(V_0 - V_G)$, where α is the gate modulation coefficient, and is a constant value of 0.062. α is obtained from the periods of Fabry-Perot interference characteristic on V_D and V_G. V_0 is the offset voltage, and is obtained from the intersecting point of the extrapolating line of the fitting lines and the line of $\ln(P_{m+1}/P_m) = 0$. Therefore, eq. (1) is transformed to

$$\ln(P_{m+1}/P_m) = -\beta e\alpha(V_0 - V_G) \tag{2}$$

Equation (2) is the transformed Arrhenius equation, in which V_G is the parameter.
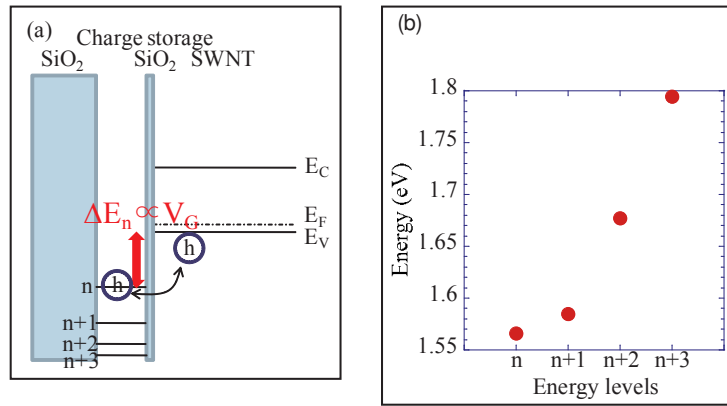

Figure 4. a) Schematic model of charge storage. When the charge storage energy level is coincident with the top of the valence band owing to applied gate voltage, the carrier goes and comes between them through the barrier with tunneling. The exiting probabilities of the carrier at the charge storage and the valence band depend on the relative height of their energy levels under equilibrium condition..(b) Estimated charge storage energy levels from the dependence of P_{n+1}/P_n on V_G shown in Figs. 3(b)-(e) and eq. (1). The energy levels increase from 0.17 to 0.28 eV with increasing number of energy levels in the region of V_G from -25 to -28 V.

From the dependence of P_{n+1}/P_n on V_G shown in Fig. 11 and eqs. (1) and (2), ΔE_n can be obtained, and is shown in Fig. 12(b). The obtained energy levels are from 1.57 to 1.79 eV.

2.4. Conclusion

In summary, we succeeded in fabricating and demonstrating a multi-functional quantum transistor using the particle nature and wave nature of holes in SWNT. This transistor can operate in the wave nature mode as an RTT and in the particle nature mode as an SHT. We were able to reveal that the principle of the characteristic transition from an SHT to an RTT is the modulation of the coupling strength between the SWNT quantum island and the electrodes by the applied V_G.

3. Control of single-hole transition at room temperature

3.1. Method

A SWNT transistor surrounded by SiNx /Al$_2$O$_3$ double gate insulator layers with quantum dot in the insulator layers was fabricated, demonstrating discrete threshold voltage shift resulting in discrete drain current modulation by single-hole transfer at room temperature.

3.2. Sample preparation

The fabrication process of the SWNT transistor surrounded by SiN$_x$ /Al$_2$O$_3$ double gate insulator layers with quantum dot in the insulator layers is shown in Fig. 1. The fabrication process of the single-charge memory is shown in Fig. 5. A SWNT was grown by the chemical vapor deposition process on the SiO$_2$ substrate, and the source and drain electrodes were formed on the SWNT, where a distance between the electrodes was 70 nm. The SiO$_2$ under the SWNTwas etched off by chemical wet process and the SWNT bridge was formed between source and drain electrodes as shown in Fig. 5 (a). Then, the SWNT was surrounded by double-layers of SiN$_x$ of 27 nm over Al$_2$O$_3$ of 3 nm using atomic layer deposition (ALD) process (FlexAL, Oxford Inst.) using tris(dimethylamino)silane for SiNx and trimethylaluminum for Al$_2$O$_3$ as a precursor as shown in Fig. 1(b).Figure 5 (c) – (g) shows scanning electron microscope (SEM) images of a device after an ALD process. Owing to thin insulator layers and highacceleration energy of SEM, the insulator layers can be seen through and the difference of the materials are recognized because of the difference of the contrast as shown in Fig. 5(c)-(g). Fig. 5(c) and (d) shows the top view and bird's eye view of the device near the gap. The gap of 10 nm length is realized between the source and drain electrode. Fig. 5(e) shows the cross sectional view around the drain electrode indicated by dashed square in Fig. 5(b). The drain electrode is fully covered by the insulator layers, and the space under the channel can be seen. Fig. 5(f)-(g) shows the side view and cross sectional view of the SWNT surrounded by the insulator layer of 30 nm thick in which the SWNT is seen as a light gray line at the center of the insulator. Fig. 5(h) and (i)are the schematic cross sectional view and 3D image of the device after the formation of the top gate electrode.

Using an isotropic deposition of the ALD process 10 nm length of top gate electrode is realized self-assembly as shown in Fig. 5(h). The 30 nm thick insulator layer was deposited from the source and drain electrode which narrowed a gap between the electrodes from 70 nm to 10 nm by the isotropic ALD deposition. Ti and Au were deposited through this gap to form a top gate electrode. Thus, the 10 nm long top gate electrode was self-assembly formed at a center of the source and drain electrode which is covered by the ALD insulator layers. The SiNx deposition by ALD was carried out with low deposition rate of 0.31 Å/ cycle. The low deposition rate enables to form the composite of nano particles of Si, N and C at the beginning of the deposition because of the low uniformity and the incomplete reaction. The composite of nano particles may act as a dot for the charge storage.
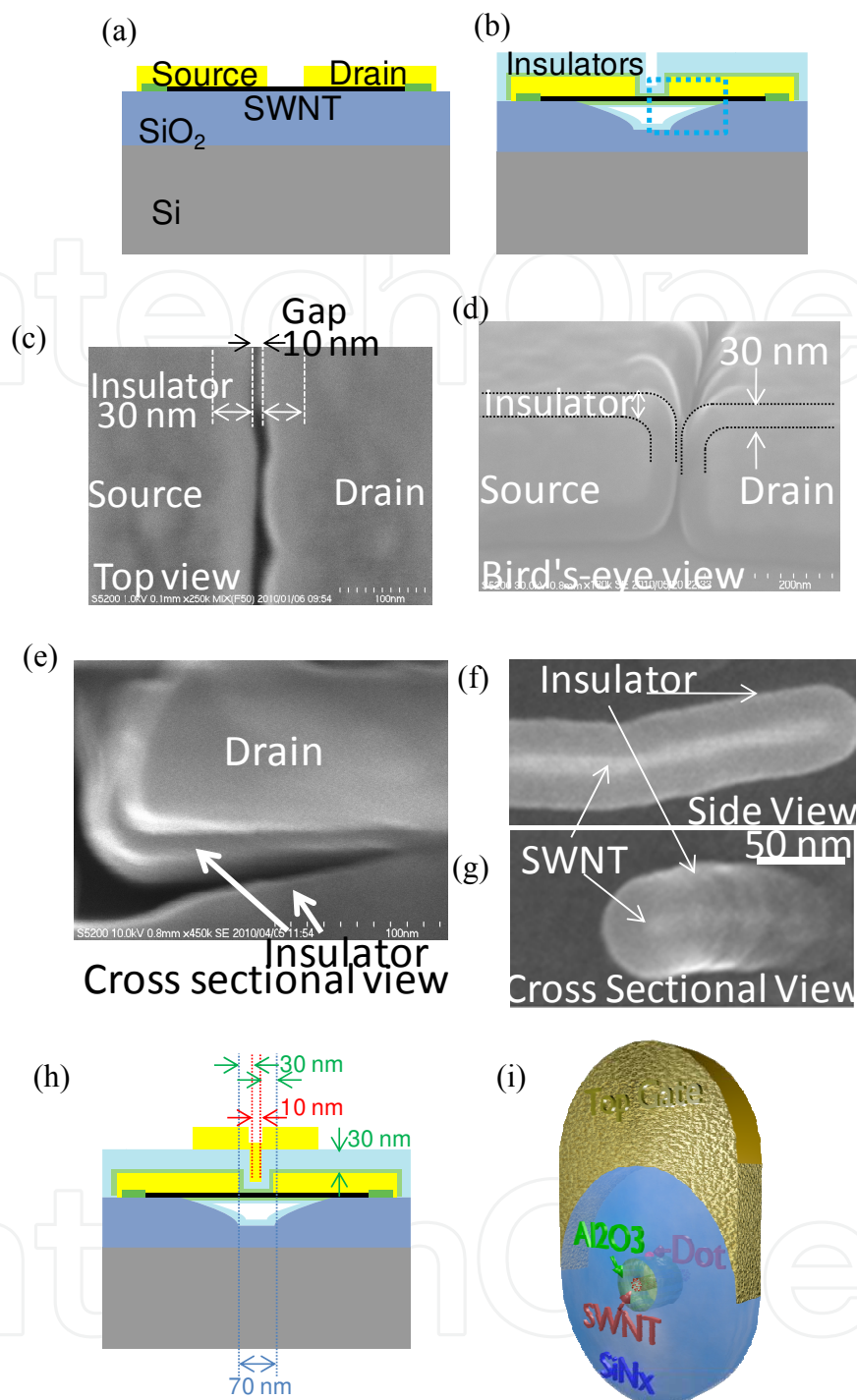
Figure 5. The device fabrication process. (a) Schematic of the device after the SiO₂etching, which is the cross sectional view along with the SWNT. (b) Schematic of the device after the ALD process, which is the cross sectional view along with the SWNT. Scanning electron micro scope images of (c) Top view, (d) Bird's eye view and (e) Cross sectional view around the drain electrode. (f) Side view and (g) Cross sectional view of the SWNT surrounded by the insulator layer. (h) Schematic of the device after the top gate electrode fabrication, which is the cross sectional view along with the SWNT. (i) 3D image around the SWNT channel.

3.3. Results and discussions

Figure 6(a) shows drain current characteristic as a function of the applied top gate voltage at room temperature. The source and drain voltage were set at -25 mV and 25 mV, respectively.
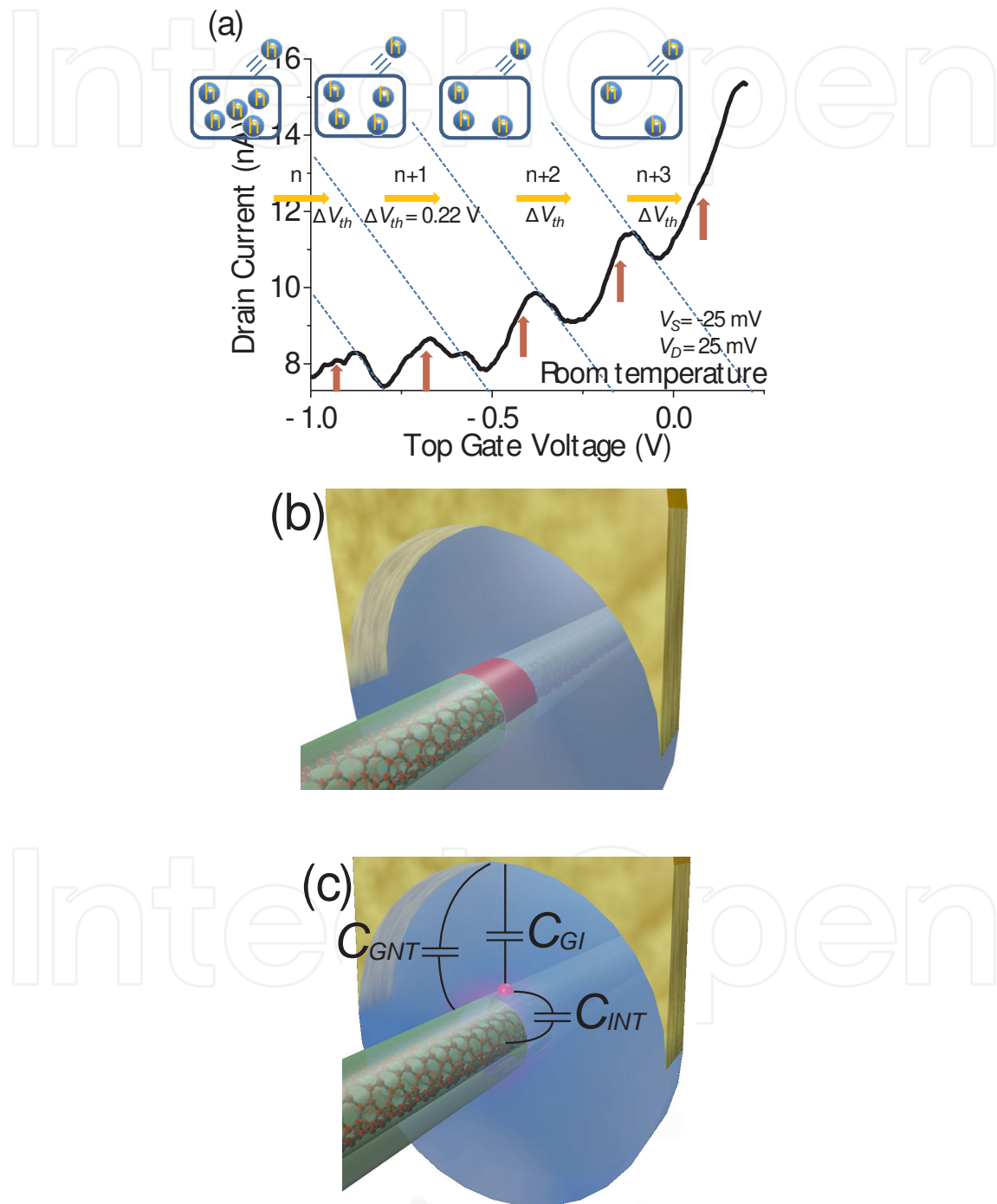

Figure 6. a) Drain current characteristic as a function of applied top gate voltage at room temperature.(b) The area under the top gate electrode, which is 10 nm length.(c) The mutual capacitances in the device.

The drain current showed the repeated threshold shift characteristic indicated by right-arrows, where the drain current repeatedly showed the drastic increases indicated by up-arrows and the gradual decreases indicated by tangential lines with increase of the applied top gate voltage as shown in Fig. 6(a). The threshold shift was observed in period of 0.22 V with increasing applied top gate voltage. The holes had been accumulated in the charge storage dot by negative gate voltage at the beginning of the measurement. By increasing the applied top gate voltage, the hole started to transfer to the SWNT channel. At this moment, the potential of the charge storage dot decreased and blocked the transfer of other holes i.e., Coulomb blockade effect. Therefore, the hole could transfer one by one, where each transfer was separated by Coulomb blockade effect. The decreased potential of the charge storage dot also impacted the SWNT channel and the drain current drastically increased because of p type channel. Therefore, the drastic increases of the drain current in Fig. 6(a) are attributed to a single-hole transfer from the accumulated charge storage dot to the SWNT channel. The gradual decreases of the drain current are attributed to the channel modulation by the applied top gate voltage as well as a conventional MOS-FET device. The charge storage dot density of $D = 1 \times 10^{12}$ cm^{-2} was estimated from the C-V measurement. The area just under the top gate electrode indicated by the red band in the Fig. 6(b) was 91.4 nm^2 from πrL, where r is the thickness of the Al$_2$O$_3$ layer, L is the length of the top gate electrode. The estimated number of charge storage dot was 0.914 from DπrL. Therefore, almost one charge storage dot exists in the area just under the top gate electrode.

Moreover, the threshold voltage shift caused by single charge transition was given by $\Delta V_{th} \sim$ e/ $(C_{GI} + C_{GNT})$ [37-41], where C_{GI} and C_{GNT} was mutual capacitances of the top gate electrode and the charge storage dot and of the top gate electrode and the SWNT as shown in Fig. 6(c)

C_{GI} and C_{GNT} were estimated to be C_{GI} = 734 zF and C_{GNT} = 20.7 zF, from the simulation by the finite element method, where conductor sphere of 1 nm diameter at 3 nm above the SWNT was assumed in the simulation as the single charge storage dot. The estimated threshold voltage shift was estimated to be 0.201 V. This is in good agreement with the threshold voltage shift of the drain current characteristic as shown in the Fig. 6(a).
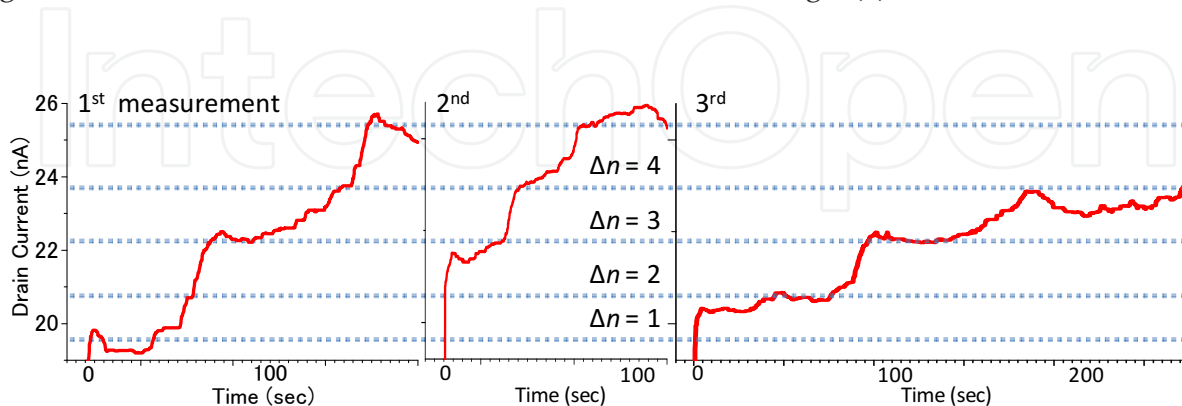

Figure 7. a) – (c) The time dependence characteristics of the drain current at room temperature. The top gate voltage of $\Delta V_{TG} = - 4$ V had been applied before the measurements, and $\Delta V_{TG} = 1$ V was applied in the measurements. Same measurements were repeated in three times and plotted in (a) – (c).

Figure 7(a) – (c) shows the time t dependence of the drain current characteristics at top gate voltage of V_{TG} = 1 V at room temperature, in which V_{TG} = -4 V had been applied before t = 0 sec. The source and drain voltages were set at 25 mV and -25 mV in the measurement. The measurement was carried out three times, and each measurement was plotted in Fig. 7(a) – (c), respectively.

The drain currents were plotted in the same time scale, however, time lengths of the measurement were different. The drain current increased with elapsed time and also showed five steps indicated by dotted lines as shown in Fig. 7(a) – (c). The increases of the drain current at each step were the same among Fig. 7(a) – (c). However, the time width of each steps showed the variety even if the steps were at the same drain current levels in Fig. 7(a) – (c). From the plots, average of the drain current width was t_{ave} = 68.82 s. Tunneling provability was roughly estimated to be 0.0145 from $1/t_{ave}$. By applying V_{TG} = -4 V before the measurement, holes had been accumulated in the storage dot. After the top gate voltage was turned to 1 V at t = 0 sec, the accumulated holes started to transfer from storage dot to the SWNT channel one by one. The SWNT channel was modulated by the transferred single-hole, and showed discrete drain current levels i.e., the current steps as shown in Fig. 7(a) – (c). In other words, discrete changes of the drain current directly corresponded to the variation of single-hole Δn in the storage dot. Therefore, the transfer of single-hole could be directly counted as the discrete modulation of the drain current at room temperature in real-time [34]. Moreover, each transfer of single-hole took several tens of second because of thick tunneling barrier of Al_2O_3 of 3 nm. The variety of time widths of each step attributed to the stochastic transfers of single-hole. These characteristics also indicate the evidence of the single-hole transfer in the device.

4. Summary

In conclusion, control of single transition in carbon nanotube transistor with quantum dot in gate insulator at room temperature was demonstrated. To obtain the narrow top gate electrode of 10 nm, the isotropic deposition by ALD process for the insulators formation was used. At the same time, the concentric circle structure of insulators was formed around the SWNT channel which was on the center. The defective deposition of SiNx on Al_2O_3 may formnano size particles at the beginning of the deposition process, which worked as charge storage dots. Because of the narrow top gate electrode, only single-dot was just under the top gate electrode which stored single-hole. Though top gate electrode could surround only the upper half of insulators that realized electric field concentration all-around the SWNT channel and caused Fowler-Nordheim tunneling which make the hole transfer to the charge storage dot. The drain current affected by the stored charge showed the threshold voltage shift as a function of the applied top gate voltage at room temperature. This threshold voltage shift is attributed to the abrupt potential energy change by the transfer of single-holes from the dot to the SWNT channel. The time dependence of the drain current after changing the top gate voltage showed the step like characteristics. The time widths of the steps corresponded to the interval of stochastic transfer of single-holes, and the number of the steps

corresponded to the variation of single-holes in the dot. By observing the steps, the individual transfers of single-holes could be counted in real-time at room temperature. The SWNT property with high sensitivity for the charges is suitable to the application of the single-charge memory. And the SWNT must be one of the leading candidates for the single-charge applications.

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References

[1] Bez, R., Camerlenchi, E., Modelli, A., & Visconti, A. (2003). Introduction to Flash Memory. *Proceedings of the IEEE*, 91(4), 489-502.

[2] Aritome, S., Shirota, R., Hemink, G., Endoh, T., & Masuoka, F. (1993). Reliability Issues of Flash Memory Cells. *Proceedings of the IEEE*, 81(5), 776-788.

[3] Iijima, S. (1991). Helical microtubules of graphitic carbon. *Nature*, 354-56.

[4] Iijima, S., & Ichihashi, T. (1993). Single-shell carbon nanotubes of 1 -nm diameter.

[5] Bethune, D. S., Kiang, C. H., de Vries, M. S., Gorman, G., Savoy, R., Vazquez, J., & Beyers, R. (1993). Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls. *Nature*, 363-605.

[6] Ajyayan, P. M., Ebbesen, T. W., Ichihashi, T., Iijima, S., Tanigaki, K., & Hiura, H. Opening carbon nanotubes with oxygen and implications for filling. Nature (1993). , 362-522.

[7] Tans, S. J., Verschueren, A. R. M., & Dekker, C. (1998). Room-temperature transistor based on a single-carbon nanotube. *Nature*, 393-49.

[8] Single- and multi-wall carbon nanotube field-effect transistors. Appl. Phys. Lett.; , 73-2447.

[9] Biercuk, M. J., Reilly, D. J., Buehler, T. M., Chan, V. C., Chow, J. M., Clark, R. G., & Marcus, C. M. M.Charge sensing in carbon-nanotube quantum dots on microsecond timescales. Phys. Rev. B (2006). , 73-201402.

[10] Guo, J., Kan, E. C., Ganguly, U., & Zhang, Y. High sensitivity and nonlinearity of carbon nanotube charge-based sensors. J. Appl. Phys. (2006). , 99-084301.

[11] Peng, H. B., Hughes, M. E., & Golovchenko, J. A. Room-temperature single charge sensitivity in carbon nanotube field-effecttransistors. Appl. Phys. Lett. (2006). , 89-243502.

[12] Kamimura, T., Ohono, Y., & Matsumoto, K. Carbon Nanotube Fabry-Perot Device for Detectionof Multiple Single Charge Transitions. Jpn. J. Appl. Phys. (2009). , 48-025001.

[13] Andresen, S. E. S., Danneau, F. W., Gunnarsson, D., & Hakonen, P. J. Highly sensitive and broadband carbon nanotube radio-frequencysingle-electron transistor. J. Appl. Phys. (2008). , 104-0033715.

[14] Ohori, T., Ohno, Y., Maehashi, K., Inoue, K., Hayashi, Y., & Matsumoto, K. Quantized characteristics in carbon nanotube-based single-hole memory with a floating nanodot gate. Appl. Phys. Lett. (2011). , 98-223101.

[15] An, K. H., Jeong, S. Y., Hwang, H. R., & Lee, Y. H. Enhanced sensitivity of a gas sensor incorporating single-walled carbon nanotube-polypyrrole nanocomposites. Adv. Mater. (2004). , 16(12), 1005-1009.

[16] Ong, K. G., Zeng, K., & Grimes, C. A. A Wireless, Passive Carbon Nanotube-BasedGas Sensor. IEEE Sensor J. (2002). , 2(2), 82-88.

[17] Li, J., Lu, Y., Ye, Q., Cinke, M., Han, J., & Meyyappan, M. Carbon Nanotube Sensors for Gas andOrganic Vapor Detection. Nano Lett. (2003). , 3(7), 929-933.

[18] Suehiro, J., Zhou, G., & Hara, M. Fabrication of a carbon nanotube-based gas sensor using dielectrophoresis and itsapplication for ammonia detection by impedance spectroscopy. (2003). LL114., 109.

[19] Abraham, J. K., Philip, B., Witchurch, A., Varadan, V. K., & Redy, C. C. A compact wireless gas sensor usinga carbon nanotube/PMMA thin filmchemiresistor. Smart Mater. Struct. (2004). , 13-1045.

[20] Kojima, A., Hyon, C. K., Kamimura, T., Maeda, M., & Matsumoto, K. Protein Sensor Using Carbon Nanotube Field Effect Transistor. Jpn. J. Appl. Phys. (2005). A) , 1596-1598.

[21] Chen, R. J., Choi, H. C., Bangsaruntip, S., Yenilmez, E., Tang, X., Wang, Q., Chang, Y., & Dai, H. An Investigation of the Mechanisms of Electronic Sensing ofProtein Adsorption on Carbon Nanotube Devices. J. Am. Chem. Soc. (2004). , 126-1563.

[22] Abe, M., Ohno, Y., & Matsumoto, K. Schottky barrier control gate-type carbon nanotube field-effect transistor biosensors. J. Appl. Phys. (2012). , 111-034506.

[23] Hakamata, Y., Ohno, Y., Maehashi, K., Inoue, K., Matsumoto, K., & External-Noise, . External-Noise-Induced Small-Signal Detection with Solution-Gated Carbon Nanotube Transistor.Appl. Phys. Express (2011). , 4-045102.

[24] Ohno, Y., Maehashi, K., Inoue, K., & Matsumoto, K. Improving faint-signal sensitivity of electrolyte-gated carbon nanotube field-effect transistors using external noise. Proc. of 2010 IEEE Nanotechnology Materials and Devices Conference (2010). , 10-13.

[25] Abe, M., Ohno, Y., & Matsumoto, K. Dependence of sensitivity of biosensor for carbon nanotube field-effect transistor with top-gate structures. J. Appl. Phys. (2010). , 107-084504.

[26] Yamamoto Y., Ohno Y., Maehashi K., Inoue K., Matsumoto K.Electrical Detection of Negatively Charged Proteins Using n-Type Carbon Nanotube Field-Effect Transistor Biosensors.Jpn. J. Appl. Phys. (2010). BD10-1-02BD, 10-4.

[27] Maehashi, K., Katsura, T., Kerman, K., Takamura, Y., Matsumoto, K., Tamiya, E., & Label, . Label-Free Protein Biosensor Based on Aptamer-Modified Carbon Nanotube Field-Effect Transistors. Anal. Chem. (2007). , 79-782.

[28] Star, J., Gabriel, K., Bradley, , & , G. Gruner Electronic Detection of Specific Protein Binding Using Nanotube FET Devices Nano Lett. (2003). , 3-459.

[29] High-Performance Carbon Nanotube Field-Effect Transistors with Local Electrolyte Gates.Jpn. J. Appl. Phys.; , 47-2060.

[30] Besteman, K., Lee, J., Wiertz, F. G. M., Heering, H. A., Dekker, C., & Enzyme, . Enzyme-Coated Carbon Nanotubes as Single-Molecule Biosensors. Nano Lett. (2003). , 3-727.

[31] Maehashi, K., Matsumoto, K., Takamura, Y., Tamiya, E., & Aptamer, . (2009). Aptamer-Based Label-Free Immunosensors Using Carbon Nanotube Field-Effect Transistors. *Electroanalysis*, 21-1285.

[32] Ohno Y., Maehashi K., Inoue K., Matsumoto K.Fabrication of room-temperature-operating carbon nanotube single-charge transistors.Sensor andMaterials.(2009). , 21-393.

[33] Kim, W., Javey, A., Vermesh, O., Wang, Q., Li, Y., & Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. Nano Lett. (2003). , 3-193.

[34] Radosavljevic´, M., Freitag, M., Thadani, K. V., & Johnson, A. T. Nonvolatile Molecular Memory Elements Based on Ambipolar Nanotube Field Effect Transistors. Nano Lett. (2002). , 2-761.

[35] Martel, R., Derycke, V., Lavoie, C., Appenzeller, J., Chan, K. K., Tersoff, J. ., & Avouris, Ph. Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes. Phys. Rev. Lett. (2001). , 256805 EOF.

[36] Kamimura, T., & Matsumoto, K. Reduction of Hysteresis Characteristics in Carbon Nanotube Field-Effect Transistors by Refining Process. IEICE Trans. Electron. (2004). E-87C , 1795-1798.

[37] Peng, H. B., Hughes, M. E. ., & Golovchenkoa, J. A. Room-temperature single charge sensitivity in carbon nanotube field-effect transistors. Appl. Phys. Lett. (2006). , 243502 EOF.

[38] Room-temperature Si single-electron memory fabricated bynanoimprint lithography. Appl. Phys. Lett.;, 83(11), 2268-2270.

[39] Yano, K., Ishii, T., Hashimoto, T., Kobayashi, T., Murai, F., & Seki, Koichi. Room-temperature single-electron memory. IEEE Trans. Elect. Dev.(1994). , 41(9), 1628-1638.

[40] Guo, L., Leobandung, E., & Chou, S. Y. Silicon Single-Electron Transistor MemoryOperating at Room Temperature. Science(1997). , 275-649.

[41] Nakajima, A., Futatsugi, T., Kosemura, K., Fukano, T., & Yokoyama, N. Room temperature operation of Si single-electron memory with selfalignedfloating dot gate. Appl. Phys. Lett. (1997). , 70-1742.

[42] Gruneis, A., Esplandiu, M. J., Gracia-Sanchez, D., & Bachtold, A. Detecting Individual Electrons Using aCarbon Nanotube Field-Effect Transistor. Nano Lett. (2007). , 7(12), 3766-3769.