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Efficient CAD Tool for Noise Modeling of RF/Microwave Field Effect Transistors

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Additional information is available at the end of the chapter

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1. Introduction

Efficient models are the key of successful designs. Widely used in modern wireless communication systems, active devices such as field-effect transistors (FETs) require up-to-date models to achieve reliable circuit/system design especially in terms of noise performance since most of communication systems operate in noisy environments. [1]-[2]. Among existing FET modeling techniques, the full-wave modeling approach can be considered as the most reliable but is computationally expensive in terms of CPU time and memory [3]-[5]. On the other side, circuit equivalent models are fast but cannot accurately integrate EM effects. Therefore, a hybrid transistor model, called the semi-distributed model (Sliced model) has been proposed [6]. With the assumption of a quasi transverse electromagnetic (TEM) approximation, this model can be seen as a finite number of cascaded cells, each of them representing a unit transistor equivalent circuit. However, this model presents some limitations. In fact, in mm-wave frequencies, it cannot precisely take into account some EM effects that can significantly degrade the overall device behavior, like the wave propagation and the phase cancellation phenomena. To efficiently include such effects more general distributed models need to be developed. In this chapter, a new distributed FET model is proposed. In this model [7]- [8], each infinitely unit segment of the device electrodes was divided into two parts namely, active and passive. The passive part describes the behavior of the transistor as a set of three coupled transmission lines while the active part that can be modeled by an electrical equivalent distributed circuit whose elements are all per-unit length.

To demonstrate the efficiency of our model in terms of noise, we applied the Laplace transformation to the device as an active multi-conductor transmission line structure and successfully compared its simulated response to measurements. Furthermore, by easily including the effects of scaling, the proposed algorithm is suitable for integration in computer-aided-design (CAD) packages for MMIC design.

2. Signal modeling of high-frequency FET

A typical millimeter-wave field effect transistor (FET) is shown in Fig.1. It consists on three coupled electrodes (i.e., three active transmission lines).

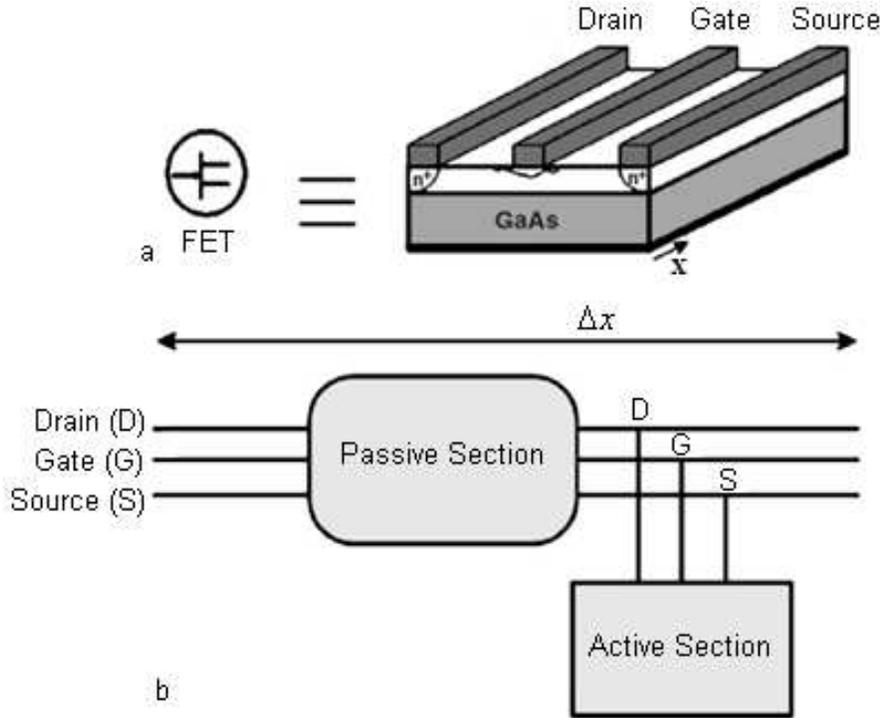


Figure 1. (a) 3D structure of FET used in millimeter-wave frequency. (b) a segment of distributed model along the wave propagation direction.

In the lower part of the microwave spectrum, the longitudinal electromagnetic (EM) field is very small in magnitude as compared to the transverse field [9]-[10]. Therefore, a quasi-TEM mode can be considered to obtain the generalized active multi-conductor transmission line equation. An equivalent circuit of a section of the transistor is shown in Fig. 2. Each segment is represented by a 6-port equivalent circuit which combines a conventional FET small-signal equivalent circuit model with a distributed circuit to account for the coupled transmission line effect of the electrode structure where the all parameters are per unit length. By applying Kirchhoff's current laws to the left loop of the circuit in Fig. 2 with the condition $\Delta x \rightarrow 0$, we obtain the following system of equations [11]-[12]:

$$\frac{\partial I_d(x,t)}{\partial x} + C_{11} \frac{\partial V_d(x,t)}{\partial t} - C_{12} \frac{\partial V_g(x,t)}{\partial t} - C_{13} \frac{\partial V_s(x,t)}{\partial t} + G_m V'_g(x,t) + G_{ds}(V_d(x,t) - V_s(x,t)) = 0 \quad (1)$$

$$\frac{\partial I_g(x,t)}{\partial x} + C_{22} \frac{\partial V_g(x,t)}{\partial t} - C_{12} \frac{\partial V_d(x,t)}{\partial t} + C_{gs} \frac{\partial V'_g(x,t)}{\partial t} = 0 \quad (2)$$

$$\frac{\partial I_s(x,t)}{\partial x} + C_{33} \frac{\partial V_s(x,t)}{\partial t} - C_{13} \frac{\partial V_d(x,t)}{\partial t} - C_{gs} \frac{\partial V'_g(x,t)}{\partial t} - G_m V'_g(x,t) + G_{ds}(V_s(x,t) - V_d(x,t)) = 0 \quad (3)$$

$$\frac{\partial V_d(x,t)}{\partial x} + R_d I_d(x,t) + L_{dd} \frac{\partial I_d(x,t)}{\partial t} + M_{gd} \frac{\partial I_g(x,t)}{\partial t} + M_{ds} \frac{\partial I_s(x,t)}{\partial t} = 0 \quad (4)$$

$$\frac{\partial V_g(x,t)}{\partial z} + R_g I_g(x,t) + L_{gg} \frac{\partial I_g(x,t)}{\partial t} + M_{gd} \frac{\partial I_d(x,t)}{\partial t} + M_{gs} \frac{\partial I_s(x,t)}{\partial t} = 0 \quad (5)$$

$$\frac{\partial V_s(x,t)}{\partial z} + R_s I_s(x,t) + L_{ss} \frac{\partial I_s(x,t)}{\partial t} + M_{ds} \frac{\partial I_d(x,t)}{\partial t} + M_{gs} \frac{\partial I_g(x,t)}{\partial t} = 0 \quad (6)$$

with

$$C_{11} = C_{dp} + C_{ds} + C_{dg} \quad C_{22} = C_{gp} + C_{dg} \quad C_{33} = C_{sp} + C_{ds} \quad C_{12} = C_{dg} \quad C_{13} = C_{ds}$$

where V_d , V_g , and V_s , are the drain, gate and source voltages, respectively, V'_g is the voltage across gate-source capacitor, while I_d , I_g , and I_s are the drain, gate and source currents, respectively. These variables are time-dependant and function of the position x along the device width. Also, M_{ds} , M_{gd} , and M_{gs} represent the mutual inductances between drain-source, gate-drain and gate-source, respectively; In the above system, we have an extra unknown parameter, i.e., the gate-source capacitance voltage V'_g . Therefore, the following equation should be included to complete the system of equations

$$V'_g(x,t) + V_s(x,t) + R_i C_{gs} \frac{\partial V'_g(x,t)}{\partial t} - V_g(x,t) = 0 \quad (7)$$

which can be then reformatted into two matrix equations

$$\frac{\partial}{\partial x} \begin{pmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{pmatrix} + \frac{\partial}{\partial t} \begin{pmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{pmatrix} \begin{pmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{pmatrix} + \begin{pmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{pmatrix} \begin{pmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{pmatrix} = 0 \quad (8)$$

$$\frac{\partial}{\partial x} \begin{pmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{pmatrix} + \frac{\partial}{\partial t} \begin{pmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{pmatrix} \begin{pmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{pmatrix} + \begin{pmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{pmatrix} \begin{pmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{pmatrix} = 0 \quad (9)$$

3. Noise modeling of high-frequency FETs

The transmission line structure, exciting by noise equivalent sources distributed on the conductors as a new noise model of the high-frequency FET is shown in Fig. 3.

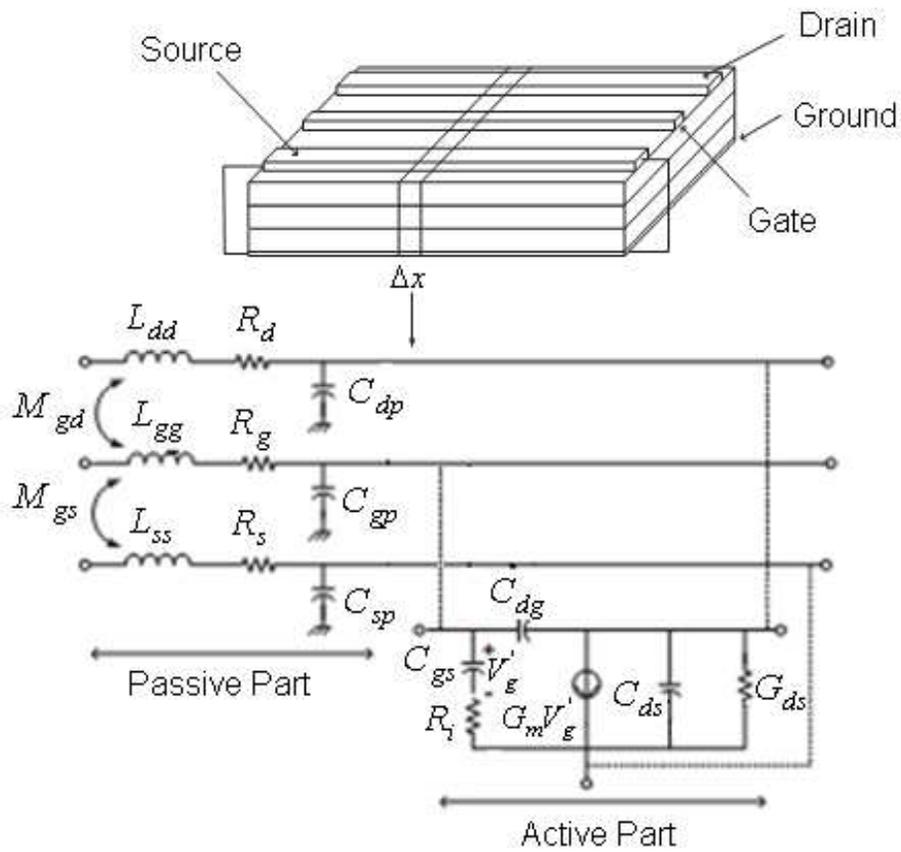


Figure 2. The different parts of a segment in the distributed model.

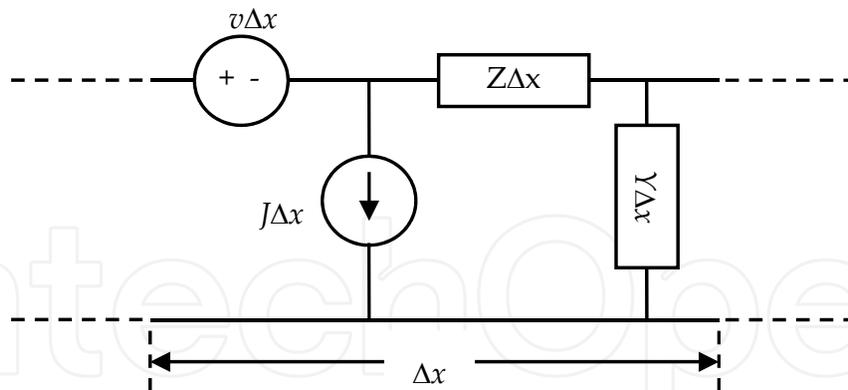


Figure 3. Differential subsection of an excited transmission line

Applying Kirchhoff's laws in time domain leads to

$$\begin{aligned} \frac{\partial}{\partial x} \mathbf{I}' + \mathbf{C} \frac{\partial}{\partial t} \mathbf{V}' + \mathbf{G} \mathbf{V}' + \mathbf{j}_n &= 0 & (a) \\ \frac{\partial}{\partial x} \mathbf{V} + \mathbf{L} \frac{\partial}{\partial t} \mathbf{I} + \mathbf{R} \mathbf{I} + \mathbf{v}_n &= 0 & (b) \end{aligned} \tag{10}$$

where

$$\begin{aligned}
\mathbf{I}(x,t) &= \begin{pmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{pmatrix} & \mathbf{V}'(x,t) &= \begin{pmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{pmatrix} & \mathbf{I}(x,t) &= \begin{pmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{pmatrix} & \mathbf{V}(x,t) &= \begin{pmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{pmatrix} \\
\mathbf{L} &= \begin{pmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{pmatrix} & \mathbf{R} &= \begin{pmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{pmatrix} \\
\mathbf{C} &= \begin{pmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{pmatrix} & \mathbf{G} &= \begin{pmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{pmatrix}
\end{aligned}$$

Note that vectors \mathbf{v}_n and \mathbf{j}_n are the linear density of exciting voltage and current noise sources, respectively. To evaluate the noise sources, we considered a noisy FET subsection with gate width Δx , as shown in Fig. 4. Thus, the unit-per-length noise correlation matrix for chain representation of the transistor (\mathbf{CA}_{UPL}) can be deduced as

$$\mathbf{CA}_{\text{UPL}} = \left\langle \begin{pmatrix} \mathbf{v}_n \\ \mathbf{j}_n \end{pmatrix} \begin{pmatrix} \mathbf{v}_n \\ \mathbf{j}_n \end{pmatrix}^+ \right\rangle = \begin{pmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{pmatrix} \quad (11)$$

Where $\langle \rangle$ denotes the ensemble average and $+$ the transposed complex conjugate. According to the correlation matrix definition, we can calculate \mathbf{v}_n and \mathbf{j}_n knowing (\mathbf{CA}_{UPL}), to completely describe the proposed FET noise model. Indeed, by solving (11), the noise parameters of the transistor can be obtained.

4. The FDTD formulation

The FDTD technique was used to solve the above equations. Applications of the FDTD method to the full-wave solution of Maxwell's equations have shown that accuracy and stability of the solution can be achieved if the electric and magnetic field solution points are chosen to alternate in space and be separated by one-half the position discretization, e.g., $\Delta x/2$, and to also be interlaced in time and separated by $\Delta t/2$ [13]. To incorporate these constraints into the FDTD solution of the transmission-line equations, we divided each line into Nx sections of length Δx , as shown in Fig. 5. Similarly, we divided the total solution time into segments of length Δt . In order to insure the stability of the discretization process and to insure second-order accuracy, we interlaced the $Nx + 1$ voltage points, $V_1, V_2 \dots V_{Nx+1}$ and the Nx current points, $I_1, I_2 \dots I_{Nx}$. Each voltage and adjacent current solution points were

separated by $\Delta x/2$. In addition, the time points are also interlaced, and each voltage time point and adjacent current time point were separated by $\Delta t/2$. Then, (10) can lead to

$$\frac{d I_k^{n+1/2} - d I_{k-1}^{n+1/2}}{\Delta x} + C_{11} \frac{d V_k^{n+1} - d V_k^n}{\Delta t} - C_{12} \frac{g V_k^{n+1} - g V_k^n}{\Delta t} - C_{13} \frac{s V_k^{n+1} - s V_k^n}{\Delta t} + G_m \frac{g V_k^{n+1} + g V_k^n}{2} + G_{ds} \frac{(d V_k^{n+1} + d V_k^n - s V_k^{n+1} - s V_k^n)}{2} + \sum_{m=1}^{N_{x+1}} \frac{n_1 v_m^{n+3/2} + n_1 v_m^{n+1/2}}{2} = 0 \tag{12}$$

$$\frac{g I_k^{n+1/2} - g I_{k-1}^{n+1/2}}{\Delta x} + C_{22} \frac{g V_k^{n+1} - g V_k^n}{\Delta t} - C_{12} \frac{d V_k^{n+1} - d V_k^n}{\Delta t} + C_{gs} \frac{g V_k^{n+1} - g V_k^n}{\Delta t} + \sum_{m=1}^{N_{x+1}} \frac{n_2 v_m^{n+3/2} + n_2 v_m^{n+1/2}}{2} = 0 \tag{13}$$

$$\frac{s I_k^{n+1/2} - s I_{k-1}^{n+1/2}}{\Delta x} + C_{33} \frac{s V_k^{n+1} - s V_k^n}{\Delta t} - C_{13} \frac{d V_k^{n+1} - d V_k^n}{\Delta t} - G_m \frac{g V_k^{n+1} + g V_k^n}{2} - G_{ds} \frac{(d V_k^{n+1} + d V_k^n - s V_k^{n+1} - s V_k^n)}{2} + \sum_{m=1}^{N_{x+1}} \frac{n_3 v_m^{n+3/2} + n_3 v_m^{n+1/2}}{2} = 0 \tag{14}$$

$$\frac{d V_{k-1}^{n+1} - d V_k^{n+1}}{\Delta x} + R_d \frac{d I_k^{n+3/2} + d I_k^{n+1/2}}{2} + L_{dd} \frac{d I_k^{n+3/2} - d I_k^{n+1/2}}{\Delta t} + M_{gd} \frac{g I_k^{n+3/2} - g I_k^{n+1/2}}{\Delta t} + M_{gs} \frac{s I_k^{n+3/2} - s I_k^{n+1/2}}{\Delta t} + \sum_{m=1}^{N_{x+1}} \frac{n_1 j_m^{n+1} + n_1 j_m^n}{2} = 0 \tag{15}$$

$$\frac{g V_{k-1}^{n+1} - g V_k^{n+1}}{\Delta x} + R_g \frac{g I_k^{n+3/2} + g I_k^{n+1/2}}{2} + L_{gg} \frac{g I_k^{n+3/2} - g I_k^{n+1/2}}{\Delta t} + M_{gd} \frac{d I_k^{n+3/2} - d I_k^{n+1/2}}{\Delta t} + M_{gs} \frac{s I_k^{n+3/2} - s I_k^{n+1/2}}{\Delta t} + \sum_{m=1}^{N_{x+1}} \frac{n_2 j_m^{n+1} + n_2 j_m^n}{2} = 0 \tag{16}$$

$$\frac{s V_{k-1}^{n+1} - s V_k^{n+1}}{\Delta x} + R_s \frac{s I_k^{n+3/2} + s I_k^{n+1/2}}{2} + L_{ss} \frac{s I_k^{n+3/2} - s I_k^{n+1/2}}{\Delta t} + M_{ds} \frac{d I_k^{n+3/2} - d I_k^{n+1/2}}{\Delta t} + M_{gs} \frac{g I_k^{n+3/2} - g I_k^{n+1/2}}{\Delta t} + \sum_{m=1}^{N_{x+1}} \frac{n_3 j_m^{n+1} + n_3 j_m^n}{2} = 0 \tag{17}$$

Applying the finite difference approximation to (7) gives

$$R_i C_{gs} \frac{(g V_k^{n+1})' - (g V_k^n)'}{\Delta t} + \frac{(g V_k^{n+1})' - (g V_k^n)'}{2} + \frac{s V_k^{n+1} + s V_k^n}{2} = \frac{g V_k^{n+1} + g V_k^n}{2} \tag{18}$$

with

$${}_dV_i^j = {}_dV((i-1)\Delta x, j\Delta t) \quad \text{and} \quad {}_dI_i^j = {}_dI((i-1/2)\Delta x, j\Delta t) \quad \text{for the drain electrode} \quad (\text{a})$$

$${}_gV_i^j = {}_gV((i-1)\Delta x, j\Delta t) \quad \text{and} \quad {}_gI_i^j = {}_gI((i-1/2)\Delta x, j\Delta t) \quad \text{for the gate electrode} \quad (\text{b}) \quad (19)$$

$${}_sV_i^j = {}_sV((i-1)\Delta x, j\Delta t) \quad \text{and} \quad {}_sI_i^j = {}_sI((i-1/2)\Delta x, j\Delta t) \quad \text{for the source electrode} \quad (\text{c})$$

and where k , m and n are integers. Solving these equations give the required recursion relations

$$V_k^{m+1} = \left(\frac{C}{\Delta t} + \frac{G}{2} \right)^{-1} \left\{ \left(\frac{C}{\Delta t} - \frac{G}{2} \right) V_k^m - \frac{I_k^{m+1/2} - I_{k-1}^{m+1/2}}{\Delta x} + \frac{\Delta x}{2} \sum_{m=1}^{N_{x+1}} (j_m^{n+1} + j_m^n) \right\} \quad (20)$$

$$I_k^{n+3/2} = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) I_k^{n+1/2} - \frac{V_{k+1}^{n+1} - V_k^{n+1}}{\Delta x} + \frac{\Delta x}{2} \sum_m (v_m^{n+3/2} + v_m^{n+1/2}) \right\} \quad (21)$$

Superposing all the distributed noise sources is equivalent to a summation in (20) and (21) over the gate width for $m = 1 \dots N_{x+1}$. Because of its simplicity, the leap-frog method was used to solve the above equations. First the voltages along the line were solved for a fixed time using (20) then the currents were determined using (21). The solution starts with an initially relaxed line having zero voltage and current [13].

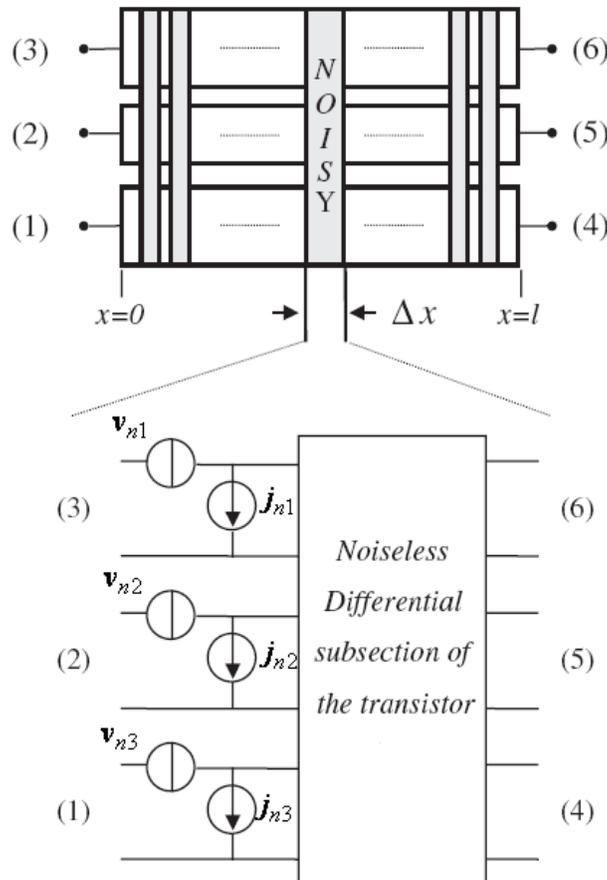


Figure 4. Noise-equivalent voltage and current sources

5. Noise correlation matrix of transistor

To find the noise correlation matrix for admittance representation of the transistor as a noisy six-port active network (as in Fig. 2), the values of port currents should be determined when they are all assumed short-circuited simultaneously. Equation (20) for $k = 0$ and $k = Nx + 1$ becomes

$$V_1^{m+1} = \left(\frac{C}{\Delta t} + \frac{G}{2} \right)^{-1} \left\{ \left(\frac{C}{\Delta t} - \frac{G}{2} \right) V_1^m - \frac{I_1^{n+1/2} - I_0^{m+1/2}}{\Delta x / 2} + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} (j_m^{n+1} + j_m^n) \right\} \quad (22)$$

$$V_{Nx+1}^{m+1} = \left(\frac{C}{\Delta t} + \frac{G}{2} \right)^{-1} \left\{ \left(\frac{C}{\Delta t} - \frac{G}{2} \right) V_{Nx+1}^m - \frac{I_{Nx+1}^{m+1/2} - I_{Nx}^{n+1/2}}{\Delta x / 2} + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} (j_m^{n+1} + j_m^n) \right\} \quad (23)$$

By considering Fig. 3, this equation requires that we replace Δx with $\Delta x/2$ only for $k = 1$ and $k = Nx+1$.

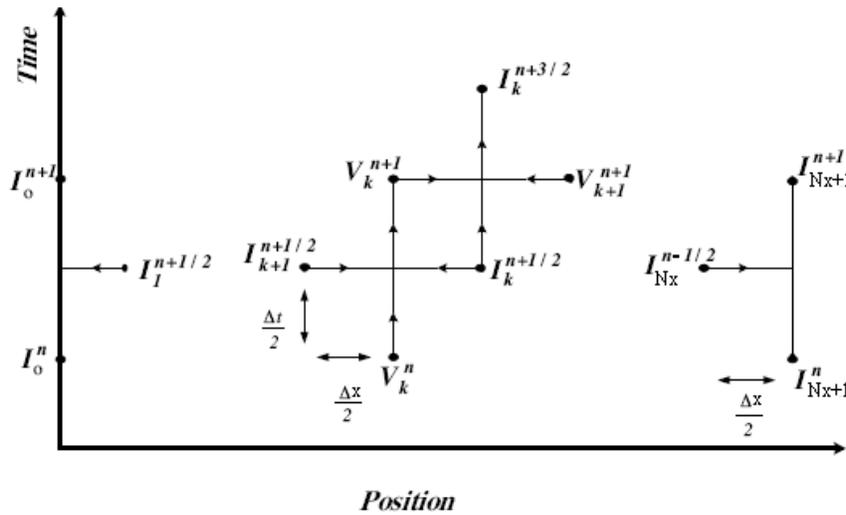


Figure 5. Relation between the spatial and temporal discretization to achieve second-order accuracy in the discretization of the derivatives.

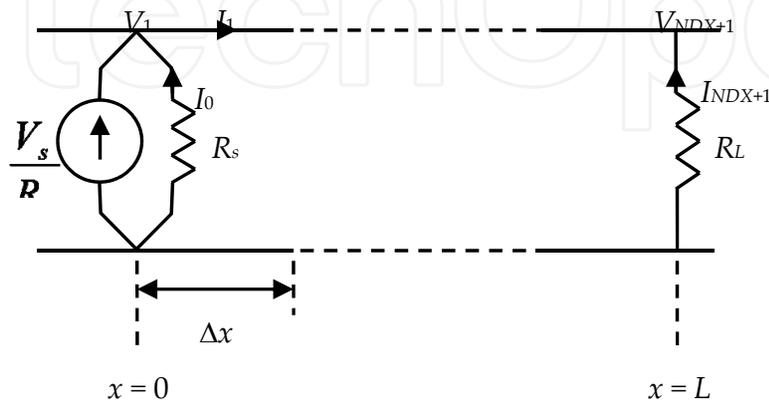


Figure 6. Voltage and current solution points. Spatial discretization of the line showing location of the interlaced points

In order to determine the transistor noise parameters, we set the input voltage source as zero ($V_s = 0$) [8]- [9]. Referring Fig. 6 we denoted the currents at the source point ($x = 0$) as I_0 and at the load point ($x = L$) as I_{Nx+1} . By substituting this notation into (22) we obtain

$$\begin{pmatrix} I_{0d} \\ I_{0g} \\ I_{0s} \end{pmatrix} = \begin{pmatrix} \frac{V_{1d}^n - V_{1d}^{n+1}}{2R_{sd}} & 0 & 0 \\ 0 & \frac{V_{1g}^n - V_{1g}^{n+1}}{2R_{sg}} & 0 \\ 0 & 0 & \frac{V_{1s}^n - V_{1s}^{n+1}}{2R_{ss}} \end{pmatrix} \quad (24)$$

Similarly, we imposed the terminal constraint at $x = L$ by substituting I_{Nx+1} into (23) as follow:

$$\begin{pmatrix} I_{Nx+1,d} \\ I_{Nx+1,g} \\ I_{Nx+1,s} \end{pmatrix} = \begin{pmatrix} \frac{V_{Nx+1,d}^n - V_{Nx+1,d}^{n+1}}{2R_{Ld}} & 0 & 0 \\ 0 & \frac{V_{Nx+1,g}^n - V_{Nx+1,g}^{n+1}}{2R_{Lg}} & 0 \\ 0 & 0 & \frac{V_{Nx+1,s}^n - V_{Nx+1,s}^{n+1}}{2R_{Ls}} \end{pmatrix} \quad (25)$$

To determine the currents I_1 and I_{Nx} at short-circuited ports ($x=0$ and $x=L$), we set $V_1 = V_{Nx+1} = 0$. The finite difference approximation of (21) for $k = 1$ and $k = Nx$ can be then written as (26) and (27), respectively.

$$I_1^{n+3/2} = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) I_1^{n+1/2} - \frac{V_2^{n+1}}{\Delta x} + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} \left(v_m^{n+3/2} + v_m^{n+1/2} \right) \right\} \quad (26)$$

$$I_{Nx}^{n+3/2} = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) I_{Nx}^{n+1/2} - \frac{V_{Nx}^{n+1}}{\Delta x} + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} \left(v_m^{n+3/2} + v_m^{n+1/2} \right) \right\} \quad (27)$$

Replacing $I_1^{n+1/2}$ and $I_{Nx}^{n+1/2}$ into (26) and (27), respectively, leads to short-circuit currents at input and output terminals.

$$I_1^{n+3/2} = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) \left(\frac{\Delta x}{2} \right)^2 \sum_{m=1}^{Nx+1} \left(j_m^{n+1} + j_m^n \right) + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} \left(v_m^{n+3/2} + v_m^{n+1/2} \right) - \frac{V_2^{n+1}}{\Delta x} \right\} \quad (28)$$

$$I_{Nx}^{n+3/2} = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) \left(\frac{\Delta x}{2} \right)^2 \sum_{m=1}^{Nx+1} \left(j_m^{n+1} + j_m^n \right) + \frac{\Delta x}{2} \sum_{m=1}^{Nx+1} \left(v_m^{n+3/2} + v_m^{n+1/2} \right) - \frac{V_{Nx}^{n+1}}{\Delta x} \right\} \quad (29)$$

Finally, the currents of the short-circuited ports can be determined as

$$\begin{bmatrix} I_1^{n+1/2} \\ I_{Nx}^{n+3/2} \end{bmatrix} \cong \begin{bmatrix} A & B \\ A & B \end{bmatrix} \begin{bmatrix} \sum_{m=1}^{Nx+1} (j_m^{n+1} + j_m^n) \\ \sum_{m=1}^{Nx+1} (v_m^{n+3/2} + v_m^{n+1/2}) \end{bmatrix} = K \begin{bmatrix} \sum_{m=1}^{Nx+1} (j_m^{n+1} + j_m^n) \\ \sum_{m=1}^{Nx+1} (v_m^{n+3/2} + v_m^{n+1/2}) \end{bmatrix} \quad (30)$$

with

$$A = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left\{ \left(\frac{L}{\Delta t} - \frac{R}{2} \right) \left(\frac{\Delta x}{2} \right)^2 \right\} \quad B = \left(\frac{L}{\Delta t} + \frac{R}{2} \right)^{-1} \left(\frac{\Delta x}{2} \right)$$

The admittance noise correlation matrix of the six-port FET noise model is then equal to

$$CY_{tr} = \left\langle \begin{bmatrix} I_1^{n+1/2} \\ I_1^{n+3/2} \end{bmatrix} \begin{bmatrix} I_1^{n+1/2} \\ I_1^{n+3/2} \end{bmatrix}^+ \right\rangle = \left\langle \left(K \begin{bmatrix} \sum j_n \\ \sum v_n \end{bmatrix} \right) \left(K \begin{bmatrix} \sum j_n \\ \sum v_n \end{bmatrix} \right)^+ \right\rangle = K \times CA_{UPL} \times K^+ \quad (31)$$

6. CAD algorithms for noise analysis of mm-wave FETs

6.1. Multi-port network connection

In Fig. 7, a noisy multiport sub-network S of scattering matrix [S] is embedded in a noisy sub-network T of scattering matrix [T], with respective noise wave correlation matrices noted [Cs] and [Ci]. Let [S_{net}] and [C_{net}] be the scattering and noise wave correlation matrices of the total network called N. The scattering matrix [T] of the embedding network T can be partitioned into sub-matrices that satisfy

$$\begin{bmatrix} b_e \\ b_i \end{bmatrix} = \begin{bmatrix} [T_{ee}] & [T_{ei}] \\ [T_{ie}] & [T_{ii}] \end{bmatrix} \begin{bmatrix} a_e \\ a_i \end{bmatrix} + \begin{bmatrix} c_e \\ c_i \end{bmatrix} \quad (32)$$

where subscript *i* designates the internal waves at the connections between the two-networks S and T while subscript *e* designates the external waves at the S_{net} terminals. The noise wave correlation matrix of network T is similarly partitioned such that

$$[C_t] = \begin{bmatrix} \overline{c_e c_e^*} & \overline{c_e c_i^*} \\ \overline{c_i c_e^*} & \overline{c_i c_i^*} \end{bmatrix} \quad (33)$$

The resulting noise wave correlation matrix is then given by [12]:

$$[C_{net}] = \left[[I] \mid T_{ei} : ([\Gamma] - T_{ii})^{-1} \right] [C_s] \left[[I] \mid T_{ei} : ([\Gamma] - T_{ii})^{-1} \right]^+ \quad (34)$$

where [I] is the identity matrix and [Γ] the connection matrix expressed as

$$[b_i] = [\Gamma][a_i] \quad (35)$$

The scattering matrix of the total network N is then given by the well known expression [11]

$$[S_{net}] = [T_{ee}] + [T_{ei}]([\Gamma] - [T_{ii}])^{-1}[T_{ie}] \quad (36)$$

Note that this result gives a complete noise characterization of the network. A direct calculation of the new scattering matrix is now possible using (36). Note that the order of the matrix to be inverted was reduced by an amount equals to the number of the external ports.

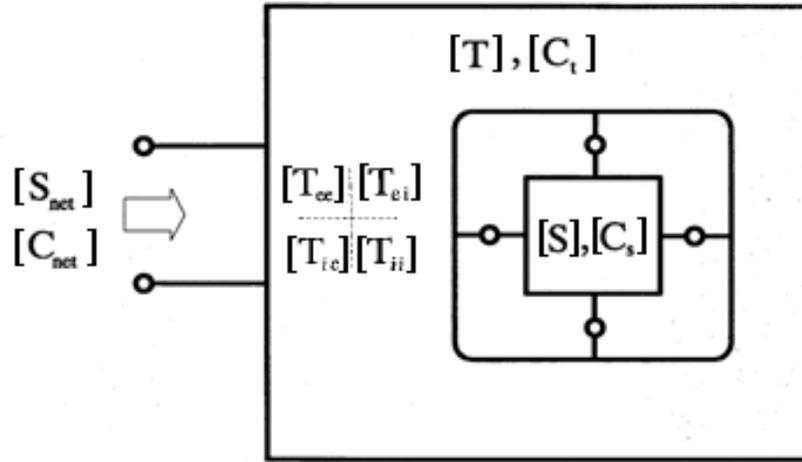


Figure 7. A multiport sub-network S is embedded into a sub-network T. The resulted network N is characterized by the scattering and correlation matrices $[S_{net}]$ and $[C_{net}]$, respectively.

6.2. Scattering and correlation noise matrices

According to the algorithm described above, let us consider the network shown in Fig. 8. In this figure, the ports of the transistor model are numbered from 1 to 24. Ports 23 and 24 are external ports while the rest are internal ports. Since most of the FETs are symmetrical, we can split their geometry into two identical parts. Figure 5 can be then decomposed into two equal parts of $w/2$ each (where w is the gate width) of respective scattering matrix $[S^{(1)}]$ and $[S^{(2)}]$. Ports 13, 14 and 15 (the drain, the gate and the source) are terminated by the respective impedances Z_d , Z_g , and Z_s , whose reflection coefficients can be expressed as

$$S^{(3)} = \frac{Z_d - 1}{Z_d + 1} \quad (37)$$

$$S^{(4)} = \frac{Z_g - 1}{Z_g + 1} \quad (38)$$

$$S^{(5)} = \frac{Z_s - 1}{Z_s + 1} = -1 \quad (39)$$

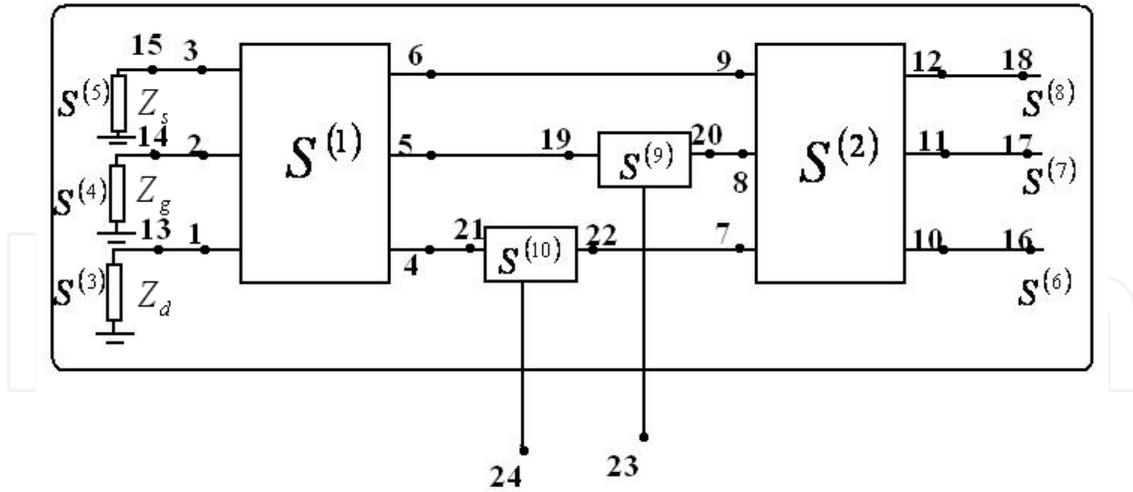


Figure 8. Circuit model of the half structure of a FET with specific internal and external ports

Let us now consider open circuit ports at $x = w/2$. We have then,

$$S^{(6)} = S^{(7)} = S^{(8)} = 1 \tag{40}$$

The only remaining components in Fig. 8 are the 3-port elements $S^{(9)}$ and $S^{(10)}$. Referring to that figure, we can observe that these components basically form the gate line and the drain line, respectively, in the transmission line model. Based on [12], their scattering matrix can be written as

$$[S^{(9)}] = [S^{(10)}] = [S_{con}] = \frac{1}{3} \begin{bmatrix} -1 & 2 & 2 \\ 2 & -1 & 2 \\ 2 & 2 & -1 \end{bmatrix} \tag{41}$$

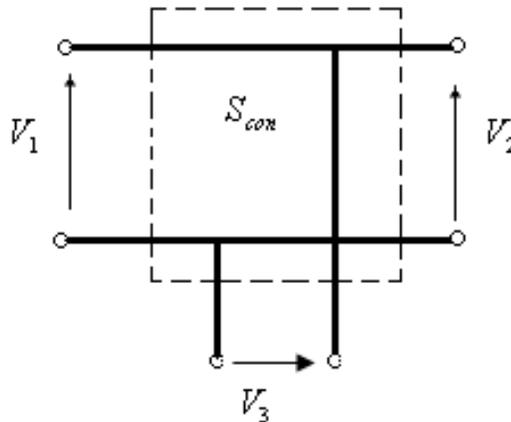


Figure 9. Connection of the series network

In order to define $[C_s]$, we need to know the noise correlation matrices in the form of scattering matrices for all circuit elements. The correlation noise matrix for the 6-port network representing half of the transistor gate width, i.e., $w/2$, can be computed using the

techniques described in [9] and [10]. As a result, we can use the proposed CAD algorithm to obtain the scattering and noise correlation matrices of the half-circuit structure.

The scattering matrix of a device is usually computed by partitioning its ports into two groups namely, external and internal ports. Thus, by separating the incoming and outgoing waves in (34), the computation of the connection matrix leads to the resulting scattering matrix

$$[S] = \begin{bmatrix}
 \begin{matrix} 23 \\ [s_{33}^{(9)}] \end{matrix} & \begin{matrix} 24 \\ 0 \end{matrix} & \begin{matrix} 1-6 \\ 0 \end{matrix} & \begin{matrix} 7-12 \\ 0 \end{matrix} & \begin{matrix} 13 \\ 0 \end{matrix} & \begin{matrix} 14 \\ 0 \end{matrix} & \begin{matrix} 15 \\ 0 \end{matrix} & \begin{matrix} 16 \\ 0 \end{matrix} & \begin{matrix} 17 \\ 0 \end{matrix} & \begin{matrix} 18 \\ 0 \end{matrix} & \begin{matrix} 19 \\ [s_{31}^{(9)}] \end{matrix} & \begin{matrix} 20 \\ [s_{32}^{(9)}] \end{matrix} & \begin{matrix} 21 \\ 0 \end{matrix} & \begin{matrix} 22 \\ 0 \end{matrix} \\
 \begin{matrix} [0_{6 \times 6}] \\ [s_{33}^{(10)}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [s_{33}^{(10)}] \end{matrix} \\
 \begin{matrix} [0_{6 \times 6}] \\ 0 \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ 0 \end{matrix} & \begin{matrix} [S^{(1)}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [S^{(2)}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} & \begin{matrix} [0_{6 \times 6}] \\ [0_{6 \times 6}] \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(3)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(4)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(5)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(6)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(7)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [S^{(8)}] \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} [s_{13}^{(9)}] \\ [s_{23}^{(9)}] \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [s_{11}^{(9)}] \\ [s_{21}^{(9)}] \end{matrix} & \begin{matrix} [s_{12}^{(9)}] \\ [s_{22}^{(9)}] \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [s_{13}^{(10)}] \\ [s_{13}^{(10)}] \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [s_{11}^{(10)}] \\ [s_{12}^{(10)}] \end{matrix} & \begin{matrix} [s_{12}^{(10)}] \\ [s_{22}^{(10)}] \end{matrix} \\
 \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [s_{13}^{(10)}] \\ [s_{13}^{(10)}] \end{matrix} & \begin{matrix} 0 \\ 0 \end{matrix} & \begin{matrix} [s_{11}^{(10)}] \\ [s_{12}^{(10)}] \end{matrix} & \begin{matrix} [s_{12}^{(10)}] \\ [s_{22}^{(10)}] \end{matrix}
 \end{bmatrix} \quad (42)$$

Then, $[C_s]$ can be written as

$$[C_s] = \begin{bmatrix}
 [0_{2 \times 2}] & [0_{2 \times 6}] & [0_{2 \times 6}] & [0_{2 \times 10}] \\
 [0_{6 \times 2}] & [C_s^{(1)}] & [0_{6 \times 6}] & [0_{6 \times 10}] \\
 [0_{6 \times 2}] & [0_{6 \times 6}] & [C_s^{(2)}] & [0_6^{(10)}] \\
 [0_{10 \times 2}] & [0_{10 \times 6}] & [0_{10 \times 6}] & [0_{10 \times 10}]
 \end{bmatrix} \quad (43)$$

Note that based on the proposed algorithm, a designer can easily obtain the scattering matrices of any microwave transistor, highlighting the ease of implementation of the proposed model into existing commercial simulators.

7. Numerical results

The proposed approach was used to model a sub micrometer-gate GaAs transistor (NE710) [14]. The device has a $0.3 \mu\text{m} \times 280 \mu\text{m}$ gate. The first step consisted to characterize the transistor. In this work, we used a bench from Focus microwave that consists on a probing station, the HP 8340B synthesized signal generator, the Agilent 8565EC spectrum analyzer,

the CMMT1808 tuners, the Anritsu ML2438A power meter, and the Agilent ML2438A power supplies (Fig. 10).

The intrinsic equivalent circuit model (Fig. 11) was obtained using well-known hot and cold modeling techniques [13]. After removing the extrinsic components via de-embedding methods, a hot modeling technique was utilized to obtain the intrinsic elements. Then, an optimization was performed by varying the values of the intrinsic FET elements in the vicinity of 10% of their mean value until the error between measured and modeled S-parameters was found acceptable (i.e., less than 2%). The obtained values of the extrinsic and intrinsic elements are summarized in Table 1.



Figure 10. Load-pull bench used to characterize the device

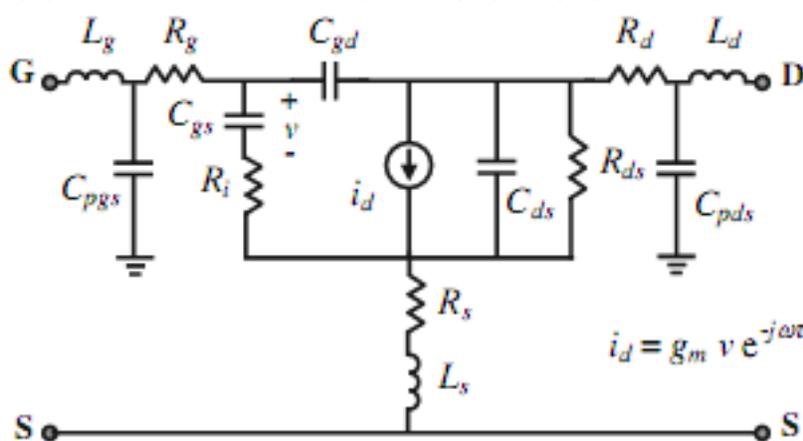


Figure 11. Small-signal equivalent circuit of a FET

Figure 12 shows a good fitting between measured and modeled data for various dc and pulsed voltages while Fig.13 shows the experimental load-pull characteristics of the transistor. When matched, it has an output power of 16 dBm with a 10% PAE at 10GHz. In Fig.10, the output RF power is shown as a function of the complex output impedance matching conditions of the device. The transistor S-parameters over a frequency range of 1-26GHz are plotted in Fig.14. As expected, compared to measurements, our proposed model is more accurate than the slice model [7], especially at the upper part of the frequency spectrum, when the device physical dimensions are comparable to the wavelength. This is due to the fact that our model is based on the full-wave equation while the slice model is based on an electrical equivalent circuit model. Figure 15 shows the noise figure obtained for three different frequencies. Thus, the proposed wave analysis can be applied for accurate noise analysis of FET circuits. To further prove the accuracy of the proposed wave approach in noise analysis, our results were successfully compared to measurements (Fig. 16).

For larger widths, the thermal noise of the gate increases due to the higher gate resistance while for smaller gate widths, the minimum noise figure increases as the capacitances do not scale proportionally with the gate width due to an offset in capacitance at gate width zero [2]. Therefore, we highlighted these effects of gate width on a transistor noise performance by simulating the minimum noise figure and the normalized equivalent noise admittance for three values of the gate width, e.g., 140, 280 and 560 μm (Fig. 17). These values were selected based on the device we modeled. In fact, the NE710 has a gate width of 280 μm , so we took half of that value as well as its double to bound the device behavior and highlight the effect of gate width on a FET performance.

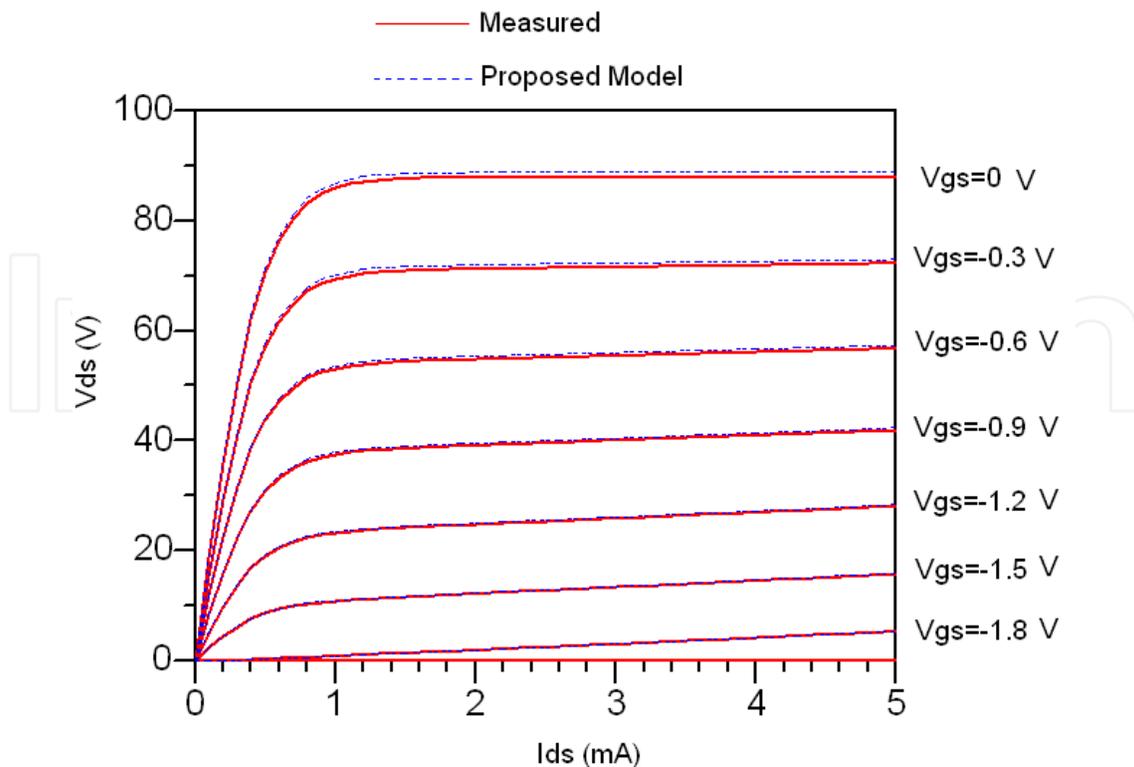


Figure 12. I-V curves for the NE710

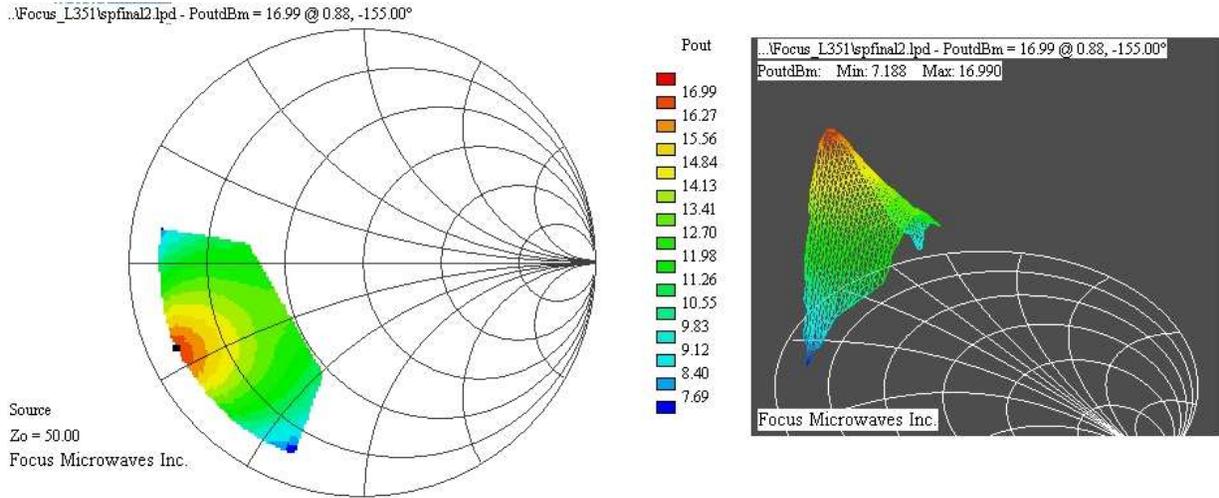


Figure 13. Output power as function of load impedance for an optimized structure at 10 GHz

Lumped Model Values	Numerical Values
L_g	0.383 nH
L_d	0.434 nH
L_s	0.094 nH
R_d	1.77 ohm
R_s	1.74 ohm
R_g	3.29 ohm
C_{pgs}	0.078 pF
C_{pds}	0.092 pF
C_{ds}	0.005 pF
C_{gd}	0.033 pF
g_m	41 mS
R_i	7.3 ohm
R_{ds}	231 ohm
C_{gs}	0.216 pF

Table 1. Values of the lumped elements (The transistor was biased at $V_{ds} = 3$ V and $I_{ds} = 10$ mA)

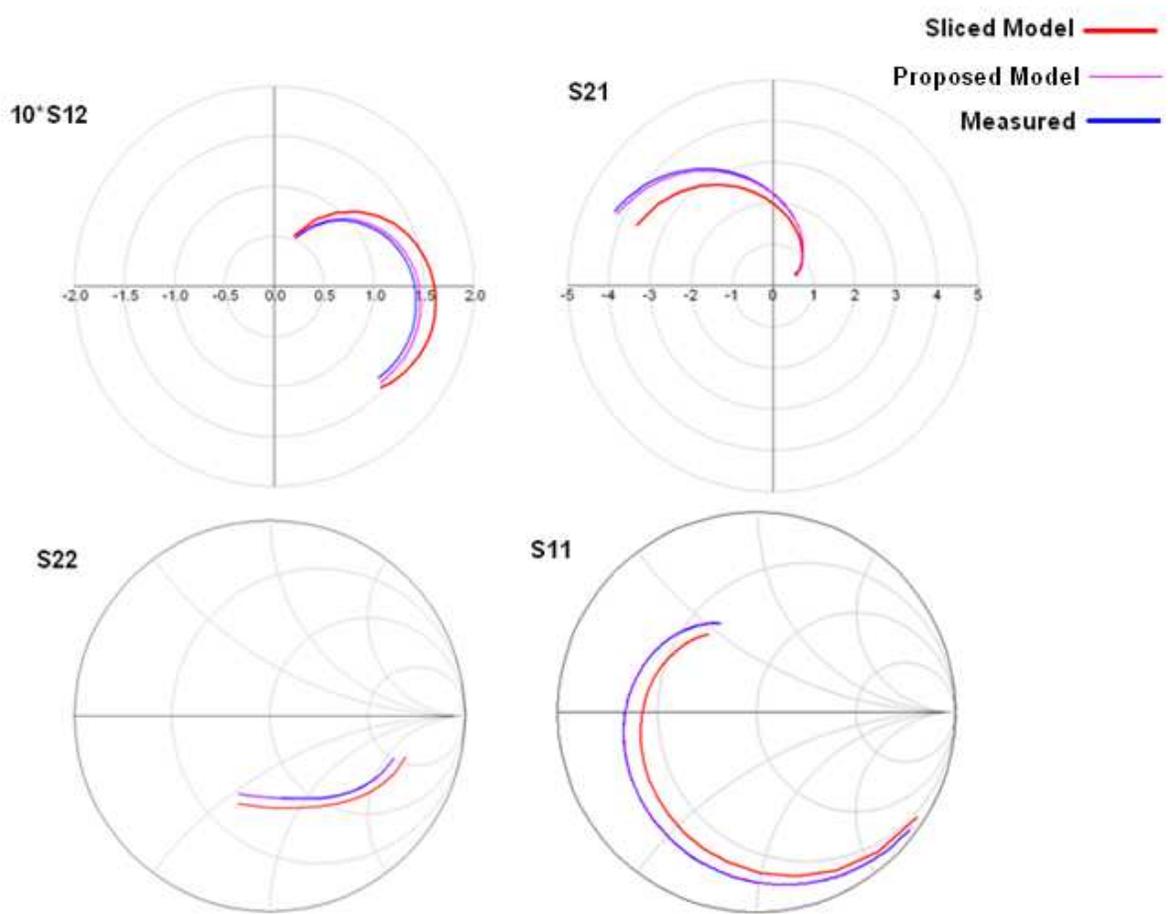


Figure 14. NE710: Comparison between the measured S-parameters and those generated by the sliced and the proposed model.

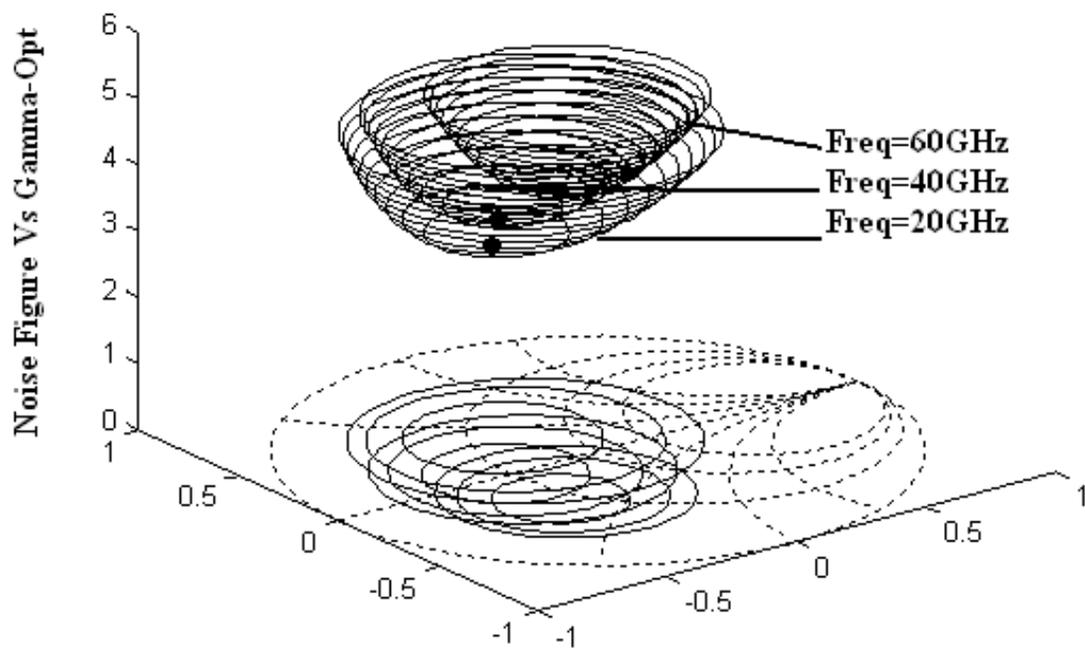
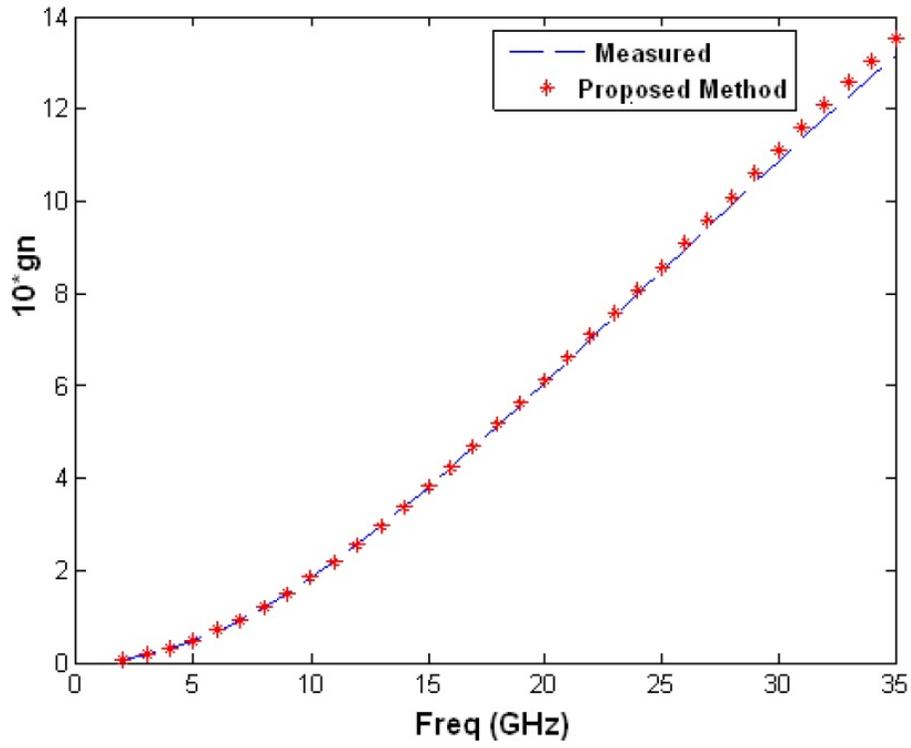
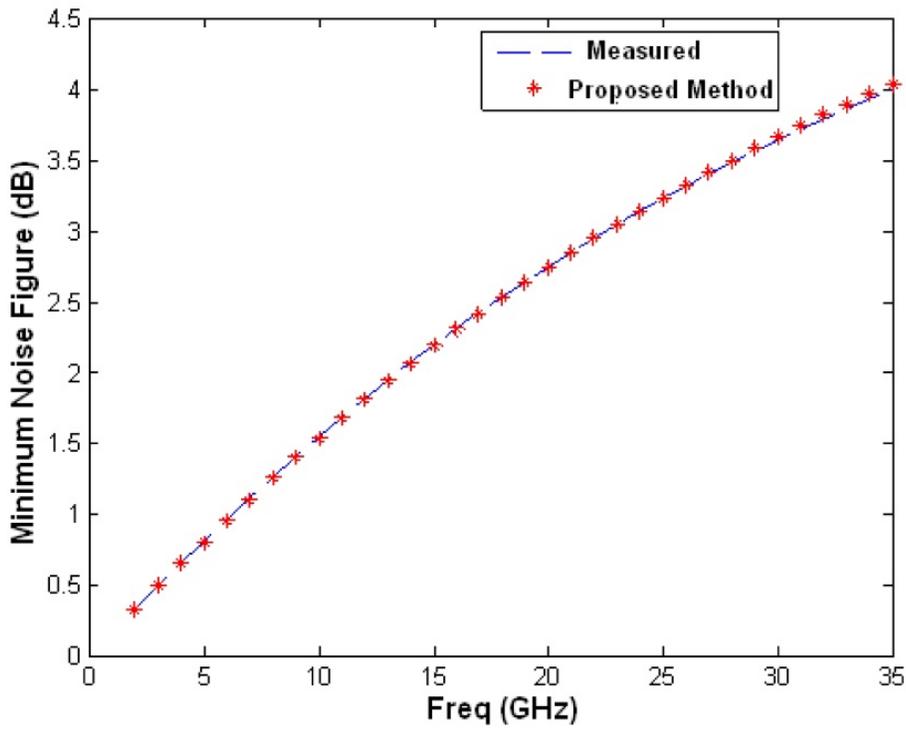


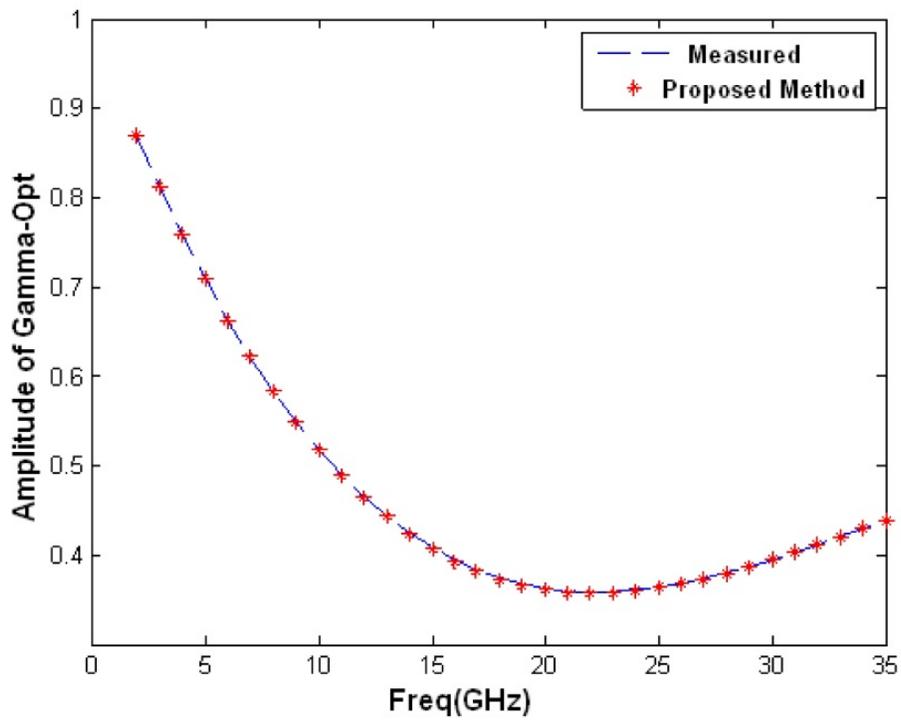
Figure 15. Noise figure circles for three different frequencies versus the source admittance



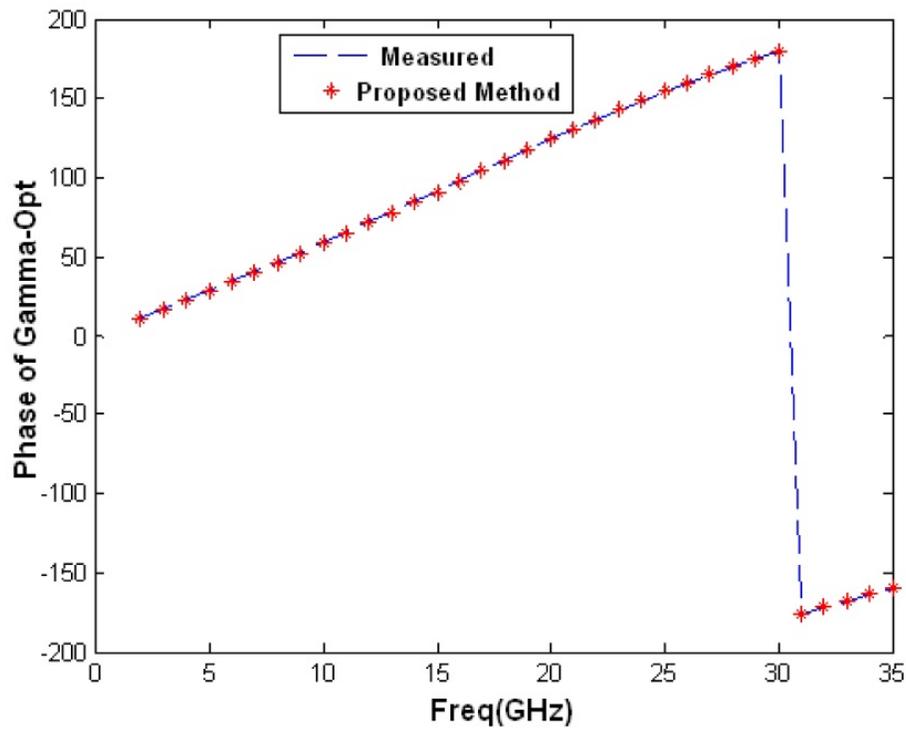
a



b



c



d

Figure 16. a. Normalized equivalent noise admittance and noise figure: Comparison between the proposed method and measurements; b. Amplitude and phase of the optimum reflection coefficient: Comparison between the proposed method and measurements

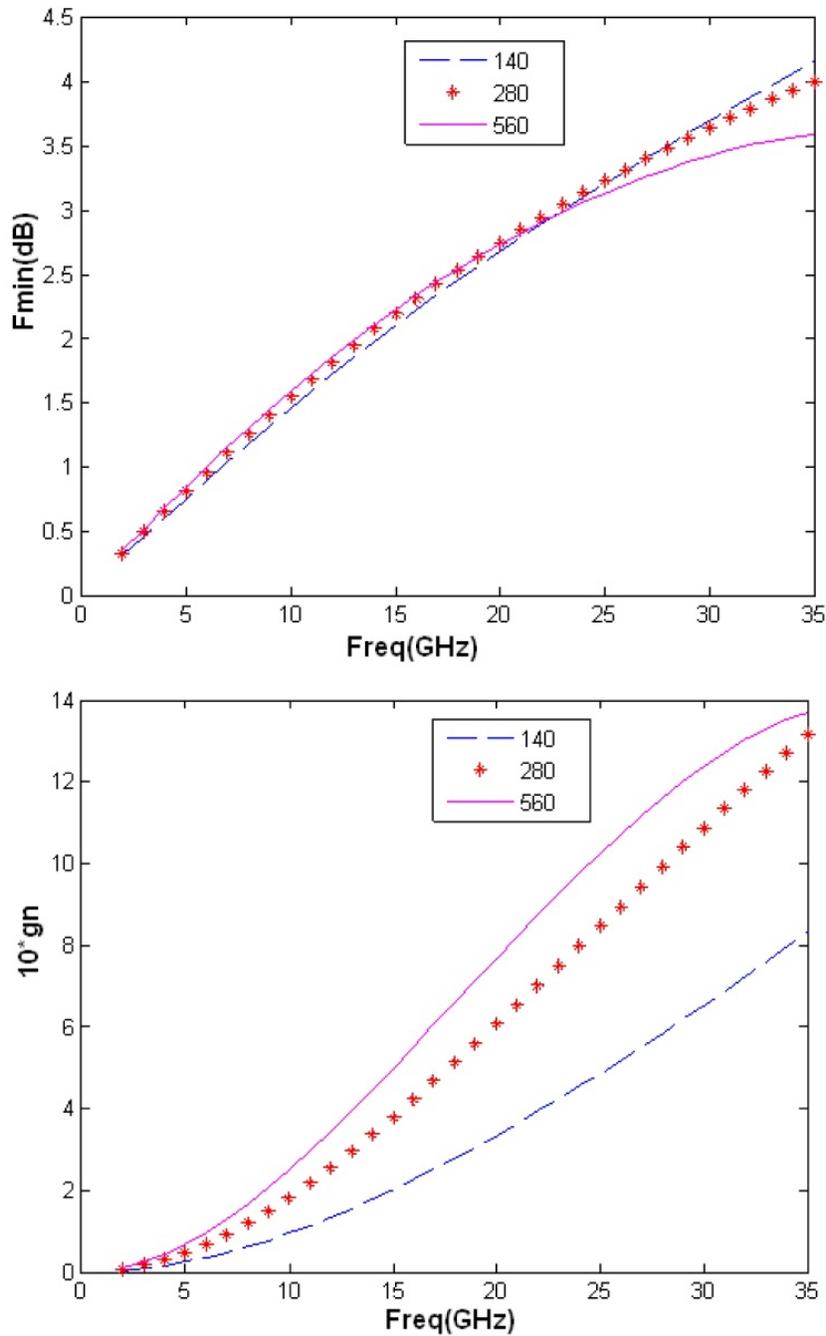


Figure 17. Minimum noise figure and normalized equivalent noise admittance of the transistor for three different values of gate width (μm)

8. Discussions

The transistor modeling approach presented in this chapter is mainly developed for computer-aided design implementation, making it suitable for any FET circuit topology up to the millimeter-wave range and thus, can be easily implemented and used in commercial software. As illustrated in Fig.18, the proposed model was implemented in ADS [15] and the results obtained from the code we developed have been successfully compared with those

obtained by the same model after being implemented in the ADS library and used as an internal device. This step shows that the proposed model can be used in any microwave integrated circuit design performed by a commercial simulator. It has also to be noted that even if the proposed model is suitable for any FET structure, large-gate width devices have been targeted in the present work. In fact, this specific type of transistors can handle high output power levels, making them suitable for power amplifier design.

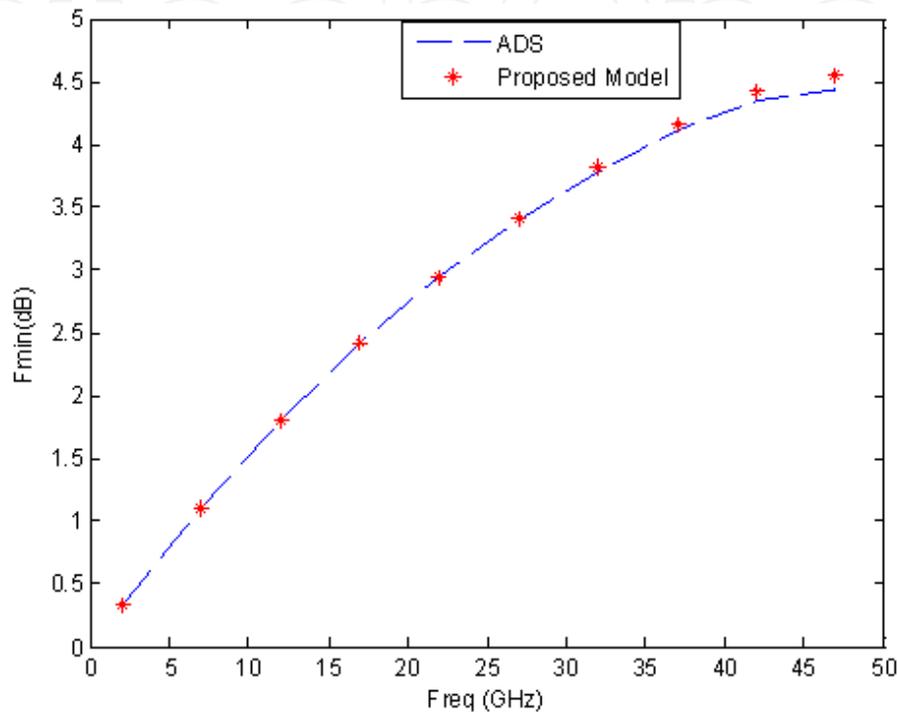


Figure 18. Comparison between simulated minimum noise figure obtained from our developed code and from ADS using our model

9. Conclusion

Using a new CAD algorithm, the noise modeling and analysis of microwave FET have efficiently been studied. In fact, since only half of a FET length is used, instead of the whole structure, the computation time will be significantly affected. Besides, the implementation of this CAD technique in modern microwave and mm-wave simulators is straightforward and will give more reliable results for circuit performance like low-noise amplifiers. Also, as for practical applications, large gate periphery devices are used to generate sufficient output power levels. With the increase of the device gate periphery, the self-heating effect and the defect trapping effect will both be more profound.

Author details

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10. References

- [1] Y.-F. Wu, M. Moore, T. Wisleder, P. Chavarkar, P. Parikh, "Noise Characteristics of Field-Plated HEMTs," *International Journal of High Speed Electronics and Systems*, vol. 14, pp. 192–194, 2004.
- [2] B. Boudjelida, A. Sobih, A. Bouloukou, S. Boulay, S. Arshad, J. Sly, M. Missous, "Modelling and simulation of low-frequency broadband LNA using InGaAs/InAlAs structures: A new approach," *Materials Science in Semiconductor Proc.*, Vol.11, pp.398-401, 2008.
- [3] A. Cidronali, G. Leuzzi, G. Manes and Franco Giannini, "Physical/Electromagnetic pHEMT modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 830-838, 2003.
- [4] W. Heinrich, "Distributed equivalent-circuit model for traveling-wave FET design," *IEEE Trans. Microwave Theory Tech*, Vol. 35, pp. 487–491, 1997.
- [5] W. Heinrich, "On the limits of FET modeling by lumped elements," *Electron. Lett.*, Vol. 22, no. 12, pp. 630–632, June 1986.
- [6] M. Movahhedi, A. Abdipour, "Efficient numerical methods for simulation of high-frequency active devices", *IEEE Trans. Microwave. Theory Tech.*, Vol. 54, pp. 2636–2645, 2006.
- [7] A. Abdipour, G. Moradi, "A CAD-oriented simultaneous signal and noise modeling and analysis of mm-wave FET structures," *AEU- Int. Journal of Electronics and Communications*, Vol. 58, pp. 65-71, 2004.
- [8] S. Gaoua, S. Asadi, M.C.E. Yagoub, F.A. Mohammadi, "CAD tools for efficient RF/microwave transistor modeling and circuit design," *Analog Integrated Circuits and Signal Processing J.*, Vol. 63, pp. 59-70, 2010.
- [9] M.C. Maya, A. Lazaro, L. Pradell, "Determination of FET noise parameters from 50 Ω noise-figure measurements using a distributed noise model", *Gallium Arsenide applications symposium. GAAS 2002*, September 2002, Milan.
- [10] R. Khosravi, A. Abdipour, "A new wave approach for signal and noise modeling of microwave/mm wave FET based on Green's function concept," *Int. J. Electronics*, Vol. 90, pp 303-312, 2003.
- [11] J.A. Dobrowolski, *Computer-aided Analysis, Modeling, and Design of Microwave Networks (Wave Approach)*, (Boston: Artech House, 1996).
- [12] J.A. Dobrowolski, *Introduction to Computer Methods for Microwave Circuit Analysis and Design* (Boston: Artech House, 1991).
- [13] W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, Vol. 37, pp. 385–388, 1989.
- [14] <http://www.nec.com>.
- [15] ADS. (2008). Agilent Technologies, Palo Alto, CA.