Chapter 10

Mechanical Characterization of Black Diamond (Low-k) Structures for 3D Integrated Circuit and Packaging Applications

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Additional information is available at the end of the chapter

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1. Introduction

As Integrated Circuit (IC) technology scales down into the nanotechnology regime, it allows millions of active components to be fabricated on a single chip in accordance with the historical trend of Moore's law. Integration of all these active elements on a single IC, multilevel on-chip interconnect system must be developed in BEOL (Back End of the Line) technology [1]. Accordingly, to meet the industry requirements of scaling for improved performance, semiconductor technologies are forced to move from well-established Al/SiO_2 interconnect technology to Cu/low-k (Copper/low dielectric constant) technology [2-3]. The main objective of this transition is to reduce cross talk noise between metal lines, propagation delays and power dissipation from RC delay. Copper and low-k inter metal dielectric layers are used as multilevel interconnects to enhance the speed of logic devices. Amongst the available low-k materials, Black diamond ™ (BD, low-k, SiOC:H) has been considered as potential inter metal dielectric material for integration in ULSI (Ultra Large Scale Integration) due to its better electrical and dielectric properties. But in dielectric material processing the key issue is the trade-off between dielectric property and mechanical strength. Hence it is very important to study the mechanical properties of BD films and Cu/BD stacks.

There are four interdependent properties which are responsible for the mechanical reliability of thin film structures and they are elastic modulus, hardness, fracture toughness and interfacial adhesion [4]. Both theoretical and experimental studies recommend that hardness and elastic modulus are the two key material characteristics affecting the CMP process [5]. Generally, mechanical properties of thin films differ from those of the bulk materials. This is mainly attributed to their microstructure, interfacial mismatch stresses and molecular restructuring of the films. Parameters used to characterize the mechanical

strength of BEOL interconnect materials include hardness, elastic modulus and adhesion/cohesion strength. Interfacial adhesion is the most important property to ensure the thermo-mechanical integrity of Cu/low-k stacks. Interfacial adhesive failure may occur during fabrication processes such as CMP and high temperature curing steps. In addition, delamination or cracking can also be observed during electronic packaging processes like reflow process, flip-chip bonding and back grinding due to thermo-mechanical stresses. This chapter further discusses on mechanical behavior of BD thin films of different thicknesses, single and dual dielectric stacks with Ta & TaN barriers. Nanoindentation experiments with continuous stiffness measurement (CSM) attachment have been performed on different BD film stacks to assess the multi-layer effect on the mechanical behavior of BD films. Effect of wafer backgrinding on the active side of the low-k structures have been studied using the Nanoindentation method as wafer backgrinding is one of the key technologies paving way to high performance three-dimensional (3D) microelectronic packages.

2. Low-K dielectric materials for BEOL (Back End of the Line) multilevel interconnect and 3D Integration applications

The contribution of the R-C delay by conventional multilevel interconnects scheme increases as the IC fabrication technology moving into further miniaturization. The introduction of Cu/low-k interconnect technology into BEOL, has progressively enhanced this condition when compared to the conventional Al/SiO_2 technology by reducing R-C delay in between interconnect lines. [6-7]. In addition to migrating to Cu/low-k multilevel interconnects at chip level, microelectronic industry is more focused on 3D IC integration and 3D packaging of chips at system level. In recent times, three-dimensional (3D) IC integration and packaging is gaining more attention because of its innovativeness, high performance, high functionality, and ability to reduce size of the final product. The major applications of the 3-D packaging include digital and mixed-signal electronics, wireless, electro-optical, MEMS and other integration technologies. At this juncture, the key technologies supporting the 3-D packaging, are as: through silicon vias (TSVs), wafer thinning or back grinding, precision alignment of wafer to wafer or chip to wafer, and wafer to wafer or chip to wafer bonding [8]. Among these key technologies, wafer thinning plays a vital role in the 3D packaging integration, as it allows to accommodate or stack more dies in one package and ultimately results in the reduction of package size. Besides the reduction of package size, the stacking of thin chips provides many other advantages, such as, more functionality per package and improved heat dissipation. Electronic packaging industry has to put a lot of R&D efforts and spend millions of dollars on the wafer thinning technologies as there is no manufacturing technology available for directly producing the ultra-thin wafers [9]. That is why in the past years, many wafer thinning methods, such as mechanical grinding, chemical mechanical polishing (CMP), wet etching and atmospheric downstream plasma (ADP), dry chemical etching (DCE) have been evolved. So far many researchers have extensively studied wafer thinning/back grinding processes in terms of die strength by assessing the quality of the grinded surface [10].

In the recent years, many researchers have extensively assessed the quality of back grinding process with the help of die strength evaluation. Die strength of the thinned wafer can be evaluated by using the different mechanical testing techniques such as three point bend test, four point bend test, ball on ring test, ball breaker tests and ring-on-ring tests. The mechanical tests are greatly influenced by several processes and material parameters such as surface roughness or finish, degree of thinning, stress relief process, quality of the dicing edge [11-15]. However the literature available related to the effect of grinding processes on the active side of the die/chip is limited, and this necessitates a focused study on the effect of wafer back grinding on the active side of chip. For the first time we have studied the effect of back grinding processes on the active side of low-k stack by using Nanoindentation method. Usually active side of the chip is a few microns in thickness, and it cannot be studied using those methods which are being used for conventional die strength evaluation. Therefore, we have chosen sophisticated method like nanoindentation technique for mechanical characterization of low-k films.

2.1. Different types of low-k materials

In the recent past, many low-k materials have been developed, and they can be broadly classified into Si-based and non-Si based. Si-based materials can be further classified into Si-based and silsesquioxane (SSQ) based, which include hydrogen-SSQ (HSSQ) and methyl-SSQ (MSSQ). Non-Si based low-k materials can be further divided into two groups, polymer based and amorphous carbon. Several types of low-k materials with varied low-k values and different deposition methods are being used in the IC fabrication technology. Table 1 lists the contemporary deposition techniques together with the k value of various silicon based, non-silicon based and polymer dielectric material candidates for the 0.13μm and 0.1μm technology nodes.

In silica based dielectric materials, usually tetrahedral silica is the elementary unit. Each silicon atom is at the center of the tetrahedron of oxygen atoms as shown in Fig. 1 (a). Typically Si based dielectric materials are dense structures with higher chemical and thermal stability. In silica based materials, dielectric constant (k) value can be lowered by replacing the Si-O bonds with Si-F bond, producing fluorinated silica glasses (FSG) or doping with C by introducing CH_3 groups [7].

Black diamond (BD) is one of the popular low-k materials and it is a trade mark of CVD processed dielectric material, introduced by Applied Materials Inc. [17]. It is silica based dielectric material, obtained by doping of silica with -CH_3 groups as shown in figure Fig. 1 (b) and it has chemical formula SiOC:H. It is also called hybrid dielectric material as it contains both organic (-CH_3) and inorganic (Si-O) constituents. The dielectric constant (k) value of silica based dielectrics ranges from 2.6 to 3. Typically BD thin films are fabricated by using the Chemical Vapor Deposition (CVD) method near room temperature using organosilane precursor in the presence of oxygen as oxidant. The lower density of the BD films is achieved by introducing network terminating species (-CH_3) into the Si-O matrix [19]. The density and dielectric value of the BD films can be altered by the selection of

terminating groups in silica network. Empirically, a larger terminating group gives lower density, because it acts as a network terminating group only and it is not part of the Si-O network. Therefore BD films retain many of the useful thermo-mechanical properties of silicon oxide. The summary of properties of BD films is given in Table 2. BD films can achieve bulk dielectric constant of around 2.5 to 2.7, and integrated ILD stack dielectric constant of <3 [20]. The glass transition temperature of the BD is well above 450°C. The dielectric constant of the BD films can be lowered mainly by introducing constitutive porosity into the microstructure [21]. By proper selection of the compatible barriers layers, thermal and mechanical properties of BD films provide evolutionary pathway to Cu/low-k interconnect technology.

Dielectric Materials	**Fabrication Technique**	**K value**
SiO_2	CVD	3.9 – 4.5
Fluorosilicate glass (FSG)	CVD	3.2 – 4.0
Polyimides	Spin-on	3.1 – 3.4
Hydrogen silsesquioxane(HSQ)	Spin-on	2.9 – 3.2
Diamond-like Carbon (DLC)	CVD	2.7 – 3.4
Black Diamond™ (SiCOH)	CVD	2.7 – 3.3
Parylene-N	CVD	2.7
B-staged Polymers (CYCLOTENE™ and SiLK™)	Spin-on	2.6 – 2.7
Fluorinated Polyimides	Spin-on	2.5 – 2.9
Methyl silsesquioxane (MSQ)	Spin-on	2.6 – 2.8
Poly(arylene ether) (PAE)	Spin-on	2.6 – 2.8
Fluorinated DLC	CVD	2.4 – 2.8
Parylene-F	CVD	2.4 – 2.5
PTFE	Spin-on	1.9
Aerogels/Xerogels (porous silica)	Spin-on	1.1 – 2.2
Porous HSQ	Spin-on	1.7 – 2.2
Porous SiLK	Spin-on	1.5 – 2.0
Porous MSQ	Spin-on	1.8 – 2.2
Porous PAE	Spin-on	1.8 – 2.2
Air Gaps	-	1.0

Table 1. Dielectric constants of various contemporary low-k materials are the interest of 0.13μm and 0.1μm technology nodes [7, 16-18].

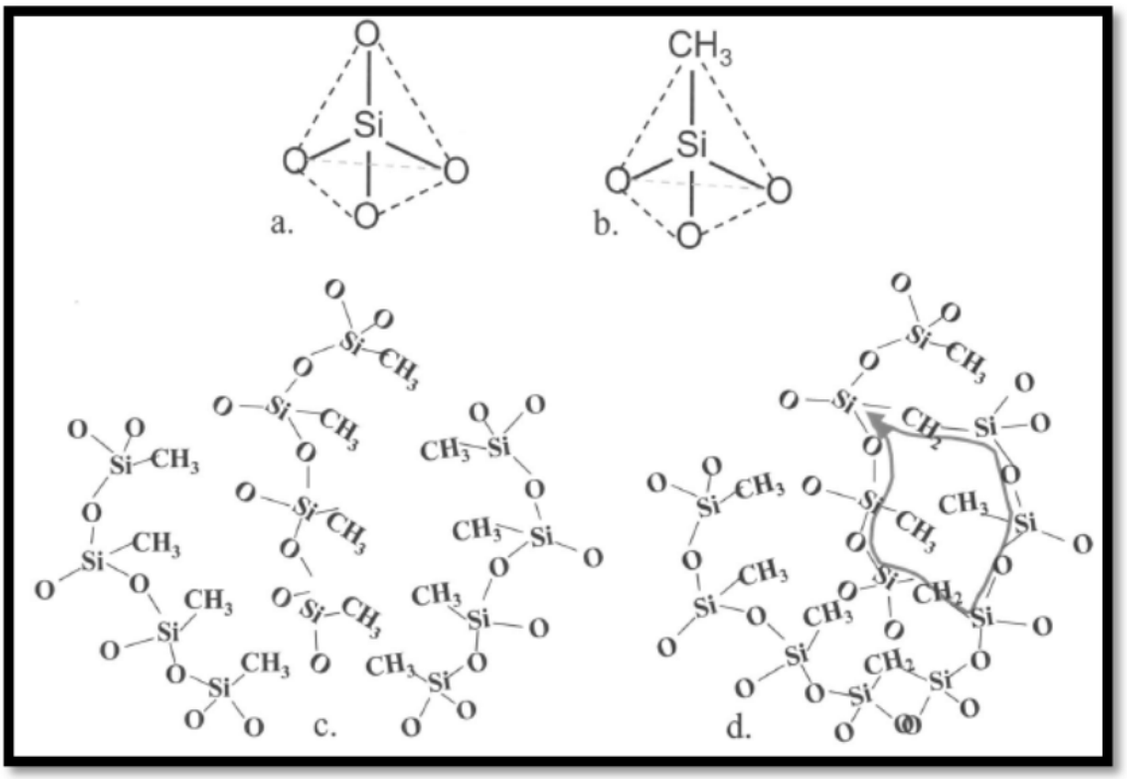

Figure 1. Elementary units of (a) SiO2 (b) carbon doped Silica, called as Black Diamond (SiOC:H) (c) C doped silica without cross linking (d) with cross linking [7]

Property	Value of the Blanket film
Dielectric Constant-Bulk film(Hg Probe)	2.5-2.7 @ 1 MHz
Uniformity (%, 1σ)	<1.5
Stress (MPa)	40-60 Tensile
Stress Hysteresis (MPa)	<20 (RT-450ºC)
Cracking Threshold (μm; blanket film)	>1.5
ASTM scratch tape test on SiN, SiON, Ta, TaN	Passed
Leakage Current (Amps/cm≤)	10-9 @ 1MV/cm
Glass transition temperature	>450ºC
Hardness (GPa)	1.5 – 3.0
Modulus (GPa)	10 - 20

Table 2. Summary of Black Diamond ™ film properties [17,21]

2.2. Required properties of low-k materials for integration

For successful integration of low-k materials into the BEOL interconnects, besides having low dielectric constant it should be chemically, mechanically and thermally stable in the system. Every IC fabrication node technology demands low-k materials with lower dielectric values and with optimum physical properties as summarized in Table 3. Choosing a new low-k material with optimal electrical, thermal and mechanical properties for current

interconnects and IC fabrication technology is very crucial. As mentioned earlier, lower dielectric constants are obtained by modifying of the molecular structure of the materials, which ultimately affects the mechanical and thermal properties of the low-k materials. Good thermal stability and low coefficient of thermal expansion is needed to prevent both, damage to the film and, property changes during subsequent thermal processing. The bulk dielectric constant of the ILD stack, when low-k film is stacked with barrier layers and liners (SiC and SiN) should be less than 3.0.

Electrical isotropic k < 3 @ 1MHz	**Chemical No material change when exposed to acids, bases and strippers**	**Mechanical Thickness uniformity <10% within and <5% wafer to wafer for 8″ wafer at 3σ**	**Thermal T_g >400 °C**
Low Dissipation	Etch rate and selectivity better than oxide	Good adhesion to metal and other dielectrics	Coefficient of thermal expansion <50ppm/°C
Low leakage current	<1% moisture absorption at 100% relative humidity	Residual stress <(±)100MPa	Low thermal shrinkage
Low charge trapping	Low solubility in H_2O	High hardness	< 1% weight loss
High electric field strength	Low gas permeability	Low shrinkage	High thermal conductivity
High reliability	High purity	Crack resistance	
High dielectric breakdown voltage > 2-3 MV/cm	No metal corrosion	Tensile modulus >1GPa	
	Long shelf life	Elongation at break >5%	
	Low cost of ownership	Compatible with CMP	
	Commercially available		
	Environmentally safe		

Table 3. Summary of required properties of low-k materials [16]

2.3. Barriers and adhesion promoters for Cu/low-k structures

BEOL multilevel interconnect structures comprise varieties of materials, such as Cu, low-k materials, oxides and nitrides. Copper interconnects in BEOL technology have some challenges such as, poor adhesion to dielectric materials and diffusion of copper into silicon substrates. Copper easily reacts with silicon and forms copper silicide at low temperatures

[22-23]. Traces of copper in silicon substrate will cause adverse effect on device operation. Most of the Interconnect metals (e.g. Cu, Ag, Au and W) except Al; do not bond well to underlying substrate and ILD. Therefore, the use of diffusion barrier layers and adhesion promoters between copper and underlying silicon substrate in ICs is mandatory. An ideal diffusion barrier material should also act as good diffusion barrier and adhesion promoters. Diffusion barriers under consideration are metal nitrides, carbides and borides, and metals such as Ti, Ta, and W. Diffusion barrier should be immiscible and non-reactive with copper. As stated by the studies, sputtered Ta and TaN films act as excellent diffusion barrier layers in Cu/low-k multilevel interconnects [24-25]. In the present investigation Ta, TaN, SiC and SiN are studied as barrier layers/cap layers in Cu/low-k stacks. SiC and SiN diffusion cap layers also acts as etch stops during the BEOL processes. Silicon nitride is widely used as cap layer; first, because it acts as an excellent barrier to copper and second, because of its etch selectivity to oxides.

3. Mechanical characterization of low-k structures by using nanoindentation

Currently most of IC fabrication technology has been migrated to Cu/low-k interconnect technology, as there is an increase of RC delay associated with the conventional Al/SiO2 interconnects used in the miniaturization of IC technology. This technology transition brings several integration challenges for the Cu/low-k interconnects because of poor thermal and/or mechanical properties of low-k thin films and Cu/low-k stacks [1]. Hence, it is very important to study the mechanical properties of different Cu/low-k structures to evaluate the device reliability. In the present investigation, mechanical properties of various Cu/low-k structures are studied by using nanoindentation technique.

The desired 'k' value of the low-k films can be attained by modifying the molecular structure of the low-k film or by introduction of organic or inorganic groups into the base structure [7]. Mechanical reliability and dielectric constant of the low-k materials are mutually dependent and have inverse relation. In case of SiO_2 based low-k materials, dielectric constant strongly depends on the density of the material, which in turn also depends upon the amount of porosity introduced, as shown in Fig 2 [27]. In chemical vapor deposition (CVD) based low-k materials, dielectric constant is decreased by the introduction of terminal methyl ($-CH_3$) groups, that will break the Si-O network and create nanopores. As the concentration of Si-O bonds decreases, percentage of pores and density non-uniformity increases, ultimately increasing the probability of mechanical failure of low-k films.

In IC fabrication technology, low-k material selection and its integration into BEOL is very crucial and it should withstand chemical mechanical polishing (CMP) without any failures. In microelectronic industry many researchers have been actively working toward finding threshold values of hardness and elastic modulus that can provide Cu/low-k system the ability to withstand CMP and wire bonding processes [28-30]. Researchers at Motorola [43] have concluded that passing the CMP process of low-k material is not a simple factor of modulus, hardness, adhesion or toughness, but a combination of all of these properties. As

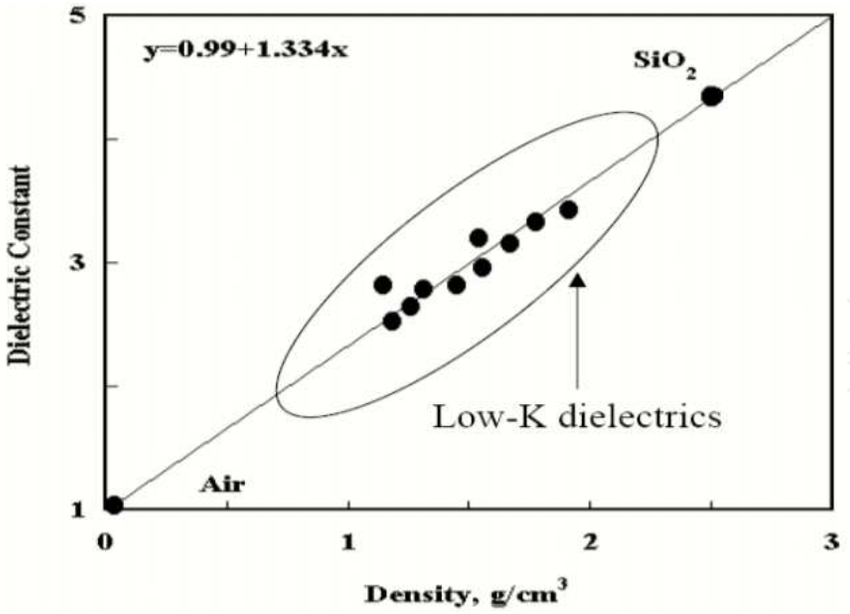

Figure 2. Dielectric constant dependence on low-k material density [27]

Dielectric thin films	Thickness (nm)	Elastic Modulus (GPa)	Hardness (GPa)	Researcher
Organo Silicate Glass (OSG)	2000	6.6-8.4	1.2-1.7	A.A. Volinsky et al [4]
USG (undoped silicate glass)	200-1000	79.06-80.66	5.65-7.52	Lu Shen et al [51]
SiLK ™	600	0.4	6.65	Lu Shen et al [55]
Porous SiLK ™	600	0.26	5.34	
MSQ –Hard	500-1000	12.5	0.936	S. Y. Chang et al [56]
MSQ-Soft	500-1000	2.7	0.19	
Low-k/barrier/Si (Anonymous)	1000	0.5	0.05	I. S. Adhihetty et al [57]
Porous low-k (carbon base)	250-540	4	0.15	Y. H. Wang et al [58]
Porous low-k (silica base)	250-540	0.35	0.45	

Table 4. Mechanical properties of various low-k materials studied by nanoindentation technique.

stated before, the mechanical properties of low-k films depends on chemical structure, amount of porosity and composition, Elastic modulus and hardness values of the different dielectric thin films varies from 2 to 14 GPa and 0.5 to 7 GPa respectively [41-45]. Volinsky et al [1] have found a linear relationship between hardness and elastic modulus for silicate low-k dielectric films in nanoindentation testing with continuous stiffness measurement (CSM) attachment. In nanoindentation testing, mechanical response of low-k films is

different from the metallic films and usually exhibits little or no plasticity [27]. Hardness and elastic modulus values of various low-k films and Cu/low-k stacks were tested with nanoindentation technique by many researchers and some of those results have been summarized in table 4. Based on the extensive literature survey and the present work, it is observed that the mechanical properties of various films and Cu/low-k stacks depend on many factors, more importantly the amount of porosity (Constitutive and Subtractive), composition, molecular structure, thickness, type of stack and diffusion barrier.

3.1. Sample preparation

Materials used in the present work include BD thin films, oxide, nitride and barrier layers. Black diamond, oxide, SiC and SiN films were prepared by using PECVD technique. Sputtering technique was employed to deposit the copper seed (150 nm), Ta and TaN layers. Copper film of 1μm thickness was deposited by electroplating process. Different stacks of these layers were deposited by different experimental techniques. All thin film samples were prepared on 8″ Si (100) wafer in semiconductor fabrication plant of class 1000 clean room environment. A thin oxide layer of thickness about 5 nm is deposited on the surface of silicon substrates to improve the adhesion between the substrate and the low-k thin films.

3.2. Continuous Stiffness Measurements (CSM)

This technique was introduced in the year 1989 by Oliver and Pethica [36-37]. The CSM technique developed over the last decade by researchers offers numerous advantages. It has the unique advantage of providing mechanical properties as a function of penetration depth. Calibration and testing procedure take very less time as there is no need for multiple loading and unloading. At high frequencies it allows to avoid obscure effects of the samples like creep, viscoelasticity and thermal drift, which cause much problem in the conventional calibration method. It allows us to measure the effect of contact stiffness changes and damping changes at the point of initial contact [38]. In CSM nanoindentation technique the contact stiffness is measured during loading of the indentation test and there is no need for separate unloading cycles. This is an ideal method to determine contact stiffness and it can measure at very small penetration depths. Hence this method is unique to measure mechanical properties of thin films of few tens of nanometers. It has an additional advantage that if the specimen shows viscoelastic behavior, the phase difference between the force and displacement signals gives idea about the storage and loss modulus of the specimen [26].

In nanoindentation experiment, the CSM technique is carried out by applying a harmonic force at relatively high frequency (69.3 Hz), which is added to increasing load, P, on the loading coil of the indenter as shown in Fig. 3. The applied current that determines the nominal load of the indenter is very small, which results oscillations to the indenter with a frequency related contact area and stiffness of the sample [39].

This technique accurately measures displacements as small as 0.001 nm using frequency specific amplification. To determine the contact stiffness of the sample, the dynamic

response of the nanoindenter has to be determined. A dynamic model which is used in CSM system is shown in Fig. 4. Major components of the dynamic model are the mass of the indenter, the spring constant of the leaf springs that support the indenter, the stiffness of the indenter frame and the damping constant due to the air in the gaps of the capacitor displacement sensing system.

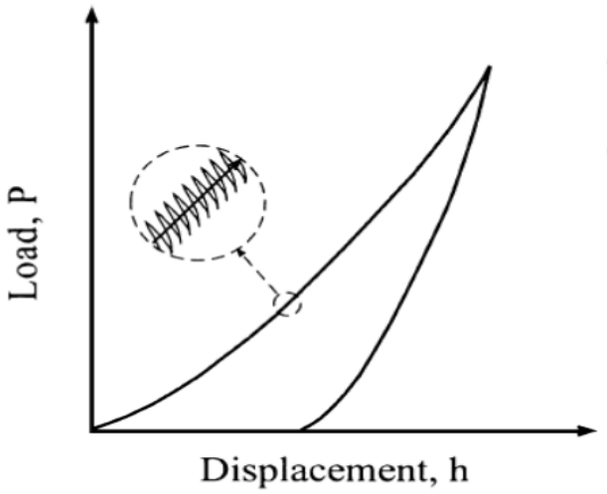

Figure 3. Schematic of nanoindentation CSM load-displacement curve [39;82].

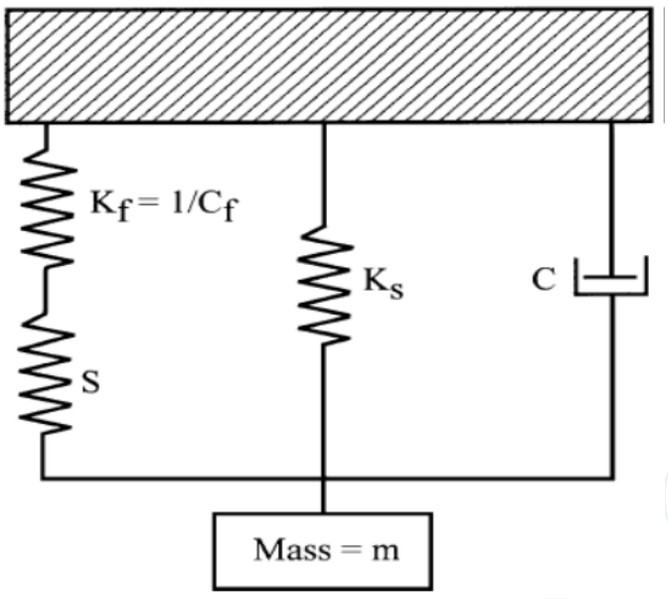

Figure 4. Schematic of components of dynamic model for the indentation CSM system [32]

By analyzing this model, the contact, S, can be calculated from the amplitude of the displacement signal from [39; 82],

$$\left|\frac{P_{OS}}{h(\omega)}\right| = \sqrt{\{(S^{-1} + C_f)^{-1} + K_S - m\omega^2\}^2 + \omega^2 D^2} \quad (1)$$

And the phase angle, ϕ between the driving force and the displacement response is

$$\tan(\phi) = \frac{\omega D}{(S^{-1} + C_f)^{-1} + K_s - m\omega^2} \quad (2)$$

Where

C_f= the compliance of the load frame (~1.13 m/MN)
K_S= the stiffness of the column support springs (~60 N/m)
D= the damping coefficient (~54 N s/m)
P_{os}= the magnitude of the force oscillation
$h(\omega)$= the magnitude of the resulting displacement oscillation
ω= frequency of the oscillation
ϕ = the phase angle between the force and displacement signals
m= mass (~4.7 gm)

4. Mechanical characterization of BD thin films with varying thickness

Thickness of the thin film structures used in the BEOL interconnects continue to decrease as the chip size decreases. Usually, thickness of the dielectric film has small effect on electrical properties [40], but it has significant influence on the mechanical properties of the film. Hence, it is very important to study the mechanical properties of these films of minute thicknesses. For this study, BD thin films of six different thicknesses, 100, 300, 500, 700, 1000 and 1200 nm have been prepared on 8" silicon substrate. Nanoindentation tests were performed on these films to study the effect of thickness on the nanomechanical behaviors. Fig.5 shows typical load-displacement curves of the BD thin films (100, 300, 500, 700, 1000 and 1200 nm) using nanoindentation CSM technique. By using this CSM technique, hardness and modulus can be determined as a function of indentation penetration depth with a single nanoindentation load-unload cycle. Berkovich indenter was employed in all experiments and a series of ten indentation tests were performed on each sample. The Poisson's ratio of the BD films of different thicknesses in nanoindentation experiment data is taken as 0.25, because the Poisson's ratio has a negligible effect on the indentation results [41]. During indentation, almost all BD films exhibit pop-in events as indicated by arrows in Fig. 5 due to failures in the films and it is evident from the optical micrographs (Fig. 6) and the corresponding pop-in events are marked on hardness and modulus vs. displacement graphs in Fig. 7. As the thickness increases, the degree of failure or the extent of damage increases in nanoindentation testing and it can be observed from the optical images shown in Fig. 6, where cracks are indicated by arrows on the micrographs. Many researchers have observed this kind of fracture behavior (pop-in event) in various types of low-k materials, bulk glasses and silica foams [42-46] Table 5 gives the information about the BD films fracture/delamination during nanoindentation testing, in terms of threshold load, threshold indentation depth and % of thickness at which film cracking occurs. For 100 nm thick film, failure is observed when the indenter tip is in the substrate and it can be seen in Fig. 5. In case of BD films with thickness 300-1200 nm, failure is observed within the films at different loads and indentation depths as shown in Fig5 and Table 5. It is found that as the BD film thickness increases the threshold load of cracking and the threshold indentation depth

increases. One common trend observed in the fracture among BD films (300-1200 nm) is that, the film failure (crack or/and delmaination) occurs at around 60-65% of the film thickness in indentation testing. This data is very useful in conventional nanoindentation processes to determine the physical properties of BD films, i.e. the threshold load for the BD films without cracking, threshold loads in CMP process and to measure the fracture toughness of the BD films.

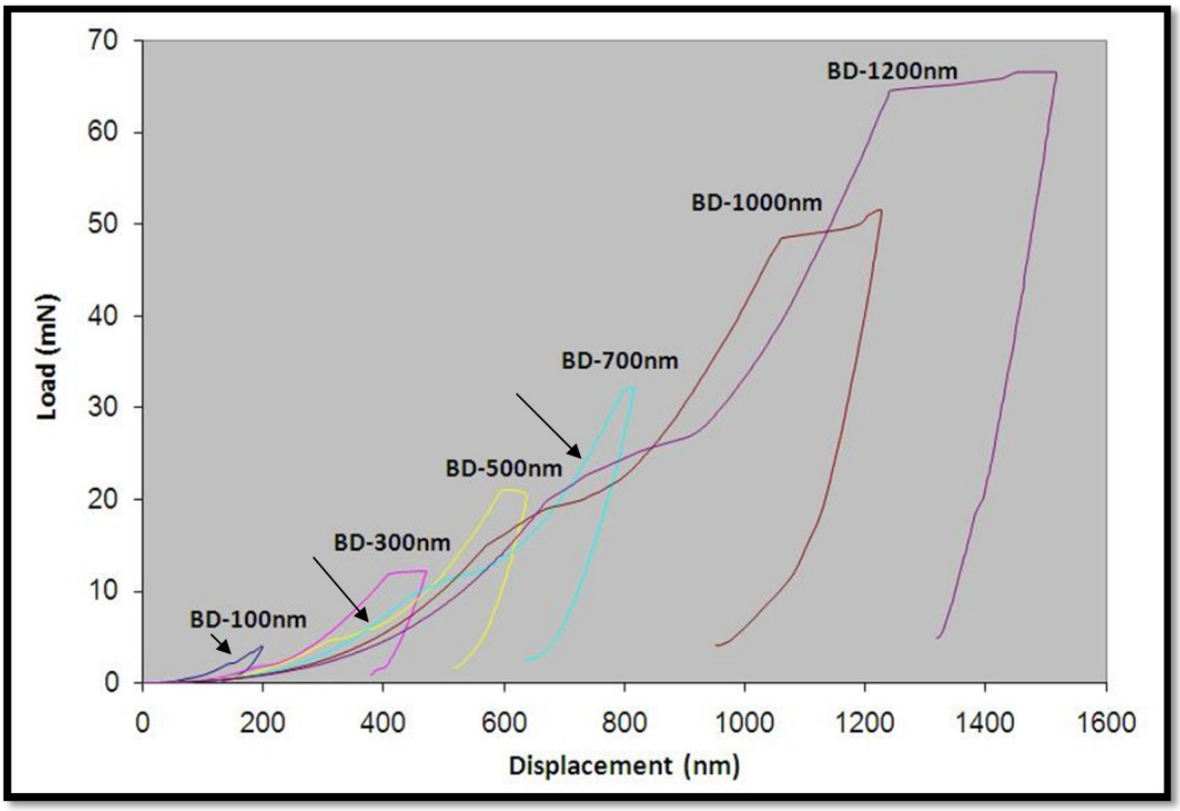

Figure 5. Load-displacement curves for Black Diamond ™ (BD) films of six different thicknesses under nanoindentation, (a) 100, (b) 300, (c) 500, (d) 700, (e) 1000 and (f) 1200 nm. Arrows on the curves indicate the pop-in events.

BD sample thickness (nm)	Threshold load of cracking (mN)	Threshold indentation depth of cracking (nm)	% of thickness at which cracking occurs (nm)
100	2.17	142	142
300	1.78	190.69	63.56
500	4.28	312.84	62.57
700	11.00	460.00	65.71
1000	18.83	644.00	64.40
1200	25.23	730.00	60.83

Table 5. Summary of fracture behavior data for all BD samples in nanoindentation testing.

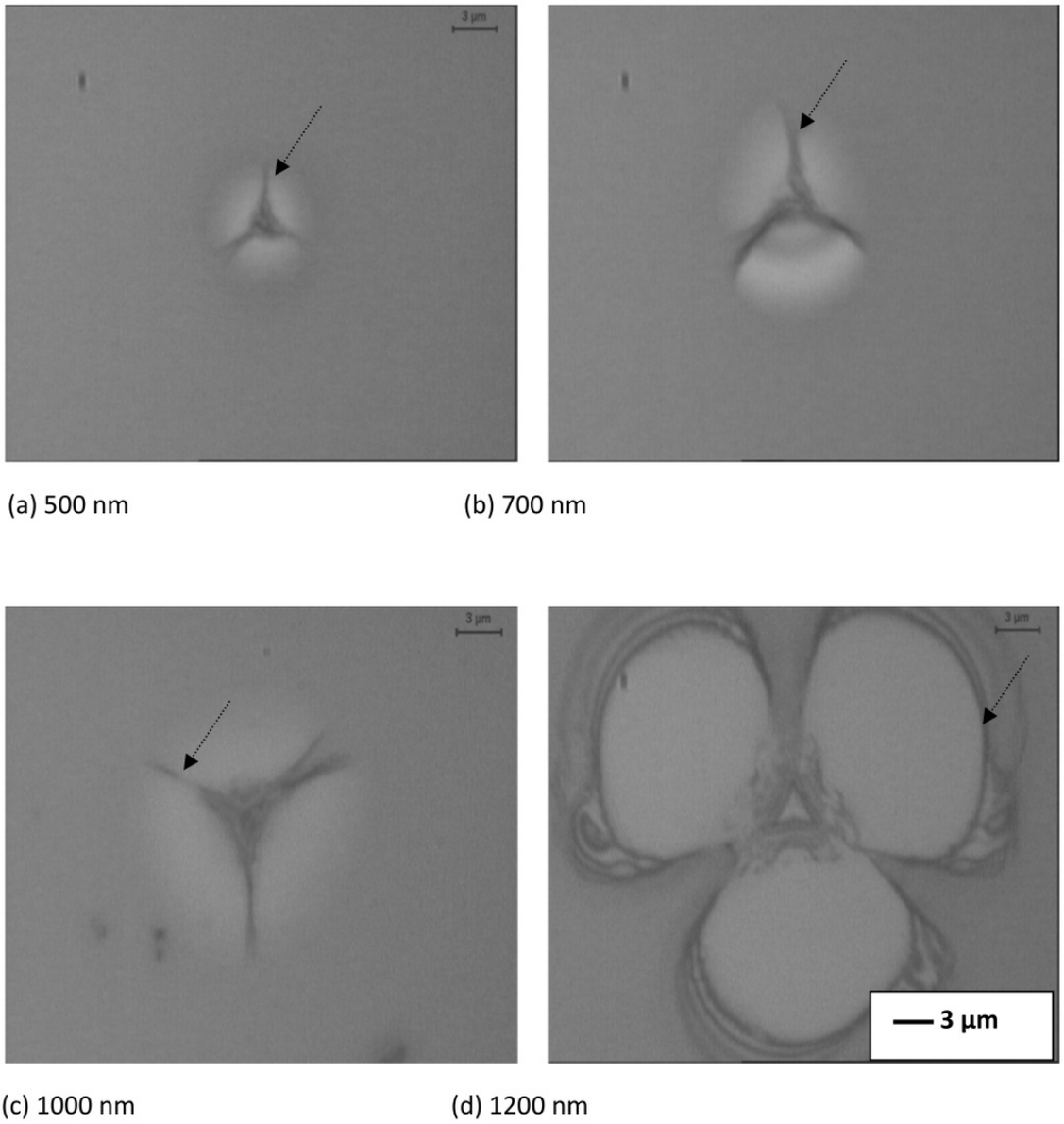

Figure 6. Optical images of residual nanoindentation impressions of (a) 500, (b) 700, (c) 1000 and 1200 nm BD thin films. Radial cracks in the films observed for all thicknesses as shown by arrows.

The hardness and elastic modulus as a function of displacement (indentation depth into the film thickness) of all BD samples are shown in Fig. 7. Results at the initial indentation depths show large fluctuations and high values of hardness and elastic modulus as the tip touches the film surface which might be due to the equipment noise and the inaccuracy of the indenter tip function at very shallow depth of indentation. As the depth of the indentation increases, both the hardness and elastic modulus reaches minima region as a property plateau and then tip starts sensing the effect of silicon substrate which results in higher hardness and elastic modulus. This phenomenon is observed only in the case of soft films on hard substrate. Usually, the initial part of the data is usually discarded in nanoindentation analysis and this kind of problem has been observed by other investigators [47-48]. Here, the averaged hardness and elastic modulus of this minima plateau region is used to define the

properties of the films. This phenomenon has been validated by comparing the properties at 1/10th of the film thickness and properties at the minima property region as shown in Table 6. There are no significant differences observed in between properties of the films at 1/10th of the thickness and properties from minimum plateau region. Hence in this scenario computing properties from minimum plateau region can be more practicable. Fig. 7 compares the mechanical properties of six different thicknesses of BD samples. Hardness and elastic modulus of the BD films (100 to1200 nm) are in the range of 1.66 to 2.02 GPa and 9.27 to16.48 GPa respectively.

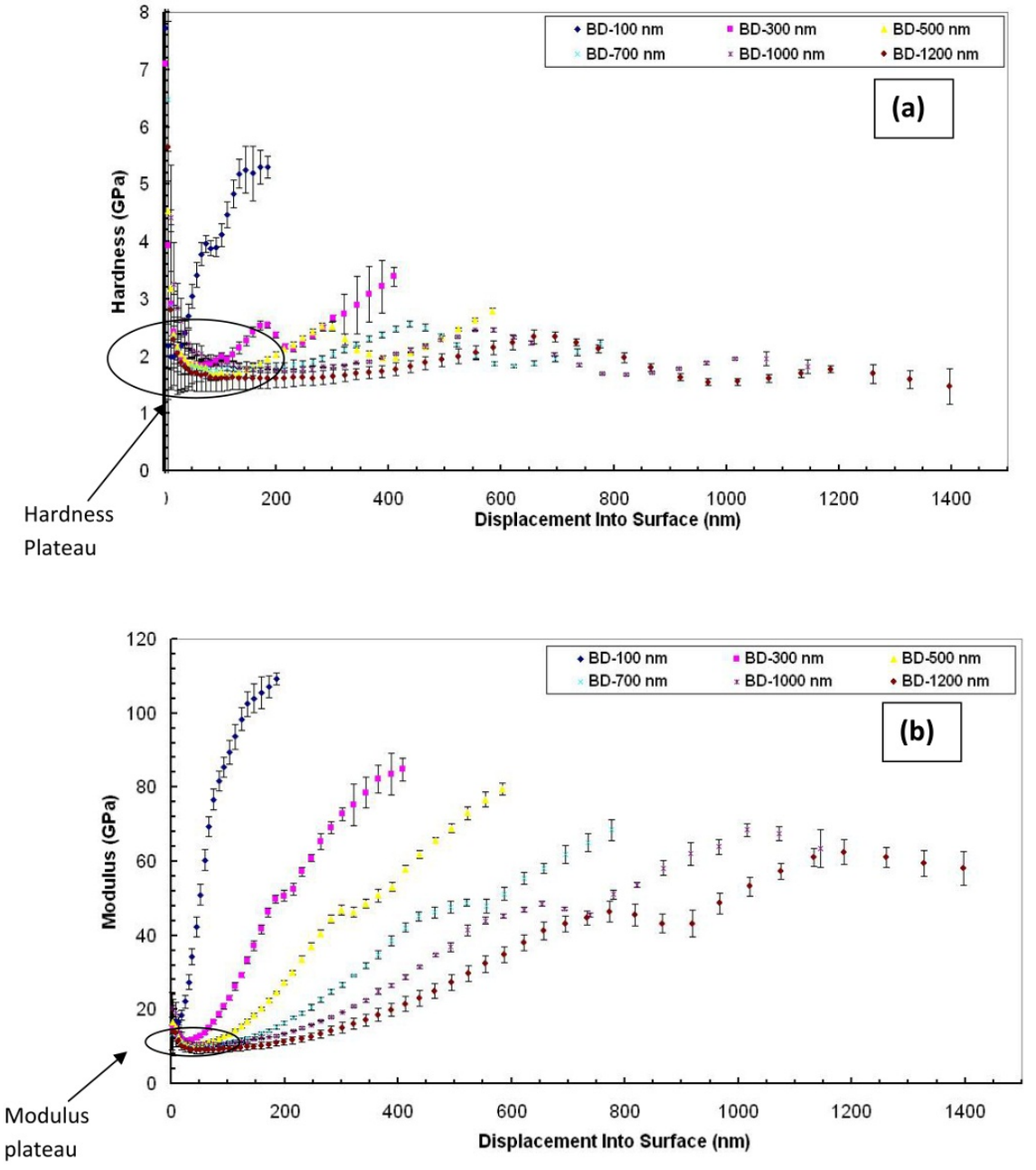

Figure 7. Hardness and (b) elastic modulus as functions of the displacement for BD films with six different thicknesses

Thickness of BD films (nm)	Property at 10% of film thickness (GPa)		Property at Plateau Region	
	H	E	H	E
100	1.99±0.25	18.53±1.5	2.02±0.36	16.48±2.1
300	1.83±0.32	13.76±1.3	1.85±0.12	11.54±1.2
500	1.63±0.14	12.91±1.4	1.70±0.05	10.58±1.5
700	1.58±0.24	11.62±1.5	1.78±0.02	9.93±1.1
1000	1.76±0.35	13.52±1.3	1.73±0.07	10.41±1.4
1200	1.62±0.84	12.72±1.5	1.66±0.09	9.27±1.7

Table 6. Summary of mechanical properties of BD films of six different thicknesses

As the indentation depth increases initially slight decrease in hardness and elastic modulus values are observed and as the indentation depth further increases these property values reach minima, then tip starts sensing the effect of the substrate which results in higher hardness and elastic modulus values. The initial decrease of properties as the indentation displacement increases is observed during nanoindentation of very thin films [49]. The averaged values of properties in minima plateau region are considered to be the real properties of the films and, in the present study, these values are used to define the properties of each film as shown table 6. The hardness values of all BD films are in the range of 1.66 to 2.02 GPa and the elastic modulus values are in the range of 9.27 to 16.48 GPa. Sharp deviations are observed in the property vs. displacement (see Fig. 7) graphs of all BD films, which corresponds to the pop-in events shown in Fig. 5, resulting from film cracking and/or delamination at the BD film-silicon substrate interface. Significant differences in mechanical properties are observed when the BD film thickness is less than 500 nm (100-500 nm), mainly in the case of elastic modulus. When the BD film thickness is greater than the 500 nm (500-1200 nm) no significant variation in mechanical properties are observed and it can be assumed that these properties are representative of the bulk properties of the BD films.

The minima plateau region for the hardness is considerably large and there is nearly no change with respect to different thicknesses, when compared with elastic modulus plateau region. The minima elastic modulus plateau region decreases as the BD film thickness decreases because the effect of substrate is more on elastic modulus for thinner films. In Fig. 7, it is observed that the sharp increase in modulus from the minima plateau region, mainly due to the effect of substrate, is much more on the elastic modulus than on the hardness of the BD films. This is because the elastic modulus is associated with the elastic deformation during nanoindentation, and in contrast, the hardness response of the material is associated with plastic deformation. Extensive simulation studies show that, the effective elastic modulus of a film experiences greater substrate effect than the hardness value [44]. BD -100 nm film shows significantly higher elastic modulus (E=16.48 GPa) when compared to higher thickness BD films and it is expected due to molecular restructuring in very thin BD films (≤100 nm), since the elastic modulus is an intrinsic material property, which largely depends on interatomic or molecular bonds [49]. Hence the higher elastic modulus of BD-100 nm film is probably expected due to stronger molecular bonding between organic (-CH_3) and inorganic (Si-O) constituents.

5. Effect of diffusion barriers on BD stacks integrity

For this study, four samples have been prepared with Ta and TaN barrier layers and dual stacks also have been prepared as BD/Ta/Si, BD/Ta/BD/Ta/Si, BD/TaN/Si and BD/TaN/BD/TaN/Si. Mechanical properties were assessed by nanoindentation technique. For single dielectric stack, the silicon substrate is first coated with Ta or TaN barrier layer of 25 nm thickness by using self-ionized metal plasma (SIP) technique at room temperature followed by the deposition of BD film of 1000 nm thickness by PECVD (plasma Enhanced Chemical Vapor Deposition) technique. For the deposition of dual dielectric stack this procedure was repeated one more time with BD films and barrier deposition. The application of Ta and TaN barrier layers to BD films improves stiffness in addition to other mechanical properties.

The thickness of single and dual dielectric stacks studied in the present work is 1025 and 2050 nm respectively. Fig. 8 shows the typical load-displacement curves of single and dual dielectric stacks. Both single and dual dielectric stacks show pop-in events. From Fig. 9 optical micrographs of residual nanoindentation impressions of single and double dielectric stacks reveal that massive failure of the films is more prominent in dual dielectric stacks. Dual dielectric stacks demonstrate massive failure which can be observed as more pop-in events in load-displacement curves especially at the interfaces, which are shown as dotted lines in Fig. 8. This can be confirmed by observing the residual nanoindentation marks as shown in Fig. 9. Hence, it is expected that crack formation and/or delamination may occur at the interfaces due to indenter penetration as observed by J. Vitiello [50]. In the current study, stacks having same barrier layer (Ta or TaN) are compared with respect to mechanical properties. Hardness and elastic modulus of single dielectric stacks are in the range of 1.43 to 1.91 GPa and 8.35 to 10.03 GPa respectively. No significant difference is observed in the case of double dielectric stacks. Mechanical properties of both single and dual stacks are given in Table 7.

5.1. Mechanical properties of the BD stacks with Ta barrier layer

Hardness and elastic modulus of both single and dual dielectric stack with Ta barrier layer is shown in Fig. 10. High hardness values at the film surface for both stacks are observed mainly due to the inaccuracy of indenter tip functions and surface roughness [47]. Large fluctuations in hardness values throughout the film thickness measurements are observed due to the failure of stacks during the nanoindentation. Substrate effect is more prominent in single dielectric stack when compared with double dielectric stack, this is because the thickness of both the stacks are different and there is difference in the number of interfaces. The hardness and elastic modulus values of single dielectric stack is higher than the values for dual dielectric stack and these properties are consistent throughout the thickness of the stacks as shown in Fig. 10. The averaged minima property plateau is used to define the property of each stack and these values are given in Table 7. Single dielectric stack has hardness of 1.91 GPa and modulus of 10.03 GPa, whereas for dual stack, the values are 1.38 and 7.98 GPa respectively. From Fig 10, sudden deviations in properties are observed mainly due to the film failure during nanoindentation process which corresponds to pop-in

events in load-displacement curves as discussed earlier. This mechanical property data of single and dual stacks are very useful in CMP performance, for example, single dielectric stack has slower removal rate when compared to dual stack for the same CMP pressure [51-52]. This is mainly due to the higher hardness value of the single dielectric stack. This mechanical characterization data will be very helpful in deciding the CMP loads as per the dielectric stacks.

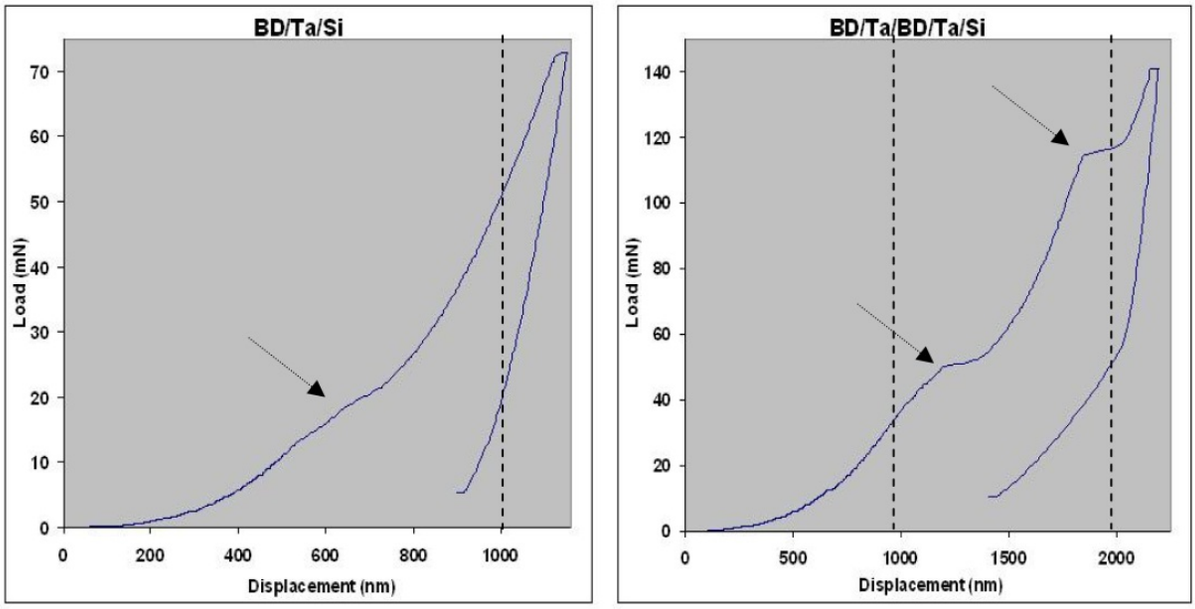

Figure 8. Typical load-displacement curves of (a) BD/Ta/Si (b) BD/Ta/BD/Ta/Si, (c) BD/TaN/Si and (d) BD/TaN/BD/TaNs/Si stacks. Arrows indicate the pop-in events.

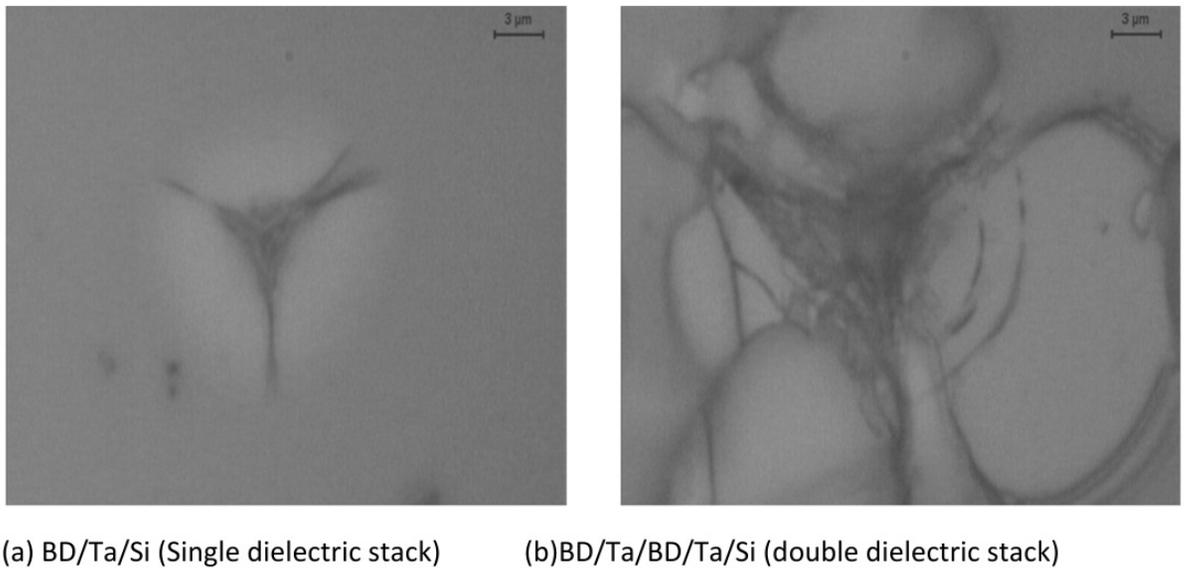

Figure 9. Optical micrographs of residual nanoindentation impression on single and double dielectric stacks.

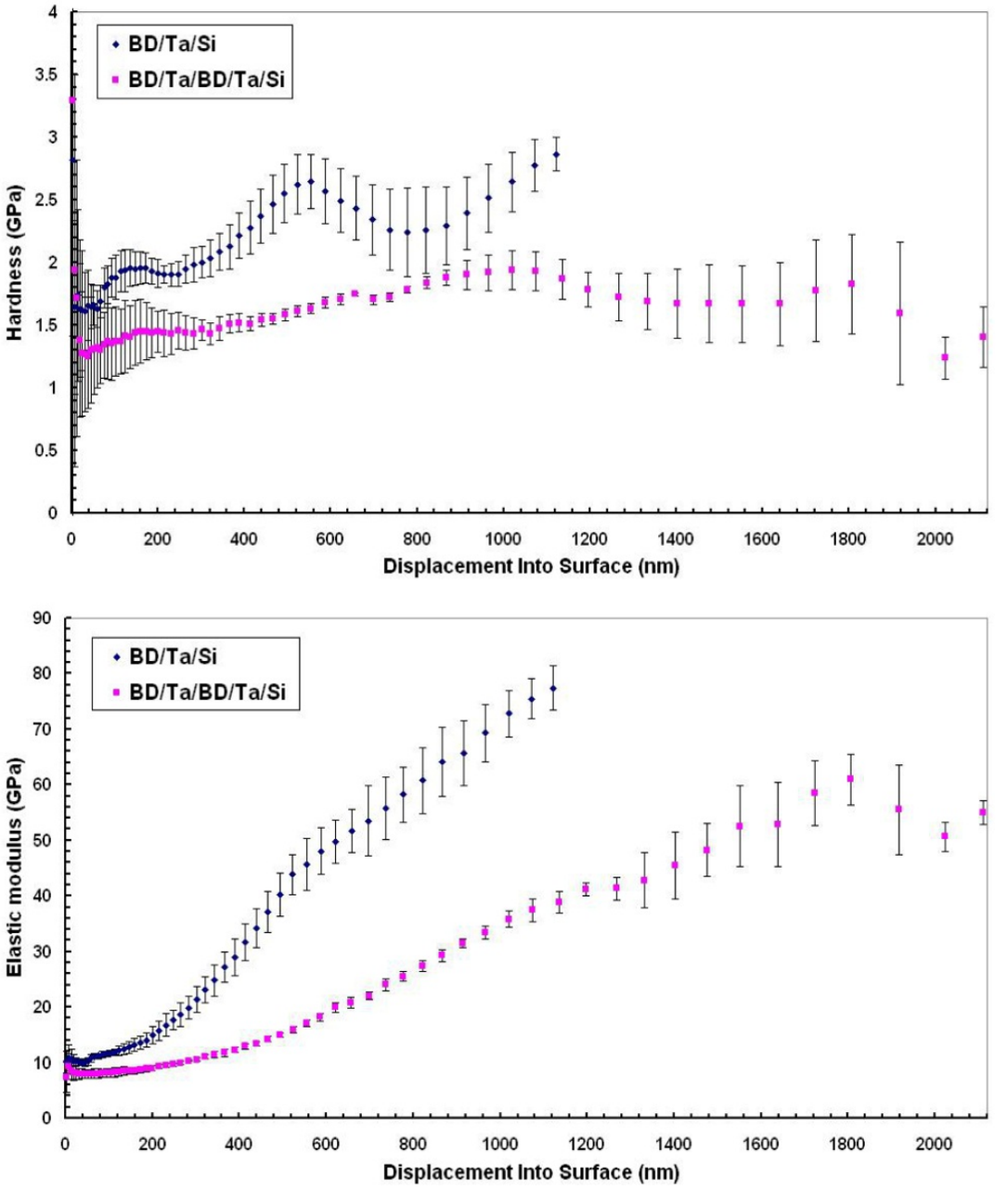

Figure 10. Hardness and elastic modulus as a function of displacement for BD/Ta/Si and BD/Ta/BD/Ta/Si stacks measured using the nanoindentation CSM technique.

5.2. Mechanical properties of the BD stacks with TaN barrier layer

The total thickness of these stacks are maintained same as in previous section, i.e. 1025 nm for single dielectric stack and 2050 nm for dual dielectric stack. Hardness and elastic modulus as a function of displacement of these stacks measured using the nanoindentation CSM technique is presented in Fig. 11. Single dielectric stacks have slightly higher mechanical properties when compared with dual dielectric stacks as summarized in table 7. In both cases, the performance of single dielectric stacks is better than that for the dual

dielectric stacks. By comparing the single dielectric stacks, BD/Ta/Si has higher hardness and elastic modulus than for BD/TaN/Si stack (Table 7). Thus barrier layer greatly affects the mechanical properties of the single stack. There is no significant difference observed in the case of BD/Ta/BD/Ta/Si and BD/TaN/BD/TaN/Si dual dielectric stacks. It is anticipated that the lower mechanical properties of dual stacks is mainly due to the presence of residual stresses. Usually, dual stacks have more residual stresses when compared with single dielectric stacks as dual-stacked samples are subjected to more processing steps. Compressive stresses in the stacks result in an increased hardness values but tensile stresses cause a decrease in hardness. Therefore, dual stacks are expected to have more tensile stresses when compared with single dielectric stacks.

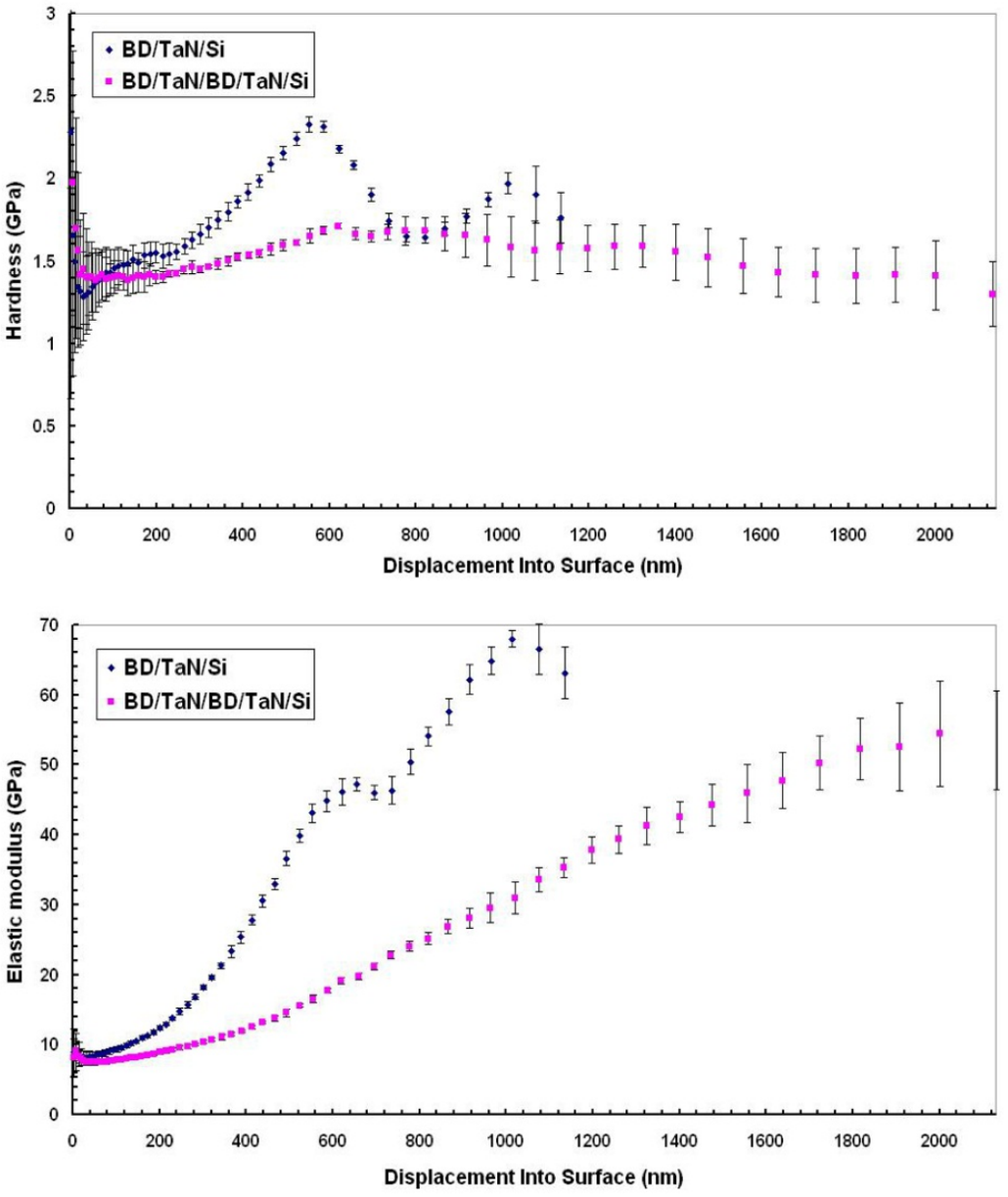

Figure 11. Hardness and elastic modulus as a function of displacement for BD/TaN/Si and BD/TaN/BD/TaN/Si stacks measured using the nanoindentation CSM technique

Multilayer Stack	Stack Thickness (nm)	Hardness (GPa)	Elastic Modulus (GPa)
BD/Ta/Si (Single dielectric stack)	1025	1.91±0.3	10.03±1.2
BD/Ta/BD/Ta/Si (double dielectric stack)	2050	1.38±0.1	7.98±1.5
BD/TaN/Si (Single dielectric stack)	1025	1.43±0.5	8.35±1.4
BD/TaN/BD/TaN/Si (dual dielectric stack)	2050	1.4±0.2	7.58±1.3

Table 7. Summary of mechanical properties of single and double dielectric stacks.

6. Effect of the wafer thinning/backgrinding on the integrity Low-k stacks

For this study, multilayer low-k stack with fifteen different thin films comprising SiN, USG, Blok (SiC), BD (Black Diamond ™, low-k), has been fabricated as shown in Fig. 12 All thin film samples were prepared on 8″ Si(100) wafer in a semiconductor processing clean room of class 1000 environment. Samples fabricated in this study are exclusively designed to study the BD (low-k) integrity in the BEOL interconnects and it resembles the Cu/low-k structure of the three metallizations. So the structure has three BD low-k layers at different levels according to the BEOL (Back End of the Line) interconnect design specifications. The total thickness of the multilayer low-k stack is around 3400 nm. Therefore present study gives an outlook about the response of the low-k test structures during back grinding process. To study the backgrinding/thinning effect on the Low-k stacks, all samples have been subjected to backgrinding process by using the commercial backgrinding system. Empirically backgrinding process involves, first coarse grinding using grit #300, then fine grinding using #2000 followed by dry polishing. A total five set of samples have been prepared for this study as, normal sample (without backgrinding), Back grinded samples of four different thicknesses (BG-500, 300, 150 & 75um).

Failure loads, hardness (H) and elastic modulus (E) normal (no back grinding) and back grinded low-k stacks (BG-500, 300, 150 & 75 μm) are computed by analyzing the nanoindentation load-displacement curves as shown in Fig. 13. From Fig. 13, it is obvious that all stacks have shown pop-in event and this event can be taken as the failure load/fracture strength of the stack. These pop-in events in the nanoindentation curves are resulting from the film cracking and delamination of the stack in the form of blisters [53]. The normal stack shows pop-in event (failure load/fracture strength of the stack) at lower loads and indentation depths, as compared to the back grinded stacks. Normal stack failed at 456.25±21.22 mN load and 2422.41±58.53 nm indentation depth, whereas back grinded stacks failed in the range of 482 to 661mN load and 2405-2979 nm indentation depth. The failure load and depth values of all types of samples are summarized in the Table. 8 and. From the nanoindentation curves and optical imaging (from Fig.14), analysis it is clearly

evident that the nanoindentation response of the normal and back grinded stacks is different in terms of failure load depth and fracture behavior. Normal stack and BG-500μm show extensive delamination and chipping, whereas other back grinded stacks (BG 300, 150, 75 μm) show delamination blister and this behavior is in good agreement with the nanoindentation pop-in event. BG-500μm exhibits the mixed response as it shows chipping-off during nanoindentation and moderate pop-in failure load of 482.17 mN and this might be due to the moderate degree of back grinding. In case of the other back grinded stacks (BG 300, 150, 75 μm), even higher nanoindentation loads are not able to damage/chip-off the low-k stack and cause interfacial delamination only. No significant difference in fracture strength (pop-in event) is observed among BG-300, 150, and 75 μm back grinded stacks and all these grinded stacks show higher facture strength/loads than the normal stack and BG-500μm. Accordingly the increase in failure load depends on the degree of the back grinding, but not much difference is observed when the wafers are grinded to 300, 150 and 75 μm. After back grinding, the strength of the low-k stack is enhanced, mainly in terms of nanoindentation load and indentation depth and this increase is understood mainly due to the application of mechanical pressure and thermal stresses during back grinding action. The back grinding pressure or load may improve the adhesion, especially Vander walls forces at the multilayered interfaces and cause the densification of the individual films of the stack. It is being investigated by many researchers in the packaging field that the back grinding processes are deteriorating the die strength, but this is not the same phenomenon with the active side of the chip stack.

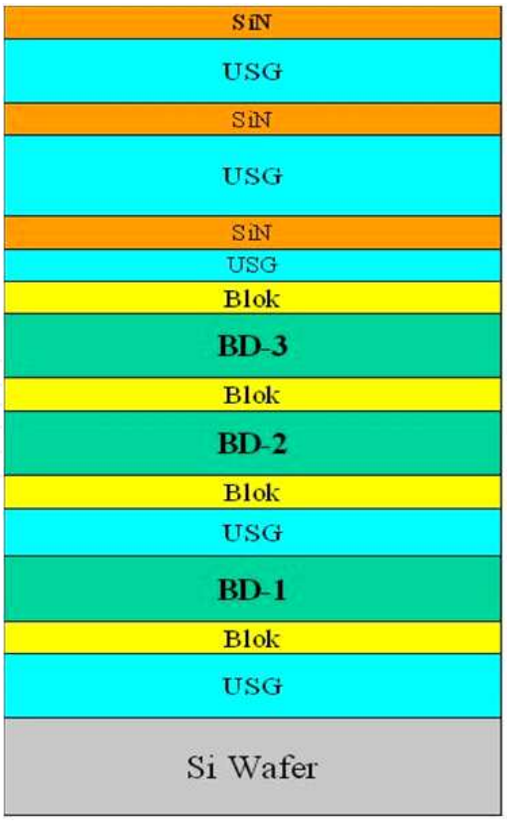

Figure 12. Low-k stack with fifteen multilayers for wafer backgrinding study

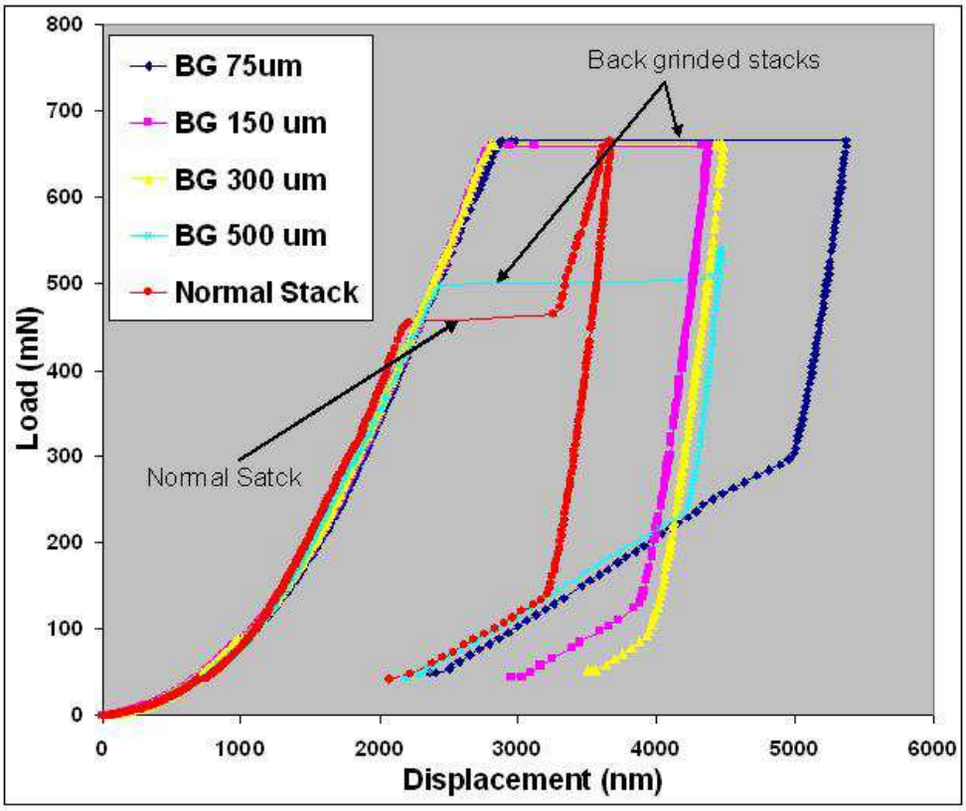

Figure 13. Typical load-displacement curves of normal and back grinded samples and its comparison.

BD samples	Fracture Behavior	
	Load (mN)	**Indentation Depth (nm)**
Normal stack	456.25±21.22	2422.41±58.53
BG-500μm	482.17±25.25	2405.86±70.47
BG-300μm	661.20±7.57	2979.79±21.58
BG-150μm	658.45±4.74	2809.01±30.60
BG-75μm	658.60±12.21	2942.52±71.20

Table 8. Summary of nanomechanical properties of normal and back grinded samples

Fig. 15 shows the hardness and elastic modulus as a function of the indentation depth for normal and back grinded stacks measured by using the nanoindentation CSM technique. Mechanical properties of all samples are not constant, but strongly influenced by the contact depth and this is mainly due to the presence of the different types of thin films with diverse physical properties and 15 interfaces. From Fig. 15, it is clear that initially all samples exhibit high hardness and modulus values due to the presence of the SiN layer on top of the stack. However, back grinded stacks show higher hardness values throughout the indentation depth and this difference is significant till ~1500 nm. Even though BG-500 μm samples shows moderate failure load values when compared to other back grinded stacks, it still shows higher mechanical properties than normal stack. There is no difference in hardness

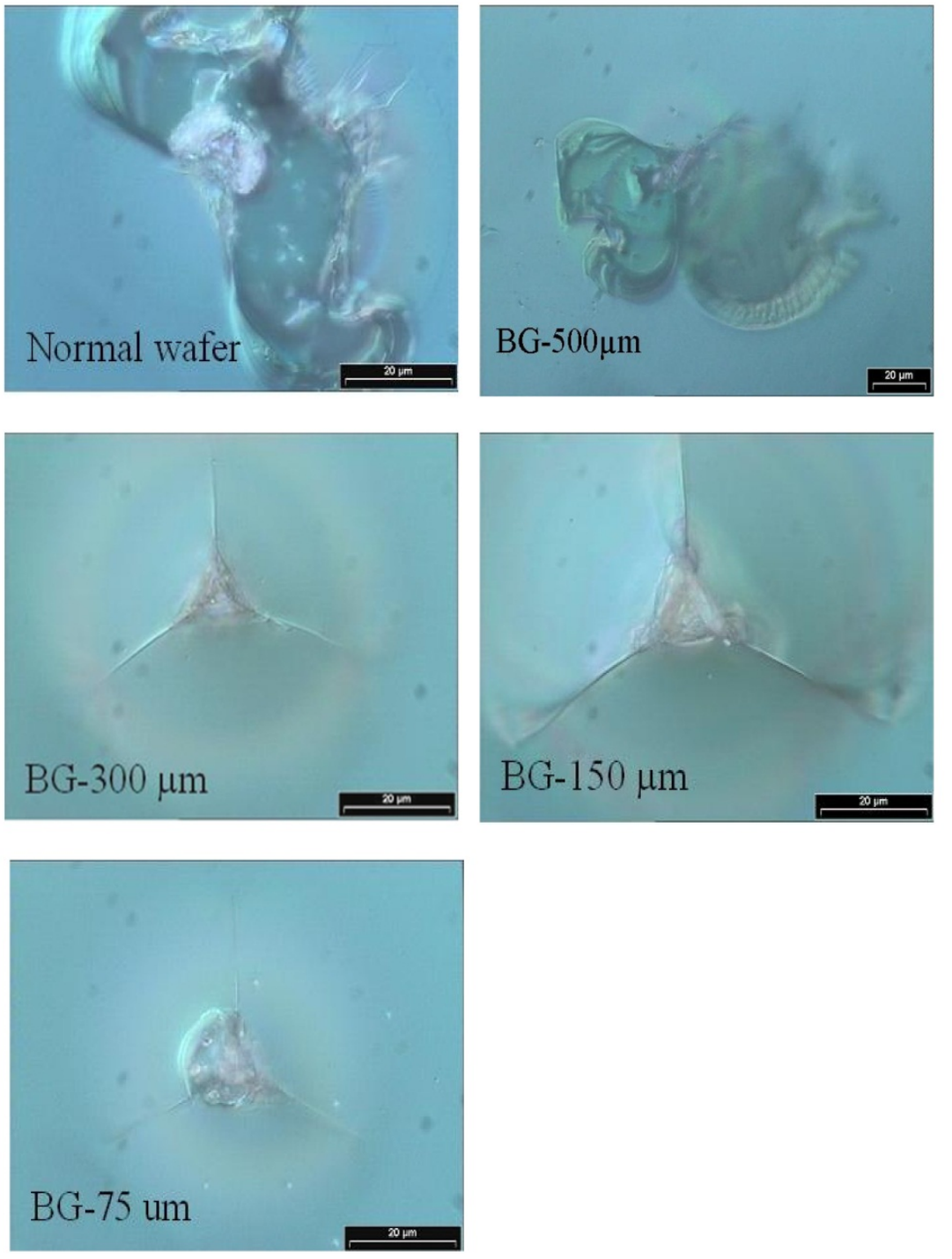

Figure 14. Optical images of residual nanoindentation impressions of normal and back grinded samples.

values among the back grinded stacks. In case of the elastic modulus, the overall trend is mixed, in which initially back grinded stacks exhibit high values and from 1000 nm depth, BG-150 µm stack follows the trend of normal stack and BG-75 & 300 µm stacks show lower modulus values. The mixed trend of modulus values of all samples is mainly due to the fact that, the elastic modulus is highly sensitive and intrinsic property. Elastic modulus is greatly

influenced by layers beneath the testing films and substrate. In the case of hardness, the difference between normal stack and back grinded stacks is very clear when compared with the modulus values. As a whole, back grinded stacks exhibit the higher hardness and elastic modulus values, and this trend is quite clear in the low-k region. This might be due to back grinding loads or pressures influencing the interfaces and causing the densification of the films, especially in the low-k region. Sekhar Et al., have extensively studied the nanoscratch behavior on the backgrinded stacks by analyzing the fracture behavior by critical loads [54]. In this study the fracture or failure strength, hardness and elastic modulus of the normal and grinded stacks are analyzed and compared at overall level as the nanoindentation analysis is very complicated and not well established for the multilayered stacks.

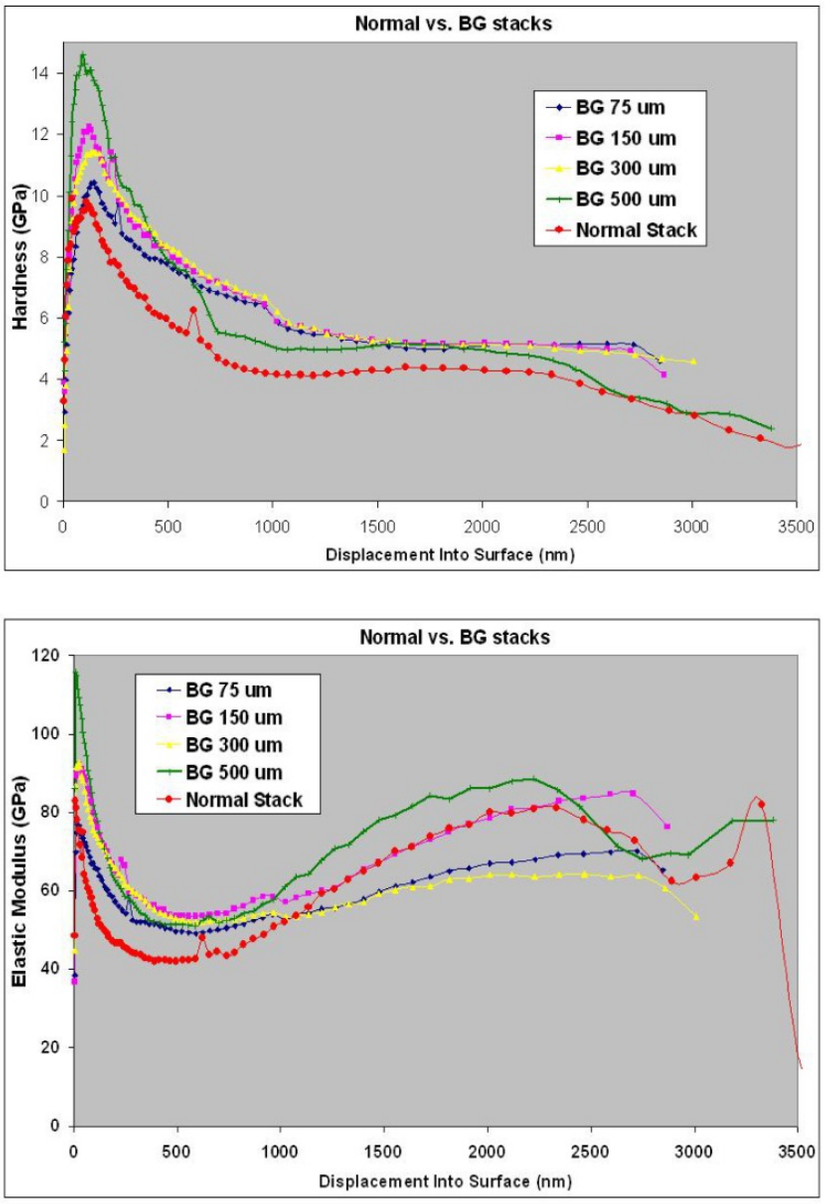

Figure 15. Hardness and elastic modulus as a function of displacement for normal and back grinded samples

7. Summary

This chapter presents the systematic mechanical characterization of the BD thin films for BEOL interconnects and 3D IC/packaging applications. For this purpose several thin film systems have been chosen which comprises, Black diamond (SiOC:H), USG (SiO2),SiC, SiN and Ta & TaN thin films which have been prepared by using PECVD technique and sputtering technique respectively. Nanoindentation tests with continuous stiffness measurement (CSM) attachment have been performed on all samples to assess hardness (H) and elastic modulus (E) properties. The CSM attachment is preferable because it provides continuous measurement of the hardness and elastic modulus as a function of indentation depth. In this study several Low-k systems have been prepared and characterized as, mechanical characterization of low-k films with different thicknesses, influence of Ta & TaN barrier layers, and effect of wafer backgrinding/thinning on the complete low-k stack which is similar to actual BEOL with three metallization. In case of the thickness dependence of mechanical properties of BD films, hardness and elastic modulus values obtained of all BD films (100-1200 nm) are in the range of 2.02to 1.66 GPa and 16.48 to 9.27 GPa respectively. Considerable thickness dependence of the properties is observed when thickness is less than 500 nm. To study the effect of barrier layers on low-k stack, single and dual dielectric stacks have been fabricated with Ta and TaN barrier layers. In nanoindentation testing, the performance of single dielectric stacks is better than the dual dielectric stacks is mainly attributed to differences in the number of interfaces, total film thickness and residual stresses.

For the first time the effect of the back grinding process on active side of the low-k chip stack has been studied by using sophisticated nanoindentation technique. It is further investigated by analyzing the fracture or failure strength (pop-in event in nanoindentation), hardness, elastic modulus of the low-k stack for both normal and back grinded samples. After back grinding process, the overall integrity of low-k stack is enhanced and thus the back grinded stacks exhibit higher nanomechanical properties than the normal stacks. This can be attributed mainly to the straightening of the low-k interfaces and densification of the BD (low-k) layers during back grinding processes. Based on the results and their detail analysis it can be said that the thermo-mechanical stresses that applied and/or generated during wafer back grinding processes affect the interfaces and nanomechanical behavior of the low-k stack, in turn enhances the overall integrity of the back grinding stacks.

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