Chapter 8

Materials and Processing for Gate Dielectrics on Silicon Carbide (SiC) Surface

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Additional information is available at the end of the chapter

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1. Introduction

Dielectrics are the materials that do not conduct current in the presence of an electric field. The applications of this material in semiconductor industries are very broad in various capacities. Nowadays, extensive research and development (R&D) are in progress to grow high quality high-k gate dielectrics on semiconductors surface. Applications include extending the limit of transistor gate capacitance beyond that of ultra thin silicon dioxide (SiO_2) and to improve the gate dielectric reliability in wide band gap semiconductor devices. SiO_2 is one of the best gate dielectric, which is continuously investigated rigorously since long lime back for silicon based metal-oxide-semiconductor (MOS) device technology. The thermally grown SiO_2 offers several key advantages in microelectronics device processing including thermodynamically and electrically stable high quality interface state density as well as better electric insulation properties. New materials are endlessly researched to fulfill the limitation of silicon across a wide spectrum of industrial applications.

Silicon Carbide (SiC) has been proven to be most suitable material, offering significant potential advantages both in high temperature as well as high power device technology. Moreover, SiC is the only material that can be thermally oxidized to grow high quality SiO_2, which enables to fabricate the MOS structures. A large drawback of SiO_2 is its low dielectric constant, which is about 2.5 times lower than that of SiC and also poorer interface properties at SiO_2/SiC. This causes a proportionally large electric field enhancement in the dielectric compared to that in the semiconductor, which is a reason why new dielectrics with dielectric constant at least similar to that of SiC and lower interface states densities are desired for device applications. There have been few successful high-k dielectrics including silicon nitride (Si_3N_4), Oxynitride, aluminum nitride (AlN), hafnium dioxide (HfO_2), tin oxide (SnO_2),

cesium oxide (CeO_2), titanium oxide (TiO_2), tungsten oxide (WO_3), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), gadolinium oxide and others have been attempted in SiC technology. This chapter covers the selection of gate dielectrics, their processing, interface properties, their electronic structure, flat band voltage shifts and electronic defects.

2. Selection of gate dielectrics

Most of the gate dielectrics material fallows the trend of decrement in their bandgap energy, when the value of their dielectric constant goes towards higher end (high-k). Therefore, the band offset alignment at the interface of gate dielectric and SiC interfaces is an important issue while integrating a high-k gate dielectric in SiC-based devices because SiC belongs to the family of wide gap semiconductor (>3 eV). Figure 1 shows the tendency of bandgap energy as a function of dielectric constant. The bandgap energy of dielectric material has a direct correlation to the leakage current through the band edge offset. Wider bandgap energy means a better chance for a larger conduction or valence band offsets at the interface of semiconductor and the gate dielectric. Furthermore, the band gap energy of high-k oxides (5-6 eV) is modest as an insulator, which may result in large leakage current because of insufficient barrier height at interface. The value of low band offsets at the high-k/SiC interface may be overcome by introducing an ultrathin SiO2 interfacial layer in between dielectric and SiC layer (Mahapatra R., 2008). Figure 2 shows the energy band diagram of metal-gate dielectric-SiC structures as well as stack layers of HfO_2/SiO_2/4H-SiC. In figure 2, HfO_2 was considered as gate dielectric while 4H-SiC was the base substrate. In a situation when the theoretical calculations of energy band diagrams are not available, nor there are measured differences between insulator and SiC energy bands, the size of the bandgap allows for a rough evaluation of the probable usability of the gate dielectric. In ideal case, symmetrical offsets for electrons and holes of the order of 2 eV, the bandgap energy of the gate dielectric should be at least 7 eV. The mechanical and structural properties of ideal gate dielectrics are as important as its electrical performance. The most recommended form of the materials is mono-crystalline structures but those are often grown at very high temperatures and precise pressures. In case of passivation, when the dielectric material is considered to be deposited as the last processing step at low temperatures, the material should have an amorphous composition. This would prevent a possible current conduction through the grain boundaries of the polycrystalline material. Moreover, a lot of research is oriented towards nanocrystalline structures and application of those could provide materials with e.g. larger bandgap, modified by small grains dimension. Other mechanical feature like surface roughness, purity, or right stoichiometry of insulators implies that a good control over the deposition process and correct film uniformity is achieved. To eliminate the mechanical stress caused by device operation at high temperature, the thermal expansion coefficient and thermal conductivity of the dielectric and SiC should be similar. The insulator should also be hard, resistant to cracks and should not be influenced by the surrounding atmosphere.

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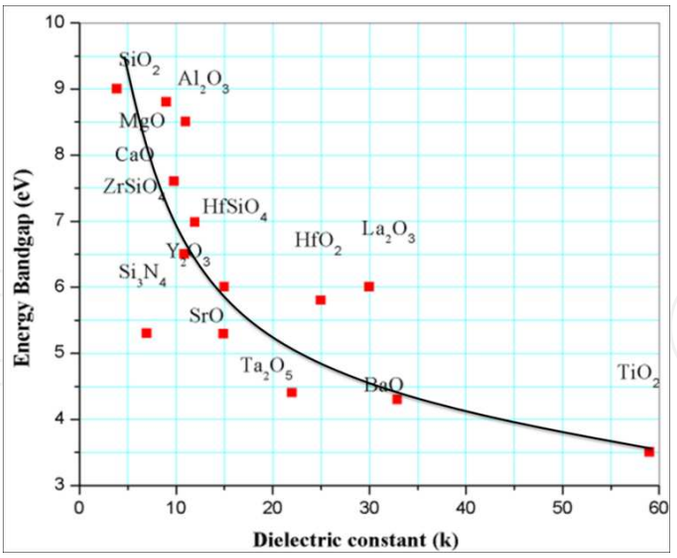

Figure 1. Variation of bandgap energy of different dielectric materials as function of its dielectric constant

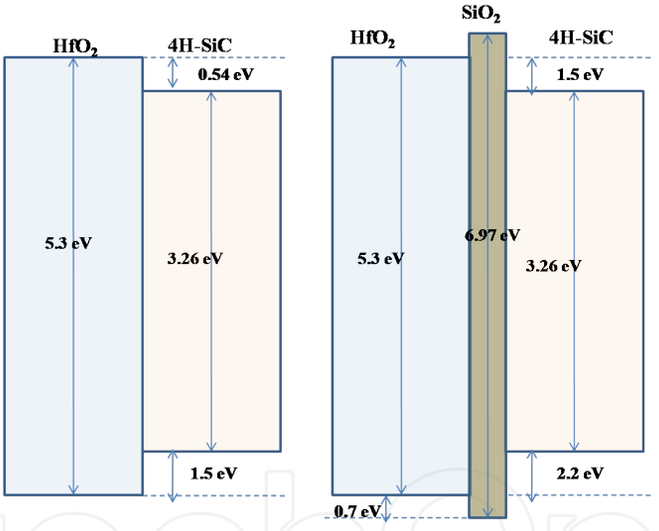

Figure 2. Energy band diagram of HfO_2/4H-SiC and HfO_2/SiO_2/4H-SiC system

However, a significant higher interface state density and inferior electrical properties were found at the SiC/oxide interface because of the interface imperfections. It has been demonstrated by many researchers that a proper annealing of gate dielectrics can reduce the density of traps and passivate the defects level. The process parameters of annealing (temperature, ambient, time etc) can also be a key factor on interface properties. The incorporation of atomic nitrogen shows favorable effects on the structural stability of gate dielectric layers (Chen Q., 2008). At high temperature operation the quality of gate dielectric degrade as the result interface properties show the poor performance. Therefore, the understanding of proper band alignment and the thermal stability at the interface is critical for the

application of high-k/SiC-base stacks for high temperature applications (Weng M-H, 2006). Another issue of interest is surface preparation techniques prior to dielectric deposition. There are standard process in Si technology is wet chemical etching in hydrofluridic acid (HF) to remove the native oxide and initial impurities. Unfortunately, this procedure does not provide much satisfactory outcome in the case of SiC as a base material. Many methods are incorporated to clean the SiC surface. The most common method is UV light cleaning, which has a sufficient energy to break carbon clusters that are present on the SiC surface.

Some basic features of gate dielectric, which can be implemented on SiC surface, are as follows

1. The value of dielectric constant (k) must have enough high that may be used for long time of year of scaling.
2. The interface of dielectric layer with SiC surface should thermally stable.
3. It must have a sufficient barrier height and band offset with SiC surface so carrier chare injection into its band can be minimize.
4. It should be compatible with processing technology.
5. It must for good and stable electrical interface with SiC surface.

3. Dielectric breakdown field

A capability to sustain a high electric field without any failure is known a dielectric strength. The dielectric breakdown (E_{BR}) is the maximum limit of electric field that dielectric can tolerate under the influence of high supply voltage. In general dielectric field can be defined as

$$E_{BR} = \frac{V_{BR}}{d} \tag{1}$$

Where V_{BR} is the breakdown voltage and d is the dielectric thickness. Dielectric strength is the inherent phenomenon of dielectric material and it mainly depends on structural properties. In the development of dielectric material, growth condition (material thickness, voltage ramp speed, critical vacuum, growth/deposition rate) and environmental condition (Temperature, humidity) are very important.

4. Materials chemistry of high K oxides

4.1. Silicon dioxide (SiO_2)

A high quality thin SiO_2 is most popular gate dielectric from the SiC based microelectronics industries to make the fabrication process cost effective. Various oxidation processes has

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been implemented such as dry oxidation, wet oxidation, chemical vapour deposition (CVD), and pyrogenic oxidation in order to achieve the most suitable process to realize the SiC-based MOS structures (Gupta S.K, 2011[a]). This condition produced a lot of effort into the implementation of SiO_2/SiC interface, in the fabrication of MOS transistor. The intricacy of SiO_2/SiC interface, in comparison to the Si based structure, causes severe problems even though the mobility is reduced by 5% of the theoretical value. The best oxide quality is obtained by the means of dry oxidation process performed at temperatures more than 1100 °C. The growth mechanism of oxide on Si substrate is limited by the diffusion of oxygen at SiO_2/Si interface. However, in case of SiC system this diffusion process countenances difficulties because of the presence of C atoms, which are present along with Si atoms. The actual growth mechanism of SiO_2 on SiC surface is not well understood yet. Hypotheses propose migration of free C atoms in almost every direction. The most probable is out-diffusion of CO_2 or CO through the grown silicon oxide but also formation of carbon clusters at the SiO_2/SiC interface and even diffusion of C into bulk SiC are possible. (Song Y., 2004) and his team have proposed a model of the thermal oxide growth on hexagonal SiC in the frame of deal and grove model. The work assumes two competitive processes influencing SiO_2 formation, one is the in-diffusion of oxygen towards the interface and the other one is the out-diffusion of CO. However, by experimental data one cannot prove that some of the carbon atoms do not stay at the interface and form very stable carbon cluster (Kobayashi H. 2003 and Wang S., 2001). Further investigation was also carried out by of thermal oxidation and re-oxidation with different by using different oxygen isotopes, which seems to confirm that unknown carbon structures exist at the interface (Cantin, J.L.2004). Atomic layer deposition (ALD) has proved a potential method for materials deposition (Leskela M., 2002). Using this technique very well controlled growth is possible, almost atomic layer by atomic layer, of the desired species from gaseous precursors. Unluckily, very few publications report efficient SiO_2 deposition using ALD technique on 4H-SiC substrate (Perez I., 2000). (Amy F., 1999) and his co worker has deposited thin Si layer on SiC surface and later thermal oxidation of the Si layer was performed. X-ray photoelectron spectroscopy (XPS) was further employed to study of such an attempt on 6H-SiC and the material formed by overplayed oxidation shows less Si and C related species in comparison with thermally oxidized samples. This method shows a less complex oxidation mechanism by comparing the case. (Avanas'ev V.V., 1997) and his team has performed verity of experiment to characterize the interface properties of SiO_2/SiC. Finally, this research group was investigated the basic mechanism of interface states distribution for SiC system. In such a system the interface traps density may arise from three main sources i.e. graphite-like carbon, carbon clusters and oxide traps. However, a similar type of paper was again presented by the same author in 2005 (Avanas'ev V.V., 1997). He concluded that that during 8 years of intensive studies this complex problem of oxidation and interface properties is still unsolved. At present time also Si and SiO_2 are very useful system, but electric field strength in SiC can reach the values 10 times higher than those observed in case of Si. In case of SiC as base material the potential barrier height between SiO_2 and SiC is even smaller, indicates toward a serious problem. Moreover, SiC based structures can operate at much more higher temperature than that of Si

based structures. Additionally, due to poorer interface properties and low value of dielectric constant of SiO_2 is not seems to be implement in future MOS structures on SiC substrate.

4.2. Hafnium dioxide (HfO_2)

HfO_2 is second most promising dielectric on SiC surface after SiO_2 due to its high dielectric constant and very high breakdown voltage. A good quality and desired thickness can be easily achieved in laboratory that is why HfO_2 based MOS device are seems to me future devices. Pure form of HfO_2, and its silicate are the potential candidate SiO_2 as a gate material in a scaled down MOS technology. A continuous research and development (R&D) on this material is considerably seems to be more advanced compared to other high-k dielectrics (Avanas'ev V.V., 1997; Tanner C. M., 2007). Moreover, K Y Cheong et al has observed a significant improvement in the performance of HfO_2/SiO_2 stack gate dielectric on 4H-SiC surface (Cheong K.Y., 2007). Atomic layer deposition (ALD) is the most advisable and recommended process to deposit HfO_2 (Cho M., 2002). However, large variations in growth rate, dielectric constant, and fixed charge are reported for HfO_2 deposited on silicon substrate. The interface stability is one of the most important issues in the deposition process. When HfO_2 is considered to be deposited on SiC surface, the accurate knowledge of thermal stability at elevated temperatures is a must.

4.3. Titanium dioxide (TiO_2)

Titanium dioxide (TiO_2) is another gate dielectric, which is explained in this chapter. The electronic bandgap energy of this material is relatively small (3.5 eV), but dielectric constant can be varied from 40 to 110. TiO_2 exist in two important phases, Anatase and Rutile, which depends on growth process. Rutile phase of TiO_2 is the thermally stable phase that presents the higher dielectric constant around 80. Other form i.e. Anatase is a thermally unstable phase, which shows a lower dielectric constant. The Anatase form can be transforming to Rutile phase by annealing the deposited material at temperatures more than 600° C. A high leakage current values and higher interface density are the most drawback of this material, which is unacceptable in the fabrication of transistor structure. In order to minimize these problems it is interesting to employ a stack layer of thin SiO_2 and TiO_2 on SiC substrate. In this way, the interface quality can be improved and the other problems may be minimized, turning this material viable and very attractive to substitute the current dielectric material on SiC surface. Variable-energy positron annihilation spectroscopy (VEPAS) was employed to investigate the atomic scale structure of TiO_2/SiO_2T gate dielectric stack on 4H-SiC surface (Coleman P.G., 2007). In this study a vacancy type defects was observed. Thin film of TiO_2 film can be deposited with many techniques likes chemical vapour deposition (CVD), RF sputtering, e-beam evaporation, metal-organic chemical vapour deposition (MOCVD) and so on. The dielectric constant of TiO_2 was reported to be 31, which is stable in the frequency range from 100 Hz to 1 MH. The critical breakdown field is 3 MV/cm. TiO_2 is seems to of be very promising material in the development of gas sensors particularly Hydrogen sensors (Weng M-H, 2006; Shafiei M., 2008)

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4.4. Aluminium oxide (Al_2O_3)

Aluminium oxide (Al_2O_3) is another gate dielectric, which has proven the demanded gate material SiC MOS structures. This material has a broad scope in semiconductor industry and the single crystal wafer of Al_2O_3 is commercially available. Crystalline form of Al_2O_3 is known as called sapphire, or α-Al_2O_3, which has the rhombohedral symmetry. The application of sapphire as passivation material for SiC is very hard due to crystalline mismatch and polycrystalline Al_2O_3 may cause large leakage trough grain boundaries of material. This material belongs to the family of wide bandgap (8.8 eV) and having the potential barrier of 2.8 eV with Si conduction band. The calculated conduction band offset for 4H-SiC system is about 1 eV, which is smaller than that of the measured on Si system. But this value is high enough to effectively prevent carrier injection at interface. However, amorphous form of Al_2O_3 seems to be an attractive candidate as a gate dielectric for SiC based structures. This material may be deposited by many different techniques such as sputtering (Jin p., 2002), plasma deposition (Werbowy A., 2000), Atomic layer deposition LD (Gao, K.Y. 2005) and so on with the suitable gaseous inlet of the precursors. ALD is seems to have the largest interest for fabrication of devices. K.Y. Gao et al has demonstrated a very good result and explained very nicely (Gao, K.Y. 2005). Post deposition annealing of Al_2O_3 in presence of H_2 environment at 500°C demonstrates a effective reduction in interface states density in the mid bandgap of the 6H-SiC. Worldwide numbers of researchers (Avice M. 2007; She J., 2000) are intensively working to explore the Al2O3/SiC interface properties. As the result the first 4H-SiC MESFET with Al2O3 as a gate dielectric was successfully demonstrated (Hino S., 2007).

4.5. Aluminium nitride (AlN)

Aluminium nitride (AlN) is also one of the very promising gate dielectric materials, which can be associated with SiC system. Its lower bandgap of 6 eV in comparison with Al_2O_3 or SiO_2 might be disappointing, but a lattice mismatch to SiC of only 1%, almost the same thermal expansion up to 1000 °C and a high dielectric constant are more encouraging. Generally, AlN is used as a buffer layer prior to grow GaN structures on SiC substrates. This is the basic cause for largest number of research associated with the epitaxial growth at very high temperatures. Low temperature deposition is also possible over verity of substrate like other techniques that are of interest for low temperature deposition of passivation layers like atomic layer deposition, RF- sputtering pulsed laser deposition. There are not so many studies were focused on electrical characterization of AlN layers on SiC surface. Some results, however, shows satisfactory insulating properties for mono-crystalline AlN with acceptable leakage currents of the order of 10-9 A/cm^2 and a breakdown field of around 4 MV/cm (Onojima N., 2002). AlN/SiC interface do not shows the promising characteristics because of charge trapping at interface. However ozone cleaning and HCl pre-treatment of SiC surface shows a tremendous improvement of the properties of dielectric layer and provides interface quality sufficient for the fabrication of MOS structures. Introduction of thin SiO_2 as a buffer layer between SiC and AlN is an additional barrier to prevent electron injection from semiconductor to dielectric, which may further decrease leakage current. This type of stack

layer of AlN/SiO_2/6H-SiC was presented in (Biserica O., 2000) and reveals a low charging effect when 100 Å SiO_2 layer was used.

5. Depositions method

SiO_2 can be thermally grown by Thermal oxidation and this growth processes have the great advantage. In similar way, high *K* dielectric must be grown/deposited. It is well known that deposited oxides are never as good as compared to grown one.

5.1. Physical Vapour Deposition (PVD)

In the process of PVD based dielectric material deposition, e-Beam evaporation and Sputtering have been intensively used. The basis different between these two methods is the step coverage: e-Beam shows negligible step coverage while Sputtering produce a film with good step coverage as shown in Figure 3. Normally pure metal like Ti, Pt, Au, Ni, Al are deposited by e-beam evaporation method followed by an oxidation at suitable temperature.

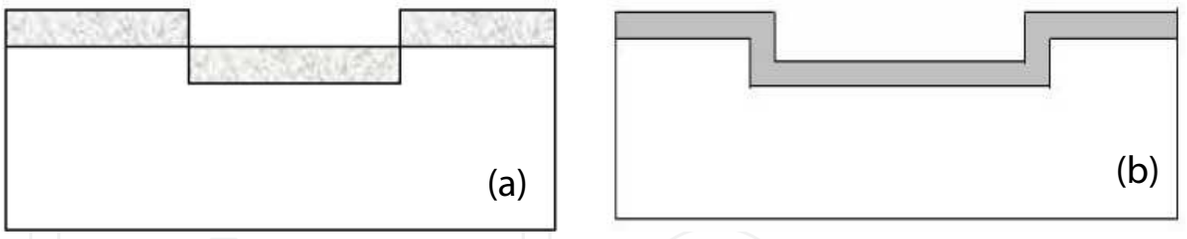

Figure 3. Schematic showing step coverage (a) poor step coverage using e-Beam method (b) good step coverage using Sputtering

In the e-beam evaporation method, a focused electron beam is used to heat a metal target to evaporate. In the high vacuum chamber, the evaporated metal radiates out from the metal target of which some portion is deposited on the mounted substrate. Generally, the target is placed at bottom and substrate is placed at the top of the vacuum chamber as shown in Figure 4. A method for producing highly pure, thin oxides is to evaporate metal by electron beam (e-beam) which is highly controllable to small thickness, and to oxidize the deposited metal by ozone or UV assisted oxidation. The advantage of this process is that it produces

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less damage than oxide sputtering and should produce the purest oxide. But it is not an exact method for commercial production.

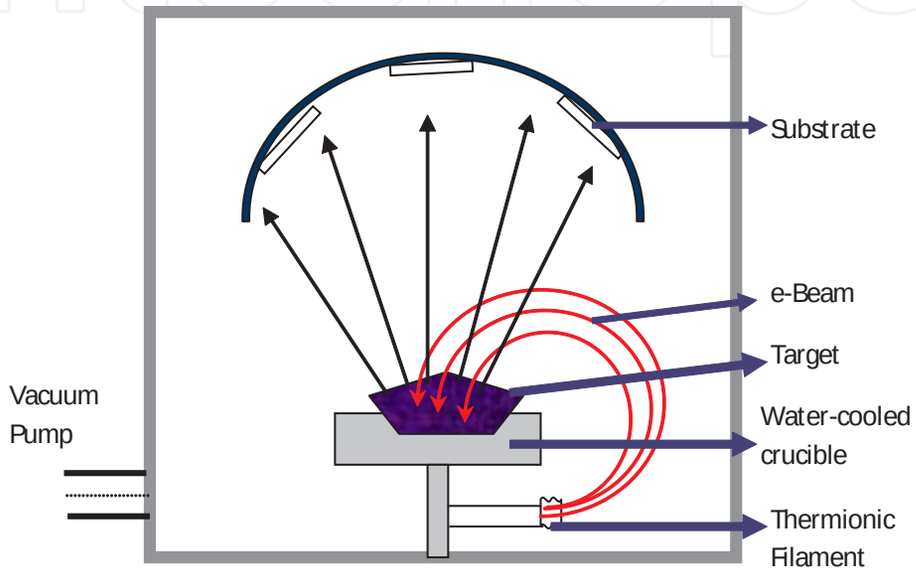

Figure 4. Schematic diagram of e-Beam evaporation system

Sputtering is generally used to deposit refractory materials, compound and alloys, which are difficult to evaporate by e-Beam method. Sputtering exists in the category of the Physical Vapor Deposition (PVD) process, in which metals are removed from the solid cathode. The whole process is carried out by bombarding the cathode with positive ions emitted from rare gas discharge. When ions with high kinetic energy are incident on the cathode, the subsequent collision knocks loose or sputters atoms from materials. The schematic of Sputtering system is given in Figure 5. Its advantage is that it is broadly available and can produce pure oxides. Its disadvantages are that oxides are insulators so sputtered oxides tend to have plasma-induced damage. Also, PVD methods deposit in line of sight, so they do not give good coverage.

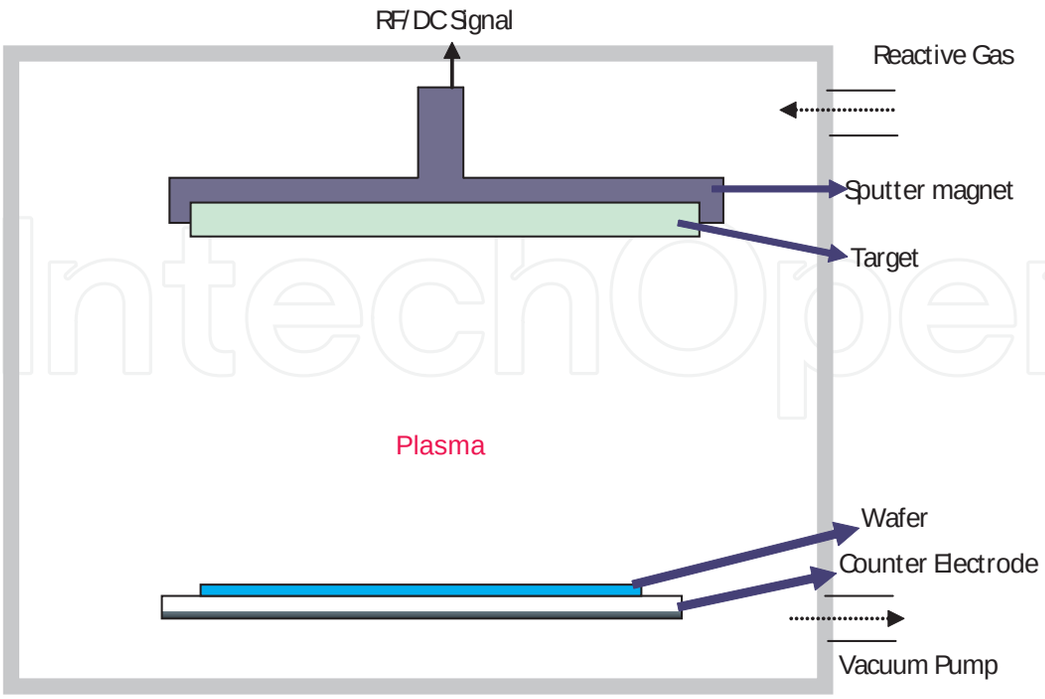

Figure 5. Schematic diagram of sputtering system

5.2. Chemical Vapour Deposition (CVD)

Chemical vapour deposition (CVD) and Atomic Layer Deposition (ALD) are preferred industrial method to deposit gate dielectrics. CVD involves the formation of a thin solid gate dielectric on a desired substrate by a chemical reaction of vapour-phase precursors. In CVD process generally a volatile metal compound as a precursor is introduced into the process chamber/tube and oxidized during deposition onto the desired substrate. CVD is widely used in the electronics industry for most of insulator deposition. It gives a conformal coverage even though a three dimension shapes because it is not just line of sight. The other major advantage is that the deposition rate is controllable over a wide range from very slow to high. It can thus be distinguished from physical vapour deposition (PVD) processes, such as evaporation and reactive sputtering, which involve the adsorption of atomic or molecular species on the substrate. The chemical reactions of precursor species occur both in the gas phase and on the substrate. Reactions can be promoted or initiated by heat (thermal CVD), higher frequency radiation such as UV (photo-assisted CVD) or plasma (plasma-enhanced CVD). Figure 6 shows the schematic diagram of horizontal CVD reactor.

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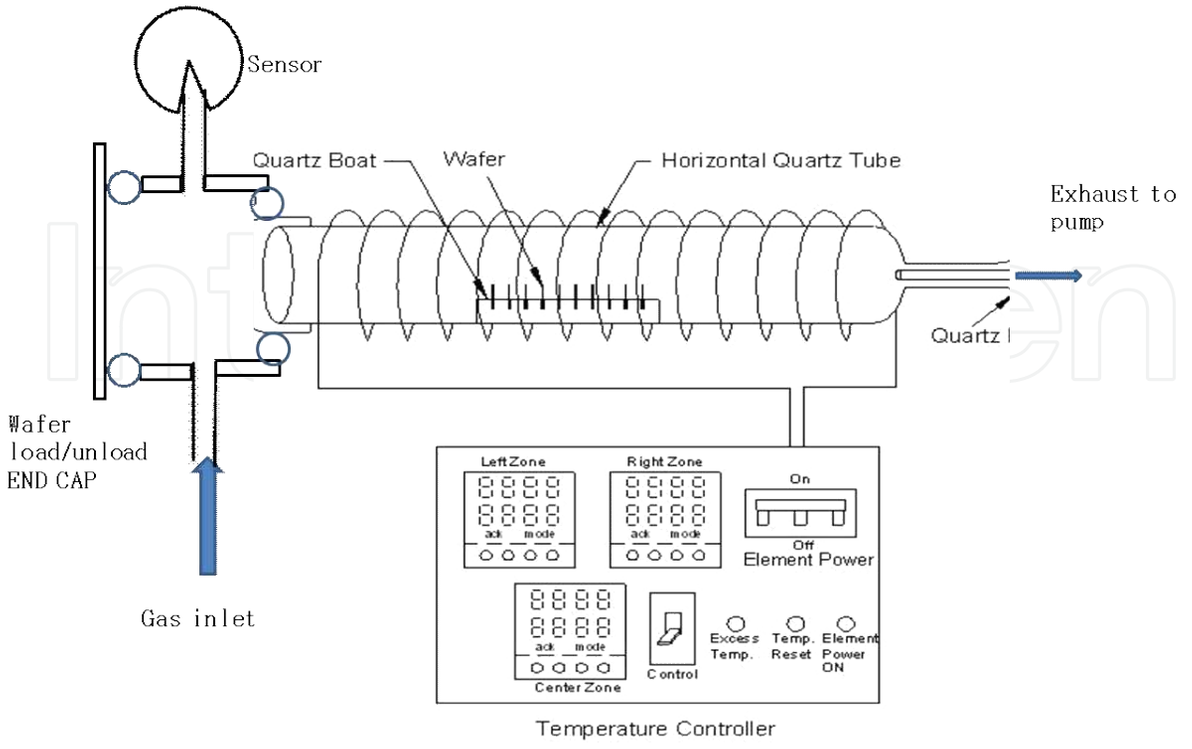

Figure 6. Schematic diagram of CVD system

5.3. Atomic Layer Deposition (ALD)

ALD was developed to recover the shortcoming, which arise due to CVD process. ALD produce a highly conformal, pinhole-free highly insulating film. It has many advantages over CVD method like able to grow the thinnest films even though all deposition methods, and the most conformal films even into deep trenches. Atomic layer deposition is a method of cyclic deposition and oxidation. In this process, the desired surface is exposed to the suitable precursor, which is further absorbed as a saturating monolayer. The rest of the precursor is then purged from the tube/chamber by passing Ar/N_2 gas. A pulse of oxidant such as $H2O_2$, ozone or H_2O, is then introduced in the chamber/tube, which must then fully oxidize the adsorbed layer to the oxide and a volatile by-product. The excess oxidant is then purged by a pulse of Ar, and the cycle is repeated. Figure 7 represent a cyclic process of ADL press. ZrO2 and HfO2 was shown as example in figure7. Slow growth rate is a major disadvantage of this process but some time it is very useful to control the thickness of films. It has been seemed that some impurities like Cl, C and H also introduce in the film during deposition process, depending on used precursor. A compatible annealing methodology is needed to remove such type of impurity and densify the deposited oxides films. ALD is an excellent method for producing many high *K* oxides. An addition of an oxide layer, which is usually much less than an atomic layer thick in each and every cycle of ALD process adds an oxide

layer, justify its nomenclature. ALD is usually carried out on a native oxide (SiO_2) surface followed by ozone cleaning of SiC surface. This limits the crucial lowest EOT that ALD can presently attain. H-terminated surface, which arises by the HF-cleaning treatment procedure, is not favorable surface. It was observed that ALD of HfO_2 and ZrO_2 from chloride or other organic precursors do not easily nucleate on HF treated SiC surface.

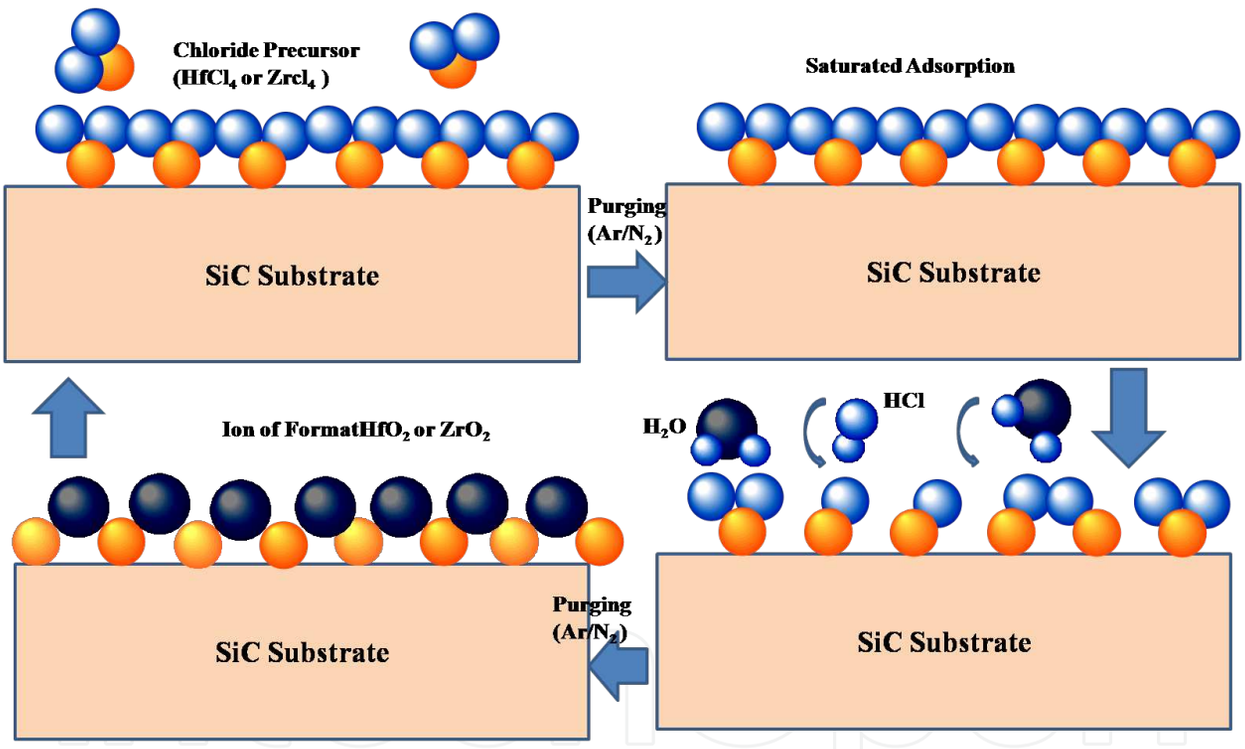

Figure 7. Schematic of the cyclic process of Atomic layer deposition process

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6. Electrical behavior of dielectric material

The quality of dielectric material can be electrically characterized by current-voltage (I-V) and capacitance-voltage (C-V) technique. In order to employ the above techniques, the grown/deposited layers on SiC should be sandwiched between two metal electrodes. A different type of current conduction mechanisms were observed and presented in this section, based on dielectric thickness and applied electric field across electrode. In this section SiO_2 was considered as a gate dielectric on SiC surface. Gupta, S.K. and his research group are continuously working to investigate the current conduction mechanism and charge management of gate dielectric material and SiC system (Gupta, S.K. 2010[a]; Gupta, S.K. 2010[b]; Gupta, S.K. 2011[b] ; Gupta, S.K. 2012).

6.1. Direct tunneling

Schrödinger equation describes that there is a finite probability that a particle can tunnel through a non-infinite potential barrier. As the width of potential barrier decreases, the probability of particles (electrons and holes) penetrating through the barrier by quantum-mechanical tunneling, rises exponentially. In sufficiently thin oxides (below 5 nm), direct quantum mechanical tunneling through the potential barrier can occur. This quantum-mechanical phenomenon can easily be understood by recognizing that the electron or hole wave function cannot immediately stop at the barrier (SiO_2/4H-SiC interface), but rather it decreases exponentially into the barrier with a slope determined by the barrier height. If the potential barrier is very thin, there is non-zero amplitude of the wave function remaining at the end of the barrier means a non-zero probability for the electron or hole to penetrate the barrier. It is well known that the barrier heights of hole tunneling in the SiO_2 layer from the metal gate and from the Si substrate are higher than the corresponding values for electrons, moreover, the hole mobility in SiO_2 is lower than the electron mobility, therefore the main contribution to conduction in SiO_2 is due to electrons. Since in n-type 4H-SiC mobility of electrons is much higher than that of hole, therefore, the described conduction mechanism in case of Si can be fully applied to 4H-SiC. The metal/SiO_2 and SiO_2/4H-SiC interfaces are at the position X = 0 and X = t_{oxt} respectively, in our notation. V_{oxt}= V (0)-V (t_{oxt}) is the voltage drop in the oxide layer, where V(x) is the potential in the oxide at position X.

At low gate voltages (figure 8 (a)), electrons can move from the gate metal through SiO_2 to the 4H-SiC substrate only by tunneling directly the entire oxide thickness i.e. by tunneling the trapezoidal potential barrier between gate and 4H-SiC substrate. The quantum-mechanical phenomenon of a trapezoidal barrier tunneling is termed as direct tunneling effect. It contributes significantly to the conduction through the SiO_2 only in ultra thin oxide layers (t_{oxt}< 5 nm). At higher gate voltage (figure 8 (b)), the band bending causes the potential barrier shape to become triangular. Electron tunnel from the gate to the SiO_2 conduction band, through the triangular potential barrier and finally, moves in the SiO_2 conduction band to the 4H-SiC substrate. The conduction mechanism

through a triangular potential is called Fowler-Nordheim (F-N) tunneling, which is described in next section.

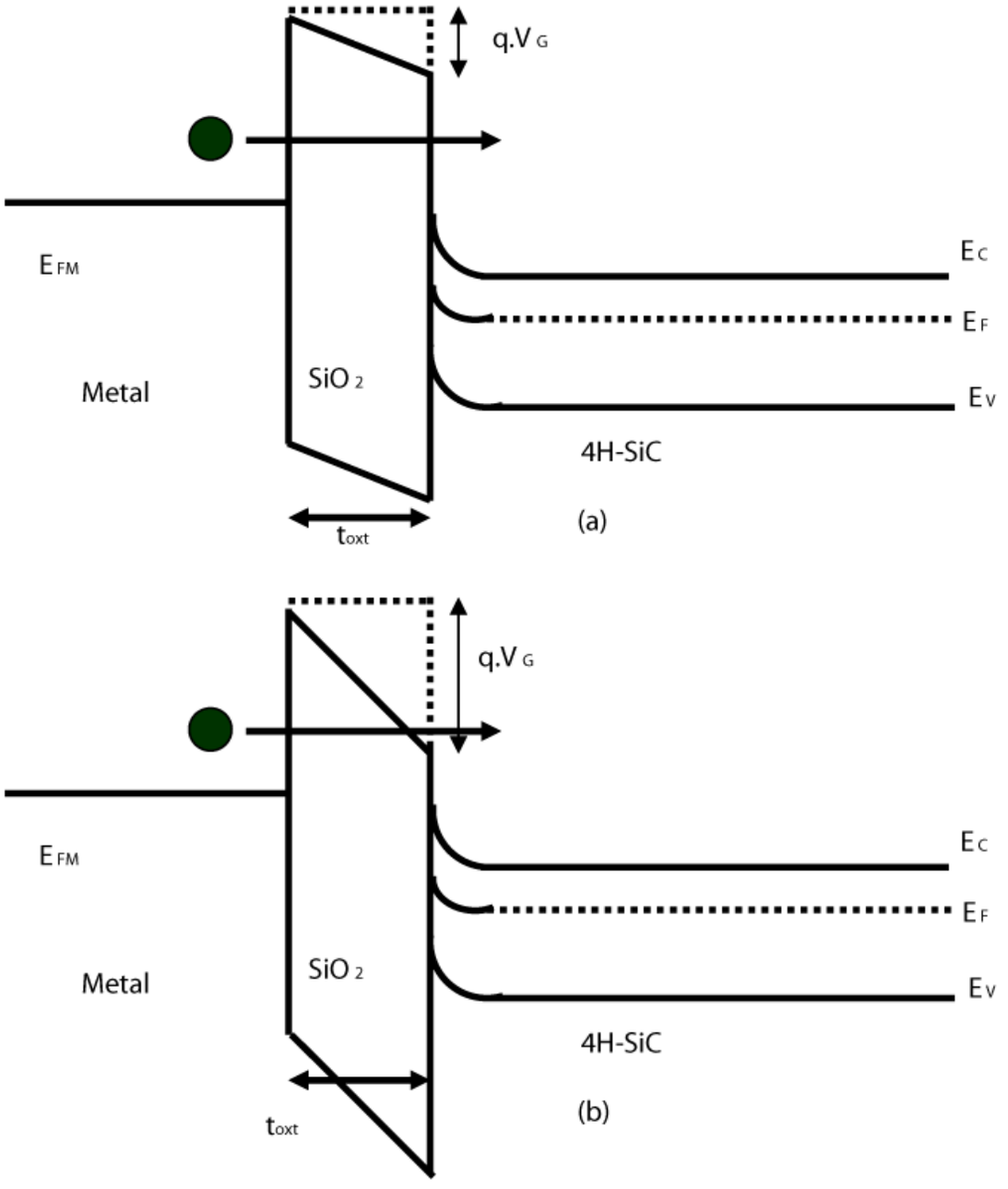

Figure 8. a) The band diagram of negative gate bias the closed circle represents one electron injected from gate to the SiC conduction band through trapezoidal energy barrier (b) tunneling across triangular energy barrier

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6.2. Fowler-Nordheim tunneling

Fowler-Nordheim tunneling in metal oxide semiconductor (MOS) can be observed when the oxide thickness will be less than 50 nm, the oxide potential barrier is usually assumed to be a triangular one, free of charge gate insulator. As a consequence, when we apply a uniform electric field across the MOS structure and thickness of the potential barrier at the semiconductor Fermi level and the potential $\phi(x)$, at the distance x from semiconductor/oxide interface vary linearly with the applied voltage.

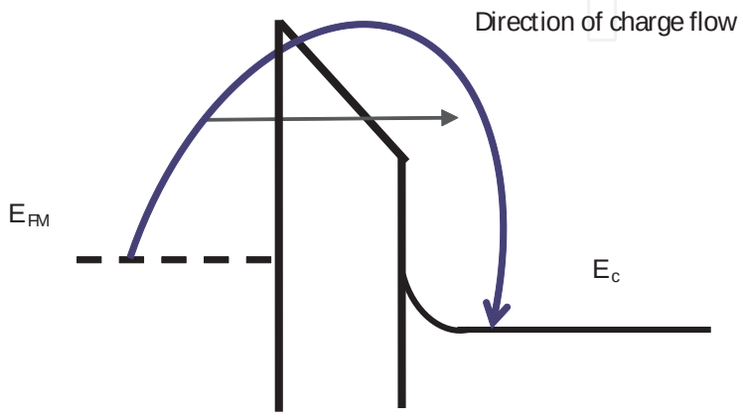

Figure 9. Energy band diagram for F-N tunneling

The insulating region is separated by an energy barrier with barrier height $q\phi_B$, measured from the Fermi energy of metal to the conduction band edge of the insulating layer. The distribution functions at both sides of the barrier are indicated as in the figure 9. In the derivation of current density (J) as a function of applied voltage we have to consider some assumptions like effective-mass approximation, parabolic bands and conservation of parallel momentum (Chung, G. Y., 2001). The net tunneling current density from metal to semiconductor can be written as the net difference between current flowing from the metal region to the semiconductor region and *vice versa.* This expression for current density is usually written as an integral over the product of two independent parts, which only depend on the energy perpendicular to the interface: the transmission coefficient T (*E*) and the supply function N (*E*).

$$J = \frac{4\pi m_{eff} q}{h^3} \int_{E_{\min}}^{E_{\max}} T(E) N(E) dE \tag{2}$$

This expression is known as Tsu-Esaki formula. This model has been proposed by Duke and was used by Tsu and Esaki for the modeling of tunneling current in resonant tunneling devices. The calculation of current density requires not only the knowledge of the energy dependent transfer coefficient, but also the energy dependent electron probability (supply

function). Using theTsu-Esaki formula for current density the Fowler-Nordheim formula can be derived as:

$$J\alpha AE^{2}_{diel}\exp\left(-\frac{B}{E_{diel}}\right) \tag{3}$$

Where,E_{diel} denotes the electric field in dielectric, A and B are constants dependent on barrier configuration for oxide layer separated by metal and semiconductor, the constants *A* and *B* are given by:

$$A=\frac{q^{3}m_{\text{eff}}}{8\pi m_{\text{diel}}hq\Phi_{\text{B}}}\quad B=\frac{4\sqrt{2m_{\text{diel}}(q\Phi_{\text{B}})^{3}}}{3\hbar q} \tag{4}$$

Where, ϕ_B is the height of the potential barrier measured from the Fermi level of metal to the conduction band in the dielectric, m_{iff} is the effective electron mass in electrode material and m_{diel} is the effective electron mass in the dielectric material. This physical model has been directly applied to in order to establish the validation of Fowler-Nordheim tunneling with the oxide thickness limit.

6.3. Schottky emission

The Schottky emission is an electrode limited process occurring across the interface between a semiconductor (or metal) and an insulating film as a result of barrier lowering due to the applied electric field and the image force as shown in figure 10. Normally, the S-E current conduction process is an electrode-limited conductivity that depends strongly on the barrier between the metal and insulator and has the proclivity to occur for insulators with fewer defects.

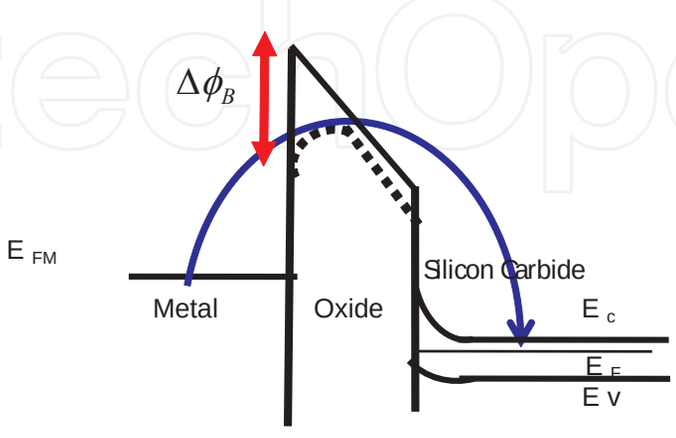

Figure 10. Energy band diagram for Schottky emission in metal oxide silicon carbide (MOSiC) structure

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Schottky emission from the metal cathode or from the oxide states is assumed to be the limiting mechanism for filling or emptying the oxide traps. For the emission from a semiconductor the Schottky emission current conduction is given by (Chang S.T., 1984)

$$J\alpha A^{*}T^{2}E\exp\left[\frac{-q\left(\varphi_{B}-\sqrt{qE/4\pi\varepsilon_{i}}\right)}{kT}\right] \tag{5}$$

Where, J is the current density; A* iseffective Richardson constant; T, the absolute temperature; q, the electronic charge; ϕ_B, the potential barrier at the metal and insulator interface; E, electric field in insulator; ε_i, dielectric constant; and k, the Boltzmann constant.

The potential barrier lowering in the MOSiC structures caused by image forces as shown in figure 10 is often neglected in the calculation of the tunneling current, based on an argument that for large barriers in the case of semiconductor and insulator the image-force lowering of the barrier is very small, and this was supported by experimental evidence at the time. In case of very thin oxides, however, this might not be the case, and the barrier lowering can have an impact on the calculation of the tunneling current.

The potential barrier lowered with respect to ideal structure has been termed to an effective trapezoidal barrier in order to account for image force effect. The image-barrier height lowering can be described by:

$$\Delta\varphi_{B}=\sqrt{\frac{qE_{m}}{4\pi\varepsilon_{0}\varepsilon_{r}}} \tag{6}$$

Where, ΔΦBis the image-barrier height lowering, and $E_m$is the applied electric field at the metal-semiconductor interface, ε_0 is permittivity of vacuum and ε_r relative dielectric constant of insulating layer.

6.4. Poole-Frenkel conduction

6.4.1. Classical theory of Poole-Frenkel conduction

In ideal metal oxide semiconductor diode, it is assumed that current conduction through the insulator is zero. Real insulator, however, show the current conduction mechanism which may the function of thickness of the insulator or applied electric field or both. In the classical Poole-Frenkel conduction model effective mechanism can be analyzed by the analogue of Schottky emission (Wright P. J., 1989) where as transport of charge carriers is governed by trapping and de-trapping in the forbidden band gap of an insulator, which reduces the barrier on one side of the trap. At zero electric field amount of free charge carriers can be determined by the trapped ionization energy (qϕ), which is the amount of energy required for the trapped electron to escape the influence of the positive nucleus of the trapping center when no field is applied. When electric field is applied, the ionization energy of trapping center decreases in the direction of

applied electric field by the amount of $\Delta\phi_B=\beta E^{1/2}$ as shown in figure 11. As the electric field increases, the potential barrier decreases on the right side of the trap, making it easier for the electron to vacate the trap by thermal emission and enter the quasi-conduction band of the crowd material. Quasi-conduction band edge is the energy at which the electron is just free from the influence of the positive nucleus. The term quasi-conduction is generally used in amorphous solid, which have no real structure. In MOSiC structure, of course, electron would escape from gate metal to the conduction band of semiconductor through the insulator. Since we will deal here with the P-F mechanism in amorphous dielectrics, we will refer to its quasi-conduction band. For the Poole-Frenkel conduction mechanism to occur the trap must be neutral when filled with an electron, and positively charged when the electron is emitted, the interaction between positively charged trap and electron giving rise to the Coulombic barrier. On the other hand, a neutral trap that is, a trap which is neutral when empty and charged when filled will not show the Poole-Frenkel effect.

According to the Poole-Frenkel model, the magnitude of the reduction of trap barrier height due to the applied electric field as shown in figure 11 is given by

$$\Delta q\varphi = \beta\sqrt{E} \tag{7}$$

Where β is Poole-Frenkel constant, is given by

$$\beta = \sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}} \tag{8}$$

Finally, quasi conduction band edge is lowered or in other words, the trap barrier height is reduced due to the applied electric field. From Equation 8, it is clear that β is a material parameter, depending on the dielectric constant. Therefore, materials with larger dielectric constants will be less sensitive to the field-induced trap barrier lowering effect in the P-F conduction.

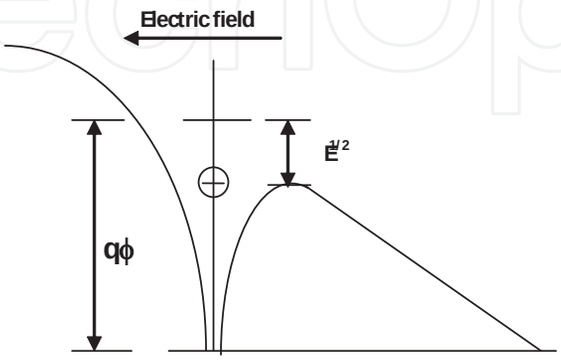

Figure 11. Figure 11.Coulombic potential distribution in the presence of applied electric field showing the Poole-Frenkel effect

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6.4.2. Poole-Frenkelconduction in MOSiC structure

P-F conduction mechanism is most often observed in amorphous materials, particularly dielectrics, because of the relatively large number of defect centers present in the energy gap. In fact, the particular host material, where the defects reside, can basically be viewed as acting only as a medium for localized defect states. Transformation of charge is therefore, mainly between localized electronic states (Lenzlinger, M., 1969). Thus it is reasonable to expect the P-F effect to occur, at least to some extent, in any dielectric. The main physical properties effecting the current conduction in different dielectrics are the relative dielectric constant, ε_r, and the ionization potential. The P-F conduction effect has been observed in many dielectric materials, which are used in microelectronic device fabrication. For example, in Si_3N_4 films, the dominating current transport mechanism is the P-F conduction. The thin films with high dielectric constants, such as Ta_2O_5 and $BaSrTiO_3$, which hold great potential for use as the gate oxide in DRAMs, have shown that current conduction in these materials is bulk-limited which is governed by the P-F conduction. Currently, one of the most important dielectric materials used in microelectronics is SiO_2, which can be easily thermally grown on SiC substrate.

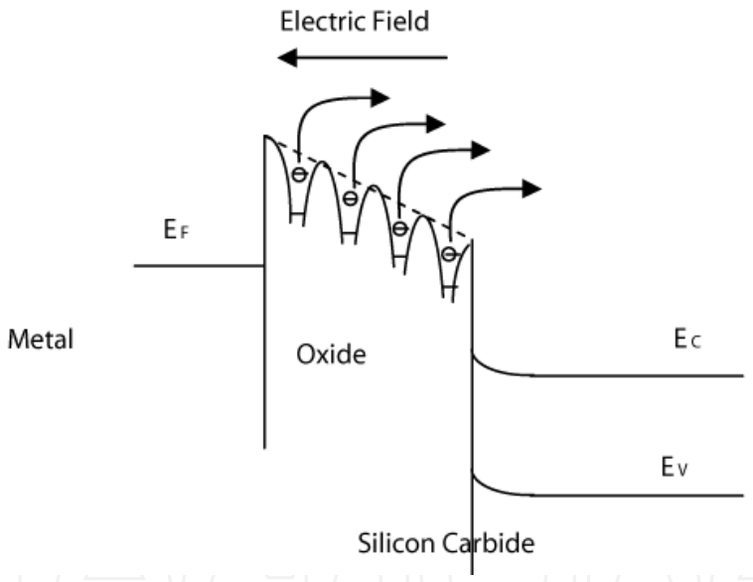

Figure 12. Energy band diagram for Poole-Frenkel conduction in MOSiC structure having multiple Coulombic traps

Figure 12 shows the P-F conduction in MOSiC structure that is basically a parallel plate capacitor. The trapezoidal band diagram of MOSiC structure drawn for the silicon dioxide layer is replaced in figure 11 by a random distribution of Coulombic traps in the vicinity of the quasi-conduction band edge as shown in figure 12. The dashed line indicates the quasi-conduction band of the oxide in the absence of any traps. When an electric field is applied as shown, the trapped electrons can enter the oxide's quasi-conduction band by the Poole-Frenkel mechanism and flow from the oxide across the SiC/SiO_2 interface into the silicon carbide conduction band edge. The Poole-Frenkel effect can be observed at the high electric field. The standard quantitative equation for P-F conduction is

$$J \alpha E \exp\left[\frac{-q\left(\varphi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right] \tag{9}$$

Where, J is the current density; T, the absolute temperature; q, the electronic charge; ϕ_B, the potential barrier at metal and the insulator interface; E, electric field in insulator; ε_i, dielectric constant; and k, the Boltzmann constant.

7. Charge management in SiO_2 on 4H-SiC

7.1. Origin and basic theory of oxide charges in SiO_2

In the prospects of technological issues on Silicon carbide based MOS system, the almost similar consideration has been adopted to investigate the charge management as silicon based MOS system. In this section, the oxide charges associated with Ni/SiO_2/4H-SiC systems have been examined with varying oxide thickness. There are general four types of charges associated with the SiO_2-Si system as shown in figure 13. They are fixed oxide charge, mobile oxide charge, oxide trappedcharge and interface trapped charge (Afanas'ev, V, V., 1996 and Schroder, D. K., 2006). The basic origin of all oxide charges and experimental methods in order to calculate these charge are presented here one by one.

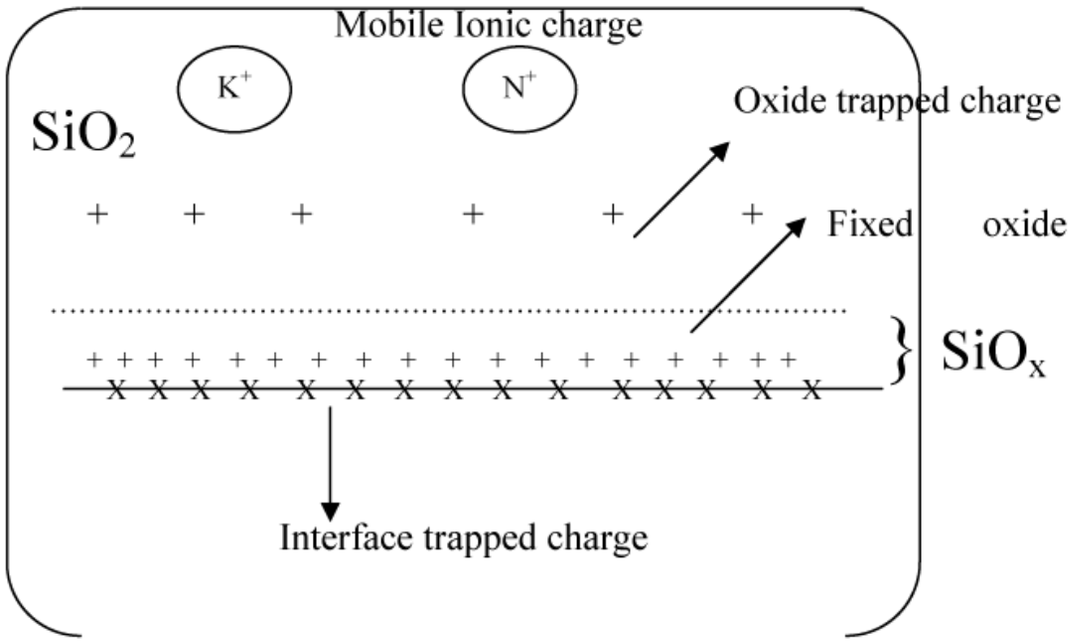

Figure 13. Allocation of different oxide charges associated with SiC MOS system

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7.2. Fixed oxide charges (Q_{fix})

These are positive or negative charges located near the SiO_2/4H-SiC (less than 25 Å from the interface) interface due to primarily structural defects in the oxide layer. The origin of fixed charge density is related to the oxidation process, oxidation ambient and temperature, cooling condition of the furnace and also on polytypes of Silicon carbide. Q_{fix} highly depends on the final oxidation temperature. For higher oxidation temperature, a lower Q_{fix}will be observed. However, if it is not permissible to oxidize the wafer at high temperatures, it is also possible to reduce the $Q_{fix}$by annealing the oxidized wafer in a nitrogen or argon ambient after oxidation.

The fixed charge can be determined by comparing the flatband voltage shift of an experimental C–V curve with a theoretical curve, provided by the oxide thickness and work function differences of metal and 4H-SiC. Fixed charge related to the flatband voltage is given by:

$$Q_{fix} = \left(\varphi_{ms} - V_{FB}\right)C_{oxt} \tag{10}$$

Where, ϕ_{MS} is the difference of work function between metal and semiconductor, which must be known in order to determine the value of $Q_{fix.}$

7.3. Oxide trapped charge (Q_{oxt})

This oxide charge may be positive or negative due to the hole and electron trapped in the bulk of the oxide. These trapping may results from ionizing radiation, avalanche injection, Fowler-Nordheim tunneling or other similar processes. Unlike the fixed charge, this chare can also be reduced by annealing treatment. Oxide charges can be trapped in the oxide during device operation, even if not introduced during device fabrication. During the device operation electrons and/or holes can be injected from the substrate or from the gate material. Energetic radiation also produces electron-hole pairs in the oxide and some of these electrons and/or holes are subsequently trapped in the oxide. The oxide trapped charge is usually not located at the oxide/4H-SiC, but is distributed through the oxide. The distribution of Q_{oxt}must be known for proper interpretation of C–V curves. Oxide trapped charge can be determined by:

$$Q_{oxt} = -V_{FB}.C_{oxt} \tag{11}$$

Where, the symbols have their usual meaning.

7.4. Mobile oxide charge (Q_{mob})

The origin of this oxide charge is due to the presence of ionic impurities such as Na^+, Li^+, K^+ and possible H^+ in the oxide films. These ionic impurities may be resulted from the ambient, which, was used for thermal oxidation. Negative ions and heavy metals ions may also contribute to this

charge. Sodium ion is the dominant contaminant. The other ionic impurities like potassium may be introduced during chemical-mechanical polishing. For mobile charge calculation the measurement temperature must be sufficient high so the charge to be mobile. Typically, the devices are heated to 200^0C to 300^0C. A gate bias, to produce an oxide field of around 10^6 V/cm is applied for a sufficiently long time in order to drift charge from interface. The mobile charge can be determined from the flatband voltage shift, according to the equation:

$$Q_{mob} = -\Delta V_{FB}.C_{oxt} \tag{12}$$

7.5. Interface trap level density (D_{it})

These are positive or negative charges, due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond breaking processes (*e.g.*, hot electrons). The interface trapped charge is located at the SiC–SiO_2 interface. Unlike the fixed charge or trapped charge, interface trapped charge is in electrical communication with the underlying SiC. Interface traps can be charged or discharged, depending on the surface potential.This charge type has been also called surface states, fast statesand interface states and so on.

There are three main approaches to investigate the problem of interface state.

1. By the comparison of measured high frequency capacitance with a theoretical capacitance with no interface traps.
2. By the comparison of measured low frequency capacitance with a theoretical capacitance with no interface traps.
3. By the comparison of measured high frequency capacitance with measured low frequency capacitance.

Interface trap change their charges sate depending on whether they are filled or empty. Acceptor interface traps are negative when filled, and neutral when empty, whereas donor interface traps are neutral when filled and positive when empty. Both types of interface traps may exist, perhaps simultaneously in the same device.

$$D_{it} = \frac{1}{q}\left[\left\{\frac{1}{C_{LF}} - \frac{1}{C_{oxt}}\right\}^{-1} - \left\{\frac{1}{C_{HF}} - \frac{1}{C_{oxt}}\right\}^{-1}\right] \tag{13}$$

8. The Metal Oxide Silicon Carbide (MOSiC) band diagram

8.1. An ideal band diagram of MOSiC capacitor

In accord to the ideal case, the value of interface traps (Q_{it}) should be zero. The relationship of surface potential to the gate voltage having interface traps zero is known as an ideal MOSiC capacitor as shown in figure 14.

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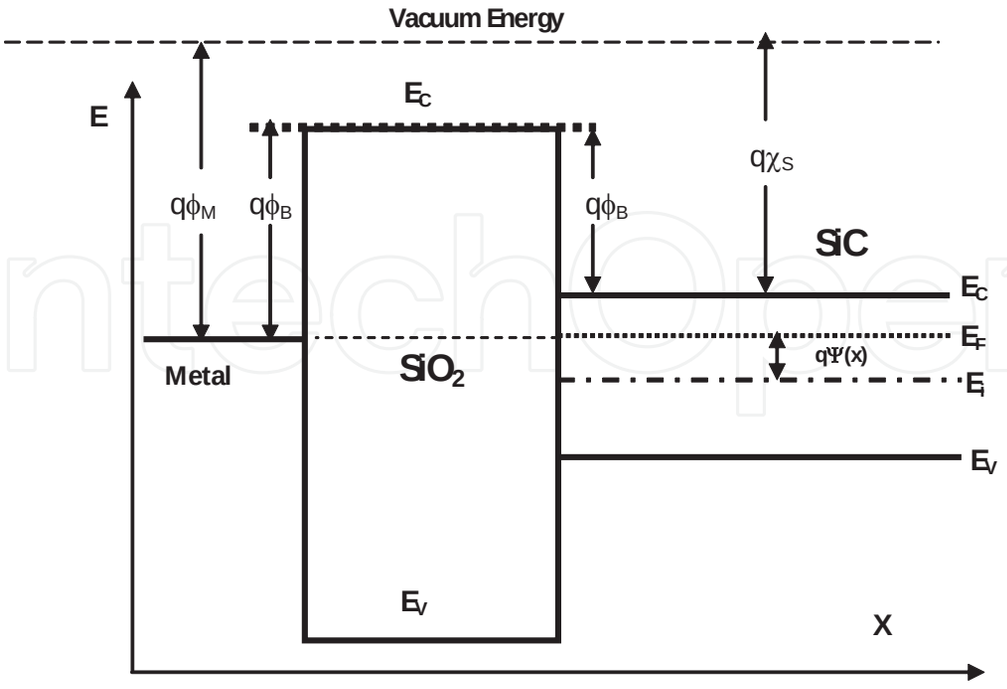

Figure 14. Flatband energy band diagram of an ideal MOSiC structure

An ideal MOS diode is defined as follows:

1. The energy difference between the metal work-functionand the semiconductor work-function is zero. Under this condition, the Fermi levels of the metal and semiconductor are aligned at equilibrium. This is equivalent with no charge flowing when they are put in contact.

2. The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with the equal but with opposite sign on the metal surface adjacent to the insulator.

3. The semiconductor Fermi level is constant from the SiC-bulk toward the interface. It is determine by the shallow doping (usually nitrogen N).

4. There are no traps at the metal/SiO_2 or SiO_2/4H-SiC interface. The SiO_2 is free of defects (structural defects, impurities, vacancies, etc.). The only allowed charge in the structure exists in the semiconductor and, with opposite sign in the metal.

5. The resistivity of the insulator (oxide) is infinity so that there are no carrier transports under Bias conduction.

8.2. The real MOSiC capacitor

In real, the oxides of any MOS capacitor features a number of charges for example fixed oxide charge, mobile charge, oxide trap charge and interface trap level density. There is also a non-zero difference between the gate metal and semiconductor work function. The electric

fields produced are compensated by a corresponding charge of the semiconductor. Since the ideal dielectric does not conduct any current, the semiconductor Fermi level remains flats. However, the bands are bending in compliance with the applied and created fields. To compensate this bending and to reach the flatband situation (Ψ=0), a gate bias has to be applied. This bias will shift the C-V characteristics of the MOS capacitor. The flatband (Ψ=0) situation is reached, when the flatband bias V_{FB} is applied:

$$V_{FB} = \varphi_{ms} - \frac{Q_{oxt} + Q_{fit} + Q_{it}(\psi_S)\Big|_{\psi_S=0}}{C_{oxt}} \tag{14}$$

The effective charge density at the interface N_{eff} is obtained from a C-V measurement and has the form:

$$N_{eff} = V_{eff} \times C_{oxt} = -(V_{FB} - \varphi_{ms}).C_{oxt} = Q_{oxt} + Q_{fit} + Q_{it}(\psi_S = 0)$$

When the interface trap density is high (>10^{11} cm-2), the flatband biases for the opposite sweep directions are different. This difference id called hysteresis:

$$\Delta VH = V_{FB}(accum \rightarrow depl) - V_{FB}(depl \rightarrow accum) \tag{15}$$

The applied gate bias is the sum of the potential drop over the oxide Voxt, the flatband voltage V_{FB} and the potential at the SiC surface Ψ_S.

$$V_G = V_{oxt} + V_{FB} + \psi_S \tag{16}$$

The oxide capacitance corresponds to the accumulated charge at the gate divided by the potential drop over the oxide

$$C_{oxt} = \frac{Q_G}{V_{oxt}} \tag{17}$$

In the ideal case, this charge equals to the space charge of the semiconductor with negative sign Q_G=-Q_{SC} (Ψ_S), whereas the space charge of the semiconductor is a function of the surface potential. All these considerations lead to the following relationship between the applied gate voltage and the surface potential. Figure 15 shows the work functions of various metals used as gate dielectric together with the energy position SiC valence and conduction band edge.

$$V_G - V_{FB} = -\frac{Q_{SC}(\psi_S)}{C_{oxt}} + \psi_S \tag{18}$$

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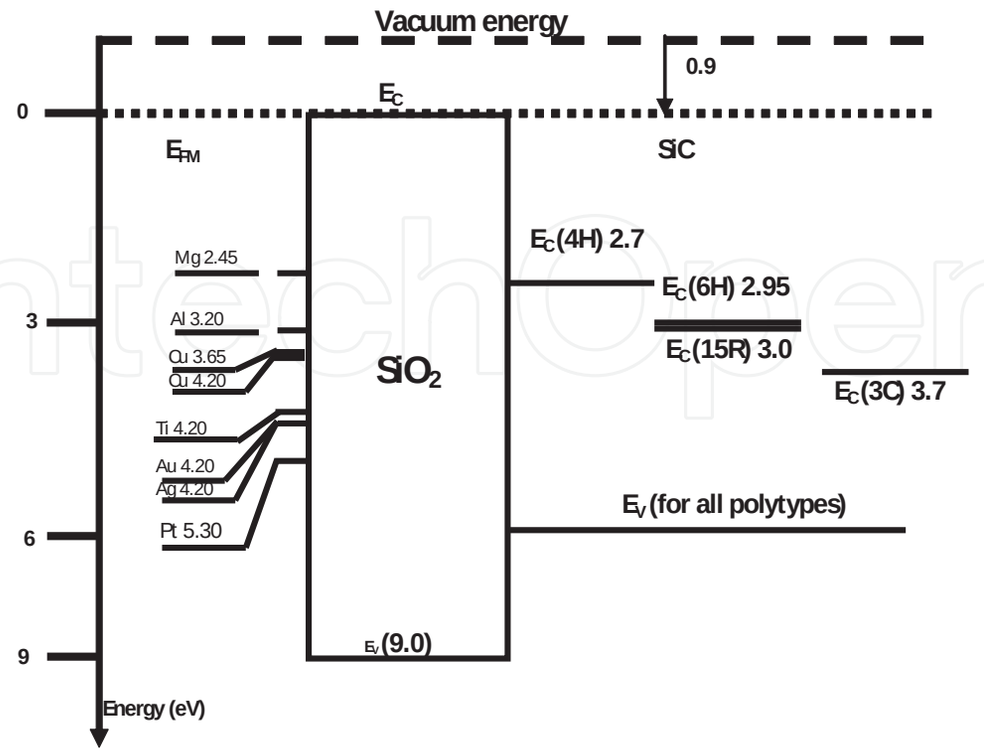

Figure 15. Work functions of various metals used as gate together with the energy position SiC valence and conduction band edge

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