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Chapter 3

Radar Sensing Using Ultra Wideband – Design and Implementation

Xubo Wang, Anh Dinh and Daniel Teng

Additional information is available at the end of the chapter

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1. Introduction

Ultra-wideband (UWB) has received significant attention for applications in target positioning and wireless communications recently. The extremely short pulses in turn generate a very wide bandwidth and offer several advantages, such as large throughput, covertness, robustness to jamming, lower power, and coexistence with current radio services. UWB not only can transmit a huge amount of data over a short distance at very low power, but also has the capability to pass through physical objects that tend to reflect signals with narrow bandwidth.

The extremely narrow pulse (usually in order of few nanoseconds to few hundred picoseconds) makes it possible to build radar with much better spatial resolution (usually 0.1 to 1 ft) and very short-range capability compared to other conventional radars. Also, the large bandwidth allows the UWB radar to get more information about the possible surrounding targets and detect, identify, and locate only the most desired target among others. The fine resolution makes the UWB radar beneficial for medical applications. The properties of short pulse indicate that the UWB signal can penetrate a great variety of biological materials such as organic tissues, fat, blood, and bone. Experiment results show that the signals with low center frequencies achieve better material penetration. Compared to a radar system with a pulse-length of one microsecond, a short Gaussian or Gaussian monopole pulse of 200ps in width has a wavelength in free space of only 60 mm, compared to 300m. Since the pulse length in conventional radar is significantly longer than the size of the target of interest, the majority of the duration of the returned signal is an exact replica of the radiated signal. Thus, the returned signal provides little information about the nature of the target. However, since the UWB pulse length is in the same order of magnitude with the potential targets, UWB radar reflected pulses are changed by the target structure and electrical characteristics. Those changes in pulse waveform provide valuable information

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such as shape and material properties about the targets. Discrimination of target using higher order signal processing of impulse signals can distinguish between materials that would not be otherwise distinguishable by the narrowband signals.

To work as UWB radar, the UWB transmitter sends a narrow pulse toward a target and an UWB receiver detects the reflected signal. This is a very simple algorithm of radar sensing which has been widely used. For biomedical radar, the target is, for example, a human heart. When the UWB pulse in propagation encounters an boundary of two types of medium with different dielectric properties, a portion of the incident electromagnetic energy is reflected back to the original medium with a reflection angle θ_r (zero reflection angle if the incident wave path is parallel to the normal line), while the other portion continues propagating through the next medium. The analogy of the transmission of UWB pulse is shown in Figure 1.

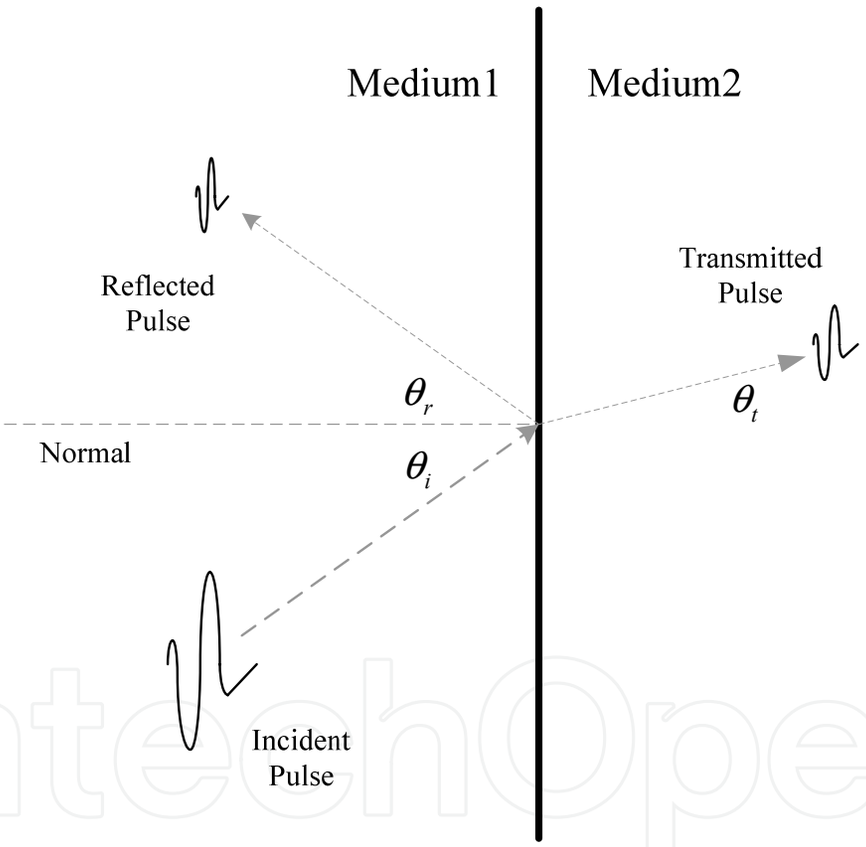


Figure 1. Pulse reflection and transmission diagram

Unlike ultrasound device, which is being widely used at the present time that requires direct skin contact, the UWB makes imaging internal organ movements without invasive surgical or direct skin contact possible. Another advantage in using UWB technology is that the UWB transceiver is simple and occupies a very small chip area as it does not require complicated frequency recovery system as in the narrow bandwidth transceiver. In addition, power consumption of the impulse based UWB systems is extremely low because the power is consumed only during pulse transmitting period.

2. UWB radar architecture

When designing a UWB radar transceiver system, two design aspects need to be considered: architecture and implementation. Different architecture set the fundamental performance capabilities of the design, and good implementation choices improves radar performances. Impulse radar detection range depends on radiated energy, transmitter and receiver design, target size, and signal processing. Among various UWB transceiver architectures, the impulse-based energy detection UWB transceiver architecture is discussed here.

An example of the impulse-based energy detection transceiver architecture is shown in Figure 2. In this architecture, the transmitter sends a pulse train toward the target. The interface between two medias produces a partial reflection. Then the receiver detects and samples this particular type of reflected pulse train, and the decision circuit makes the final decision. Pulses are diffracted and scattered by different tissue layers and organs in human body. Channel distortion and power loss easily destructs the reflected pulses and make them undistinguishable. The rang-gate is designed to look for the destined reflected pulse rather than wait and receive every reflected pulse from every location and try to identify the expected return pulse, which in many cases are very week and tangled with other return pulses. The receiver samples only the pulses arriving at the receiver during a very narrow time window after pulse transmission, as shown in Figure.3. By estimating the distance of the expected target, a delay time is chosen.

This proposed transceiver architecture enormously reduces the circuitry complexity and power consumption. The transmitter consists of a modulator, a pulse generator, and a variable gain amplifier (VGA) driver. An on-off keying (OOK) modulation scheme is used to modulate the pulse. The VGA and driver are used to amplify output and match output impedance. The receiver consists of a low noise amplifier (LNA), a correlator, an integrator, a clocked voltage comparator, and a delay controller. The input clock train and control signal are modulated to a sequence of clock pulse, which then enters the pulse generator to produce a pulse train. This pulse train is passed onto a driver amplifier and then to an UWB antenna. The reflected pulse is caught by the antenna in the non-coherent receiver and amplified by a LNA. The signal then is squared by a multiplier at the asynchronous receiver. The squared output is then fed into an integrator and clocked comparator to boost up the voltage and reconstruct the signals. The range controller uses logic gates to switch on/off the LNA and disable the sampling operation of the comparator for range finding.

3. UWB radar transmitter

Two classes of UWB signals are utilized to transmit symbols in UWB system: carrier-free impulse signal, and carrier-based short sinusoidal signal. The impulse UWB signal is often represented using Gaussian (different orders of Gaussian derivatives), Rayleigh, or Hermitian pulse. The advantages of impulse signal are that the impulse-based transceiver architecture often very simple and consume the least amount of power due to its low pulse repetition rate and low duty cycle. However, the drawback for impulse-based signal is the

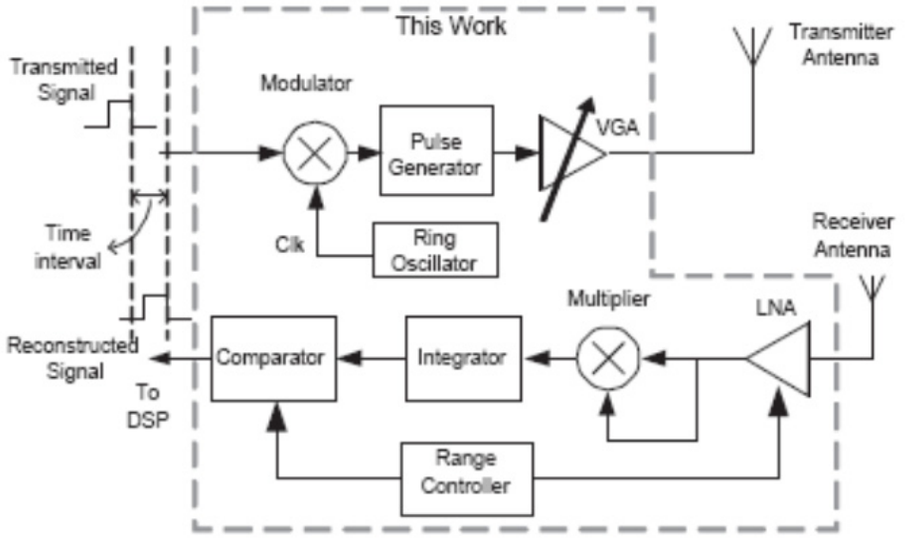


Figure 2. An example of the architecture of the UWB transceiver

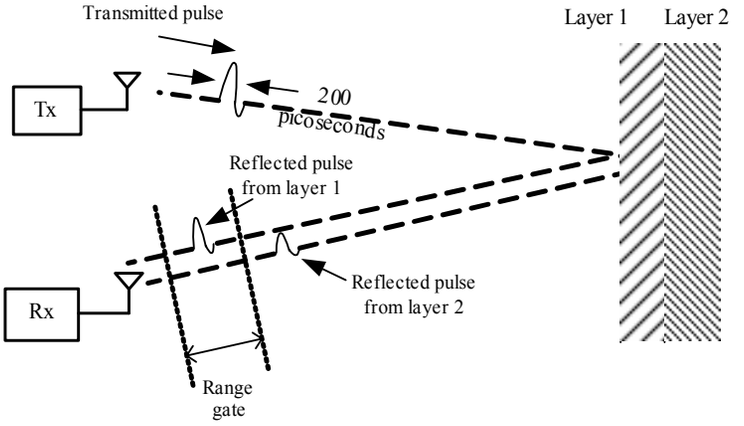


Figure 3. A range gate at receiver opens briefly after a fixed delay time to sample the reflected pulse.

frequency characteristic is largely determined by the pulse shape. Compared to the impulse-based signal, the carrier-based UWB uses sinusoidal wave instead of short pulse to represent signals, and these signals are easier to manage within the FCC spectrum and produce less distortion. Both two classes of UWB transmitter are discussed in following sections.

3.1. CMOS high-order pulse digital transmitter

In this section, a pulsed-UWB BPSK transmitter using higher order Gaussian pulse with digital circuit implementation is discussed. This transmitter outputs tenth-order Gaussian derivative BPSK-modulated pulses. By implementing the transmitter in digital circuit, the pulses can be switched on/off between very short pulse intervals. One way to reduce transmitter power is to avoid the use of circuit blocks that operate constantly or have long setting time and start-up times such as voltage controlled oscillator (VCO).

The proposed UWB high-order Gaussian pulse transmitter with pulse tuning capability is shown in Figure 4. The proposed transmitter consists of two Gaussian derivative pulse generators, a variable gain driver amplifier, and peripheral circuit. The input of the transmitter is a baseband signal. A D-type flip-flop as a frequency divider is used to expand the control signal for pulse generators. The baseband signal is also used to triggered the generation of the pulse generator. The baseband signals are BPSK modulated such that one pulse generator outputs positive Gaussian derivative pulses when the baseband signal is logic high, and the other pulse generator outputs negative Gaussian derivative pulses when the baseband signal is logic low.

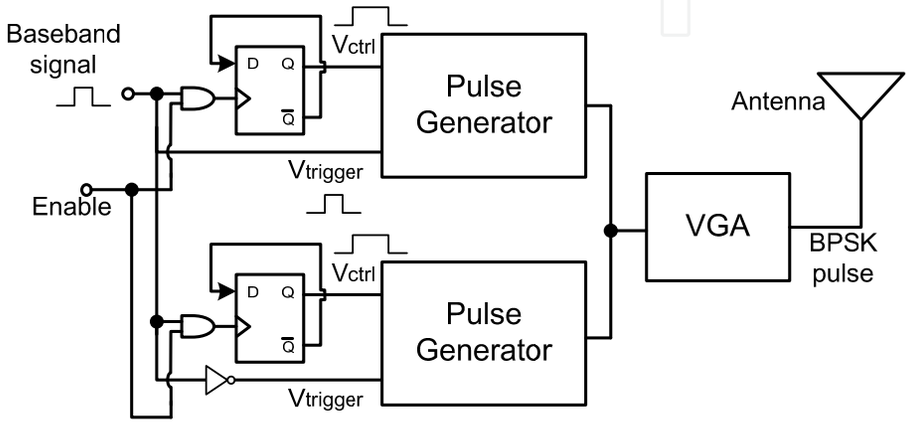


Figure 4. Proposed transmitter architecture.

As seen from the transmitter block diagram, the proposed transmitter is not using any clock signals. This greatly reduces the power consumption of the circuit at the tradeoff of lower pulse repetition frequency (PRF), which is not the ultimate concern for the bio-radar sensing applications. The average transmitter output power emission in the UWB band is limited to -41.3dBm/MHz. But gated UWB systems can also transmit at higher power levels and then sit quietly only if the average emission power density during the time period still satisfies the power limitation. The enable signal in the transmitter controls the gating timing. When the transmitter is configured to operate with gating control at 25 percent duty cycle during transmission of baseband signals from a transmitter to a target, the impulse UWB transmitter can achieve up to four times better performance. This gated signal can then achieve the same average transmit power as a continuous signal while occupying only a fraction of the channel time available for transmissions in the UWB system.

The core component of the pulse generator is the edge generator, as shown in Figure 5. The edge generator generates the basic element which is the Gaussian pulse. Each rising edge of the Vtrigger triggers positively-peaked pulses through a NOR gate and negatively-peaked pulse through a NAND gate. The pulse width and pulse amplitude are controlled through the delay elements. The pulse generation logic is that when one XOR input is slower than the other XOR input, the time difference between these input produces a positive normally distributed voltage pulse (usually represented by Gaussian distribution), and when the inverted NAND input is slower than the other NAND input, the time difference of these

two input produces a negative normally distributed voltage pulse. The polarity of the edge generator output is control by Vctrl. The Vctrl select either the positive pulse or the negative pulse to pass to the output through the AND and OR logic gates.

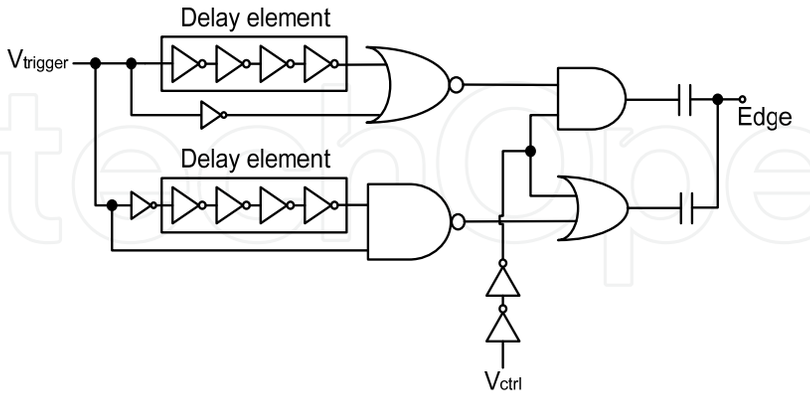


Figure 5. Edge generator circuit with edge tuning capability.

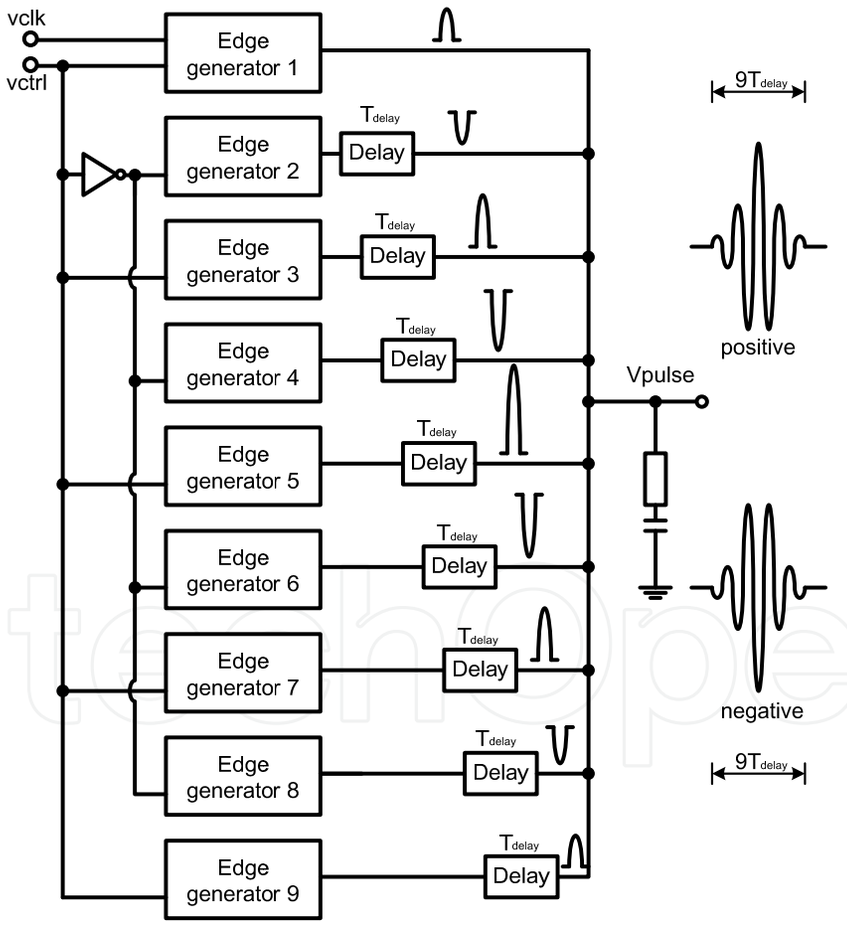


Figure 6. Block diagram of the pulse generator.

The Gaussian derivative pulse generator, as shown in Fig. 6, consists of an array of edge generators connected in parallel. Each edge generator produces a single pulse with different amplitude and the same pulse width T_{delay}. The delay in each edge generator is adjusted

based on the shape factor of the tenth derivative of the Gaussian pulse. The control signal is inverted at the 2nd, 4th, 6th, and 8th edge generators to produce pulses with negative polarity at these locations. The trigger signal Vtrigger is delayed one pulse width Tdelay at the input of the 2nd edge generator, delayed two pulse width 2*Tdelay at the 3rd edge generator, 3*Tdelay at the 4th edge generator, 4Tdelay at the 5th edge generator, 5*Tdelay at the 6th edge generator, 6*Tdelay at the 7th edge generator, 7Tdelay at the 8th edge generator, and 8*Tdelay at the last stage. The final output of the tenth derivative Gaussian pulse is constructed based on each single edge generator output. The total pulse width is 9*Tdelay.

The design is a transmitter prototype. It not only can generate tenth-order Gaussian derivative, but any pulse combinations, either Gaussian derivatives or rectangular or Gaussian modulated sine pulses by controlling the delay elements in each edge generator and the number of edge generators used based on different orders of derivative of Gaussian pulse, the bandwidth, and the center frequency.

The transmitter prototype mentioned in last section was designed and simulated in TSMC 90nm CMOS with 1.0V voltage supply. The base-band signal was generated at 100Mbps to leave enough headroom for pulse generation. The positive and negative tenth derivative Gaussian pulses were generated, as shown in Figure 7. The pulse width was adjusted to 0.5ns through the delay components. The transmitter output peak-to-peak amplitude is 130mV, and the amplitude ranges from 35mV to 500mV.

A Monte Carlo simulation was performed to validate the robustness of the transmitter circuit against process voltage and temperature variations and mismatches. The Monte Carlos simulation results of the tenth-order Gaussian derivative pulses are shown in Figure 8. The simulated power spectral density plot of the transmitter output with simulated white noise added is shown in Figure 9.

The layout of the proposed transmitter is shown in Figure 10. The transmitter core occupies a chip area of 200um by 140um. Simulating on a 1V voltage supply, the transmitter draws average 9.037mW when generating the tenth-order Gaussian derivative pulses at a pulse repetition frequency of 50MHz. The pulse width is 0.6ns. The transmitter has output pulse energy of 3.1pJ/pulse.

3.2. CMOS Gaussian pulse transmitter

The proposed impulse-based UWB technique enormously reduces the circuitry complexity and power consumption. Figure 11 shows the block diagram of the transmitter which consists of a modulator, a pulse generator, and a variable gain amplifier (VGA) driver, and a ring oscillator. An on-off keying (OOK) modulation scheme is used to modulate the pulse. The VGA and driver are used to amplify and adjust the output pulse, as well as for impedance matching. The incoming data V_{data} is modulated with clock train generated by the ring oscillator, yielding a sequence of clock pulse, which then enters the pulse generator to produce a pulse train. This pulse train is passed onto a driver amplifier and then to an

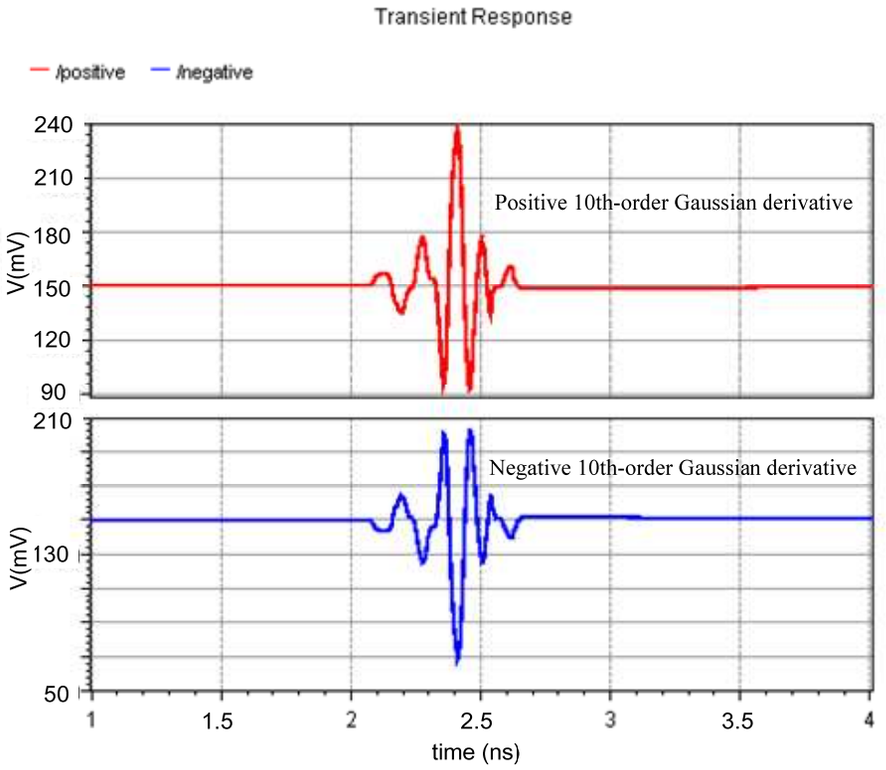


Figure 7. Simulated tenth order Gaussian derivative pulses.

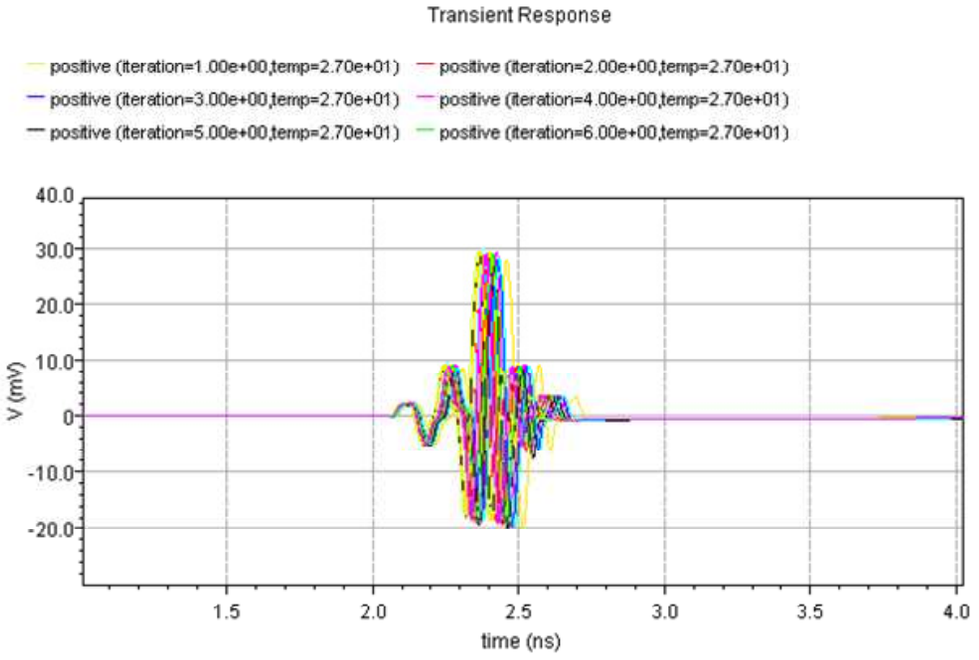


Figure 8. Monte Carlo simulation of the transmitter.

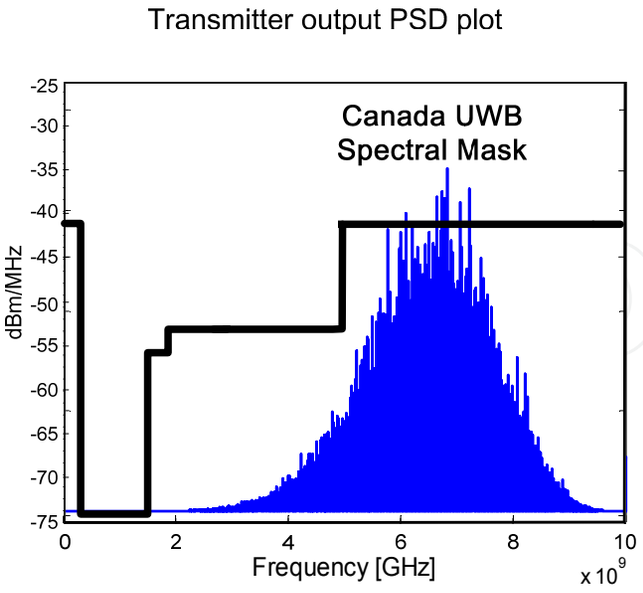


Figure 9. Simulated power spectral density of the pulse.

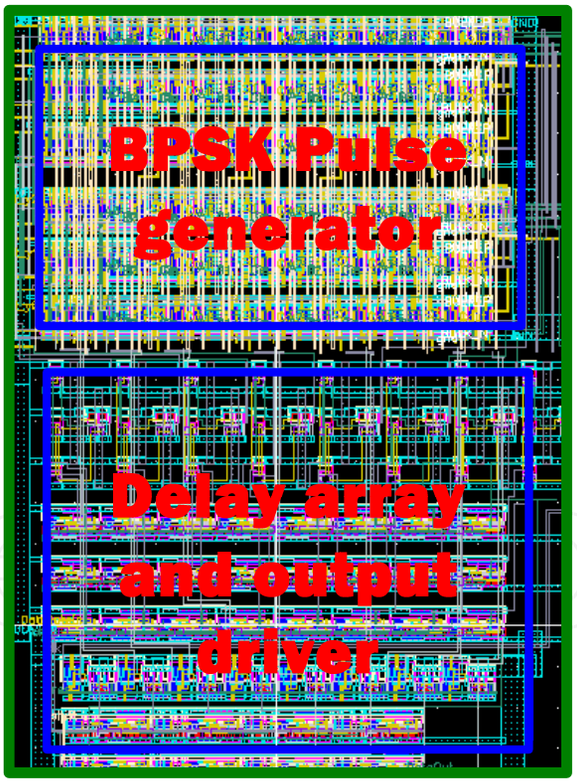


Figure 10. Layout of the proposed digital transmitter.

UWB antenna. The output pulse amplitude is adjustable through the variable gain amplifier in the driver. The range controller uses logic gates to switch on/off the VGA. The transmitter is fabricated using CMOS 90nm process, and the whole design consumes less than 0.5mA of static current.

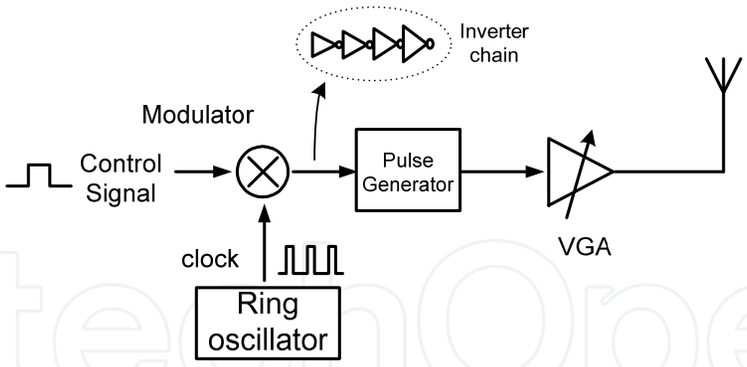
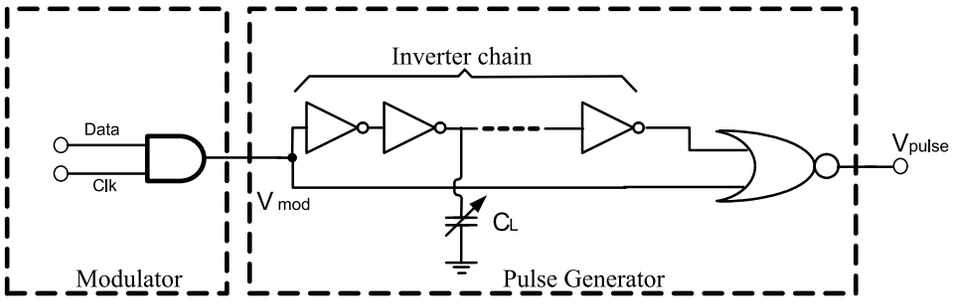
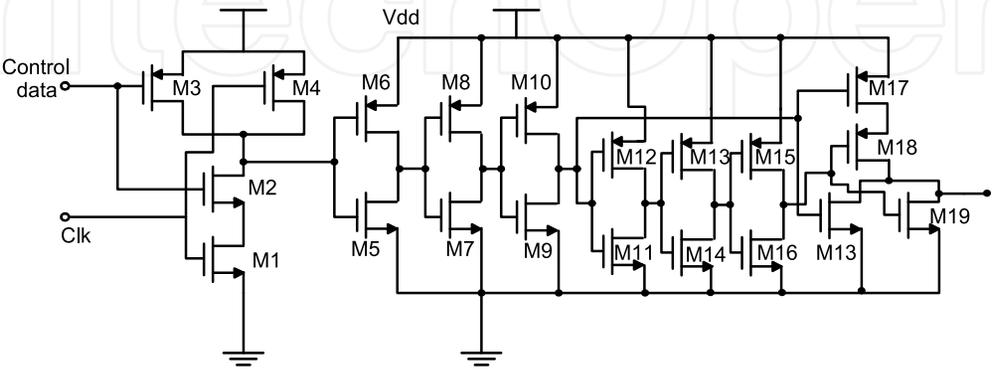


Figure 11. Proposed IR-UWB transmitter

Fig. 12(a) shows two critical components of the transmitter: the OOK modulator and the pulse generator. The clock signal Clk, generated by a ring oscillator, has a period of 1ns and a pulse width of 500ps. The clock train is modulated by the input data with OOK modulation by an AND gate. The number of pulses in one bit of data is determined by both the bit length and the clock frequency. For radar sensing purpose, it is the best interest of the energy-collecting receiver to include more pulses in a single pulse train sent to the target for a good SNR and easy detection. In communication cases, the number of pulses representing one bit is set less for higher data transmission rate. The clock rate is higher than the data rate to ensure reliable modulation and demodulation. Figure 12(b) illustrates the pulse generator and modulator in the transistor level.



(a) Pulse generator and modulator



(b) Pulse generator circuit

Figure 12. Pulse generator and modulator circuit in transistor level

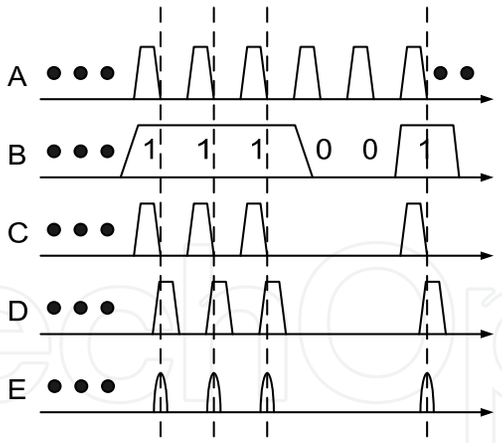


Figure 13. Timing waveforms of the transmitter

The signal flow at each block of the proposed transmitter is illustrated in Figure 13. The transmitter clock signal is represented by A. B is the input digital sequence. The modulated clock train C passes through an inverter chain to sharpen the rising and falling edge of the each clock signal. The modulated clock train is then split into two signal paths and fed into a NOR gate. Signals in one path is delayed and inverted, as shown by D. The NOR gate only outputs high when both inputs are low, and the time for both inputs be low is the delay time set by the inverter chain in the delay path. The signal E represents the output pulses. The output pulse width is determined by this delay time. The output pulse width can be adjusted by changing the delay of the inverters, which in turn, by varying the load capacitance of the inverters. Figure 14 shows the simulated pulses with various pulse widths when changing the load capacitance of the inverters C_L. This load capacitance C_L is implemented using a CMOS varactor.

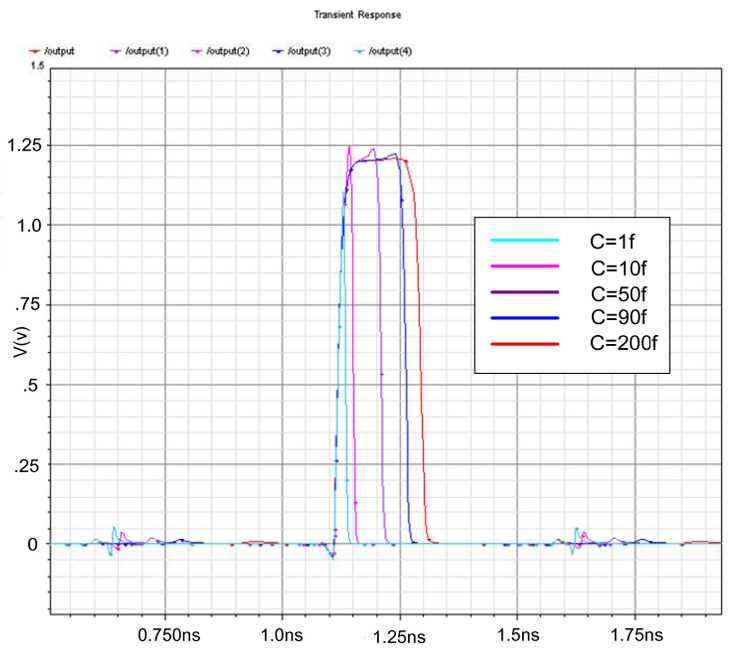


Figure 14. Simulation of different pulse widths

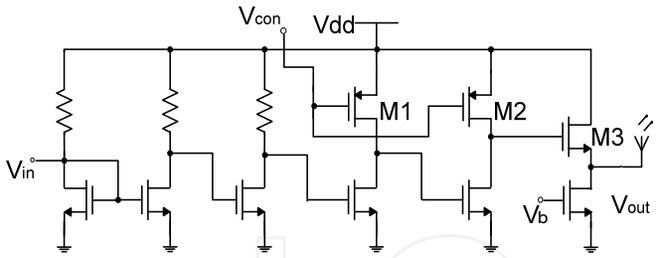


Figure 15. Driver amplifier and VGA

The driver amplifier is used to amplify and shape the spectrum of the out-going short pulses, to adjust the transmitting pulse amplitude, and to match output impedance. As shown in Figure 15, the variable gain driver amplifier consists of three stages. The first stage employs three cascade common-source amplifiers with load resistors. Each amplifier is designed with relatively low gain to achieve a high bandwidth. The second stage consists of two cascade common-source amplifiers with PMOS transistors load. By analyzing the high frequency operation of a cascaded common-source amplifier, the voltage gain can be shown as

$$A_V = \frac{-g_m Z_L}{1 + g_m Z_S} \tag{1}$$

For a MOS transistor biased in the linear region, a linear resistance is

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(v_{GS} - V_t)} \tag{2}$$

The value of the resistance r_{DS} is controlled by varying the value of v_{GS}. The overall gain of the driver amplifier is therefore

$$gain = \frac{-g_m Z_L - g_m \left(\mu_n C_{OX} \frac{W}{L}(v_{GS} - V_t) \right)^{-1}}{1 + g_m Z_S} \tag{3}$$

The two PMOS transistors are tuned in the triode region and the equivalent resistances are controlled by the control voltage Vcon. Simulation shows that the change of Vcon from 0V to 0.15V corresponds to output pulse level from 30mV to 560mV, as shown in Figure 16. The last stage is an output buffer for 50ohms impedance matching purpose.

The impulse UWB transmitter was designed and implemented using standard ST 90nm CMOS technology with 1.2V power supply to verify the proposed idea. A chip photograph of the fabricated test circuit is shown in Figure 17. The active transmitter area measures $50\text{um} \times 100\text{um}$. The transmitter die is housed using CQFP44 package and the chip is mounted on a PCB for measurement. The fabricated impulse transmitter module is tested under normal operating environment. Figure 18 illustrates the measurement setup. For digital data input, a pattern generator is used to provide a 250Mb/s bit sequence data. The

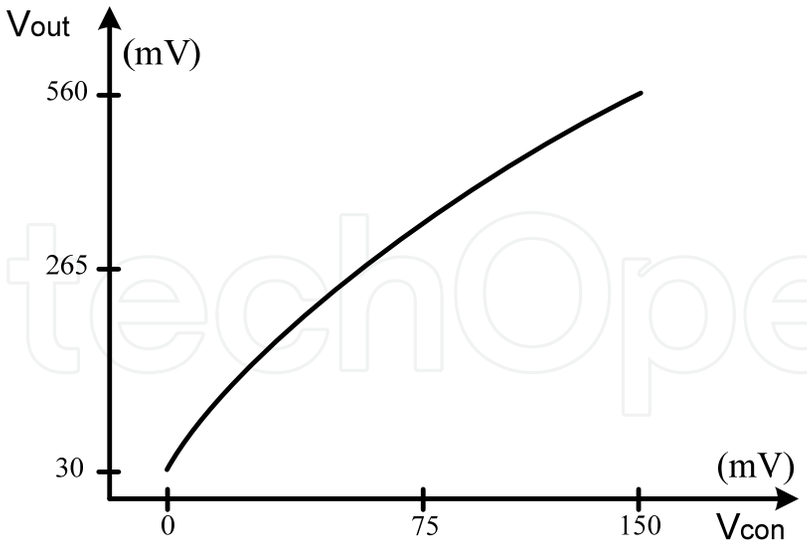


Figure 16. Output pulse amplitude vs. different control voltage

internal clock generator of the transmitter provides a 500MHz square wave clock signal. The output of the transmitter is connected to a high frequency oscilloscope through a SMA cable. The power supply of the chip package is 1.2V.

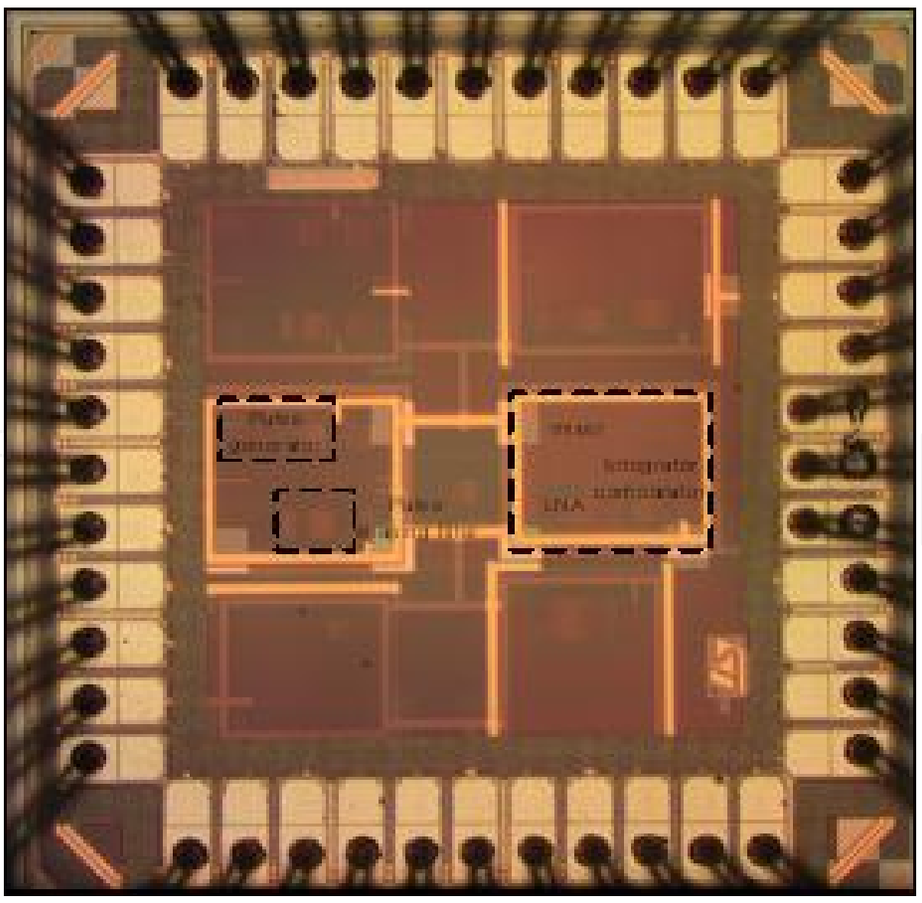


Figure 17. Photograph of the transceiver die

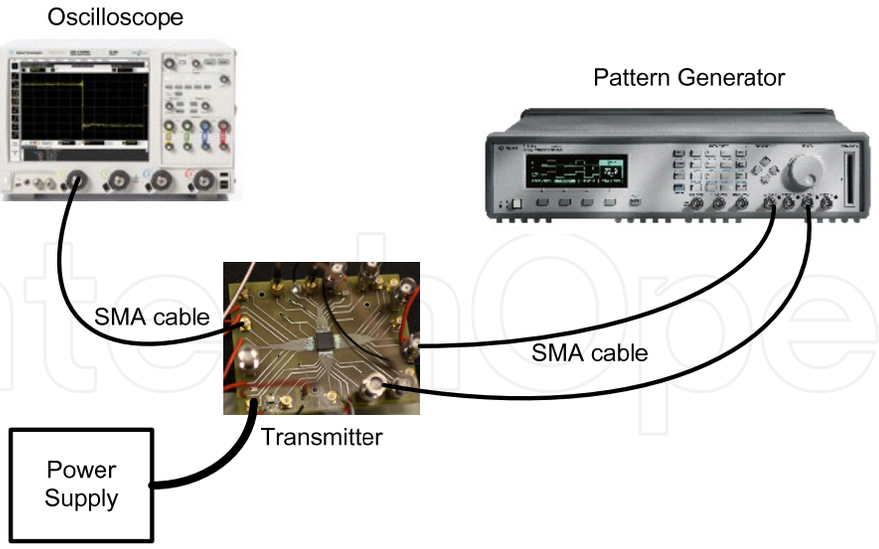


Figure 18. Measurement setup for the performance test of the proposed transmitter

In one of the tests, the pattern generator inputs a digital sequence with a pattern of 111001 at 250Mb/s, as shown in Figure 19, to the transmitter module. The corresponding transmitter output pulses are shown in Figure 20 with the scale doubled. The first derivative of the Gaussian pulse at the receiver side is shown in Figure 21. Each pulse-width is 1ns and has an amplitude of 177mV.

Figure 22 shows the measured output pulse waveforms of the implemented transmitter in another test where a single bit data is applied as an input. The pulse has a close-to-maximum amplitude of 521mV at a 50 Ω load and a pulse width of 1ns when the VGA control voltage was set at 0.14V. The output pulse has a minimum amplitude of 30mV.



Figure 19. Waveform of input

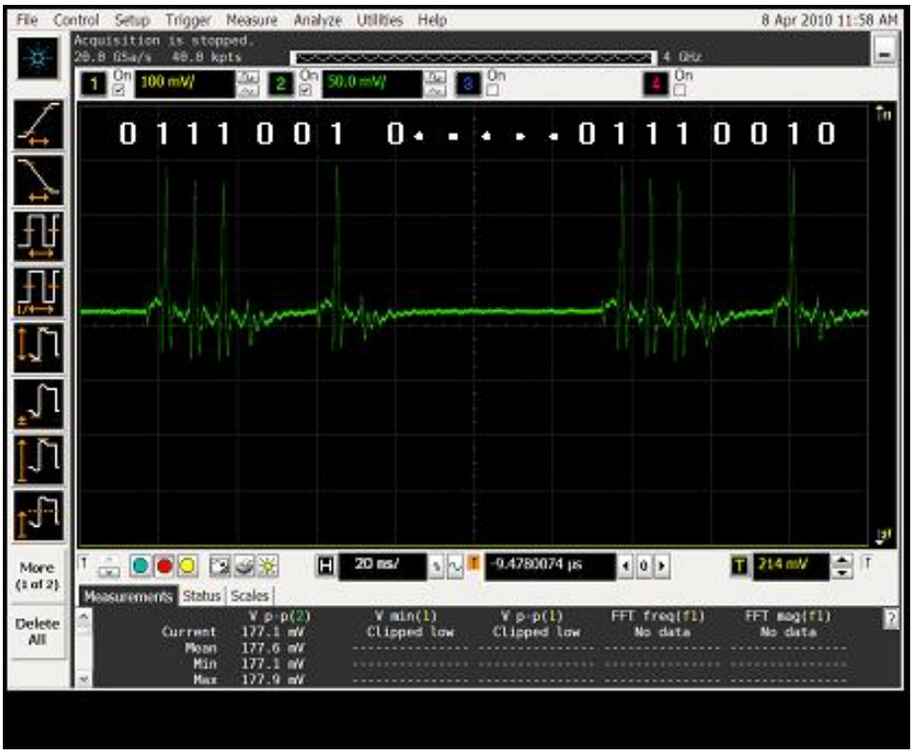


Figure 20. Measured transmitter output pulses

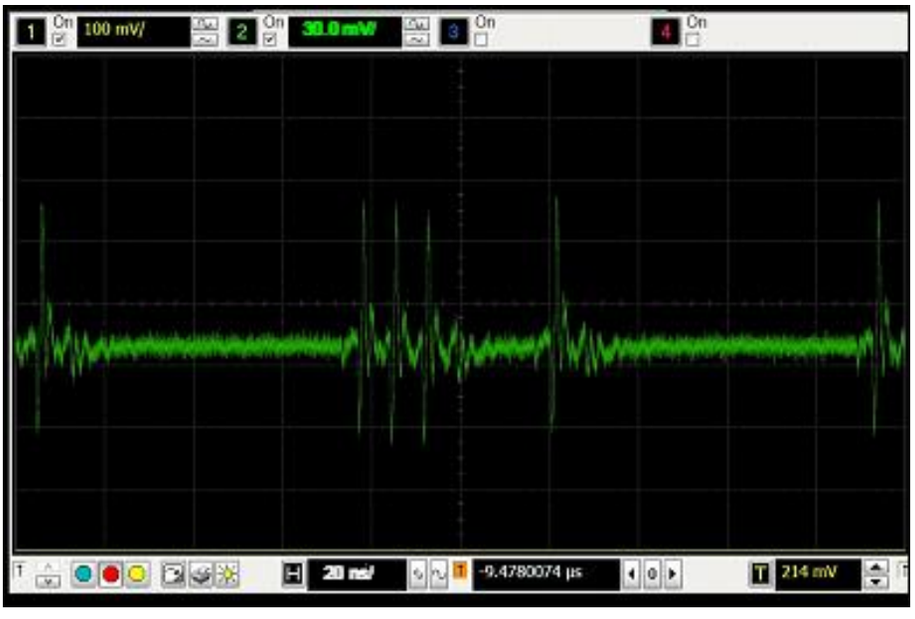


Figure 21. Measured first derivative of the pulses at receiver side

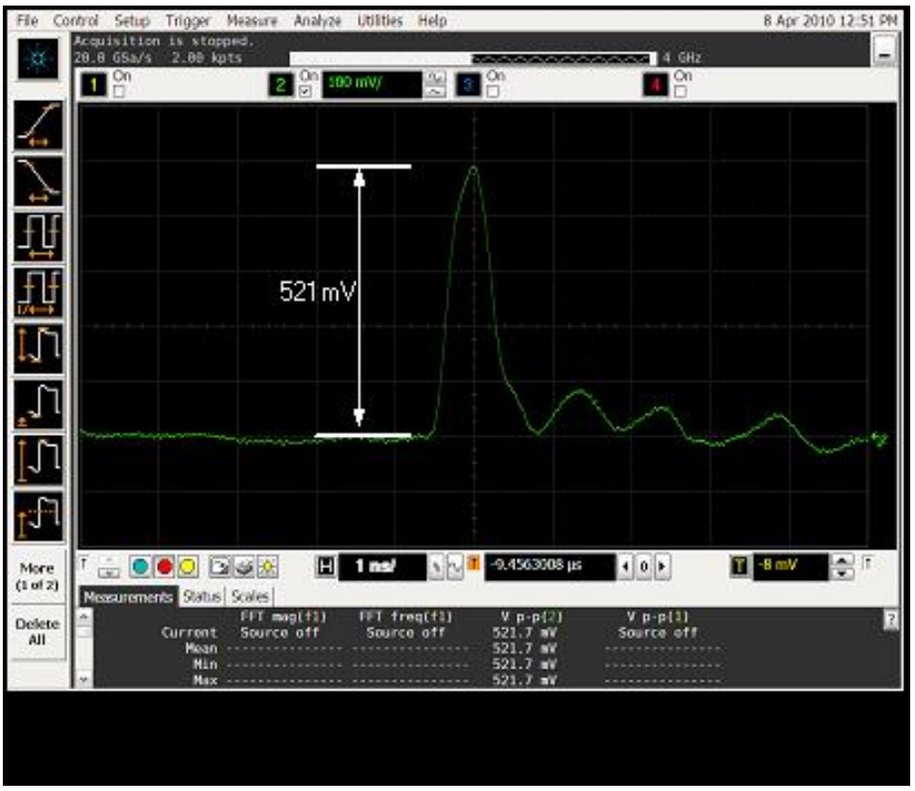


Figure 22. Single measured Gaussian pulse

The power spectral density of the transmitter modulated output pulse train is calculated using discrete Fourier transform on the measured UWB signal. Figure 23 shows the calculated power spectral density in dBm/MHz unit with the FCC spectral mask.

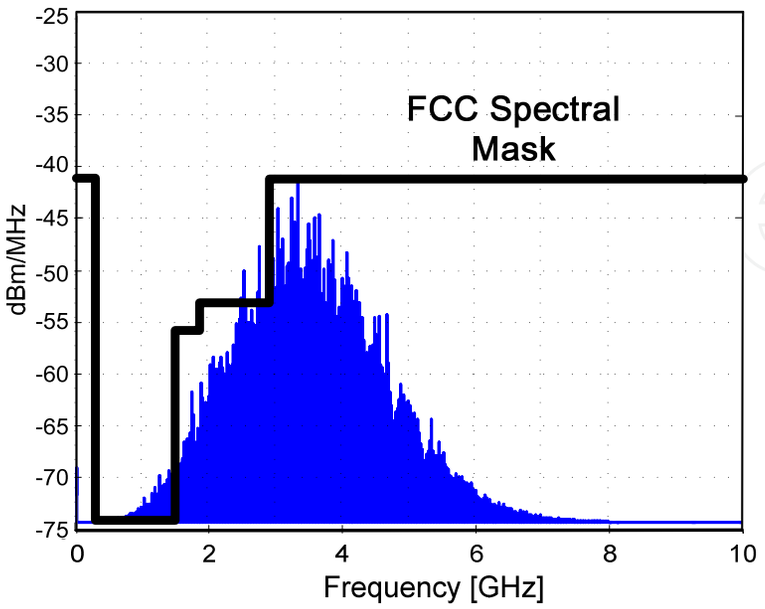


Figure 23. Power spectrum density of the output pulse

3.3. Other types of transmitter

In this section, the proposed system, which is shown in Figure 24, uses carrier-based continuous wave to represent information. The proposed non-coherent UWB transceiver transmits signals at different carrier frequency within the full 3-10 GHz band. This allows the radar to detect the targets with more details since more waves at different frequencies are reflected from dielectric boundaries favoring different frequencies. The signal at the transmitter is generated by a voltage controlled oscillator. The digital signal with specific envelop shape is multiplied with the output wave of the VCO to generate a modulated waveform consisting of multiple cycles of sinusoidal waves with small bandwidth. The carrier frequency can be adjusted over the total UWB frequency band by varying the capacitance value of the capacitor bank in the circuit. For radar sensing, a low repetition rate is desired. The transmitter employs a switching mechanism to reduce the power consumption and avoid the oscillation start-up transient delay and oscillation leakage. The proposed receiver contains a LNA, a down-conversion mixer, a filter and ADC. By using this approach, there is more flexibility on power spectrum control and output frequency selectivity, at the cost of higher power and more complexity compared to the first approach. Figure 25 shows the transmitter architecture in detail. It consists of a tunable LC oscillator, a voltage multiplier, a variable gain amplifier (VGA) driver, and a pulse generator. In this proposed design, the incoming data *Vdata* is split into two paths: one enters the LC oscillator and controls the on/off switch of the oscillation, the other path is fed into the pulse generator to trigger a square voltage pulse with a narrower pulse width. After the square pulse *Vdata* switches both the LC oscillator and the multiplier on and the oscillation reaches a steady state, the pulse generator output *Vpulse* with narrower time window is multiplied with the sinusoidal carrier to produce the transmitter output signal.

The voltage oscillator is realized based on the LC oscillation circuit using a cross-coupled transistor pair as shown in Figure 26. The oscillation frequency is determined by the resonance frequency of the inductor in each arm and the capacitor bank capacitance. The cross-coupled transistors create a negative impedance of value -1/gm at the drain of M1 and M2. The oscillator resonant frequency is set at 1/sqrt(LC), where L and C is the inductance and capacitance of L1 and capacitor bank, respectively. The signal Vdata turns on/off the oscillator by switching the PMOS M3 on/off. This signal also controls on/off of the multiplier, which is implemented using a Gibert Cell.

The signals at each block of the proposed transmitter are illustrated in Figure 27. The transmitter input signal Vdata controls signal C and B, and signal B generates signal D. The oscillator generates the carrier waveform with different center frequency within the 3-10GHz UWB band. The tuning is achieved through selecting different capacitors and adjusting the control voltage of the varactor in the capacitor bank. The six capacitors divide the 3-5GHz and 6-10GHz band into six sub-bands. By tuning voltage of the varactor in the capacitor bank, each single sub-band has a frequency tuning range of 500MHz. The overall tuning range of the capacitor bank covers the whole 7GHz UWB band. The simulated power spectral density of the transmitter output at different center frequency is shown in Figure 28.

Six transmitter outputs at frequency 3.1GHz, 4GHz, 4.8GHz, 6.3GHz, 8GHz, and 9GHz, tuned through the capacitor bank, are shown. The transmitter core area is 0.051 mm^2. The overall average power consumption of the transmitter at frequency of 9GHz is 1.85mW.

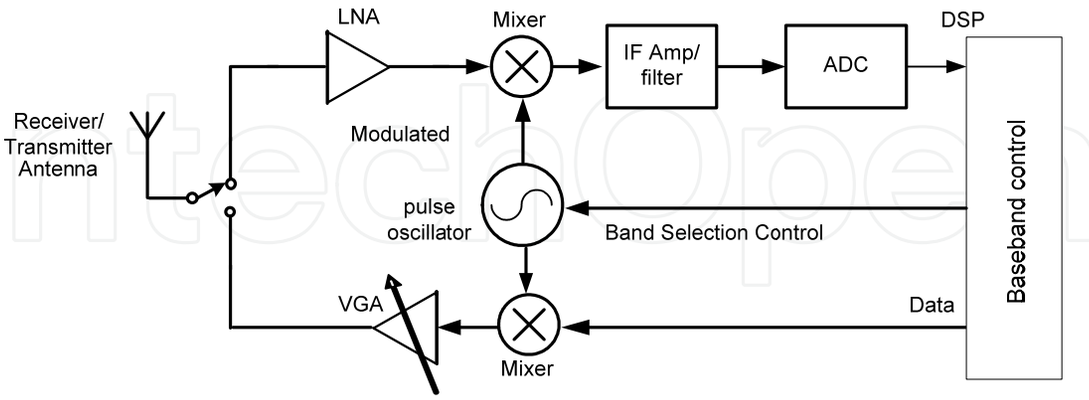


Figure 24. Proposed carrier-based UWB transceiver architecture

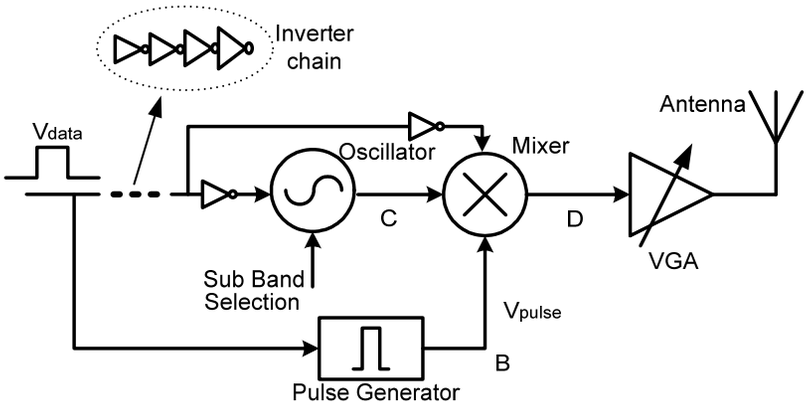


Figure 25. Proposed carrier-based transmitter

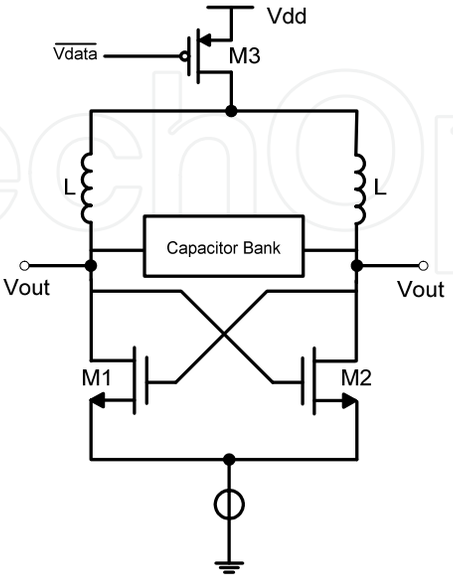


Figure 26. LC oscillator circuit

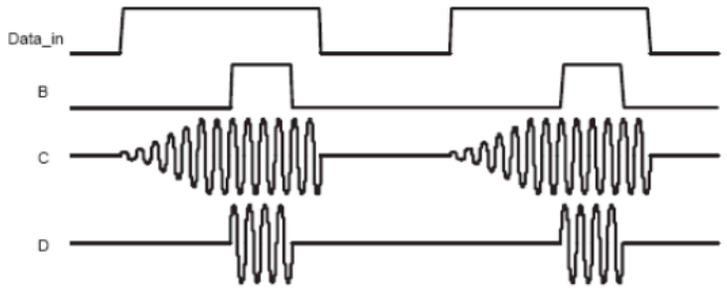


Figure 27. Waveforms of the carrier-based transmitter

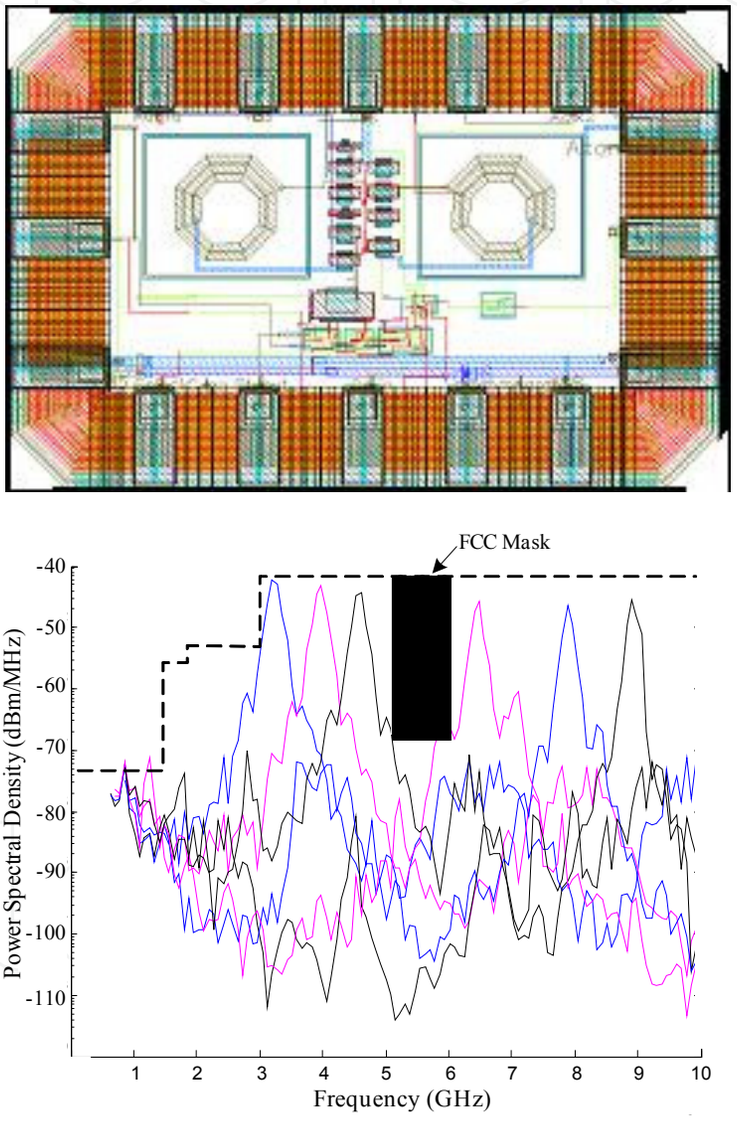


Figure 28. Transmitter layout and simulated PSD of the designed pulse generator output.

4. UWB radar energy detection receiver

Receiver design is another major challenge in UWB system. To detect the UWB signals, the goal of the UWB radar is to develop the method to maximize the signal-to-noise ratio (SNR).

Figure 29 shows an impulse-based UWB radar receiver. It consists of a LNA, a voltage multiplier, an integrator, and a clocked voltage comparator.

The LNA, shown in Figure 30, consists of two common-source, common-gate cascade amplifiers. The cascade configuration with inductive peaking (L2, L4) improves the reverse isolation and frequency response. The input matching network includes L1, C1, and L3. The inductors can be replaced by bonding wire to save chip area.

A Gilbert cell, as shown in Figure 31, is used to implement the voltage multiplication. For non-coherent receiver, the correlator uses the received signal as a signal template. The gates of M1, M3, and M6 are the correlator inputs. An analog integrator is used to collect the charges in a pulse or a pulse train. By integrating the pulse voltage, the voltage level of the received signal is much more distinguishable than noise. The integration time is adjusted through a voltage controlled capacitor C and R. A sense amplifier, as shown in Figure 32, is employed as a clocked comparator because of its sensitivity and low circuit complexity. Transistor M3, M4, M8, and M9 form a flow-through latch to sense the voltage difference between the input voltage and the reference voltage. Cascode input configuration is employed to minimize feedthrough of the clock signal. The range gating signal is combined with the comparator clock to control the sampling time of the comparator. The comparator is functioning only at the window when the range gating signal is on.

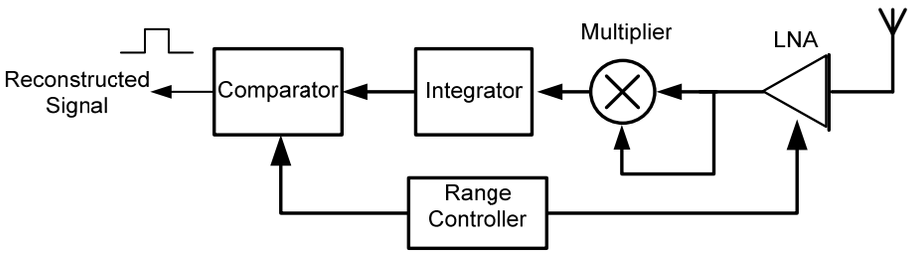


Figure 29. Impulse-based UWB receiver

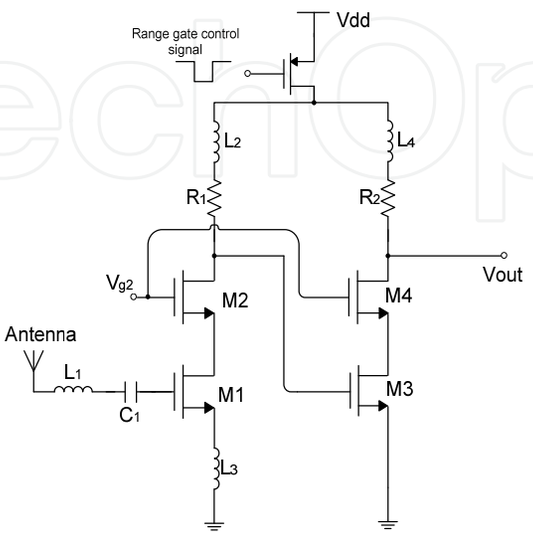


Figure 30. LNA circuit

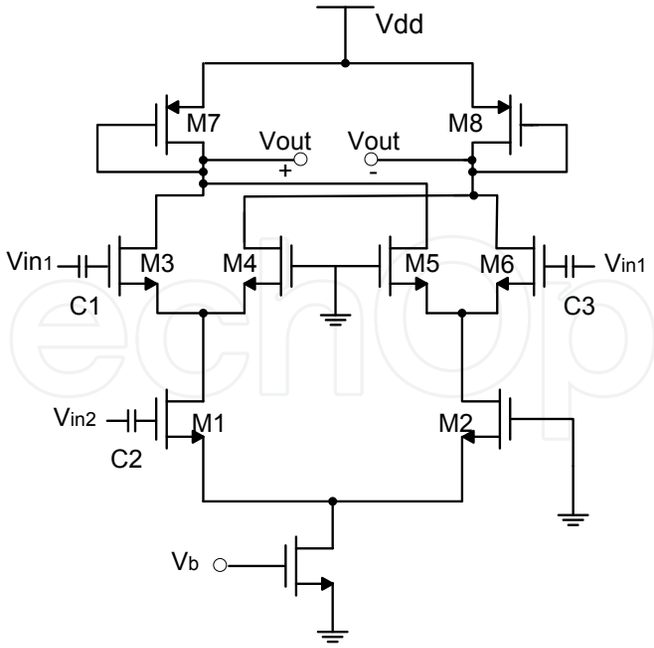


Figure 31. Multiplier circuit

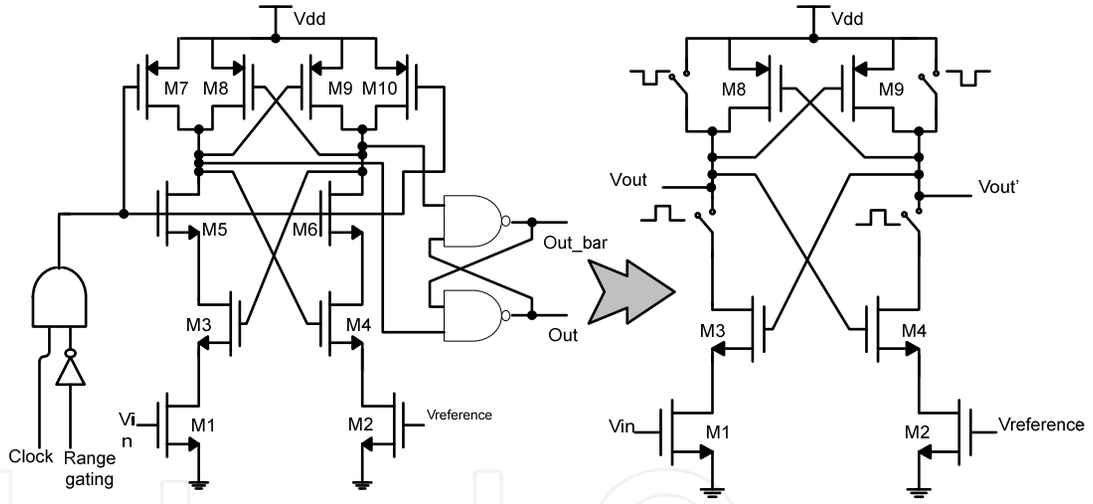


Figure 32. Comparator

Figure 33 shows the receiver for carrier-based UWB receiver. It consists of a wideband low noise amplifier, bandpass filters, square circuit, energy integrator, and comparator. The principle operation of the receiver involves energy correlation and detection at each different frequency sub-band. This energy detection topology is chosen because it reduces the sensitivity of the receiver required to immune noise and multi-path. The signal detected by antenna is amplified by the LNA and filtered by a bank of bankpass filters into 500 MHz sub-bands in UWB band. The filtered signal is squared and integrated over a fixed period of time t, and then quantized by a decision-making circuit. For non-coherent receiver, there is no need for synchronization mechanism, and thus reduce the complexity of the receiver circuit. For the case of OOK modulation scheme, there are two possible situations: signal energy collected or only noise energy collected. The greatly relaxes the required SNR for ADC operation.

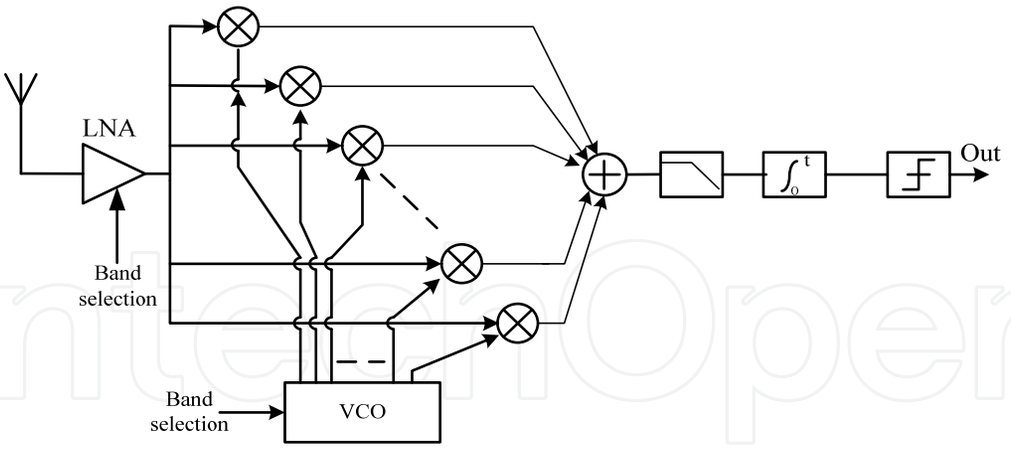


Figure 33. Carrier-based UWB receiver

Another advantage of this receiver topology is it can receive and process different frequency content at the same time, ie. The parallel receiver structure. This will increase the data rate by a factor of N, where N equals to the number of the filters in the filter bank.

5. Conclusion

Many published works have discussed the CMOS transceiver design for communications, but few demonstrated the CMOS transceiver design for medical radar sensing. This chapter demonstrates the design of biomedical radar sensing on the single CMOS integrated UWB transceiver. The advantage of using integrated CMOS UWB technology in biomedical sensing is that this technology provides ultra-low power, ultra-low cost, and ultra-low area solutions with much accurate and reliable performance. This chapter proposes an integrated radar system architecture which can achieve the radar sensing for heart rate monitoring, and explores and implements the integrated single chip radar transceiver circuit in CMOS IC. This chapter shows the implementation of the low-power low cost CMOS biomedical radar using UWB pulse for bio-monitoring.

This chapter can be expended further to apply in biomedical imaging using impulse radio radar. By characterizing the reflection properties of different tissues inside human body, an image of fluoroscopy of the human body can be generated under UWB radar scanning. The UWB radar will lead a technology breakthrough in the medical imaging area.

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