We are IntechOpen, the world's leading publisher of Open Access books
Built by scientists, for scientists

6,900
Open access books available

185,000
International authors and editors

200M
Downloads

154
Countries delivered to

Our authors are among the

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS
BOOK CITATION INDEX
INDEXED

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

A Successive Approximation ADC using PWM Technique for Bio-Medical Applications

Tales Cleber Pimenta, Gustavo Della Colletta,
Odilon Dutra, Paulo C. Crepaldi,
Leonardo B. Zocal and Luis Henrique de C. Ferreira

Additional information is available at the end of the chapter

1. Introduction

Analog to digital (A/D) converters provide the interface between the real world (analog) and the digital processingdomain. The analog signals to be converted may originate from many transducers that convert physical phenomena like temperature, pressure or position to electrical signals. Since these electrical signals are analog voltage or current proportionals to the measured physical phenomena, its necessary to convert them to digital domain to conduct any computational. Nowadays, the development of the IC technology resulted in a growth of digital systems. A/D converters are present in the automotive industry, embedded systems and medicine for example. Thus, A/D converters have become important and the large variety of applications implies different types of A/D conversions.

For the A/D type considerations, the analog input should be characterized as one of the following three basic signal types [3].

- Direct current (DC) or slowly varying analog signals.

- Continuous changing and single event alternating current (AC) signals.

- Pulse-amplitude signal.

For sampling the first type of signals, typical A/D conversion architectures are slope, voltage to frequency, counter ramp and sigma-delta. The second signal type is better sampled using the successive approximation, multistep and full parallel A/D conversion architectures. The last signal type uses successive approximation, multistep, pipeline and full parallel architectures.

After choosing the A/D converter architecture, it is important to keep in mind that any of them have nonlinearities that degrade the converter performance. These nonlinearities are accuracy parameters that can be defined in terms of Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). Both have negative influence in the converter Effective Number of Bits (ENOB) [2].

- Differential Nonlinearity (DNL) is a measure of how uniform the transfer function step sizes are. Each one is compared to the ideal step size and the difference in magnitude is the DNL.
- Integral Nonlinearity (INL) is the code midpoints deviation from their ideal locations.

Therefore it is important to design implementations capable of improving the ADCs performance by improving DNL and INL.

Physiological signals have amplitudes ranging from tens of μV to tens of mV and the frequencies spanning from DC to a few KHz. By considering those features and the application requirements, in order to make a reliable conversion, A/D converter may not have missing codes and must be monotonic. This can be accomplished assuring that the DNL error is less then *0.5* of last significant bits (LSBs).

2. Biomedical Application

Advances in low power circuit designs and CMOS technologies have supported the research and development of biomedical devices that can be implanted in the patient. These devices have a sensor interface specially designed to acquire physiological signals, usually composed of an operational amplifier with programmable gain and reconfigurable band-width features, low pass filter and an A/D converter [8, 10]. The signals are acquired and digitalized in the sensor, thus protecting data from external noise interference.

Specific research on A/D converters for biomedical application is focused on design low power circuits regardless of the monotonic feature, once DNL error is above *0.5 LSBs*, affecting the converter accuracy [5, 6]. The proposed Successive Approximation architecture offers both low power consumption and high accuracy features for use in biomedical applications.
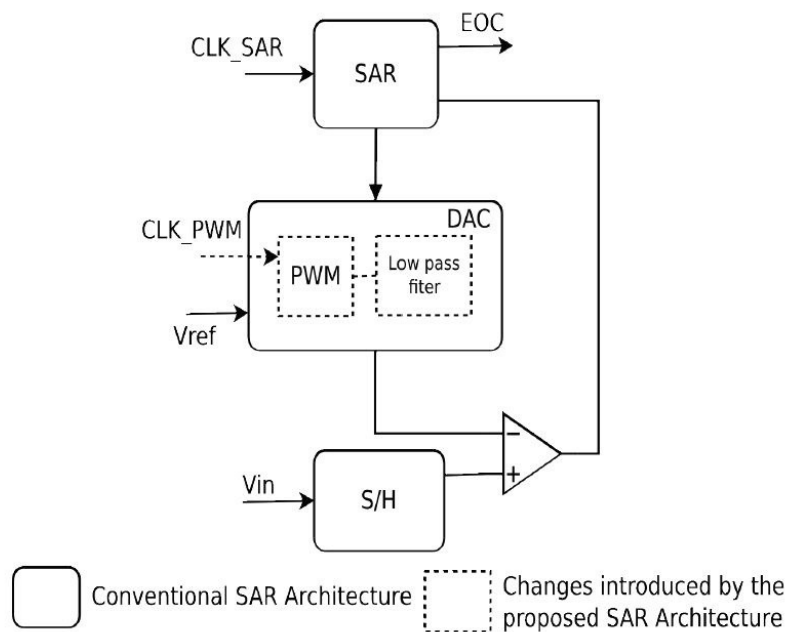
3. Conventional SAR architectures

Figure 1 illustrates the block diagram of the conventional SAR architecture. It is composed of a Successive Approximation Register that controls the operation and stores the output converted digital data, of a digital-to-analog converter stage (DAC), a comparator usually built with a operational amplifier and of a sample and hold circuit. The output can be taken serially from the comparator output or parallel from the SAR outputs.

The operation consists on evaluating and determining the bits of the converted digital word, one by one, initiating from the most significant bit. Thus the SAR architecture uses n clock

cycles to convert a digital word of n bits. The successive approximation architecture provides intermediate sample rates at moderate power consumption that makes it suitable for low power applications.

The internal DAC stage, illustrated in Figure 1 is usually designed using capacitor networks that are susceptible to mismatches caused by the fabrication process variation, since the design is based on absolute capacitance values. These mismatches affect the converter accuracy, thus increasing the DNL and INL errors.

(a) Conventional and proposed architecture block diagrams.
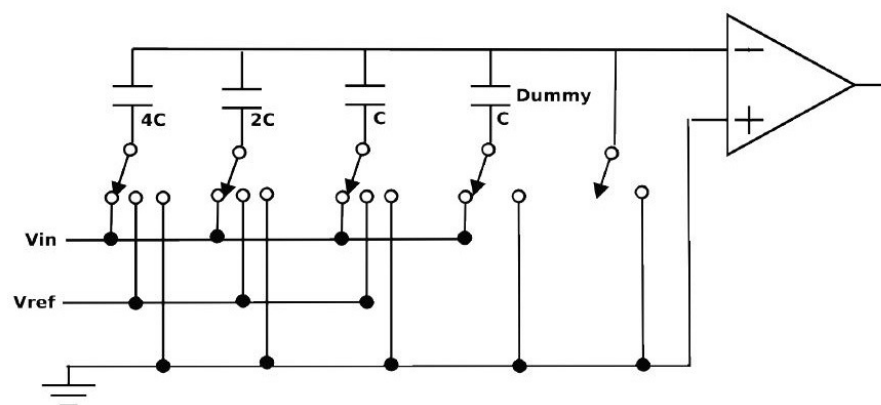
(b) Conventional internal DAC stage.

Figure 1. Conventional and proposed SAR architecture and conventional internal DAC stage.

4. Proposed Architecture

The presented architecture aims to eliminate the mismatches introduced during fabrication process by replacing the conventional internal DAC based on capacitor networks by a digital PWM modulator circuit and a first order low pass filter.

Figure 1 shows the block diagram of the proposed architecture (dotted line) as a modification on a conventional one (full line).

A PWM signal can be stated in terms of an even function, as illustrated in Figure 2 [1]. By using Fourier series, it can be represented in terms of equations (1) to (4).
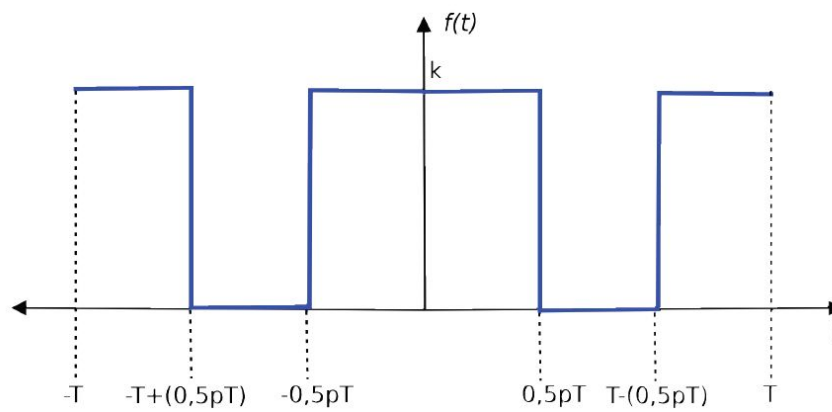

Figure 2. PWM signal stated as an even function.

$$f(t) = A_0 + \sum_{n=1}^{\infty} [A_n cos(\frac{2n\pi t}{T}) + B_n sin(\frac{2n\pi t}{T})] \tag{1}$$

$$A_0 = \frac{1}{2T}\int_{-T}^{T} f(t)dt \tag{2}$$

$$A_n = \frac{1}{2T}\int_{-T}^{T} f(t)cos(\frac{2n\pi t}{T})dt \tag{3}$$

$$B_n = \frac{1}{2T}\int_{-T}^{T} f(t)sin(\frac{2n\pi t}{T})dt \tag{4}$$

where A_0 represents the fundamental frequency, A_n states the even harmonics and B_n states the odd harmonics.

By performing the integral on a PWM signal with amplitude *(f(t)=k)*, the results are given by equations (5) to (7).

$$A_0 = kp \tag{5}$$

$$A_n = k\frac{1}{n\pi}[sin(n\pi p) - sin(2n\pi(1-\frac{p}{2}))] \tag{6}$$

$$B_n = 0 \tag{7}$$

where p denotes the duty cycle.

That result shows that the PWM signal consists of a DC level and a square wave of zero average, as illustrated in Figure 3. Only the DC level is necessary in order to implement an internal DAC stage, since any DC level varying from zero to k can be obtained by selecting the proper duty cycle.
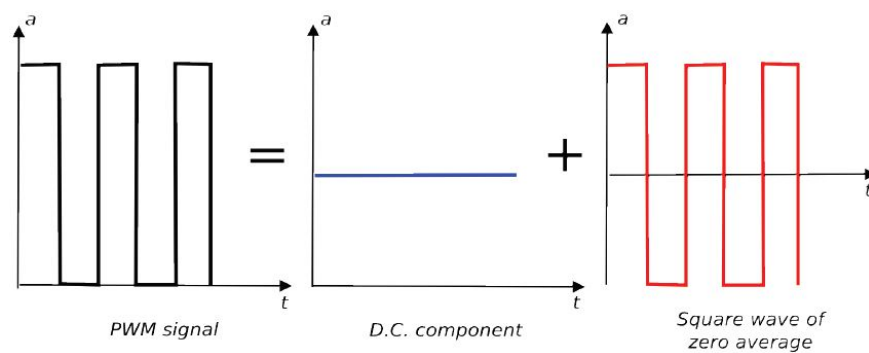

Figure 3. PWM signal split in a D.C level plus a square wave.

A way of recovering the DC level is to low pass filter the PWM signal. Since there is no ideal filter, the recovered DC level will have a certain ripple, as illustrated in Figure 4.
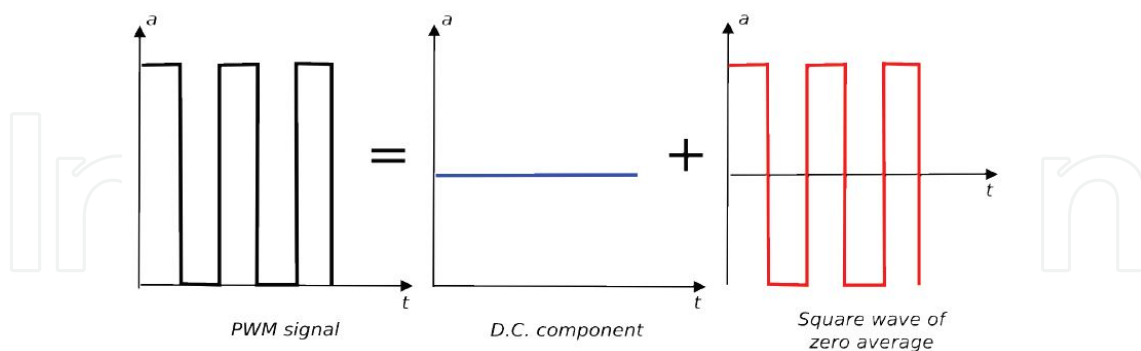

Figure 4. Low pass filtering the PWM signal.

4.1 Modeling

This section provides the modeling of a *4 bit* A/D Converter. Functional models for the SAR, PWM generator, Low pass filter and comparator blocks are discussed. Also the equating necessary to determine the filter features and clock frequencies is developed. SAR and PWM

generator digital circuits are modeled using VHDL hardware description language. Comparator and the first order low pass filter are modeled using compartmental blocks.

A macro level simulation is performed using MatLab in order to validate the architecture. Electrical and post layout simulations are performed using Spectre simulator. The A/D converter Layout is developed in *0.5 μm* standard CMOS process using Cadence Virtuoso and NCSU Design Kit (Free design kit available from North Caroline State University).

4.1.1 Successive Approximation Digital Logic

The Successive Approximation logic evaluates every digital word output bit according to the clock (CLK) signal. Thus, initiating by the most significant bit, one by one, the bits are evaluated and determined, until the last significant bit. Figure 4 illustrates the SAR digital circuit. The control logic is based on a simple shift register. There is also a flip-flop array that stores the input selection (SEL) that is attached to the comparator output.

On a reset (RST) signal, the shift register is loaded with 10000 and the flip-flop array is loaded with 0000. The combinational logic based on OR gates assures the value 1000 at the output (Q_3-Q_0). When the first clock pulse arrives, the shift register value is changed to 01000 while the flip-flop array remains with the same value, except for the most significant bit, since it has been already determined. Thus, the SAR output will show something like *X000*, where *X* represents the previously determined value.

One special feature is to use an extra flip-flop in the shift register to indicate the end of conversion (END), enabling the converted digital word to be read in the rising edge of the fifth clock pulse.
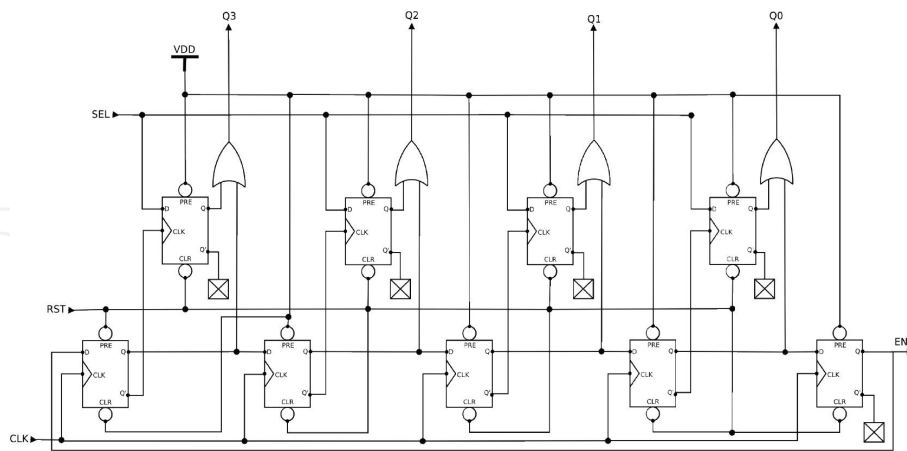

Figure 5. Successive Approximation Register.

4.1.2 Low Pass Filter

Circuits powered by *2.5V* using a *0.5 μm* standard CMOS process, as in this case, can operate at *2MHz* maximum frequency, limiting the operation to about *200 Hz* of sampling rate, re-

garding the proposed architecture design. These feature lead to a high value of capacitance in the RC first order low pass filter, which is impracticable to be integrated. An alternative used to validate the proposed architecture is the implementation of an external first order RC low pass filter, as show in Figure 6.

4.1.3 Digital PWM Modulator

The digital PWM modulator circuit is capable of varying the duty cycle of the output (PWM) according to the digital input word (D_3™ D_0). The circuit is illustrated in Figure 7 and consists of registers, a synchronous *4-bit* counter, a combinational reset and a combinational comparison logic.
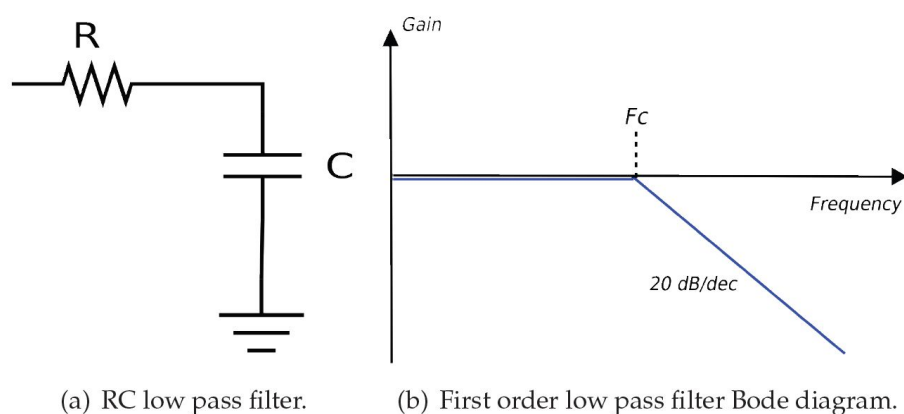

(a) RC low pass filter.   (b) First order low pass filter Bode diagram.

Figure 6. External RC first order low pass filter.

On a reset (RST) pulse, the counter resets to *0000* and the registers store the input word. The counter is incremented at every clock (CLK) cycle and the comparison logic assures that the output remains set while the counter does not reach the value stored into the registers. When it occurs, the output resets and the count continues until the counter reaches the end of counting. The reset logic makes the output flip-flop to set every time the counter resets, thus assuring that the output is set at the beginning of the counting. At this time, the registers are updated with the value present in the input (D_3- D_0) from the SAR output. The reset logic also has a flip-flop responsible for synchronizing the output of the AND gate to the clock signal, since the AND inputs arrive at different timings.

4.1.4 Inverter Based Comparator

The inverter based comparator circuit is used in order to decrease power consumption, since there is no quiescent power consumption. Figure 8 illustrates the comparator stage that uses a low power consumption architecture [7].

The circuit uses lagged clock signals to avoid overlapping, therefore assuring that the switches S_1, S_2 and S_3 do not close at the same time. At time ϕ_1, the switch S_2 is open and the switches S_1 and S_3 are closed, thus charging the capacitor C with V_{in}-V_{th}, where V_{th} is the in-

verter threshold voltage. Consequently any voltage variation during time ϕ_2 will be sensed by the inverter.

At time ϕ_2, the switches S_1 and S_3 are open and S_2 is closed, thus applying to the capacitor C the voltage produced by the PWM generator. This produces a voltage variation in the inverter input and the comparator makes the decision.

The switches S_1, S_2 and S_3 were replaced by solid state switches based on a nMOS transistor. After passing through a booster circuit, the clock signal is applied to the transistors gates.

4.1.5 Equating

The previous subsections illustrated the functional models for each stage of the proposed *4-bit* A/D converter. Nevertheless is still necessary to determine the low pass filter features and the clock frequency for the digital stages, SAR, comparator and PWM generator.

The comparator must evaluate every time the SAR tests a new bit, so they have to be synchronized by the same clock signal. Assuming that all N bits must have to be determined before a new sampling begins, equation (8) states the clock frequency for the comparator and the SAR stage.
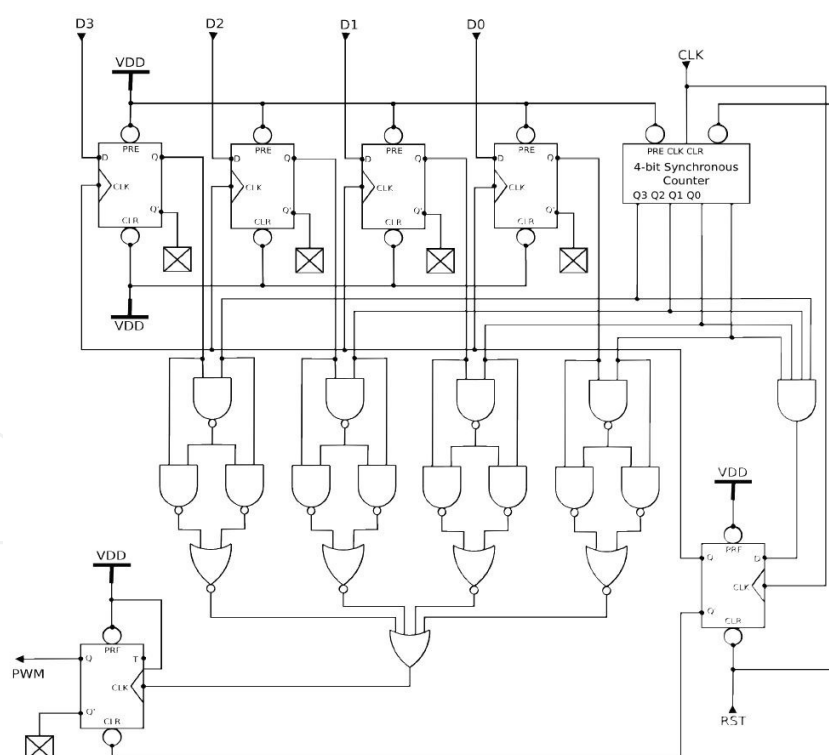

Figure 7. Digital Pulse Width Modulation generator.

$$f_{SAR} \geq f_s \times N \tag{8}$$

where N represents the shift register number of bits, including the EOC bit and f_s represents the sampling rate.

Now, the low pass filter time constant ought to be determined. Equation (9) shows the cut off frequency for the first order filter.

$$f_c = \frac{1}{2\pi\tau} \tag{9}$$

where f_c represents the cut of frequency and τ states the filter time constant.

Assuming $5\,\tau$ to accommodate a signal, equation (9) can be rewritten as equation (10)

$$f_c = \frac{1}{2\pi 5\tau} \tag{10}$$

From Figure 1, it can be observed that the filter must respond faster or at least at the same rate the SAR tests each bit. Thus, equation (11) states the maximum time constant for the low pass filter.
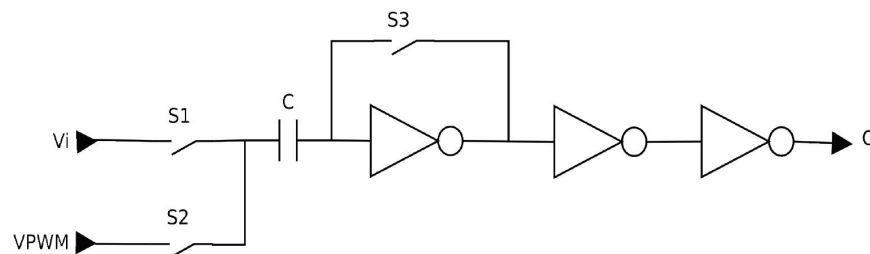
$$\tau \leq \frac{1}{2\pi 5 f_{SAR}} \tag{11}$$

Figure 8. Inverter comparator circuit.

The frequency of the PWM signal must have to be characterized in order to be properly filtered. Since there is no ideal filter, the filtered signal will present a ripple. The PWM signal can be stated in terms of DC level and a sum of even harmonics, as in 12.

$$F_{PWM}(t) = A_0 + \sum_{n=1}^{\infty} A_n cos(\frac{2n\pi t}{T}) \tag{12}$$

Taking into account only the even harmonics, as stated in 13, the energy carried by them can be determined.

$$g_n(t) = A_n cos(\frac{2n\pi t}{T}), \quad n = (0, 1, 2, ...) \tag{13}$$

It is known that the energy is proportional to $\left(g_n^2(t)\right)$. The maximum energy occurs at $\frac{\partial}{\partial p}g_n^2(t)=0$. Thus:

$$
\begin{aligned}
\frac{\partial}{\partial p}g_n^2(t) &= \frac{\partial}{\partial p}\left(A_n^2 cos^2\left(\frac{2n\pi t}{T}\right)\right) \\
&= cos^2\left(\frac{2n\pi t}{T}\right)\frac{\partial}{\partial p}(A_n^2) \\
&= cos^2\left(\frac{2n\pi t}{T}\right)2A_n\frac{\partial}{\partial p}(A_n)=0
\end{aligned}
\tag{14}
$$

Equation 14 shows that the cosine term is independent of the duty cycle p and that the maximum energy occurs when $\frac{\partial}{\partial p}A_n=0$, as shown in 15.

$$
\begin{aligned}
\frac{\partial}{\partial p}A_n &= \frac{\partial}{\partial p}\left(\frac{1}{n\pi}[sin(n\pi p)-sin(2n\pi(1-\frac{p}{2}))]\right) \\
&= cos(n\pi p) + cos(2n\pi(1-\frac{p}{2})) \\
&= cos(n\pi p) + cos(2n\pi - n\pi p) \\
&= cos(n\pi p) + cos(2n\pi)\cdot cos(n\pi p) + sin(2n\pi)\cdot sin(n\pi p)=0
\end{aligned}
\tag{15}
$$

It can be observed that $cos(2\ n\ \pi)$ is unity for any value of n, the term $sin(2\ n\ \pi)$ is zero for any value of n. Thus, equation 15 can be rewritten in terms as 16.

$$
\frac{\partial}{\partial p}A_n=2cos(n\pi p)=0
\tag{16}
$$

Equation 16 shows that the maximum energy in each harmonic is obtained at different duty cycles.

Since there is no ideal filter, after the low pass filtering, the harmonics will not be completely eliminated, but attenuated. It is necessary to evaluate the minimum attenuation required by system, once it is directly linked to ripple amplitude present in the filtered DC level.

Since the first harmonic caries the most energy, it is reasonable to take just it into account to characterize the low pass filter.

Thus, considering the first harmonic ($n=1$) and the maximum energy scenario $\left(p=\frac{1}{2}\right)$, isolating the first harmonic term $A_n cos\left(\frac{2n\pi t}{T}\right)$, the maximum ripple expression can be expressed by 17. Figure 9 illustrates the PWM signal, where h_1 represents the ripple amplitude variation given by the first harmonic.

$$
h_1=\frac{2k}{\pi}cos\left(\frac{2n\pi t}{T}\right)
\tag{17}
$$

It is important to notice that the cosine term introduces a variation interval of $-\dfrac{2k}{\pi} \leq \dfrac{2k}{\pi}$ in the ripple amplitude. Equation 18 shows the maximum peak to peak variation.

$$h_{1_{pp}} = \frac{2k}{\pi} - \left(-\frac{2k}{\pi}\right) = \frac{4k}{\pi} \tag{18}$$

Figure 9 illustrates two sequential quantization levels defined by the filtered PWM signal. If the ripple present in two sequential quantization levels overlaps, the converter will lead to a wrong conversion.
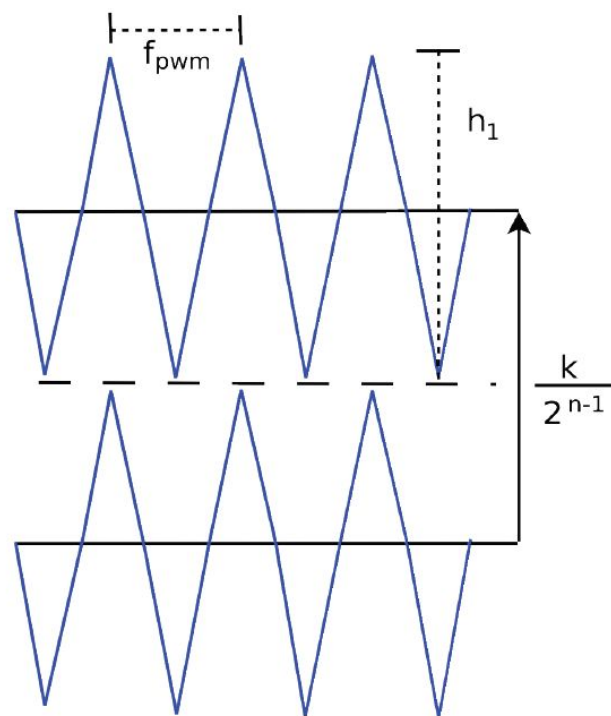

Figure 9. Maximum ripple amplitude.

Thus, equation (19) states the minimum attenuation necessary to keep ripple under an acceptable value.

$$-h_{1_{pp}} A \leq \frac{k}{2^{N-1}}$$

$$-\frac{4k}{\pi} A \leq \frac{k}{2^{N-1}}$$

$$A \geq \frac{\pi}{2^{N+1}} \tag{19}$$

$$A_{dB} \geq 20 log\left(\frac{\pi}{2^{N+1}}\right)$$

Since equation (19) expresses the attenuation in *dB*, the easier way to determine the PWM frequency is to plot the Bode diagram of the previously designed low pass filter and look directly into the frequency that provides the minimum necessary attenuation, as shown in Figure 10. Higher attenuation will decrease the ripple amplitude assuring the correct behavior of the A/D converter and a maximum attenuation is limited by the maximum frequency achieved by the PWM signal.

Finally, the PWM generator design requires a clock frequency 2^{N-1} times greater then output PWM signal, as stated by equation (20).

$$f_{pwm}^{clk} = 2^{N-1} f_{pwm} \qquad (20)$$

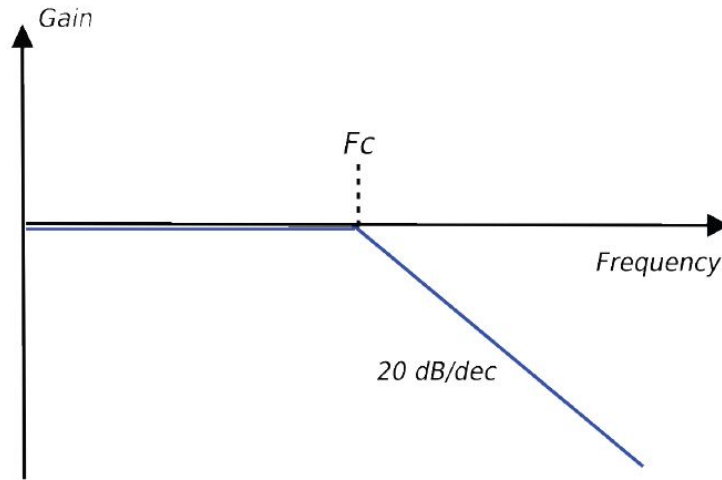where f_{pwm}^{clk} states the clock frequency and f_{pwm} states the PWM signal frequency.

Figure 10. Determining the PWM signal frequency.

5. Simulations

The *4 ™ bit* SAR ADC using PWM technique was designed for the ON *0.5 μ m* CMOS process using Cadence Virtuoso. simulations were conducted on Spectre simulator.

Figure 11 shows the circuit layout that occupies *0.749 mm²*. The main simulation results are given in table I.

It can be observed that the proposed architecture improved the A/D Converter accuracy, since the DNL and INL values are less then 0.1 LSB and also that it consumes low power.
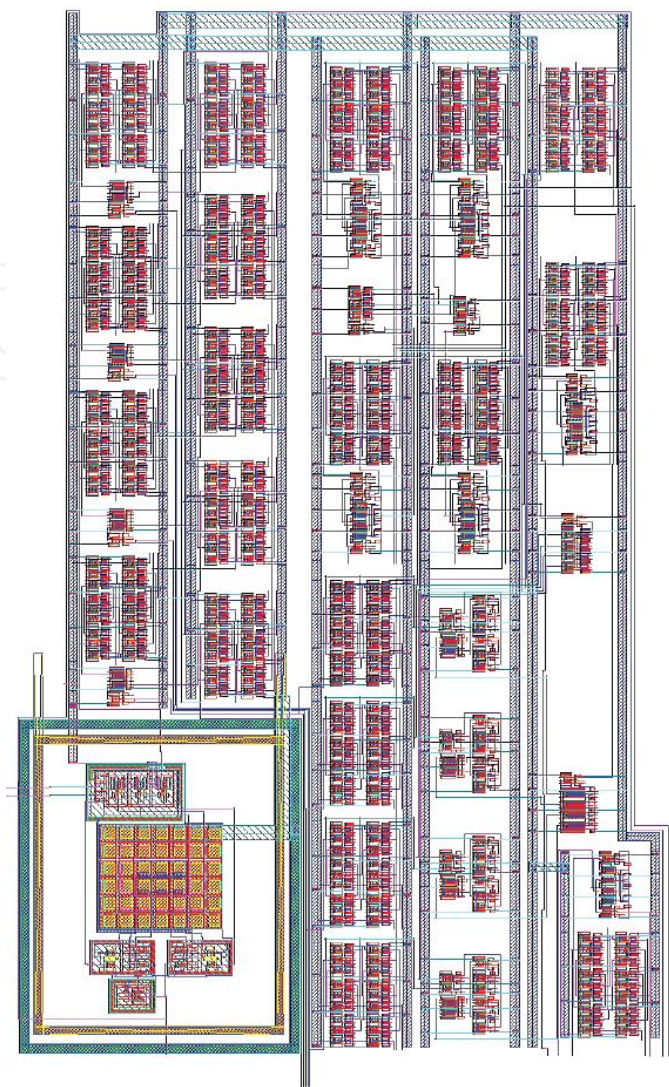
Figure 11. Circuit layout.

Technology	0.5 um
Supply Voltage	2.5 V
Max. Sampling frequency	200 Hz
ENOB (@166.67 Hz)	3.7549-b
DNL(max)	0.086 LSB
INL(max)	0.99 LSB
Power Consumption	16 uW
FoM (Figure of Merit)	7.11 nJ/conv.-step

Table 1. SAR ADC simulated performance.

Figure 12 shows the post layout simulation of DNL and INL for a slow ramp input. The values are good, lower than *0.086 LSB* and *0.1 LSB*, respectively, showing that the characteristic of proposed architecture does not differ too much form the ideal one.
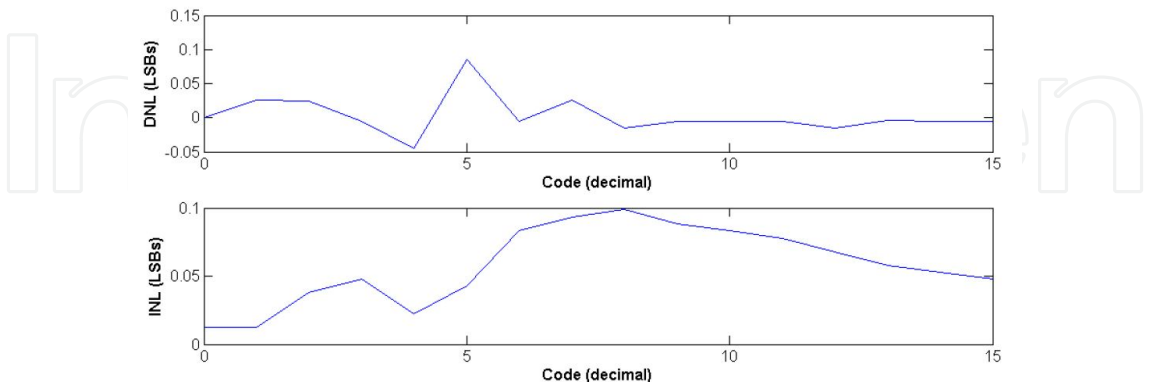

Figure 12. DNL and INL post simulation results.

Figure 13 illustrates the output frequency spectrum for a *32* point DFT. When ADC is tested with sinusoidal input at 166.67 Hz for a 15.63 Hz signal, it gives a good SNDR value of 24.36 dB, which results in 3.7549 effective number of bits (ENOB), thus proving the high accuracy achieved by the proposed architecture.
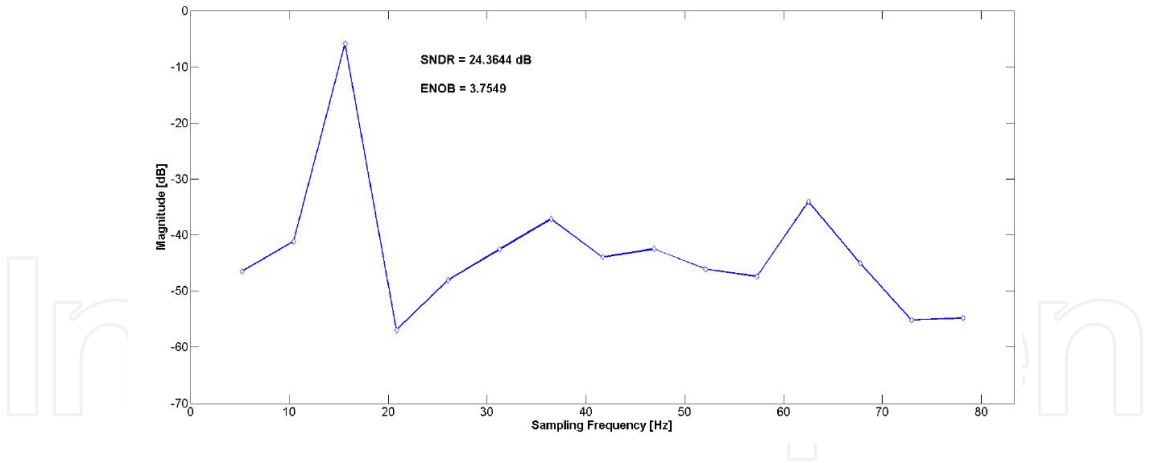

Figure 13. ADC simulated output frequency spectrum.

6. Future Research

The 4-bit layout was fabricated trough MOSIS education program. The prototypes will be tested and the results will be compared to the simulations.

After chip characterization, a proper integrated low pass filter will be implemented in a new prototyping. A new ADC with a larger number of bits will be developed in order to better investigate the non-linearities, ENOB and FoM results.

7. Conclusion

In order to validate the proposed architecture, a *4 ™ bit* SAR A/D converter was designed in *0.5μ m* CMOS standard process. The layout was developed using CADENCE Virtuoso and occupies *0.749 mm²*. Post-layout simulations conducted in Spectre simulator using the BSIM3v3 model show that the modifications introduced in the internal DAC stage contribut- ed to minimize DNL (*0.086 LSB*) and INL (*0.099*) errors, as expected.

They also contributed to improve A/D converter accuracy, since the SNDR was improved to *24.36 dB* of *25.84 dB* maximum theoretical value, leading to *3.75* effective bits.

The feature of being almost fully digital contributes to reduce the circuit complexity, the sili- con area and power consumption.

The features of high accuracy and low power consumption make the proposed architecture suitable for biomedical applications.

This architecture can be extended to build higher resolution converters by only adding more hardware to the digital stages or building pipeline structures.

Author details

Tales Cleber Pimenta[*], Gustavo Della Colletta, Odilon Dutra, Paulo C. Crepaldi,
Leonardo B. Zocal and Luis Henrique de C. Ferreira

*Address all correspondence to: tales@unifei.edu.br

Universidade Federal de Itajuba-UNIFEI, Brazil

References

[1] Alter, D. M. (2008). Using pwm output as a digital-to-analog converter on a tms320f280x digital signal controller. Technical report, Texas Instruments.

[2] Eid, E.-S., & El-Dib, H. (2009). Design of an 8-bit pipelined adc with lower than 0.5 lsb dnl and inl without calibration. *Design and Test Workshop (IDT), 2009 4th Interna- tional*, 1-6.

[3] Hoeschele, D. F. J. (1994). Analog-to-Digital and Digital-to-Analog Conversion Techniques. John Wiley e Sons, 2nd edition.

[4] Lin, Y. Z., Liu, C.C., Huang, G. Y., Shyu, Y. T., & Chang, S. J. (2010). A 9-bit 150-ms/s 1.53- mw subranged sar adc in 90-nm cmos. *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*, 243-244.

[5] Lu, T. C., Van, L. D., Lin, C. S., & Huang, C.-M. (2011). A 0.5v 1ks/s 2.5nw 8.52-enob 6.8fj/conversion-step sar adc for biomedical applications. *Custom Integrated Circuits Conference (CICC), 2011 IEEE*, 1-4.

[6] Mesgarani, A., & Ay, S. (2011). A low voltage, energy efficient supply boosted sar adc for biomedical applications. *Biomedical Circuits and Systems Conference (BioCAS), 2011 IEEE*, 401-404.

[7] Mikkola, E., Vermeire, B., Barnaby, H., Parks, H., & Borhani, K. (2004). Set tolerant cmos comparator. *Nuclear Science, IEEE Transactions on*, 51(6), 3609-3614.

[8] Ng, K., & Chan, P. (2005). A cmos analog front-end ic for portable eeg/ecg monitoring applications. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 52(11), 2335-2347.

[9] Talekar, S., Ramasamy, S., Lakshminarayanan, G., & Venkataramani, B. (2009). A low power 700msps 4bit time interleaved sar adc in 0.18um cmos. *TENCON 2009-2009 IEEE Region 10 Conference*, 1-5.

[10] Zou, X., Xu, X., Yao, L., & Lian, Y. (2009). A 1-v 450-nw fully integrated programmable biomedical sensor interface chip. *Solid-State Circuits, IEEE Journal of*, 44(4), 1067-1077.