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All-Optical Autonomous First-in–First-out Buffer Managed with Carrier Sensing of Output Packets

Hiroki Kishikawa, Hirotaka Umegae,
Yoshitomo Shiramizu, Jiro Oda, Nobuo Goto and
Shin-ichiro Yanagiya

Additional information is available at the end of the chapter

1. Introduction

Along with rapid progress of optical fiber links in the physical layer of networks, optical processing in the control layer such as data links and internet layers is expected to realize photonic networks. Various kinds of architectures of optical routers and switches have been exploited. Optical buffering is one of the indispensable key technologies for avoiding packet collision in these network nodes.

Various optical buffering systems have been reported [1,2]. Most of them consist of optical fiber delay lines (FDLs). Although optical slow light can be a potential candidate to adjust short delay timing [3,4,5], FDLs are regarded to be most useful elements for packet buffering. Basically, two kinds of architectures of buffers with FDLs have been considered. One is a feedforward architecture, consisting of parallel FDLs that have different lengths corresponding to desired delay times. A combination of input and output buffered switch [6] and multistage FDL buffer [7] were reported as feedforward architectures. The other is an architecture consisting of feedback-looped FDLs. It potentially provides infinite delay time if waveform distortion caused by loss, noise, dispersion etc., is managed to be compensated. However, the FDLs can provide only a restricted function of a finite delay time as buffers because the optical packet cannot be read out during the propagation in the FDLs.

In most of the proposed architectures, electrical processing for scheduling and management has been employed [8-12]. Although flexible control including quality of service (QoS) can be realized using such a control method, simple autonomous control is preferable for simple and low-power consumption buffering.

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We have proposed an autonomous first-in-first-out (FIFO) buffer management system using all-optical sensing of packets [13]. Each of FDLs in the reported system stores a single packet. In this chapter, we describe architecture and operation of the buffering system. The buffering performances such as packet loss rate (PLR) and delay time are evaluated by numerical simulation.

2. Proposed Buffering System

2.1. Architecture of the Buffering System

The proposed buffering system consists of N parallel buffering modules and a combiner as shown in Fig.1. Each module can manage the buffering in autonomous fashion by exchanging the information signals that include utilization of output port as indicated by dashed lines. Packets forwarded by the buffering modules are transmitted to output port through an $N \times 1$ combiner.
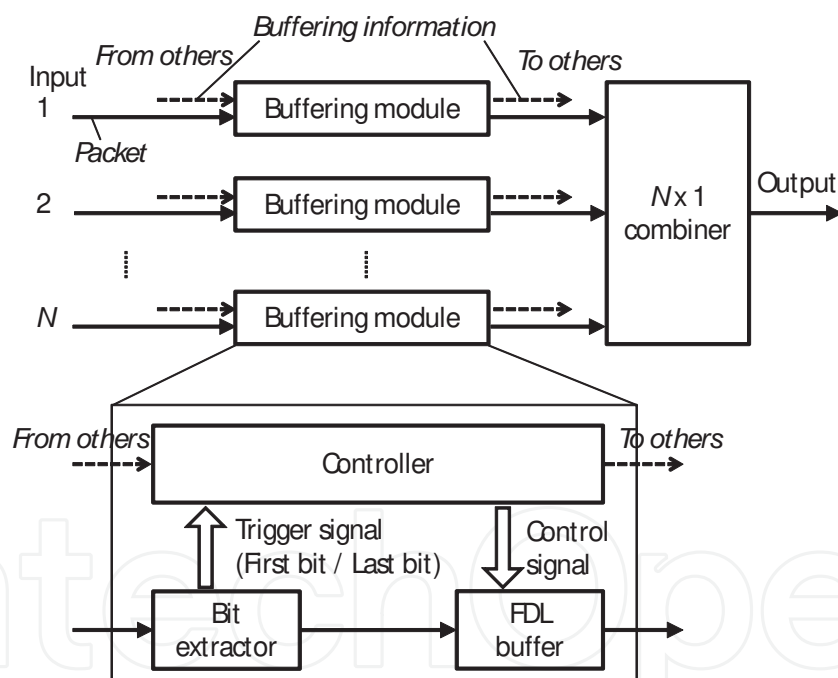

Figure 1. Schematic diagram of proposed buffering system.

The structure of a buffering module is also shown in inset of Fig. 1. It consists of a bit extractor, a controller, and an FDL buffer. The bit extractor creates trigger signal by detecting the first bit and the last bit of incoming packets. The first and last bits can be composed of specific coded bit patterns. Optical code-correlation processing can find the start and the end of the packet as the first and the last bits, respectively. The controller generates control signal autonomously by using the trigger signal. The FDL buffer stores and forwards packets by using the control signal.

2.2. Configuration of the Controller

Figure 2 shows the schematic diagram of the controller composed of four components. Controller A creates timing clock C_1 to be used to open the buffer for storing packets. Controller B creates 'store' signal which indicates the actually storing FDL in the buffer. Controller C creates another timing clock C_2 to be used to forward the already stored packets. Controller D creates 'forward' signal and the buffering information to other modules which indicates whether the buffer is now forwarding packets or not.

Figure 3 shows the configuration of controller A. Timing clock C_1 corresponds to the extracted first bit of incoming packets. The extracted last bit is not used in this case. However, it is reserved for future enhancement of the buffering system.
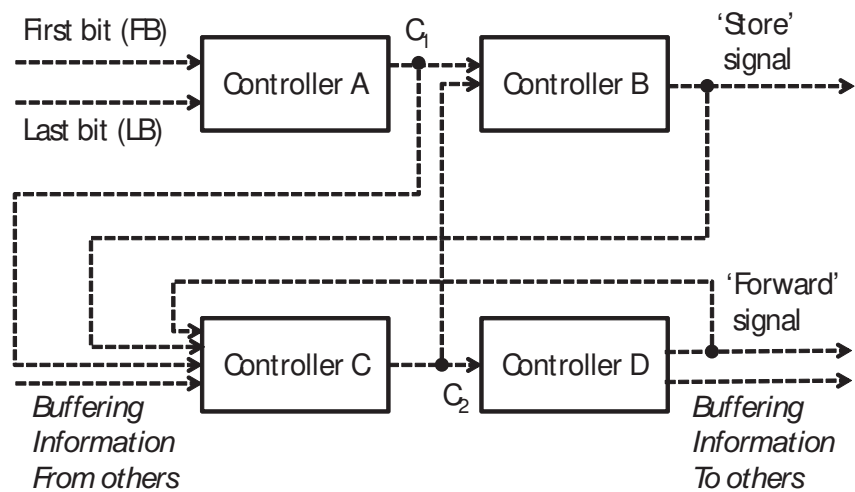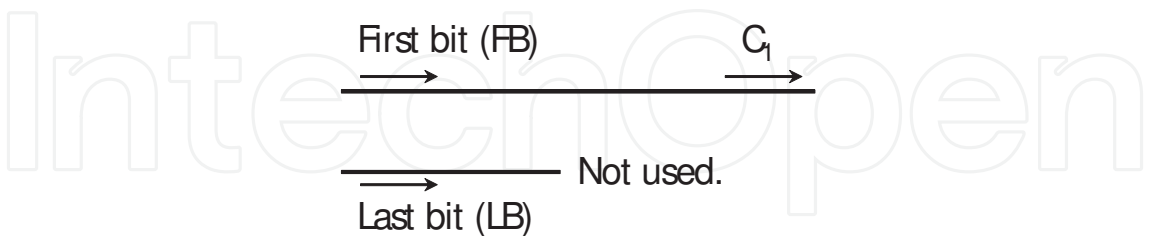

Figure 2. Schematic diagram of the controller.

Figure 3. Configuration of controller A.

Figure 4 shows the configuration of controller B. It autonomously generates 'store' signals by processing C_1 and C_2. The number of 'store' signals is $M+1$ where M corresponds to the number of FDLs in the buffer. In order to indicate actual storing position, none or only one of the 'store' signals becomes on-state. When C_1 comes, position of on-state moves up from #1 to #($M+1$), namely, initially all off-state turns to #1-on, then moves to #2-on, #3-on, and so

on. On the contrary, when C_2 comes, position of on-state moves down from #(M+1) to #1. There are some delay lines with delay time of T_{FIFO}-T_1 and T_1, where T_{FIFO} and T_1 are delay of single FDL in the buffer and 1-bit, respectively. Note that these components are expressed by some sort of logic circuits. Although it depends on the function and the performance such as operating speed, power consumption, and footprint, both electrical and optical logic circuits might be candidates to be employed.

Figure 5 shows the configuration of controller C. It autonomously generates C_2 by processing C_1, 'store' signal, buffering information signals from other modules, and 'forward' signal mentioned below. The operation of controller C is similar to the FDL buffer for packets. Therefore, we describe the detailed operation in the latter section about FDL buffer.

Figure 6 shows the configuration of controller D. It autonomously generates 'forward' signal by processing C_2. The 'forward' signal keeps on-state for a period of T_{FIFO} by using the flip-flop triggered by C_2.
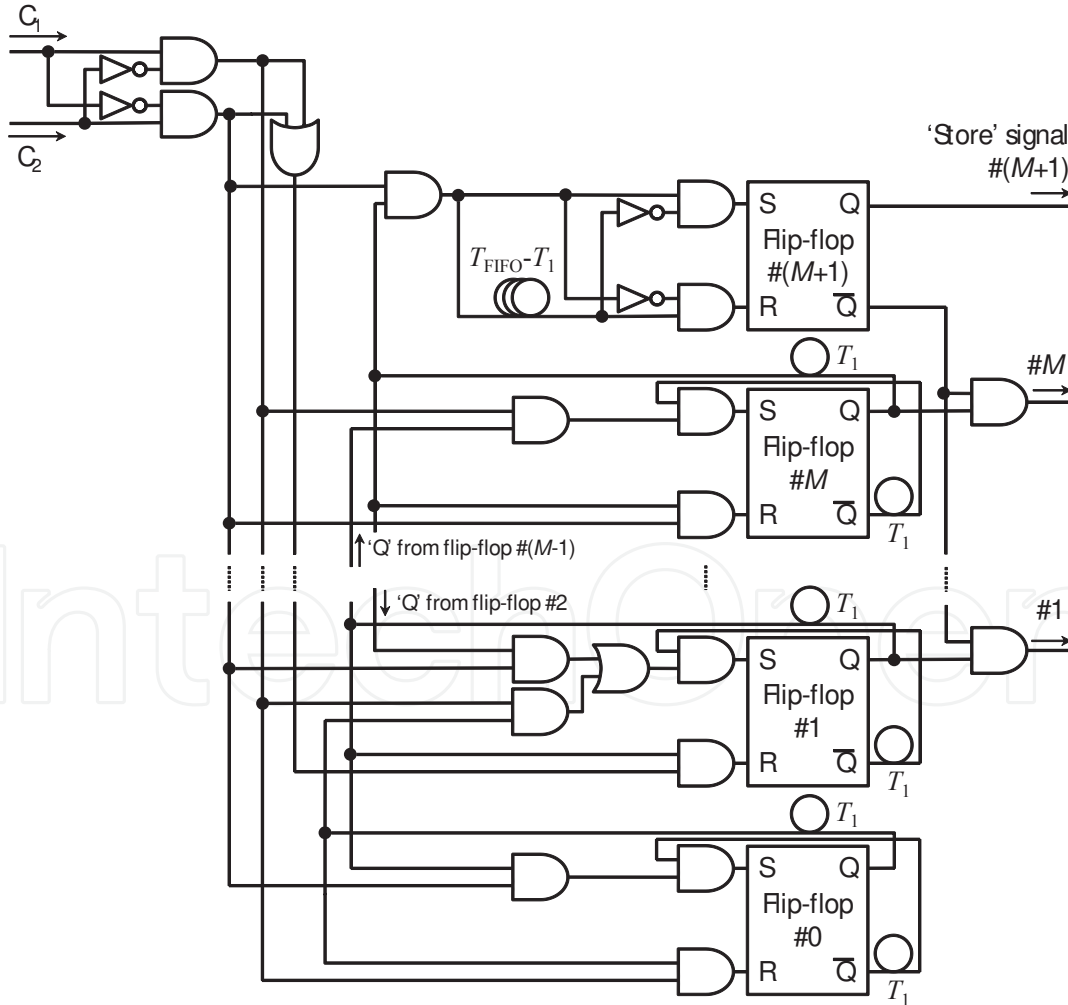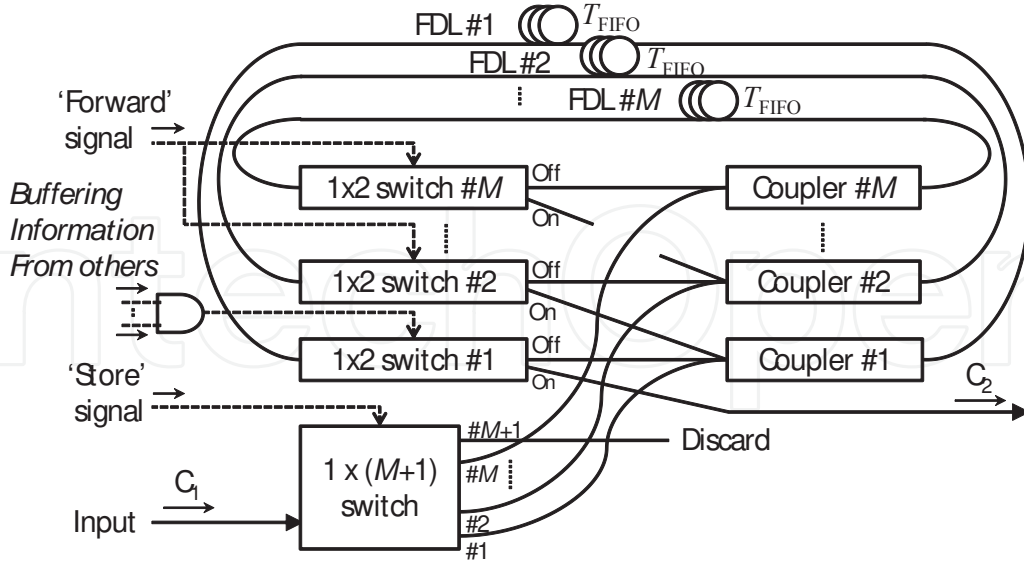

Figure 4. Configuration of controller B.

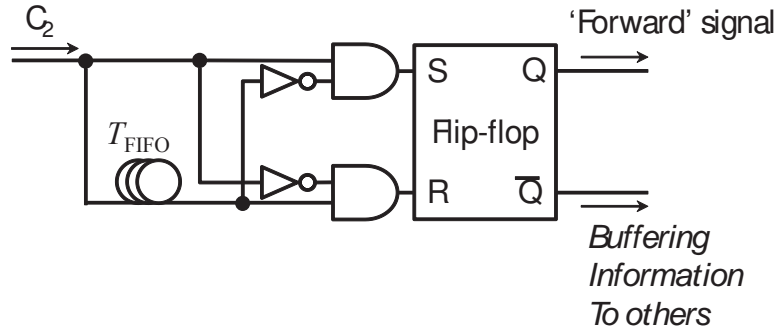**Figure 5.** Configuration of controller C.

Figure 6. Configuration of Controller D.

2.3. Configuration of the FDL Buffer

The FIFO buffer consists of M parallel FDLs that have delay time of T_{FIFO}, a $1 \times (M+1)$ input switch, $M1 \times 2$ output switches and couplers as shown in Fig. 7. The buffer stores and forwards packets by using 'store' and 'forward' signals, respectively. The stored position is determined by the state of 'store' signal. Namely, when k-th signal is on-state ($k=1,..,M$), incoming packets are switched to k-th FDL by the input switch. In case that $(M+1)$-th signal is on-state, then incoming packets will be discarded because all of the FDLs have already been occupied with other packets. The stored packets are forwarded to output by controlling the output switches. When the 'forward' signal is incident, all of the output switches move the stored packets to next neighbor FDLs. Note that T_{FIFO} is designed to be greater than or equal to the maximum packet length.
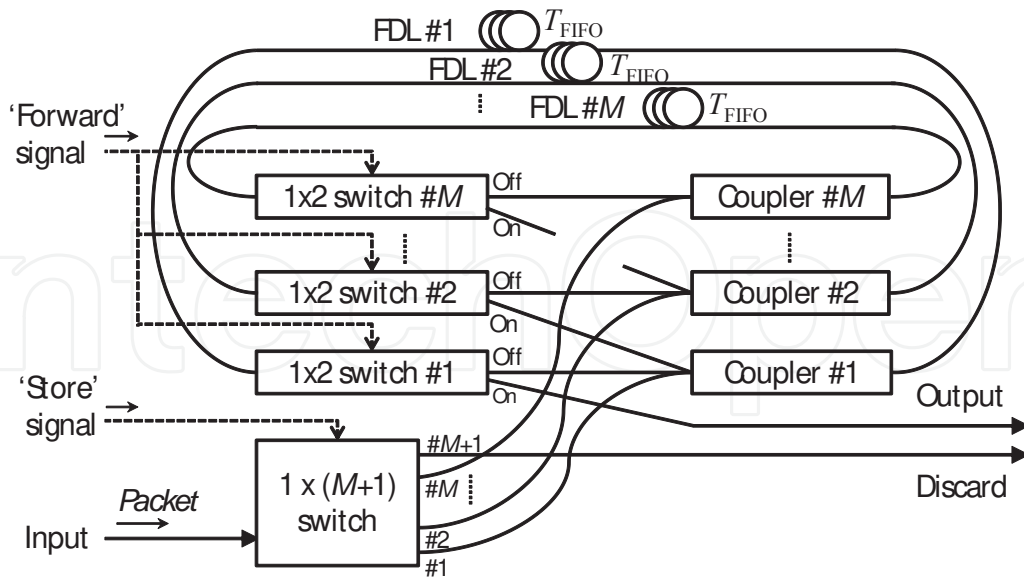
Figure 7. Configuration of the FDL buffer.

2.4. Operation Overview of Buffering

An example of timing chart for buffering process of a module is shown in Fig. 8.
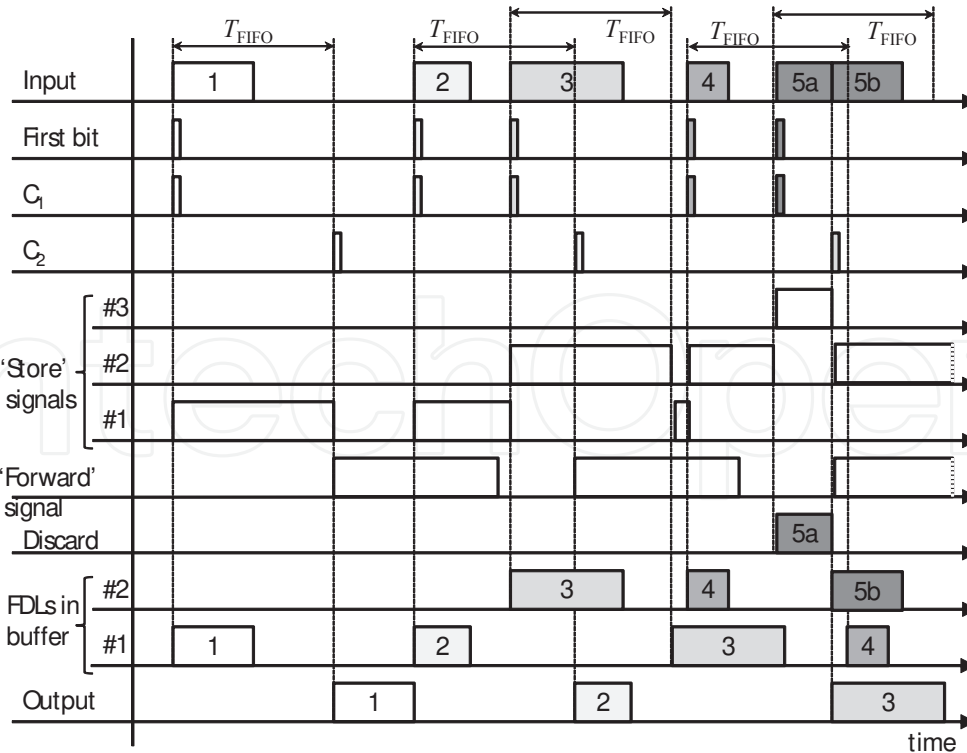

Figure 8. Timing chart example of a module of the buffer.

We assume that there are initially no packets stored in the FDLs, and then five packets are arriving sequentially with random timing and variable lengths. The number of FDLs M is assumed to be M=2.

When packet no.1 is incident, 'store' signal #1 turns on triggered by the first bit and C_1. The state of the 'store' signal is kept for a period of T_{FIFO}. When T_{FIFO} is expired, 'forward' signal turns on triggered by the C_2. Then, stored packets no.1 is forwarded to output. If another module has already been open for forwarding, the 'forward' signal of this module does not turn on in order to avoid collision between this module and the forwarding module. When packet no.3 is incident before the expiration period T_{FIFO} of packet no.2, it is stored into another FDL because each FDL is designed for storing only a single packet.

Although similar operation can be seen for following packets, packet no.5 is slightly different. The front part of it is discarded because all FDLs have already been occupied by other packets. When packet no.3 is forwarded, FDL #2 is open for storing. At the moment, the rear part of packet no.5 is stored into there. Note that the packet no.5 is therefore treated as a broken packet when it gets out from the buffer.

3. Computer Simulation

Two kinds of characteristics such as packet loss rate (PLR) and average delay time are investigated by computer simulation. We assume in the simulation that packets arrive randomly and have variable lengths from L_{min}=10 to L_{max}=150 bytes. We define load at input port by the ratio of the packet existence length to a unit length. For simplicity, operation speed of the composed devices, such as switching speed of some spatial switches and flip-flops, rise time of logic gates, are assumed to be much faster than bit-rate of arriving packets. Therefore, bit-rate is not specified in our simulation.

3.1. Packet Loss Rate

The PLR is verified with changing the number of FDLs M, length of each FDL L, number of input N, and the load. Because of a finite number of FDLs in the buffer system, overflow may occur when the load exceeds the capacity of the buffer, resulting in rejection of the overflowed packets. Even if the load is less than the capacity, collision of packets may occur when packets forwarded by some modules are simultaneously coming into the following combiner as shown in Fig.1. Therefore in the simulation, the overflow and the collision are both treated as loss of packet.

Figure 9 shows the PLR as a function of the load at module #1 with the number of FDLs M as a parameter. The number of modules is N=2. The load of the module #2 is set to 0.5. The length of each FDL is L=L_{max}. It is found that the PLR increases with load at module #1. Moreover, the PLR decreases when M increases.

Figure 10 shows the PLR as a function of the load at module #1 with the length of FDLs L as a parameter. The number of modules is N=2. The load of the module #2 is set to 0.5. The

number of FDLs is M=10. It is found that the PLR increases both with load at module #1 and L. This is because incoming packets are separately stored in different FDLs, resulting in many FDLs are occupied with unused space remained. When L becomes long, the duration of occupation becomes long, and then it takes longer time to get out from the buffer. Therefore, it may cause the increase of packet loss because of the occupied FDLs.
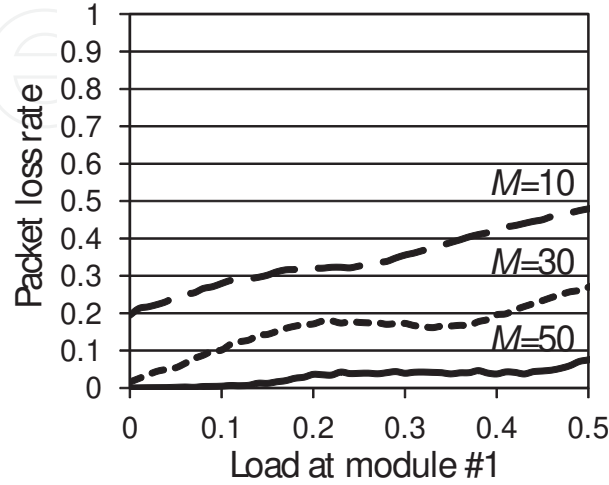
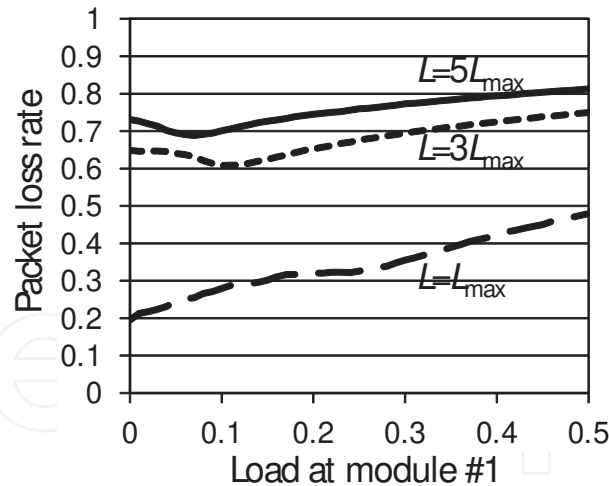

Figure 9. PLR with parameter M.

Figure 10. PLR with parameter L.

Figure 11 shows the PLR as a function of the load at module #1 with the load at module #2 as a parameter. The number of modules is N=2. The number of FDLs is M=30. The length of each FDL is $L=L_{max}$. It is found that the PLR increases with load at module #1 and #2.

Figure 12 shows the PLR as a function of the load at module #1 with the number of module N as a parameter. The number of FDLs is M=30. The length of each FDL is $L=L_{max}$.

Loads of modules other than #1 are all set to 0.3. It is found that the PLR increases with load at module #1 and N.
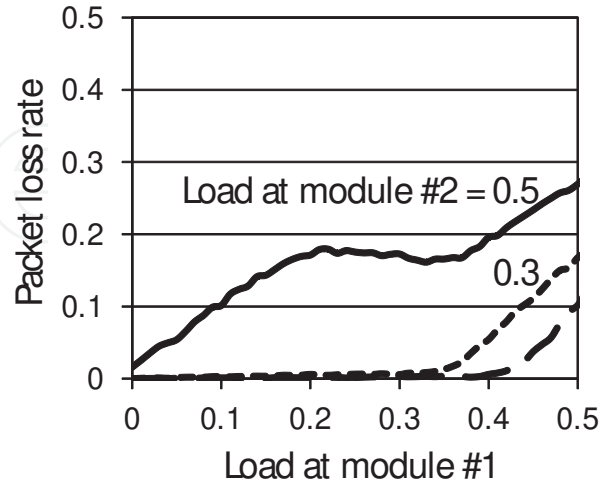

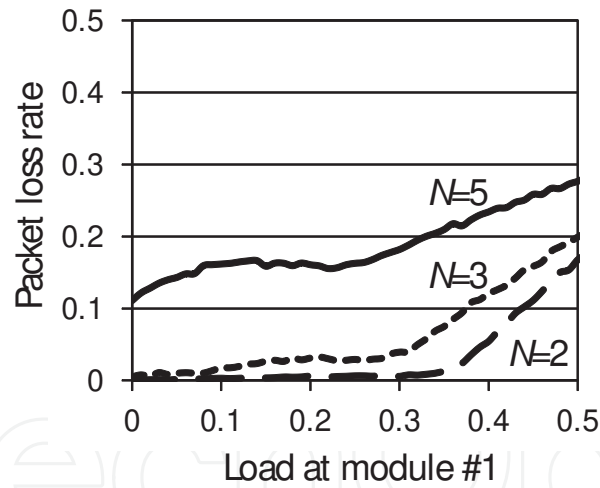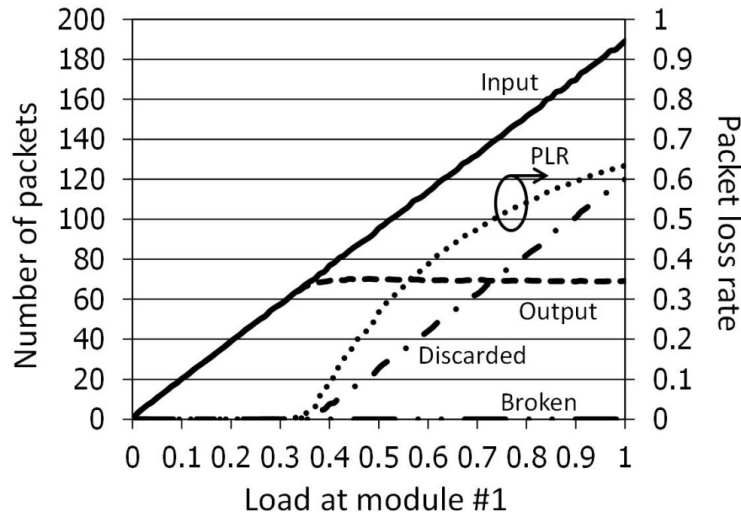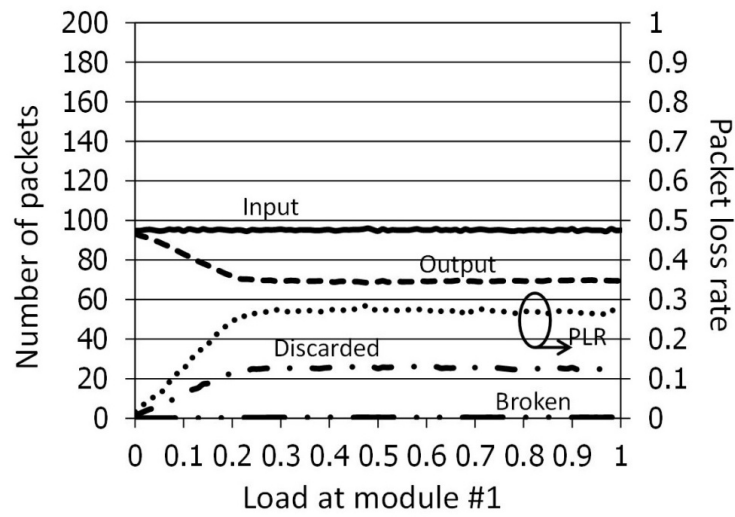**Figure 11.** PLR with parameter load at module #2.

Figure 12. PLR with parameter N.

Figure 13 shows the breakdown of such numbers as input, output, discarded and broken packet in (a) module #1 and (b) module #2. Parameters are set to as follows; the number of modules is N=2, the number of FDLs is M=30, the length of each FDL is $L=L_{max}$, the load of module #1 is changed, and that of module #2 is 0.5 fixed. It is found from Fig. 13(a) that the number of output packets saturates up to 70 when the load at module #1 exceeds 0.3. This is because it starts overflow at that point, namely the number of discarded packets increases in proportion to the input. As a result, the PLR also increases. In case of module #2 shown in Fig. 13(b) that the fixed number of input initially exceeds its overflow limit, and so the num-

ber of discarded packets increases up to a certain value. Then, the number of output decreases to the same level as that of module #1. Therefore, this 2×1 buffer puts the identical output priority to the two modules.

(a) Module #1

(b) Module #2

Figure 13. Breakdown of such numbers as input, output, discarded, and broken packet in each module.

3.2. Average Delay

Packets stored and forwarded through the buffer have been experienced a certain amount of delay determined mainly by the load and parameters M and L. We examine the average delay time by computer simulation.

Figure 14 shows the average delay as a function of the load at module #1 with the number of FDLs M as a parameter. The number of modules is $N=2$. The load of the module #2 is set to

0.5. The length of each FDL is $L=L_{max}$. It is found that the average delay increases with load at module #1 and M.

Figure 15 shows the average delay as a function of the load at module #1 with the length of each FDL L as a parameter. The number of modules is $N=2$. The load of the module #2 is set to 0.5. The number of FDLs is $M=10$. It is found that the average delay increases with load at module #1 and L.
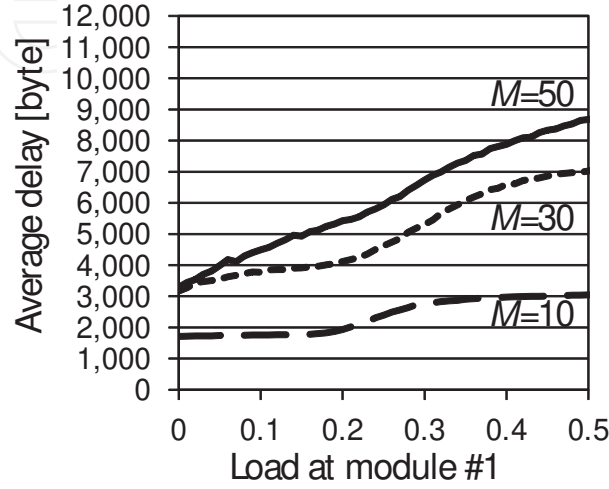

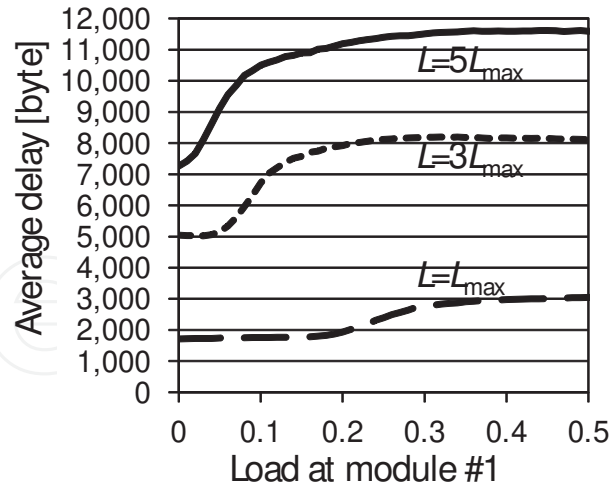**Figure 14.** Average delay with parameter M.

**Figure 15.** Average delay with parameter L.

Figure 16 shows distribution and moving average indicated by dots and solid curves, respectively, of delay time as a function of packet arrival time to each module with loads as parameters. The load of the module #1 is changed between 0.3, 0.5, and 0.7. The load of the module #2 is set to 0.5. The number of modules is $N=2$. The number of FDLs is $M=30$.
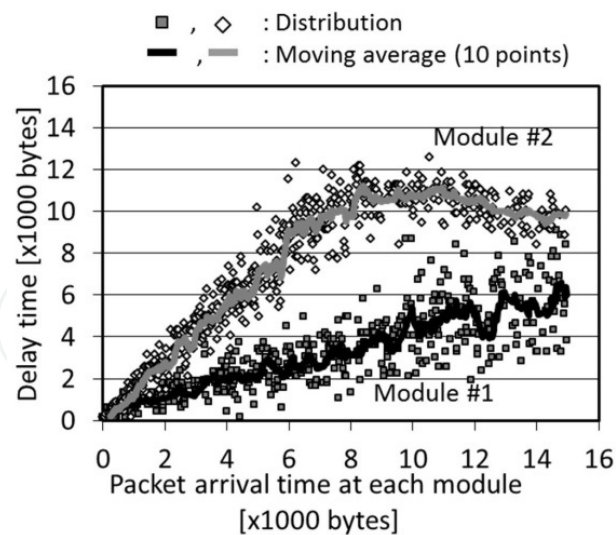
(a)   Load at module #1=0.3, and load at module #2=0.5
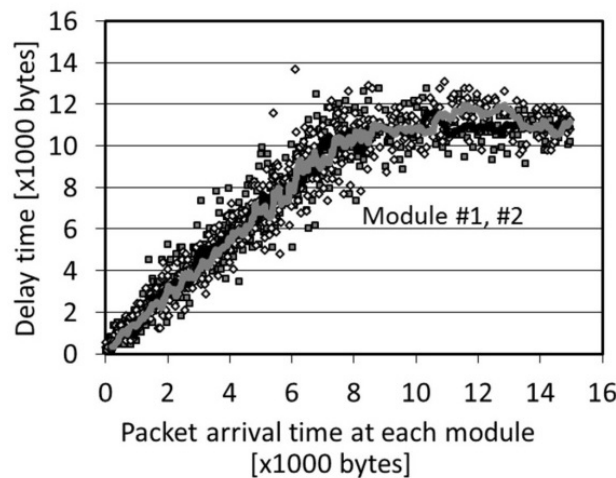
(b)   Load at module #1=0.5, and load at module #2=0.5
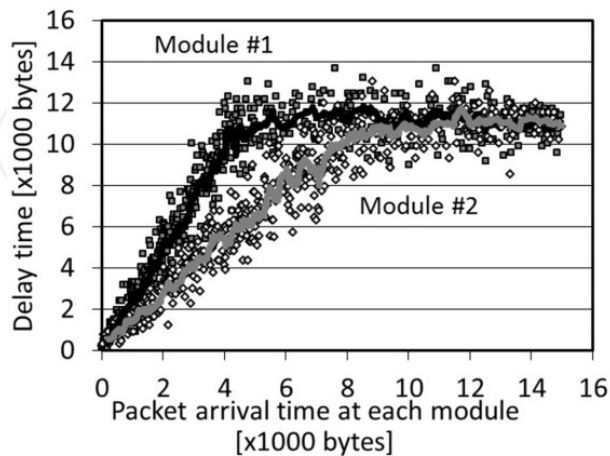
(c)   Load at module #1=0.7, and load at module #2=0.5

Figure 16. Distribution of delay time at each module.

The length of each FDL is $L=L_{max}$. It is found that the delay time shows linear increase with packet arrival time because of the growth of buffer occupation. Moreover, the delay time shows saturation where the buffer occupation comes up to a maximum capacity. In addition, the heavily-loaded module, which corresponds to module #2 at Fig. 16(a) whereas module #1 at (c), shows faster increase and saturation than another module.

4. Conclusion

We have proposed an autonomous first-in-first-out buffer with capability of storing a single packet in each of FDLs. Characteristics of PLR and average delay have been investigated by numerical simulation. As a result, the PLR and the average delay have a trade-off relation at such parameters as number of FDL M and length of each FDL L. Therefore they should be determined by system demand. Smaller M and larger L can be options for implementing the system from viewpoints of footprint, power consumption, and avoid complicated control. Our future works include detailed investigation of buffering performance considering response time in switching and other constituent devices, and experimental verification.

Author details

Hiroki Kishikawa[1], Hirotaka Umegae[1], Yoshitomo Shiramizu[2], Jiro Oda[2], Nobuo Goto[1*] and Shin-ichiro Yanagiya[1]

*Address all correspondence to: goto@opt.tokushima-u.ac.jp

1 Department of Optical Science and Technology, The University of Tokushima, Japan

2 Department of Information and Computer Sciences, Toyohashi University of Technology, Japan

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