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Ion Implantation-Induced Layer Splitting of Semiconductors

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1. Introduction

Ion implantation is considered to be a precise technology for the dopant introduction not only in semiconductors but also in metals and insulators (Plummer et al., 2000; Sze, 1998). The other way of introducing dopants is the plasma treatment (Sze et al., 1998). However, ion implantation in semiconductors is extensively used for various applications in the field of optoelectronics, micro/nano-electro-mechanical systems, power electronics etc (Plummer et al., 2000; Sze, 1998). In particular, ion implantation in silicon (Si) using light ions such as hydrogen (H) has gained significant attention since last two decades (Bruehl, 1995; Tong & Gösele, 1999; Lee et al., 2004). This is because hydrogen in semiconductors, whether introduced intentionally or unintentionally, is known for its role in the defects and dopant passivation (Pankove & Johnson, 1991; Chabal et al., 1999). Moreover, as H in semiconductors is chemically reactive, it influences the transport mechanisms of the charge carriers and ultimately the device performance (Chabal et al., 1999; Höchbauer et al., 2002). The H-implantation in Si started a new era in the electronic industry when it was first time coupled with the direct wafer bonding technique (Bruehl, 1995). This coupled process is now called as ion-cut process, which was commercially employed by SOITEC, France by the name of Smart-Cut™ process. This process came into existence by the end of twentieth century when first time the engineered substrates such as silicon-on-insulator (SOI) were realized (www.soitec.com). Since then SOI technology really helped in boosting the device performance because of its numerous advantages leading to high speed microprocessors, low power consumption, low leakage current, low parasitic and latch-up effects etc (Bruehl, 1995; Tong & Gösele, 1999; Christiansen et al., 2006). After that, the ion-cut process was studied and successfully extended to germanium (Ge) for the fabrication of germanium-on-insulator (GeOI) substrates (Deguet et al., 2006). Since then Si and Ge processing technologies have grown upto high maturity, which are now applied on industrial scale in a regular basis. But, ion-cut process lacks its maturity when it is applied to other semiconductors due to various technical as well as commercial reasons (Radu et al., 2003; Cioccio et al., 1996; Moutanabbir et al., 2010). Nevertheless, this process is experimentally demonstrated on a small scale in silicon carbide (SiC), indium phosphide (InP) and gallium nitride (GaN) (Cioccio et al., 1996; Singh et al., 2010). In the past couple of years the extensive studies have been carried out in understanding the ion-cut process in these and

some other technological important semiconductors, such as (gallium arsenide) GaAs, silicon germanium (SiGe), and aluminium nitride (AlN) (Radu et al., 2003; Singh et al., 2005, 2010). These studies have shown that ion-cut process in these semiconductors still holds promise for potential applications in devices.

1.1 Basics of H-implantation-induced Blistering in Semiconductors

Ion-cut process consists of H-implantation in semiconductors and direct wafer bonding techniques (Bruel, 1995; Christiansen et al., 2006). The implanted H ions induce damage within the semiconductor, which during implantation or after post-implantation annealing results in deformations of the implanted surface (Tong & Gösele, 1999; Hayashi et al., 2008). If these deformations are in the form of surface blisters, then it is referred as surface blistering and if they are in the form of regions from where the implanted surface is completely detached, then it is called surface exfoliation (Fig. 1) (Kucheyev et al., 2001). However, there is no difference between the H-implantation parameters that lead to blistering/exfoliation or layer splitting/layer transfer using direct wafer bonding.

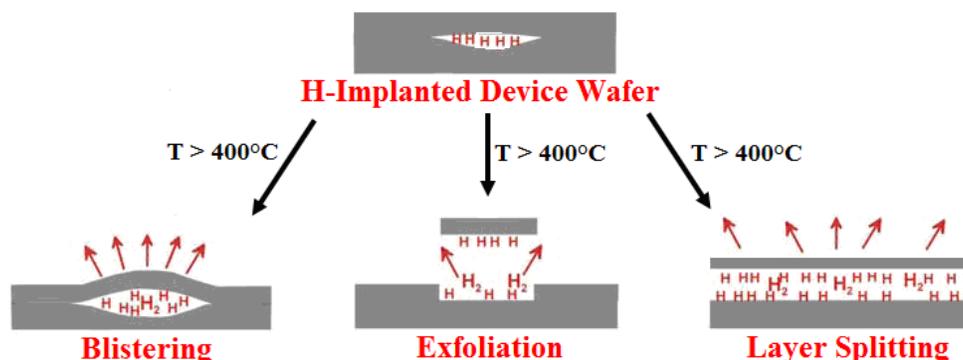


Fig. 1. Schematic illustration of the H-induced surface blistering, surface exfoliation and layer splitting process after post-implantation annealing at elevated temperature (T).

In some cases large area exfoliation, where the implanted surface is completely removed over a large regions, also occurs (Dadwal et al., 2010). The detailed understanding of the hydrogen implantation-induced surface blistering mechanisms is very essential from the prospect of successful application for ion-cut process. H-implantation induces various types of defects within the damage region, which upon annealing agglomerates to extended defects like nanocracks/microcracks (Chabal et al., 1999; Höchbauer et al., 2002). These extended defects act as efficient trapping centres for the implanted H. The implanted H gets segregate into these defects in molecular form, which thereby creates internal pressure and hence takes them to an overpressurized state. When this internal pressure reaches to the fracture limit of the implanted material, it ultimately lifts the implanted surface in the form of surface blistering/exfoliation (Kucheyev et al., 2001; Di et al., 2008; Padilla et al., 2010). However, the detail mechanisms of the surface blistering are very complex and which even in the highly matured SOI technology are still not fully understood (Moras et al., 2010).

1.2 Layer transfer of semiconductors

Hydrogen implantation-induced surface blistering/exfoliation can be extended to the transfer of a thin layer of the implanted semiconductor (donor wafer) onto an appropriate

foreign substrate (handle wafer) using ion-cut process (Höchbauer et al., 2002; Singh et al., 2010). In this process the implanted wafer is bonded to a handle wafer after following the standard wafer cleaning procedure (Tong & Gösele, 1999). Then these bonded wafers are subjected to thermal annealing at elevated temperatures for the sufficient duration. The thermal treatment induces defects migration and agglomeration, which leads to layer cracking parallel to the bonded interface. Hence, it gives transfer of implanted layer from the parent substrate onto the handle substrate (Bruehl, 1995; Tong & Gösele, 1999; Moutanabbir et al., 2010). However, the layer splitting is only possible if bonding energy of the bonded interface between the handle wafer and the implanted layer is much stronger than the implanted layer and the donor wafer. Moreover, one can transfer multiple layers from the single donor wafer by tuning the energy of the implanted H ions. This feature of ion-cut process makes it very attractive in the case where donor wafer is highly expensive and is mostly available in small sizes such as in the case of III-V nitride semiconductors, like GaN and AlN (Kucheyev et al., 2001; Moutanabbir et al., 2010).

1.3 Brief chapter description

This chapter is basically an attempt to shed light and give an overview about the implantation-induced layer splitting of the semiconductors using ion-cut process. The layer splitting is discussed in some of the important compound and conventional semiconductors for the realization of current and new generation technology. This chapter is divided into ten sections including introduction and reference section. Each section is further divided into different subsections. The extensive studies of the layer splitting mechanisms in Si makes ion-cut process highly matured in it and, that is why highly explored in the layer transfer applications (Tong & Gösele, 1999). Therefore, the implantation-induced ion-cut process in Si is not discussed in this chapter. The focus is given to some other technologically important semiconductors such as Ge, SiGe, GaAs, InP, GaN, AlN and other important semiconductors for the understanding of the H-induced layer splitting mechanisms.

2. Ge and SiGe alloys

Ge and its alloy with Si, which is SiGe, are two important materials which have promising applications in the integrated circuits (ICs) technology because of the higher carrier mobility and optimum forbidden bandgap (Singh et al., 2005; Huang et al., 2001). Specifically in Ge, the hole mobility is about $1800 \text{ cm}^2\text{V}^{-1}\text{sec}^{-1}$. Whereas in SiGe, depending upon the concentration of Ge in Si, mobility enhancement of the charge carriers to the values up to $40000 \text{ cm}^2\text{V}^{-1}\text{sec}^{-1}$ could be achieved in the modulation doped structure of the strained Si (sSi) on silicon germanium-on-insulator (SGOI) (Huang et al., 2001). The process of H-implantation-induced layer splitting was used to transfer thin layers of Ge and SiGe without investigating its dependence on the implantation temperatures. Therefore in the following subsections we have discussed temperature dependent behaviour of the H-induced layer splitting process in these materials.

2.1 H-implantation in Ge

H-implantation in Ge results in ion induced defects which are quite similar to that in H implanted Si. These defects are vacancies, interstitials and their complexes with the

implanted H (Akatsu et al., 2005; David et al., 2009). When H is implanted in Ge, it results in surface blistering/exfoliation depending upon the implantation and post-implantation annealing parameters (Akatsu et al., 2005; Dadwal et al., 2009). For instance, Fig. 2 shows 100 keV H ion implanted Ge samples at different implantation temperatures. For the implantation at liquid nitrogen (LN₂), the surface exfoliation is observed in the form of craters of different size (Fig. 2a). The room temperature (RT) H-implantation displayed large area exfoliation after post implantation annealing at 500 °C for 30 min (Fig. 2b). This large area exfoliation is extended upto few 100 square micrometer over the implanted surface. However, H-implantation at higher temperature of 300 °C results surface exfoliation in the as-implanted state (Fig. 2c) (Dadwal et al., 2009).

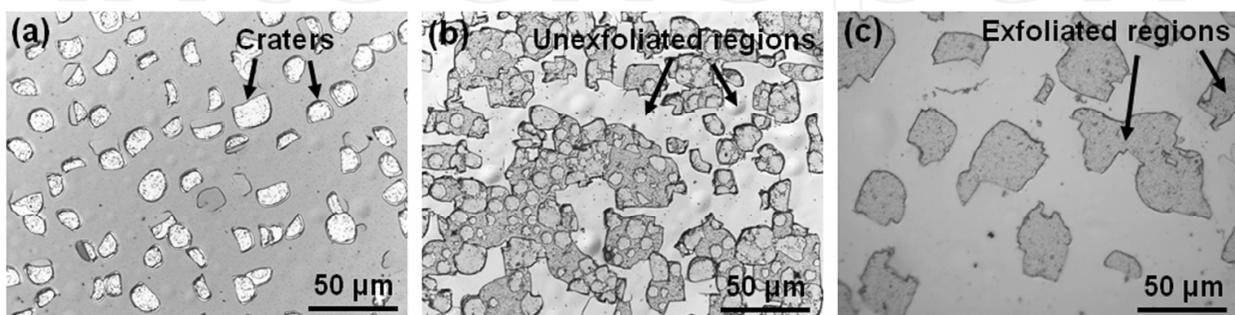


Fig. 2. Nomarski optical images of the 100 keV H implanted Ge at (a) LN₂, (b) RT after post-implantation annealing at 500 °C for 30 min, and (c) 300 °C in the as-implanted state (Dadwal et al., 2009).

The increase of implantation temperature shows pronounced diffusion of the H-induced defects and their re-arrangements within the damage band, which leads to the formation of extended defects like microcracks (Zahler et al., 2007). The role of implanted H is to passivate the internal damage lattice, which results in molecular hydrogen within these extended defects during implantation or after post-implantation annealing. These extended defects filled with H₂ molecules are responsible for the surface craters or exfoliation depending upon the implantation temperature (Dadwal et al., 2009). Since diffusion of the implanted species is also a time dependent process, that is why post-implantation annealing at temperature lower than 500 °C for time less than 30 min does not produced any surface deformation. However, one may obtain the H-induced surface blistering at an annealing temperature lower than 500 °C but the annealing should be performed for duration longer than 30 min. This blistering study of the H implanted Ge was successfully used for the fabrication of GeOI substrates where bulk Ge acted as donor substrate and the transferred layer thickness was about few thousands of angstroms (Deguet et al., 2006; David et al., 2009). The root mean square roughness (RMS) of the transferred layer was below 0.2 nm and Z range value was around 2 nm on a 5 × 5 μm² scan area after the chemical mechanical polishing (CMP) step.

2.2 H-implantation in SiGe

The introduction of Ge in the Si lattice results in new applications of the SiGe alloy in the fabrication of strained SiGe (sSiGe) based high speed devices and modern complementary-metal-oxide-semiconductor (CMOS) technology (Singh et al., 2005; Huang et al., 2001). When Ge adds into the Si lattice it gets strained. Depending upon the molar composition of

Ge, gate length of the sSiGe based CMOS devices and bandgap in base region of the SiGe heterojunction bipolar transistors (HBTs) varies accordingly which gives its importance in the said applications. The typical value of Ge composition in the SiGe alloy ranges between 15–30% of Si. However, with the increase in Ge concentration in Si lattice, quality of the transferred sSi layer starts degrading due to the over concentration of Ge. This allows agglomeration or precipitation of Ge during the wafer bonding or in the post-implantation annealing step (Huang et al., 2001). Hence, in order to prepare high speed electronic circuits and optoelectronics, the wider range of Ge concentration is preferable. For that, understanding of the implantation-induced blistering parameters is essential in order to normalize the layer splitting process at different Ge concentrations. In particular, if we consider H-implantation in $\text{Si}_{0.70}\text{Ge}_{0.30}$, it does not results surface blistering/exfoliation in the as-implanted state for the implantation at LN_2 and RT (Dadwal et al., manuscript under preparation). However, their post-implantation annealing at higher temperature of $400\text{ }^\circ\text{C}$ for 1 hr showed surface blistering/exfoliation depending upon the implantation temperature (Fig. 3).

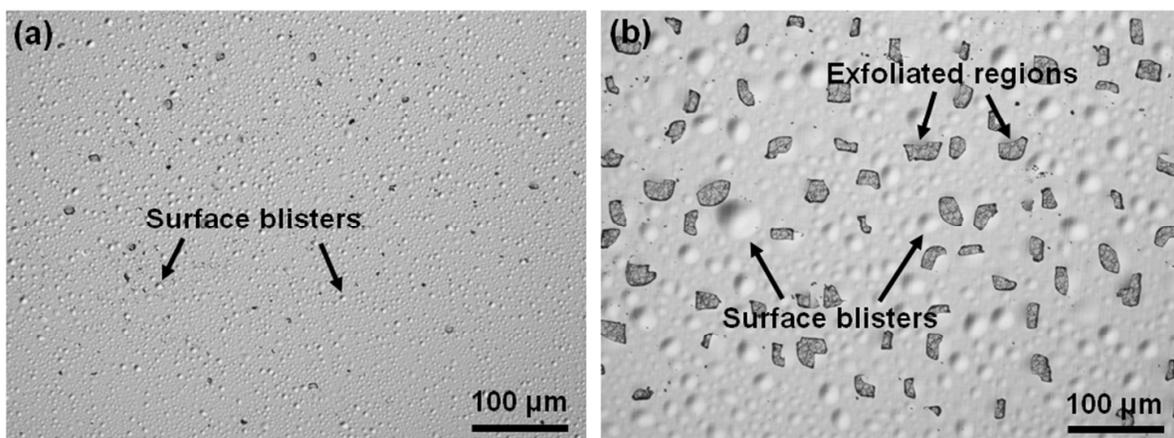


Fig. 3. Nomarski optical images of the 100 keV H implanted $\text{Si}_{70}\text{Ge}_{30}$ for a fluence of $1 \times 10^{17}\text{ cm}^{-2}$ at (a) RT and (b) LN_2 after post-implantation annealing at $400\text{ }^\circ\text{C}$ for 1 hr (Dadwal et al., manuscript under preparation).

With the increase of post-implantation annealing temperature to $500\text{ }^\circ\text{C}$, the RT implanted SiGe samples also undergo surface exfoliation for the same annealing time of 1 hr. However in the LN_2 implanted SiGe samples, surface exfoliation dominate on a large scale after post-implantation annealing at $500\text{ }^\circ\text{C}$ for 1 hr (Dadwal et al., manuscript under preparation). In comparison to H-implantation at RT, H-implantation at LN_2 undergoes effective segregation of the H-induced extended defects within the narrow damage band and is responsible for the surface exfoliation after post-implantation annealing. Such type of H-induced extended defects in the form of platelets and microcracks are very recently been reported in blistering study of the H-implantation in $\text{Si}_{0.70}\text{Ge}_{0.30}$ (Singh et al., 2011). These extended defects are not only oriented along (001) plane but also along {111} planes, and are capable of deforming top implanted layers in the form of surface blisters and craters (Fig.4).

This implantation temperature dependence of the blistering study can provide a meaningful information in the prospective of high Ge contained SiGe layer transfer of good quality. Specifically, the surface blistering/exfoliation at the lower implantation and annealing temperature seems to be more appropriate in the fabrication of sSGOI substrates with high

Ge concentration. This is because of some issues related to the thermal and lattice mismatch between the donor and handle substrate. H implanted $\text{Si}_{0.85}\text{Ge}_{0.15}$ has shown high quality layer splitting in the fabrication of strained silicon-germanium-on-insulator (sSGOI) substrates (Huang et al., 2001). This was done by bonding of the H implanted $\text{Si}_{0.85}\text{Ge}_{0.15}$ epitaxial layers with the oxidized Si wafer followed by annealing at 500–600 °C to induce layer splitting. The final RMS roughness of the transferred $\text{Si}_{0.85}\text{Ge}_{0.15}$ layer was less than 1 nm (Huang et al., 2001).

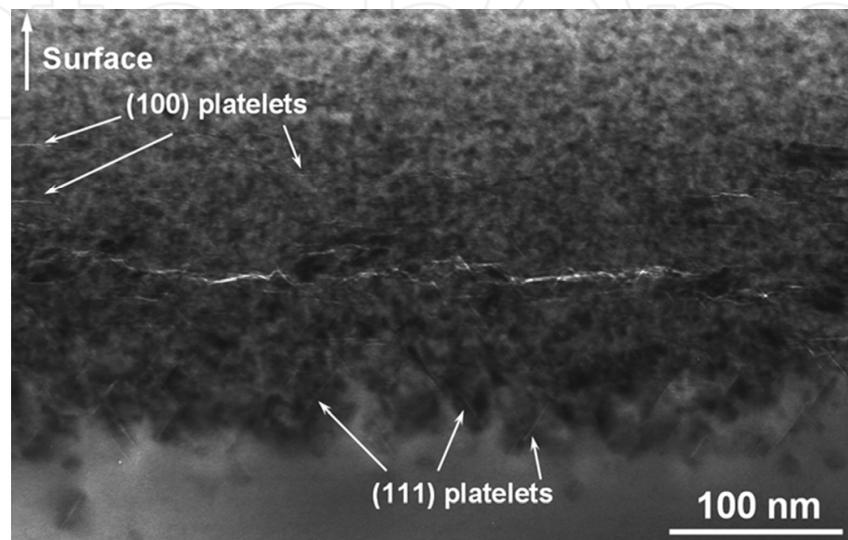


Fig. 4. Cross-sectional transmission electron microscopy (XTEM) image of the 120 keV H^+ ion implanted $\text{Si}_{0.70}\text{Ge}_{0.30}$ with a fluence of $1 \times 10^{17} \text{ cm}^{-2}$ after post-implantation annealing at 500 °C for 5 min (Singh et al., 2011). doi:10.1088/0268-1242/26/12/125001

3. GaAs

GaAs is the first binary compound semiconductor which was used in the fabrication of electronic devices after conventional semiconductors such as Si. The combination of GaAs with the low lattice matched Ge provides fruitful platform for the integration of the GeOI substrates with the III-V materials. Moreover, being a direct bandgap material, it is an alternative mean of revolutionizing GaAs technology when it combines with ion-cut process (Radu et al., 2003). If GaAs is implanted by H ions in the temperature range of about 100–250 °C, the surface blistering results depending upon implantation fluence in the range of about $(0.3\text{--}2) \times 10^{17} \text{ cm}^{-2}$. The hydrogen induced surface blistering is due to overlapping of the microcracks oriented along $\{111\}$ and $\{100\}$ planes (Fig. 5). It results in the formation of larger cracks of size more than 1 μm , giving layer cracking near to the peak region of the damage concentration. However, surface blistering can be probable even at a higher H fluence. In general, the H-induced surface blistering is not effective for layer splitting applications because of its much temperature sensitive nature due to the beam heating effects. In addition to this, helium (He) implantation in GaAs provides control surface blistering and even large surface area exfoliation only after post-implantation annealing for a fluence of $5 \times 10^{16} \text{ cm}^{-2}$ (Radu et al., 2003). This controlled surface blistering has laid basis for the He-induced GaAs layer splitting applications. Hence in GaAs, in comparison to He-implantation, ion fluence is higher for H-implantation in achieving the surface blistering/exfoliation.

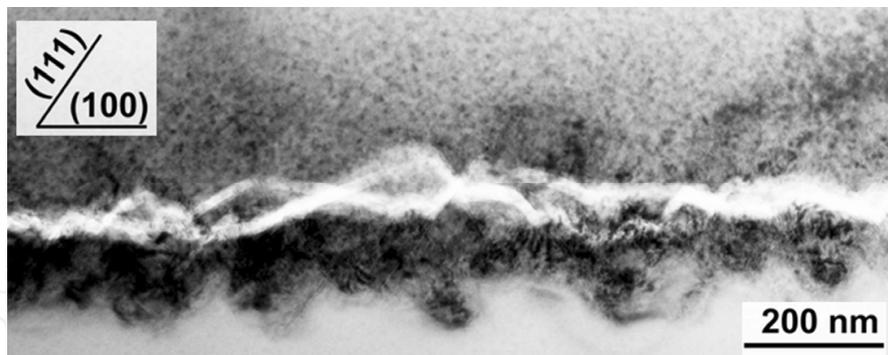


Fig. 5. XTEM image of the 130 keV hydrogen implanted (100) GaAs wafer at 100 °C with a fluence of $3.5 \times 10^{16} \text{ cm}^{-2}$ (Radu et al., 2003). Reprinted with permission from Radu et al., (2003), American Institute of Physics

Moreover, H and He co-implantation method is also used for the layer splitting of GaAs. The GaAs co-implantation with H_2^+ ions of energy 160 keV and fluence $3 \times 10^{16} \text{ cm}^{-2}$, and with He ions of energy 105 keV and fluence $5 \times 10^{15} \text{ cm}^{-2}$ showed controlled surface blistering only after post-implantation annealing. This is due to the formation of relatively narrow damage band decorated with bubbles, platelets like defects over the whole damage band (Radu et al., 2003). The surface blistering in H and He co-implanted GaAs is observed only for the implantation at RT.

3.1 Role of implantation temperature

In general, the implantation temperature is very critical for the ultimate surface deformations in the form of surface blistering/exfoliation. There are many reasons responsible for this temperature dependent blistering behaviour of the implanted semiconductors (Kucheyev et al., 2001; Lee et al., 2004). The prominent facts are that, blistering is a temperature and time dependent process where implanted species should get released from the passivated defect sites for their segregation and the formation of extended defects like platelets. The platelets formation is necessary for the surface blistering/exfoliation (Moutanabbir et al., 2010). In the case of GaAs, if implantation temperature goes beyond the range of about 100–160 °C, the surface blistering does not occur due to the out diffusion of H from the damage region. Hence it does not allow the agglomeration of H for the formation of extended defects like platelets, which are the precursors for the surface blistering. Similarly if the implantation temperature is lesser than 100 °C, then implanted H does not get sufficient migration to undergo proper interactions with the implantation-induced defects, which further hinder the surface blistering/exfoliation. Hence the implanted ions should possess a sufficient minimum energy called as activation energy for the surface blistering or ion-cut process.

3.2 GaAs layer splitting

The layer splitting of GaAs using ion implantation and direct wafer bonding technique can be done by choosing an appropriate handle substrate. In comparison to H-implantation, the He implanted GaAs wafer is used in the layer transfer process onto Si substrate (Radu et al., 2003). However, the layer transfer occurred partially. But, H and He co-implantation provides complete and uniform transferred layer of the implanted GaAs onto Si substrate using intermediate Si-on-glass (SOG) layer (Fig. 6).

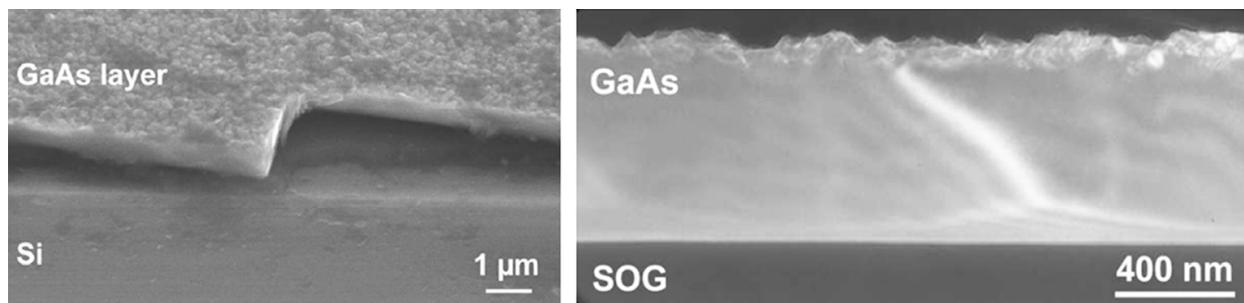


Fig. 6. Transferred GaAs layers onto Si-on-glass/Si substrate with (a) scanning electron microscopy image of the He implanted GaAs at RT after post-implantation annealing at 200 °C for 14.5 hr and (b) XTEM image of the bonding interface between the transferred GaAs layer and SOG layer using H and He co-implantation at RT followed by post-implantation annealing at 225 °C for 14 hr (Radu et al., 2003). Reprinted with permission from Radu et al., (2003), American Institute of Physics

The transferred GaAs layer obtained by the co-implantation is little bit more rough in comparison to the partially transferred GaAs layer obtained by He-implantation alone (Radu et al., 2003). This is due to the reason that surface morphology of the transferred GaAs layer depends upon the implantation-induced extended defects, like microcracks orientation and their overlapping within the damage region (Fig. 7).

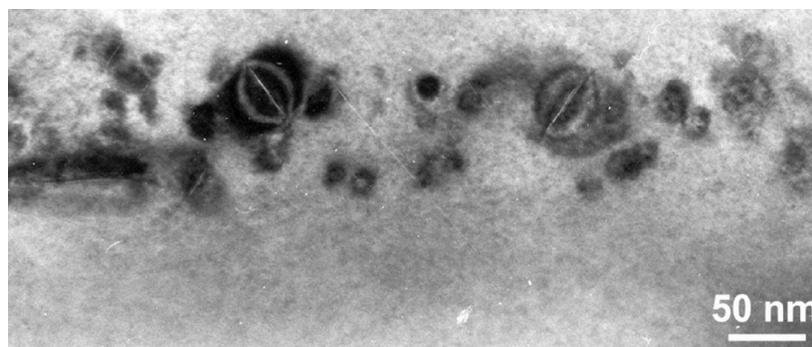


Fig. 7. XTEM image of the platelets and microcracks in the as-implanted (100) GaAs by He (105 keV, $5 \times 10^{15} \text{ cm}^{-2}$) followed by H_2^+ (160 keV, $3 \times 10^{16} \text{ cm}^{-2}$) implantation at RT (Radu et al., 2003). Reprinted with permission from Radu et al., (2003), American Institute of Physics

During co-implantation, H-implantation induces platelets formation oriented along (100) and (111) planes, which gives zig-zag overlapping of the microcracks in the as-implanted state (Fig. 7). Hence it results in relatively high surface roughness to the transferred GaAs layer after post-implantation annealing in comparison to only He implanted GaAs, where platelets are mostly oriented along (100) planes that are parallel to the implanted surface.

4. InP

The implantation-induced layer splitting of InP using hydrogen has strong dependence on the implantation temperature as well as the post-implantation annealing parameters (Hayashi et al., 2004; Chen et al., 2008). The problem becomes more severe if the temperature of the sample holder rises during implantation. The rise in the sample holder temperature during implantation can activate the implanted hydrogen and it starts diffusing out of the damage region. This eventually results in the absence of blistering/exfoliation in

InP even after post-implantation annealing. It was reported by the Tong *et al* that in the case of InP the surface blistering or layer exfoliation occurred after post-implantation annealing only if the implantation temperature was between 150–250 °C (Tong *et al.*, 1999). The Hayashi *et al* have shown that hydrogen implantation-induced out-of-plane tensile strain within the damage region also influences the blistering/exfoliation behaviour in InP (Hayashi *et al.*, 2004). This out-of-plane tensile strain gives rise to in-plane compressive stress within the damage region which is dependent upon the implantation temperature. Moreover, H-implantation at higher temperature produced much less out-of-plane tensile strain in comparison to the low temperature implantation. The origin of this induced strain within the damage region is related to the implantation-induced distortion of the crystal lattice in the form of point defects and their clusters (Chen & Di *et al.*, 2008). It was reported by Singh *et al* that instead of hydrogen, He-implantation can also be used for achieving layer splitting in InP (Singh *et al.*, 2006). This is because in InP the diffusivity of the implanted He ions is not very sensitive to the implantation temperature. In this report four-inch diameter InP wafers were used and the implantation temperature was kept at either RT or -15 °C. This resulted in controlled surface blistering/exfoliation only after the post-implantation annealing in the temperature range of 225 to 400 °C. Moreover, in this work, 100 keV He implantation was done with a fluence of $5 \times 10^{16} \text{ cm}^{-2}$. This resulted in the formation of implantation-induced extended defects. Such defects are in the form of microcracks located within the damage band after post-implantation annealing at 250 °C (Fig. 8). These microcracks after post-implantation annealing at 250 °C for sufficient long time of about 30 min undergo agglomeration and are responsible for the surface blistering/exfoliation (Singh *et al.*, 2006).

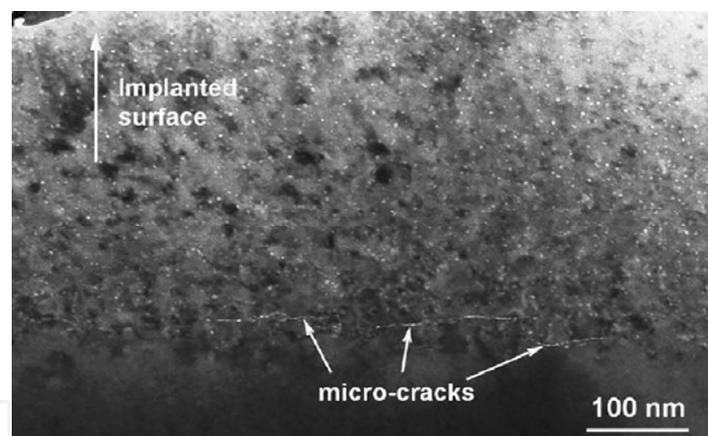


Fig. 8. XTEM image of the damage band of 100 keV He implanted InP with a fluence of $5 \times 10^{16} \text{ cm}^{-2}$ and annealed at 250 °C for 25 min (Singh *et al.*, 2006). Reprinted with permission from Singh *et al.*, (2006), Elsevier

He ion implantation in combination with direct wafer bonding was also used for the transfer of InP layer onto Si. It results in the formation of InP-on-insulator engineered substrate. For instance, He implanted InP wafer with spin-on-glass (SOG) layer was used in the wafer bonding with oxidized Si wafer. The post-implantation annealing of this bonded pair at relatively low temperature of 200 °C for sufficiently long time of 20 hr results in the transfer of thin InP layers onto the Si substrate (Singh *et al.*, 2010). This provides an attractive platform for the fabrication of single crystalline layers of device quality which has potential to reduce the cost of fabricated devices based on this InP-on-insulator technology. The other way of layer transfer of InP can be done by using lattice matched InGaAs. The trick involves in this technique is to keep away the InP from ion implantation and actually perform the H-

implantation in InGaAs using InP/InGaAs heterostructure (Chen & Jing et al., 2008; Dadwal et al., 2011). The energy of the implanted H ions is chosen in such a manner that it creates maximum damage only within the InGaAs. The advantage of using InGaAs is to achieve the control blistering only after post-implantation annealing at the elevated temperature due to the weak dependence of H diffusivity in it. Therefore, the H-implanted InP/InGaAs heterostructure can be used potentially for the transfer of thin InP layers on the in-expensive substrate like Si using direct wafer bonding technique and subsequent annealing. This allows the fabrication of high quality InP layers which are almost free from any growth related defects, and hence it results in the decrease of carrier scattering with enhanced device performance (Chen & Jing et al., 2008; Dadwal et al., 2011).

5. GaN

The nitride technology is quite dominant in the field of optoelectronics, high frequency and high power devices (Padilla et al., 2010). In the main list it includes blue, deep ultra violet (UV) high brightness light emitting diodes (HBLEDs), laser diodes (LDs), UV detectors and high electron mobility transistors (HEMTs). This has significant impact on the modern high definition (HD) display and solid state lighting. However, the main barrier in the commercialization of these nitride devices is in terms of their cost. The reasons of this are lack of availability of the high quality materials and various technical issues related to the manufacturing of their devices. In particular, GaN has drawn lot of interest in the today nitride technology from the prospect of ion-cut process in the III-V nitrides. In spite of highly expensive free standing fs-GaN substrate, using ion-cut process, one can re-use the same substrate in multiple times which ultimately reduces the cost of fabricated devices. With this advantage, the applications of ion cut process in GaN are mostly explored by the H-implantation but on a small scale (Moutanabbir et al., 2010). Hence in order to fully employ this ion-cut process in GaN, understanding of the layer splitting mechanisms is very essential, which can be done by studying the implantation-induced surface blistering/exfoliation (Moutanabbir et al., 2010). When GaN is implanted by H ions with suitable implantation parameters followed by annealing at particular parameters, it results surface blistering in the as-implanted state as well as after post-implantation annealing (Fig. 9) (Dadwal et al., manuscript under preparation).

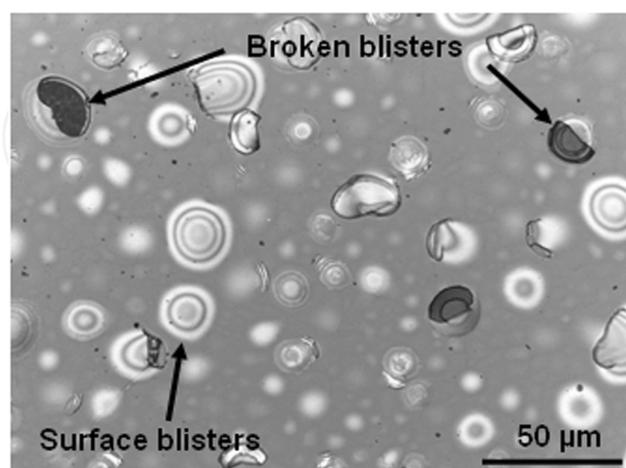


Fig. 9. Nomarski optical image of the 100 keV H⁺ ion implanted GaN with a fluence of $2.5 \times 10^{17} \text{ cm}^{-2}$ at RT after post-implantation annealing at 500 °C for 30 min (Dadwal et al., manuscript under preparation).

H-implantation in GaN usually requires a higher fluence for the surface blistering/layer splitting to occur after post-implantation annealing at higher temperature. The critical value of a fluence in the 100 keV H implanted GaN is about $2.5 \times 10^{17} \text{ cm}^{-2}$ (Tauzin et al., 2005). This minimum required fluence is order of magnitude higher than the conventional H implanted semiconductors like Si and GaAs, respectively. There are many reasons which are responsible for this higher H-implantation fluence in GaN, such as very efficient dynamic annealing of the implantation-induced defects, interaction and trapping of the H with the induced defects and some particular properties of the GaN (Kucheyev et al., 2001). Moreover, due to the efficient dynamic annealing nature of the induced defects, they undergo defects annihilation even during the implantation if the implantation temperature increases to a higher value. Hence, higher temperature implantation can result in easier agglomeration of the induced defects, which shows surface blistering/exfoliation in the as-implanted state. This surface blistering/exfoliation is due to the formation of the H-induced defects within the damage region. The damage region investigations have shown that these induced defects could be of the type of point defects V_{Ga} , point and H defects complexes $V_{\text{Ga}}V_{\text{N}}$, $V_{\text{Ga}}\text{-H}_n$ for $n \leq 4$ and eventually planer defects like nanovoids (Moutanabbir et al., 2010) (Fig. 10a). After post-implantation annealing or H-implantation at higher temperature results in the agglomeration of these defects to microcracks lying along different planes within the damage band (Fig. 10b). These H-induced microcracks in an overpressurized state undergo overlapping and combination to each other, and hence resulted in surface blistering/exfoliation. However, the way with which H interacts with the lattice atoms during the implantation and after post-implantation annealing is a subject of further study.

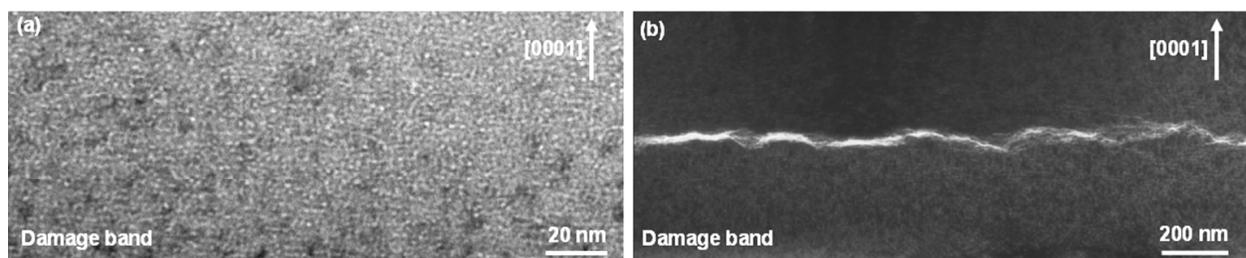


Fig. 10. High magnification XTEM images of the damage band in the 100 keV H^+ ion implanted GaN with a fluence of $2.5 \times 10^{17} \text{ cm}^{-2}$ at (a) RT and (b) 300 °C in the as-implanted state (Dadwal et al., manuscript under preparation).

The study of H-implantation-induced blistering can be extendable to the layer transfer work also using direct wafer bonding. The epitaxial grown thin film of GaN on sapphire has shown a layer transfer onto the foreign sapphire substrate (Tauzin et al., 2005). However in the case of free standing fs-GaN substrate, only partial area layer transfer is achievable so far (Moutanabbir et al., 2010). One of a main obstacle of this is the implantation-induced in-plane compressive stress within the damage band, which leads to bowing of the whole GaN wafer away from the implanted surface. For example, in the case of two inch H implanted fs-GaN wafer, the RT H-implantation results in increase of the wafer bow from its original value of 1–2 μm to higher value of more than 20 μm , which makes difficulty in its bonding with other wafer. One of the suggested method in order to minimize this wafer bowing problem is by performing H-implantation in the back side of the already H implanted GaN wafer. This can results in decrease of wafer bow of the H implanted GaN wafer with

effective bow value is sufficiently lower for performing direct wafer bonding (Moutanabbir et al., 2010). Hence for the success of ion-cut process in GaN, understanding of the implantation-induced stress behaviour is very important. In this context the latest studies have shown that, implantation-induced stress is strongly depends upon the implantation temperature (Padilla et al., 2010). The analysis showed that there exists biaxial stress in the damage region for the implantation at different temperatures. This means that the out-of-plane tensile strain induces in-plane compressive stress in the damage region. The measured compressive stress was about -1.0 GPa in the LN₂ and about -0.5 GPa in the RT implanted GaN samples after post-implantation annealing at 500 °C for 30 min (Dadwal et al., manuscript under preparation). The H-implantation at low temperature have very less dynamic annealing effects, which results in large implantation-induced damage and hence large induced stress in comparison to the RT implanted GaN. Therefore, the RT implantation could be an effective way for the GaN layer splitting, but only partial success has achieved. This ion-cut process using fs-GaN wafer has unique technological importance because once this process is optimized completely, it will enable various types of highly efficient and low cost nitride devices.

6. AlN

The nitride technology has also attracted great attention towards AlN next to GaN due to its higher direct bandgap and thermal conductivity, and along with some other special physical properties (Dadwal et al., 2010). Hence, it makes AlN as a perfect material for the fabrication of high power lasers and highly efficient UV optoelectronic devices. Another advantage of AlN is its high melting point which is almost double than Si. This makes it as an excellent candidate for the device applications which need to work at high temperatures. In addition, its radiation hardness aspect makes it suitable material for space and military applications. However, the AlN technology is still in their infancy stages and it needs a greater look-up to study this material not only in the technological but material point of view also (Dadwal et al., 2010). But the fs-AlN wafers are very expensive and are mostly available upto two inch of diameter. Hence working on these lines, the recent studies are concentrated more towards the material aspects of AlN epitaxial layers and the possibilities of combining it with ion-cut process (Dadwal et al., 2010). Once the ion-cut process gets its maturity in AlN, one can think about the reduction of cost of this AlN technology. Even the high quality epitaxial layers of AlN in combination with ion-cut process have a potential for the fabrication of low cost nitride devices. That is why, first part of the ion-cut process which is ion implantation-induced damage study is mostly considered in the recent studies (Dadwal et al., 2010; Singh et al., 2010). It mostly includes the influence of H-implantation and post-implantation annealing parameters on the induced damage. These investigations show that depending upon the implantation and annealing parameters, H-implantation in thin film AlN results in the formation of surface blistering/exfoliation either in the as-implanted state or after post-implantation annealing at higher temperature (Fig. 11).

In addition to the surface blistering/exfoliation in H implanted AlN, large area exfoliation is also observed after post-implantation annealing for the implantation at higher temperature of 300 °C (Fig. 11b). It means that the exfoliated area extends over hundreds of square micrometers. This is a special type of the surface deformation in the H implanted AlN and is not observed in its other family of materials like GaN. Current investigations have shown that such type of deformation in the H implanted AlN is probably due to the nature of

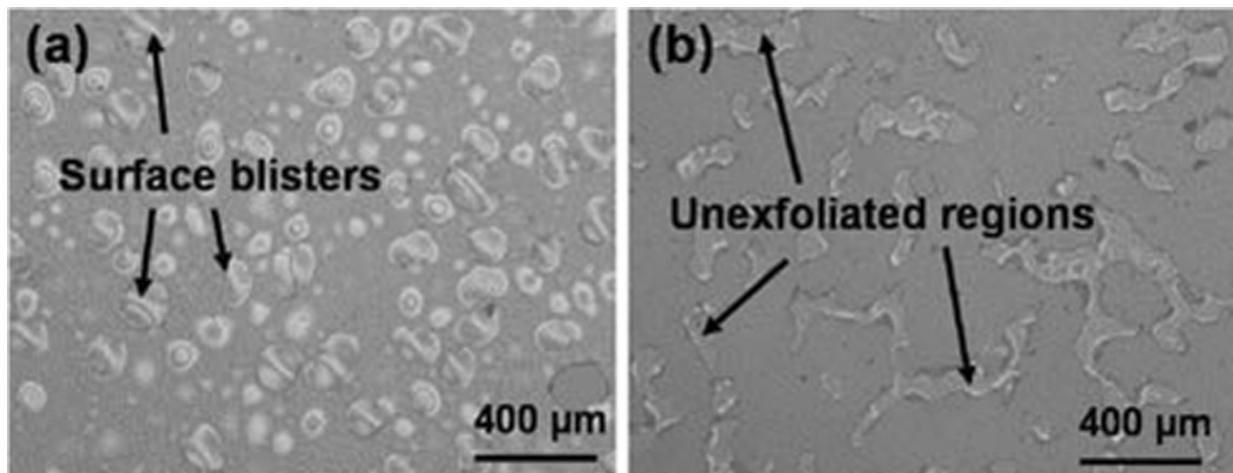


Fig. 11. Nomarski optical microscopy images of the 100 keV H^+ ion implanted AlN with a fluence of $1 \times 10^{17} \text{ cm}^{-2}$ at (a) RT and (b) 300 °C after post-implantation annealing at 800 °C for 1hr (Dadwal et al., 2010).

extended defects like nano/microcracks distributions within the narrow damage band (Fig. 12). The damage band is decorated with the H filled nanovoids which serve as precursors for the surface blistering/exfoliation (Dadwal et al., 2010). These nanovoids after post-implantation annealing agglomerate to nanocracks. This agglomeration happens parallel to the implanted surface and is clearly shown in Fig. 12b. These nanocracks finally converted to the microcracks after post-implantation annealing for the sufficient long time and which are responsible for the surface blistering/exfoliation. However, the further investigations are underway in order to understand the large area exfoliation phenomenon in detail. But if we consider these surface deformations from the ion-cut point of view, then after direct wafer bonding there is no any practical difference between the surface exfoliation and large area exfoliation. This is because of the fact that the host wafer acts as a stiffener and it allows the implantation-induced surface deformations to migrate more towards the lateral manner and parallel to the bonded interface during the annealing of the bonded wafers at elevated temperature.

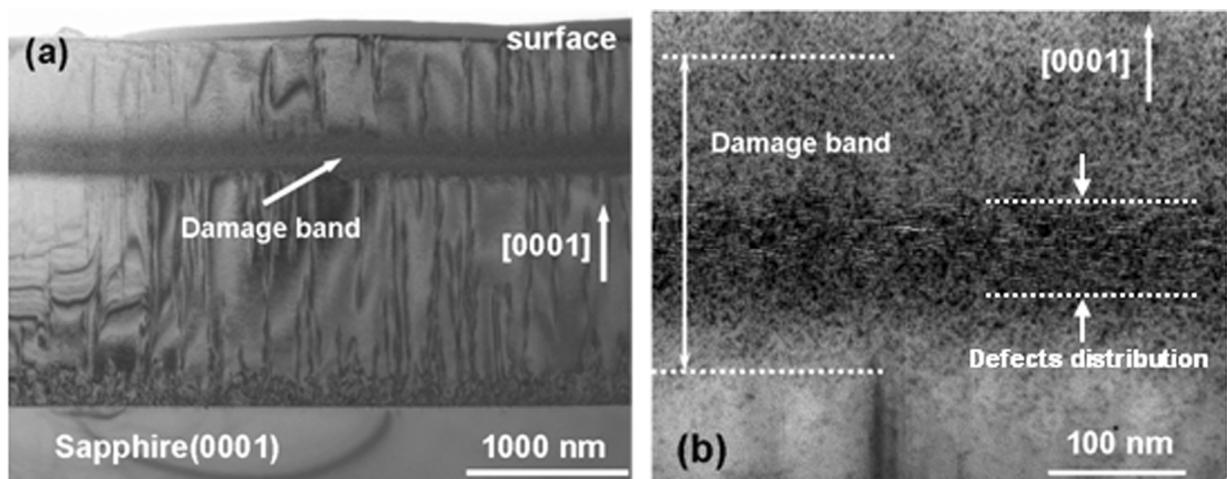


Fig. 12. (a) XTEM images of the damage band in the 100 keV H^+ ion implanted AlN at 300 °C with a fluence of $1 \times 10^{17} \text{ cm}^{-2}$ and (b) High magnification TEM image of the same damage band showing the narrow distribution of the extended defects (Dadwal et al., 2010).

The value of a critical fluence for the surface blistering/exfoliation in H implanted AlN after post-implantation annealing is $1 \times 10^{17} \text{ cm}^{-2}$ (Dadwal et al., 2010). This value of the critical fluence is less than the H implanted GaN but higher than the conventional semiconductors like Si. Since AlN and GaN has a same chemical structure, so one would expect the same reasons could be also applicable for the high implantation fluence in the H implanted AlN. The other aspect of AlN is the higher surface roughness of its thin film and of fs-AlN wafer. The typical value of a root mean square surface roughness is about 25 nm, which is a very higher and is not acceptable for the direct wafer bonding. However, unlike Si chemical mechanical polishing (CMP), the surface planarization of AlN is difficult and its available technology is different and expensive than Si. In the device point of view, AlN technology is still lacking behinds the other nitride materials. But the device quality fs-AlN wafer in combination with ion-cut process have definite possibilities to fabricate high quality AlN thin layers, which can provides fruitful platform for the low cost AlN technology.

7. Other semiconductors

Ion-cut process has also been extended to some other technological important semiconductors, like ZnO, GaSb and CdZnTe. In most of these semiconductors H-implantation is explored in the initial investigations of the implantation-induced surface blistering/exfoliation, which is then used in the layer transfer process (Hobart et al., 1999). In this section a brief overview of the ion-cut process in these semiconductors is given.

7.1 ZnO

H-implantation in ZnO is considered to be another valuable mean for the use of this material in the high temperature operating devices just like AlN. However, H-implantation in ZnO is mainly restricted onto the study of implantation-induced surface blistering/exfoliation. This is because of ion-cut process in ZnO is not completely investigated, especially related to wafer bonding part. In addition to this, the higher H-implantation fluence requirement in ZnO makes large damage to the crystal structure, which still needs greater investigations to apply this material for the layer transfer purpose. Like GaN and AlN, H-implantation in ZnO also results surface blistering/exfoliation depending upon the H fluence and annealing parameters. But, the minimum fluence for the surface blistering/exfoliation to occur after post-implantation annealing is about $2.5 \times 10^{17} \text{ cm}^{-2} \text{ H}_2^+$ ions (Singh et al., 2010). This minimum fluence requirement is even larger than nitride semiconductors like GaN and is could be due to the efficient dynamic annealing of the induced defects. The implantation of H ions less than this critical fluence does not show any surface blistering even after post-implantation annealing at higher temperature. However, H-implantation with a fluence of $2.8 \times 10^{17} \text{ cm}^{-2}$ results surface exfoliation in the as-implanted state (Singh et al., 2010). The investigation of H-implantation-induced damage shows the formation of H-induced microcracks within the damage band in the as-implanted state, which upon thermal annealing at higher temperature result in the formation of surface blistering/exfoliation (Fig. 13). The thickness of the exfoliated ZnO layer is about 450 nm, which is close to the projected range 400 nm of the 100 keV hydrogen ions in ZnO. This projected range is calculated by the Stopping and Ranges of Ions in Matter (SRIM2003) simulation program.

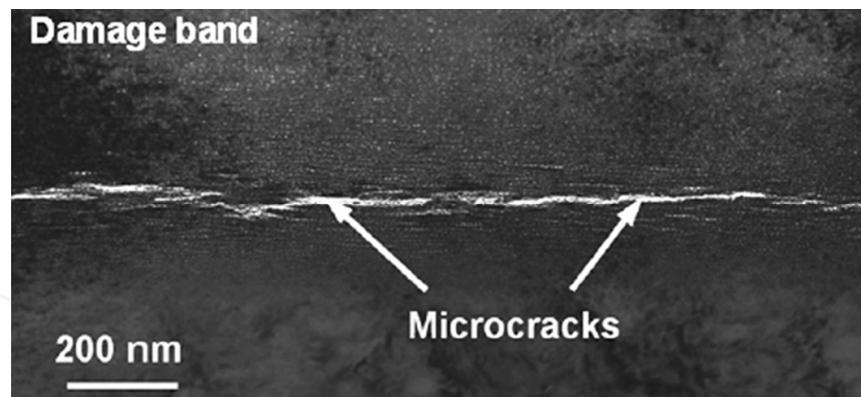


Fig. 13. XTEM image of the damage band in the 100 keV H_2^+ ion implanted ZnO with a fluence of $2.5 \times 10^{17} \text{ cm}^{-2}$ in the as-implanted state (Singh et al., 2010). doi:10.1088/0268-1242/22/11/003

The higher implantation fluence for the surface blistering in ZnO is directly related to the higher implantation time requirement to fulfil the required fluence. This means that implanted H ions need sufficient time to interact with the host lattice atoms and form defect sites, which then acts as source for the extended defects like microcracks formation during the higher temperature treatment. The layer splitting of ZnO is still not achieved. Therefore it needs thorough study of the surface blistering/exfoliation and its wafer bonding.

7.2 GaSb

GaSb epitaxial layers can be transferred using H ion implantation and direct wafer bonding technique. The H-implantation in GaSb with a fluence of $5\sim 8 \times 10^{16} \text{ cm}^{-2}$ at RT results surface blistering after post-implantation annealing at 60–600 °C (Hobart et al., 1999; Zheng et al., 2000). The thermal annealing treatment of the H implanted GaSb is studied for time 1 to 80 min under both isothermal and isochronal conditions. In both annealing conditions there is an increase of the lateral size of surface blisters/exfoliated regions (Zheng et al., 2000). The blistering kinetics study showed activation energy value each for the higher and lower annealing temperature regime. That is 0.30 eV in the annealing temperature range of 90–230 °C and 1.8 eV in the annealing temperature lower than 90 °C (Zheng et al., 2000). The higher temperature activation energy is related to diffusion of the implanted H in the damage lattice. Whereas lower temperature activation energy may be governed by the trapping-detrapping mechanisms of the induced defects similar to H implanted Si. The onset time for the surface blistering at higher annealing temperature is much shorter than the annealing at the lower temperature. These parameters of the blistering study are applied in the thin layer transfer of n-type GaSb onto GaAs wafer by using borosilicate glass (BSG) as an intermediate layer. The H implanted GaSb wafer is then bonded with GaAs at RT followed by annealing at 100 °C for 2 hr. The final layer splitting is then achieved by annealing of the bonded wafers at 160 °C for 30 min (Zheng et al., 2000).

7.3 CdZnTe

H-implantation-induced surface blistering/exfoliation study is also extended to ternary semiconductors like CdZnTe (Miclaus et al., 2005). Again, the main motive of these studies

is to find out the possibilities of the layer transfer of CdZnTe depending upon its constituents molar concentration. For example, H-implantation in $\text{Cd}_{0.96}\text{Zn}_{0.04}\text{Te}$ is studied for the implantation energy in the range of 40–200 keV with an ion fluence of $5 \times 10^{17} \text{ cm}^{-2}$ (Miclaus et al., 2005). The co-implantation work using boron (B) ($5 \times 10^{15} \text{ cm}^{-2}$, 147 keV) and H ($5 \times 10^{16} \text{ cm}^{-2}$, 40 keV) is also used for the implantation at 77 or 273 K (Miclaus et al., 2005). The H implanted samples at low temperature of 77 K results in surface blisters after post-implantation annealing at 150–300 °C. However, implantation at 253 K does not result surface blistering even after post-implantation annealing at higher temperature. This pronounced blistering phenomenon at lower implantation temperature is could be due to the less efficient dynamic annealing of the induced defects. In addition, co-implantation of H with boron (B) at lower temperature results in surface blistering with an advantage that blistering occurs at lesser annealing time for an annealing temperature which depends upon both implanted ions fluence. The increase in H fluence leads to the decrease of implantation-induced blistering time. This means that B-implantation promotes the damage formation and H-induced internal pressure within the damage region for the surface blistering (Miclaus et al., 2005).

8. Conclusions and future perspective

We have presented an overview of the ion implantation-induced surface blistering/exfoliation and their use for the layer splitting of the different technological important compound semiconductors. In most of these semiconductors H-implantation-induced blistering/exfoliation was investigated for the potential application in ion-cut process. In the case of Si, Ge and SiGe alloys, both controlled blistering as well as layer splitting/transfer has been successfully demonstrated in the earlier studies. However, in the case of III-V semiconductors like GaN and AlN, they are reportedly very resilient to H-implantation-induced damage due to the dynamic annealing effects. The critical H fluence for the surface blistering in GaN is $2.5 \times 10^{17} \text{ cm}^{-2}$, whereas in AlN it is $1 \times 10^{17} \text{ cm}^{-2}$. However blistering kinetics shows that, the blistering occurs at lower post-implantation annealing temperature in the case of H implanted GaN in comparison to the H implanted AlN. This fact is very important in the case of ion-cutting process because of the heterogeneous wafer bonding where low temperature annealing is preferable. This blistering study has its main significance in the layer splitting of these nitride semiconductors for the establishment of low cost nitride technology. The free standing wafers of GaN and AlN are very expensive and are mostly available in the small sizes. But using these free standing wafers one can transfer its multiple layers onto the foreign inexpensive substrate. As a result these free standing wafers can be utilized for multiple times which ultimately reduce the cost of fabricated nitride devices. The H-implantation in others compound semiconductors like GaAs and InP for the layer splitting purpose is more or less not appropriate due to its high diffusivity in the damage region. This makes the process very sensitive to the implantation temperature and if implantation parameters go beyond the critically defined window parameters, then no blistering/exfoliation will occur at all. Hence during H-implantation, the temperature at which implantation is perform should be properly checked in order to achieve the controlled surface blistering only after post-implantation annealing. However, He-implantation is an appropriate alternative in order to achieve the controlled surface blistering and layer splitting of GaAs and InP. This is because the He is less mobile within the implantation-induced damage,

which results its less sensitivity towards the implantation temperature. Hence using He-implantation and direct wafer bonding technique, GaAs layer has been successfully transferred onto the foreign substrate Si. Similarly using He-implantation, InP layer transfer is also successfully demonstrated onto the Si substrate. In addition to this, the layer transfer of nitride semiconductors like GaN and AlN is not fully achieved. Only the epitaxial layers of GaN has been successfully transferred onto the sapphire substrate using H-implantation and direct wafer bonding technique. However, till now the layer transfer from the free standing GaN substrate is only partially attained. The minimum critical fluence for the controlled surface blistering in the H implanted GaAs and InP is about two times lesser than the H implanted GaN, AlN and ZnO. Moreover, the fundamental mechanisms behind the H ion implantation-induced surface blistering/exfoliation in these compound semiconductors are not fully understood, even though in some of the compound semiconductors the layer transfer is fully achieved such as GaAs and InP. In fact, the H-induced layer splitting mechanisms is not completely understood even in the conventional semiconductors also like Si and Ge. Hence, further investigations are required in these technological important semiconductors in order to fully explore the advantages of the ion-cut process.

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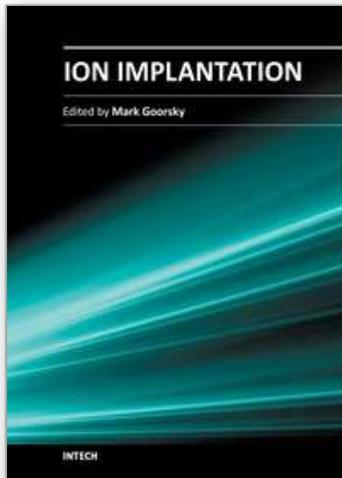
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Ion implantation presents a continuously evolving technology. While the benefits of ion implantation are well recognized for many commercial endeavors, there have been recent developments in this field. Improvements in equipment, understanding of beam-solid interactions, applications to new materials, improved characterization techniques, and more recent developments to use implantation for nanostructure formation point to new directions for ion implantation and are presented in this book.

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