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FPGA Implementation of Inverse Fast Fourier Transform in Orthogonal Frequency Division Multiplexing Systems

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1. Introduction

In modern communication systems, Orthogonal Frequency Division Multiplexing (OFDM) systems are used to transmit with higher data rate and avoid Inter Symbol Interference (ISI). The OFDM transmitter and receiver contain Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT), respectively. The IFFT block provides orthogonality between adjacent subcarriers. The orthogonality makes the signal frame relatively secure to the fading caused by natural multipath environment. As a result OFDM system has become very popular in modern telecommunication systems. Beside all the advantages of OFDM system, there is a main drawback of high Peak to Average Power Ratio (PAPR). There have been many approaches on reducing PAPR in time domain and frequency domain. Some of them work in time domain such as Partial Transmit Sequence Insertion (PTS) and some other methods perform in frequency domain such as Dummy Sequence Insertion (DSI) and Selected Mapping (SLM) methods (Bauml et al., 1996; Muller et al., 1997). Since according to (Baxley et al., 2007), the SLM method reduce PAPR with the least computational complexity and least additional modification requirements on the current technology, therefore most of recent researches have considered SLM based method modifications for their work. Most of these methods modified the OFDM transmitter in a way that multiple IFFT processors are required for implementation. This will increase the number of additions and multiplications that are needed for implementation.

In this Chapter, the OFDM system and the main block of IFFT are introduced. The IFFT block is implemented on FPGA and verification results are discussed. The Optimum Phase Sequence Insertion with Dummy Insertion (OPS-DSI) method is one of recent PAPR reduction techniques and a good example of application for IFFT processor is studied in this Chapter and the FPGA implementation result is verified with simulation results.

2. OFDM system

Fig. 1 shows how OFDM signal is processed. The data input signal with high data rate is split into narrow band channels with lower data rate and then, they are modulated by using general signal modulation (PSK, QAM) and followed by with Inverse Fast Fourier

Transform (IFFT) which provides orthogonality between adjacent sub-channels. After IFFT, the last portion of signal is copied to the head to provide immunity to Inter Symbol Interference (ISI) which is shown by Cyclic Prefix (CP) in Fig. 1.
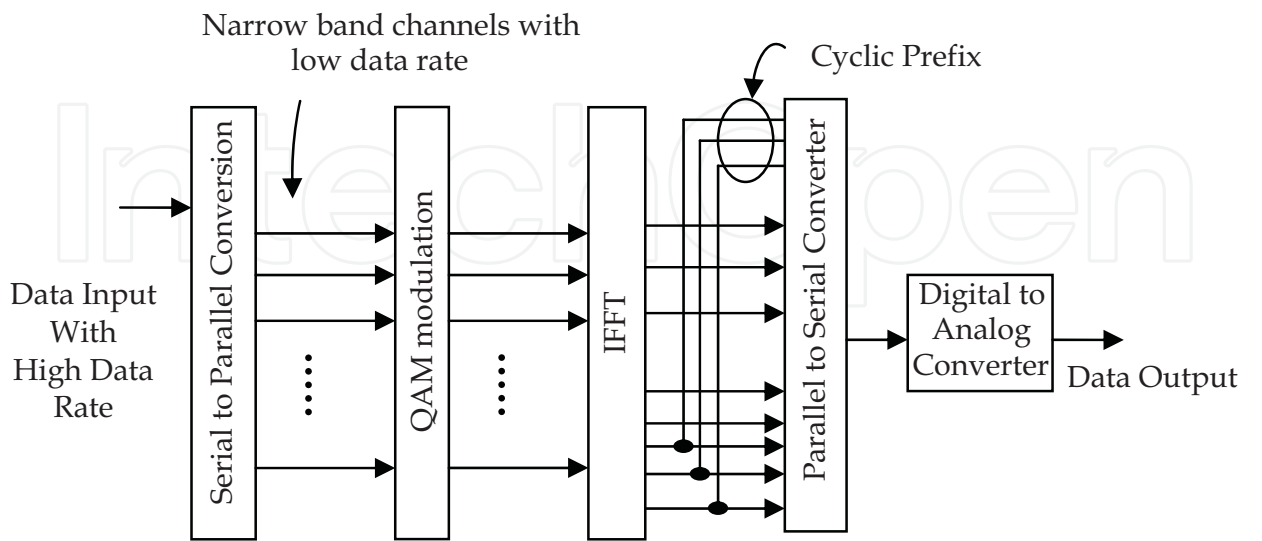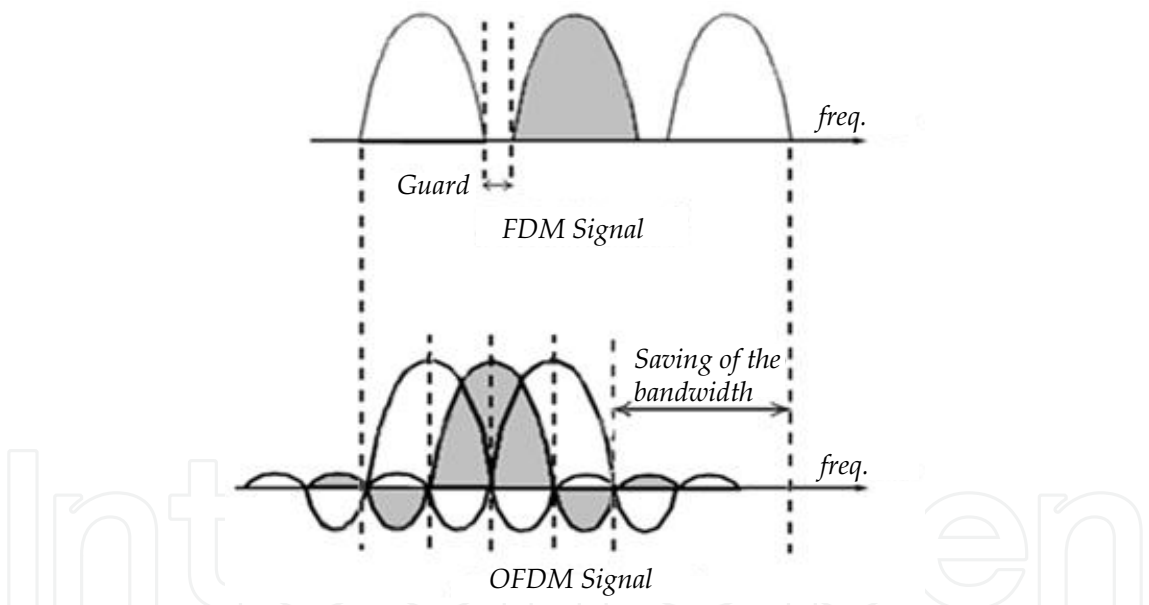

Fig. 1. The OFDM signal structure

Fig. 2. Comparison between FDM and OFDM signals

Although OFDM process is similar to Frequency Division Multiplexing (FDM) signal but, there are some differences. FDM is a single carrier signal in which signal is divided into frequency bands with some guard interval between them to avoid interferences. This is not an issue in OFDM signal since neighboring subcarriers are orthogonal to each other; overlapping does not create interference and the bandwidth is used more efficiently as shown in Fig. 2.

The OFDM is a form of Frequency Division Multiplexing (FDM) scheme and Multicarrier Modulation (MCM) scheme. In FDM, each signal is divided to smaller signals named

subchannel with different frequency widths. Each subcarrier carries a signal at the same time in parallel. Every subcarrier is modulated by a constellation symbol.

3. IFFT implementation on Field Programmable Gate Array (FPGA)

Field Programmable Gate Arrays (FPGAs) are configurable and re-programmable digital logic devices, and programming code is usually written in Hardware Description Languages (HDL).
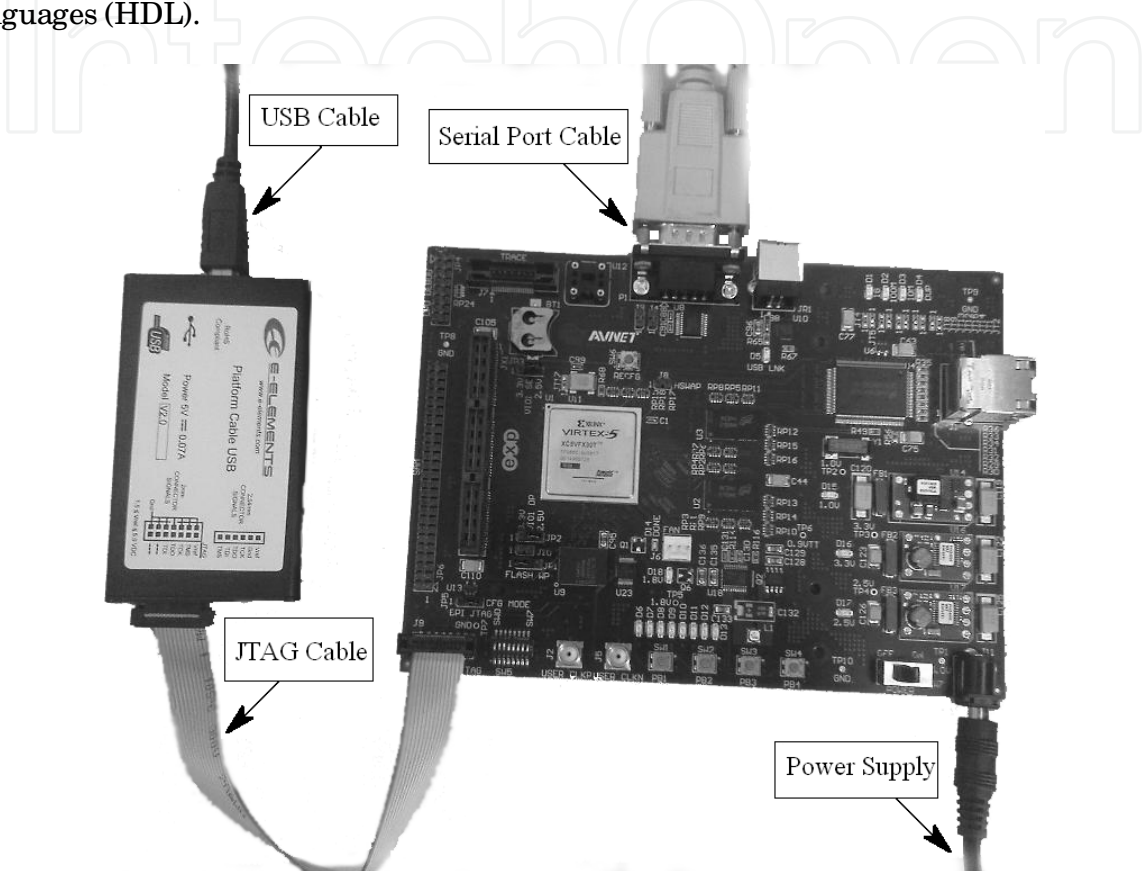

Fig. 3. Virtex-5 Pro development board

Virtex-5 FXT Evaluation Kit is used for implementation which has the Xilinx Virtex-5 XC5VFX30T-FF665 FPGA chip. The datasheet of this FPGA is provided in Appendix D. This board also has 64 MB DDR2 SDRAM memory and 16 MB FLASH memory with variety of I/ O gates which makes it suitable for a typical implementation.

As shown in Fig. 3, the JTAG-USB cable is connected to the JTAG connector of the FPGA board for programming the FPGA. This cable should be connected to the USB port of the PC. The other connector is named serial port which is used to command while the program is performing.

This section introduces fundamentals of IFFT block prototype at the transmitter and the FFT block at the receiver. The basic equations of the FFT and the Inverse FFT (IFFT) are given by:

$$X(k) = \sum_{n=1}^{N-1} x(n) e^{-j2\pi kn/N} \; , k=0,...,N-1 \qquad (1)$$

$$x(n) = \frac{1}{N} \sum_{n=1}^{N-1} X(k) e^{-j2\pi kn/N} \ , n=0,...,N\text{-}1 \tag{2}$$

where N is the transform size or the number of sample points in the data frame and $j = \sqrt{-1}$. $X(k)$ is the frequency output of the FFT at k^{th} point where $k=0, 1, ..., N\text{-}1$ and $x(n)$ is the time sample at n^{th} point with $n=0, 1,..., N\text{-}1$.

Due to the symmetric of the exponential matrix $e^{-j2\pi kn/N}$, it can be represented as twiddle factor that is shown with W_N^{nk}. The computation can be performed faster by using twiddle factor as it depends on the number of points used and there is no need to recalculate it and the values can be referred to a matrix of twiddle factors. As the transform time is very crucial in FFT process, there is always a trade-off between the core size and the transform time. In Xilinx there are four architectures of Pipelined-Streaming I/O, Radix4-Burst I/O, Radix2-Burst I/O and Radix2-Lite-Burst I/O. They have different features to cover different time and size requirements.

In Pipelined Streaming I/O architecture, the data is processed continuously. The Radix4 uses an iterative approach to process the data. The data is loaded and processed separately. It is smaller in size than the pipelined solution howeverhas a longer transform time. The third architecture has the same iterative approach as Radix4 althoughthas longer transform time. The Radix2 is based on Decimation In Frequency (DIF) and separates the input data into two halves of:

$$X(0), X(1),..., X(\frac{N}{2}-1) \ and \ X(\frac{N}{2}), X(\frac{N}{2}+1),..., X(N-1) \tag{3}$$

The FFT formula for both even and odd conditions can be written in two summations as follows:

$$X(k) = \sum_{n=0}^{\frac{N}{2}-1} a(n) W_{\frac{N}{2}}^{nk} \ , where \ a(n) = x(n) + x(n + \frac{N}{2})$$

$$and \tag{4}$$

$$X(2k+1) = \sum_{n=0}^{\frac{N}{2}-1} b(n) W_{\frac{N}{2}}^{nk}, where \ b(n) = x(n) - x(n + \frac{N}{2})$$

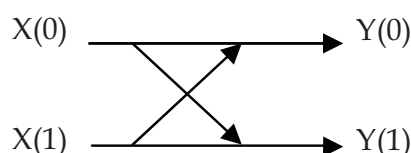This operation for 2 points can be graphically presented in Fig. 4.

Fig. 4. Two point butterfly graph

where $Y(0)=X(0)+X(1)$ and $Y(0)=X(0)\text{-}X(1)$, respectively. This FFT flow graph is called butterfly graph. When the number of point is increased, the butterfly is expanded. Radix2 scheme in third architecture separates the input data into two halves therefore the butterfly

is smaller. This means it is smaller in size than the Radix4 solution. The forth scheme is based on the Radix2 architecture. The "Radix2-Lite-Burst I/O" uses a time-multiplexed approach to the butterfly and the butterfly is even smaller howeverthe transform time is longer. In this project the Radix2-Burst I/O architecture as shown in Figure 5.4, is used due to the less hardware resource requirement compared to the other algorithms to prototype FFT (Yiqun et al., 2006).
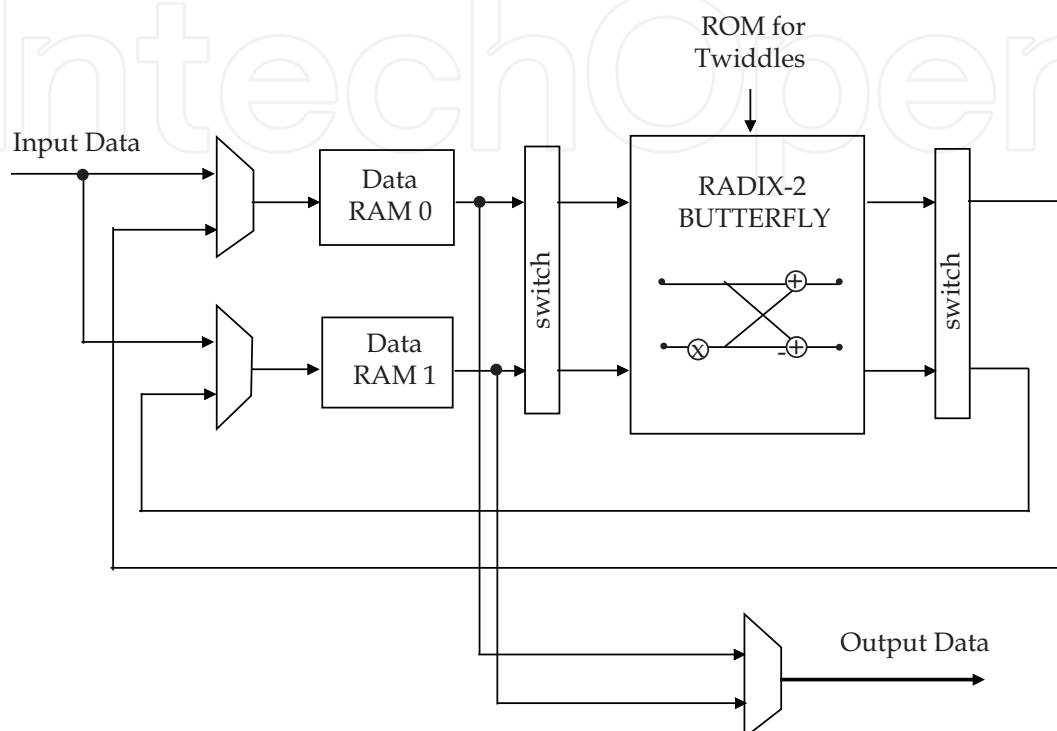
Fig. 5. Block diagram of the Radix2-Burst I/O architecture (Hemphill et al., 2007)

The signal cannot be simultaneously loaded and unloaded like Radix4, Burst I/O architecture and the loading should be stopped during the calculation of the transform.

The point sizes can be from 8 to 65536 and a minimum of block memories is used in this algorithm. When the point size is equal or less than 1024, both block memory and distributed memory can be used for data memories and phase memories.

In order to have accurate IFFT block, the model of targeted FPGA should be indicated in AccelDSP tool window. The AccelDSP is a synthesis tool that transforms a design in Matlab into a hardware module. This module can be VHDL or Verilog code. This tool controls an integrated environment with other design tools such as Matlab and Xilinx ISE tools.

There is a browser in GUI that shows the design hierarchy, the M-files, and the generated HDL source files. In this project, AccelDSP is used to generate the IFFT and FFT blocks. To guide the synthesis process, the design objects in the project explorer window is used. There are some parameters that should be defined here.

One of the important parameters in design of IFFT block is the algorithm to implement it which was discussed before and it is selected the Radix. The other parameter is the IFFT length that denotes the number of differential points in the IFFT. There is also option for I/O
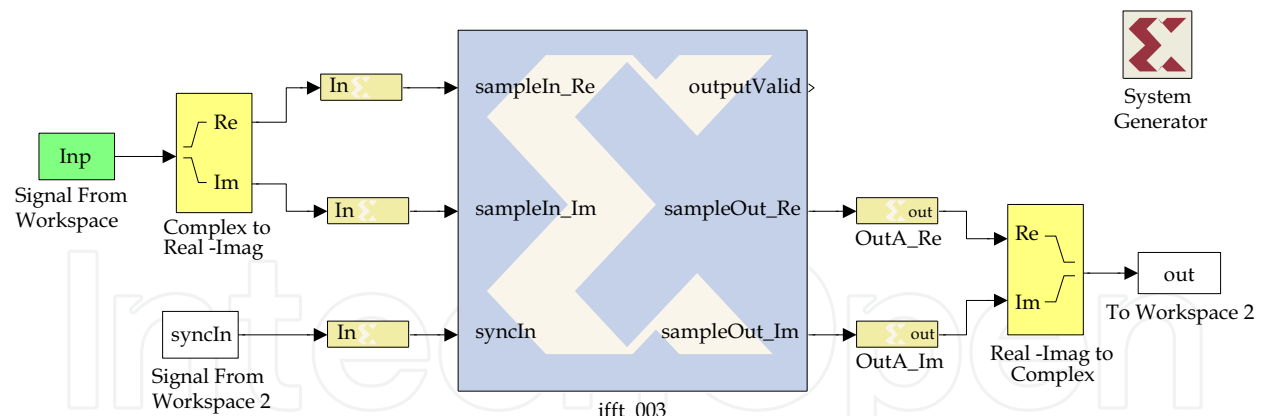
Fig. 6. System Generator block diagram of IFFT block and input output blocks

format. With the data I/O format option in AccelDSP GUI, input and output data can be initialized. Single buffering does not parallel any operations. Double buffering parallels the loading and unloading of frames of data. Natural Order I/O only applies to Single Fly architectures. Decimation Algorithm will naturally have inputs or outputs in digit/bit reverse ordering; DIF has natural order input and digit/bit reverse output, DIT has digit/bit reverse input and natural order output. The 'Yes' will force input and output to be natural order regardless of decimation type. The input data can be set to complex or real. Decimation algorithm parameter will be set to Decimation In Time (DIT) or Decimation In Frequency (DIF) algorithm. Scaling is the 1/IFFT Length ratio that can be set. Complex multiplier is another option that chooses different complex multiplier architectures. Round Mode sets the Quantizer round mode property for all data path quantizers. If Floor is selected for round mode, the numbers between 0 and -1 will be rounded to 0 and all the other numbers, bigger than zero and lower than -1, will round to the closest number. For example -1.8 will be -2. There is also a section for input data width that shows the number of bits used to represent the input. Input Data Fract Width shows the number of bits used to represent fractional part of input word width. Twiddle width is another parameter that shows the number of bits used to represent twiddle factors. In addition twiddle factor width is the number of bits used to represent the fractional part of phase factors. The range of the phase factors is (-1, 1) and therefore 2 bits are always needed for the integer part of the phase factors. The fractional part will always, twiddle factor width=twiddle width - 2. The data width can be also modified for output of IFFT. Output data width depends on the scaling option. If Scaling is set to 'Yes', output data width = input data width. If scaling is set to 'No', output data width = input data width + $log2$ (IFFT length) + 1. The output data fractional width indicates the greater of input data fractional width or twiddle fractional width.

Another important setting in AccelDSP tool is about the form of flow in the design. For this particular application, the flow should be set to System Generator. At the end of design, a library including the IFFT block with desired name is created. From Matlab simulink environment the library and IFFT block is accessible.

When the IFFT block is inserted in simulink window, some other components are required to complete the model which is shown in Fig. 6. These components are Input data, signal Synchronization line, output gate, and complex to real imaginary converter. At this time the

model should be able to run successfully. As shown in Fig. 6, the centre block with Xilinx sign at the background is the IFFT model which is generated by AccelDSP tools.

Then with system generator block, the NGC Netlist file can be generated. This file contains information that the ISE software is able to analyze it and estimate the hardware resource consumption which is presented in a table in ISE.

4. Results and discussions

When the IFFT block is designed in AccelDSP tool, the fixed point model of the design is generated. The AccelDSP automatically runs a MATLAB fixed-point simulation. Then the verification process can be done visually which is to compare the Fixed-Point Plot with the Floating-Point Plot to verify a match.

Fig. 7 presents an amplitude comparison between generated fixed point model of IFFT design with N=256 and Radix 2 shown by (a) and floating point model of this design which is shown by (b). The x-axis unit is the Number of samples per time (N). It can be observed that these two results are the same and therefore the IFFT processor is verified in terms of amplitude.
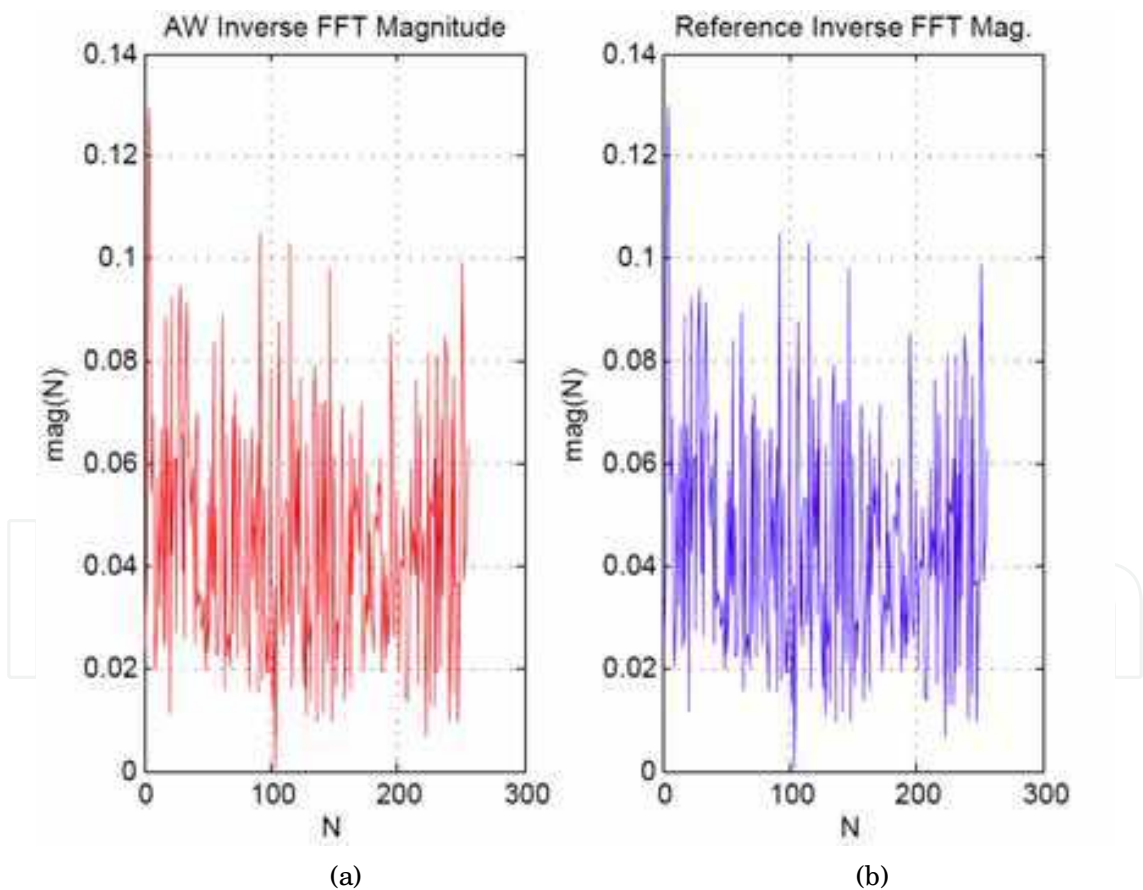

Fig. 7. Magnitude comparison between (a) fixed point model and (b) floating point model

The Angle comparison between fixed point model and floating point is presented in Fig. 8. As shown by Fig. 8 (a) and (b), the angle of signal in fixed point model of IFFT and the angle of signal in floating point model of the design overlap each other.
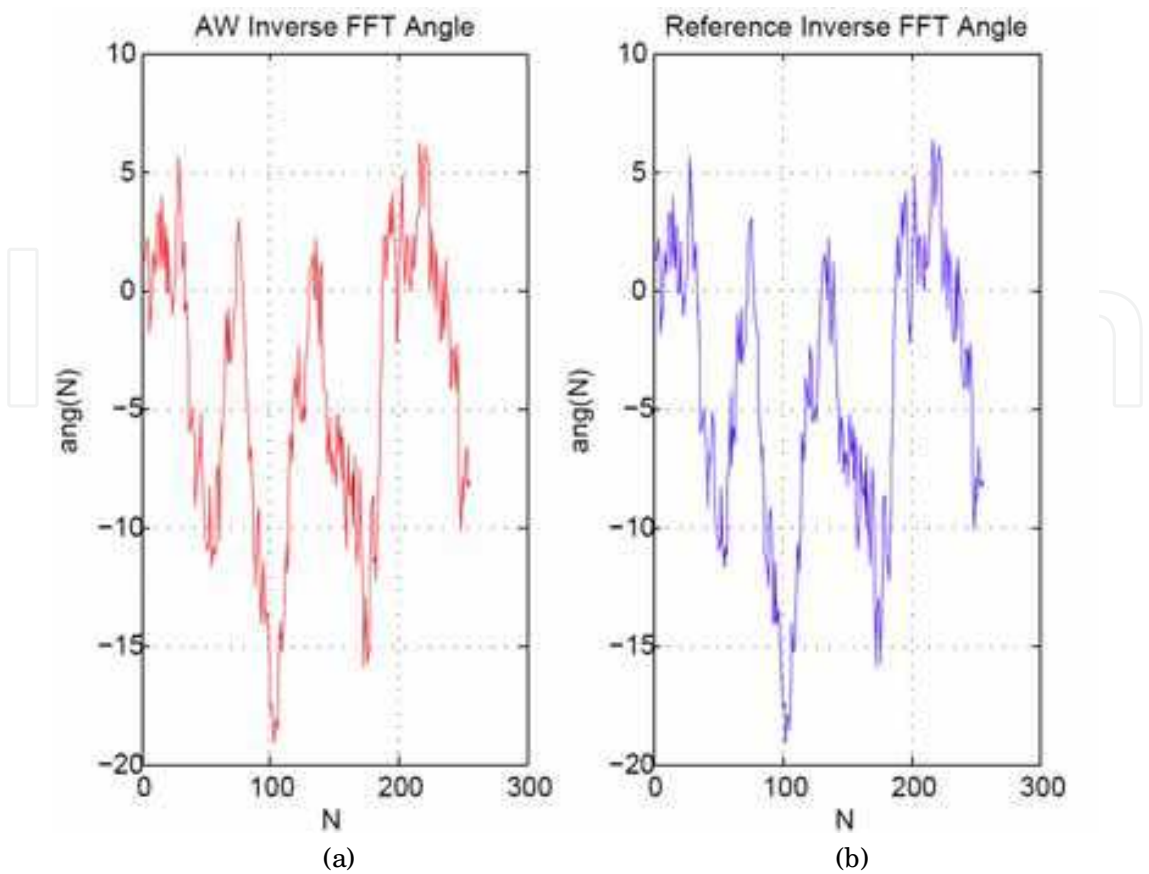
Fig. 8. Angel comparison between (a) fixed point model and (b) floating point model

The other form of verification can be performed using real and imaginary constellation graph. In order to verify designed IFFT, the AccelDSP tool generates real and imaginary constellation graphs and the verification can be done visually. Fig. 9 presents constellation based on IFFT with N=256 and Radix 2. In Fig. 9, the real part of fixed point model is shown by (a) which agree with (c) which is the real part in floating point model of IFFT design. The imaginary part of fixed point model is shown by (b) in Fig. 9 and it agree with (d) which is the imaginary part of floating point model of IFFT design.

As a result of discussed verifications, the error between fixed point model and floating point model is negative which is presented in Fig. 10. The other important parameters in designing hardware modules are hardware resource consumption and power consumption. These parameters can be estimated using Xilinx ISE tool. First the NGC Netlist file should be generated using System generator block in Matlab simulink and then through ISE the hardware consumption can be measured. In ISE GUI, from file folder, the saved project can be opened and then using Implement Top Module bottom, the hardware resource consumption table is generated which is presented in Table 1.

The main consideration is the percentages of DSP48 and IO Utilization. As shown in Table 1, the DSP48 and IO Utilization units of IFFT are used 6% and 16%, respectively.

The power consumed by the implemented DSI-SLM scheme is estimated by ISE XPower analyzer, Xilinx tool, after the place and route process. The processor consumes a total power of about 630 milliWatts and dynamic power of 10 milliWatts. Table 2 presents the details of power report. The ISE tool is also able to generate power consumption report.
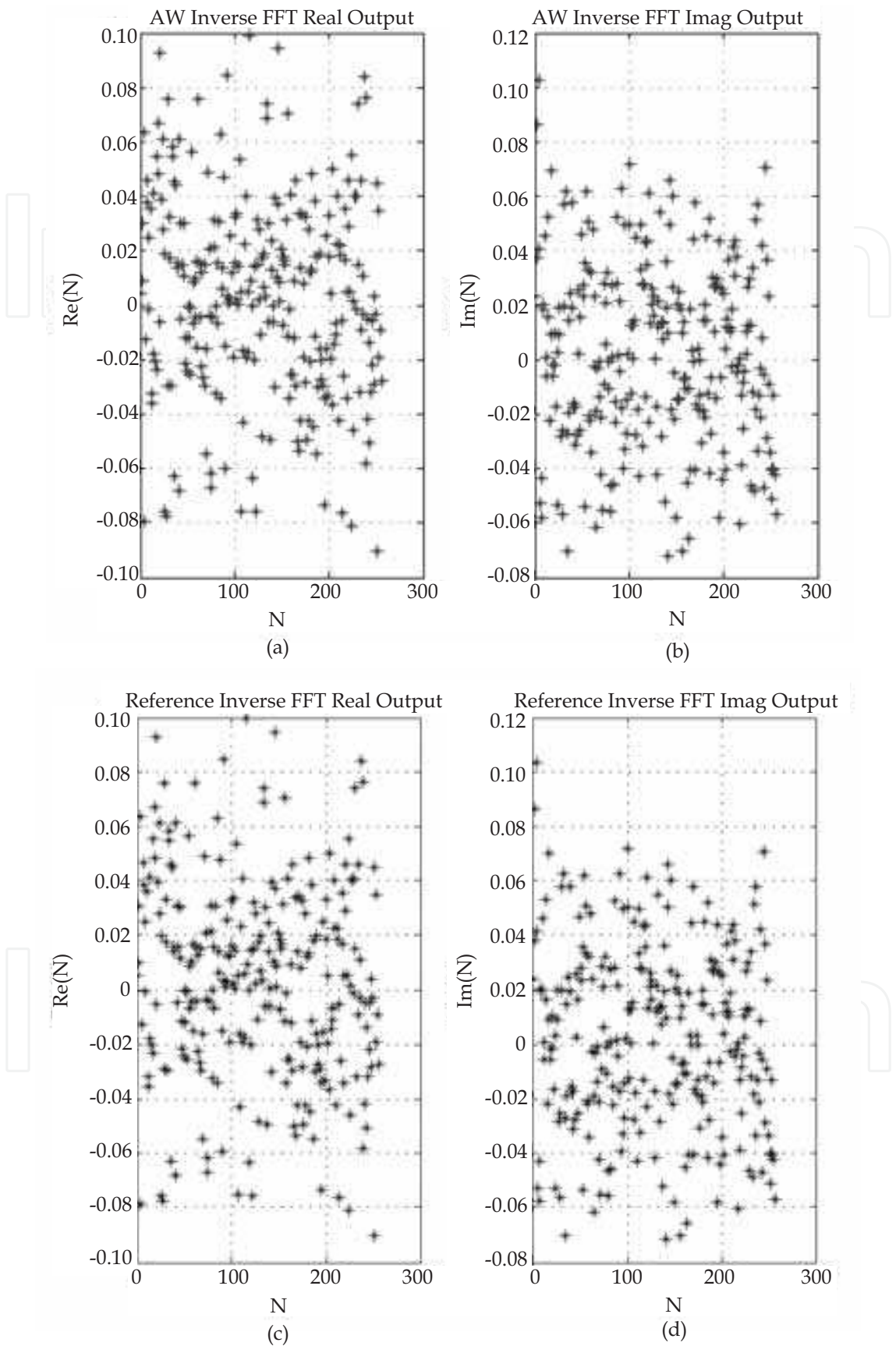
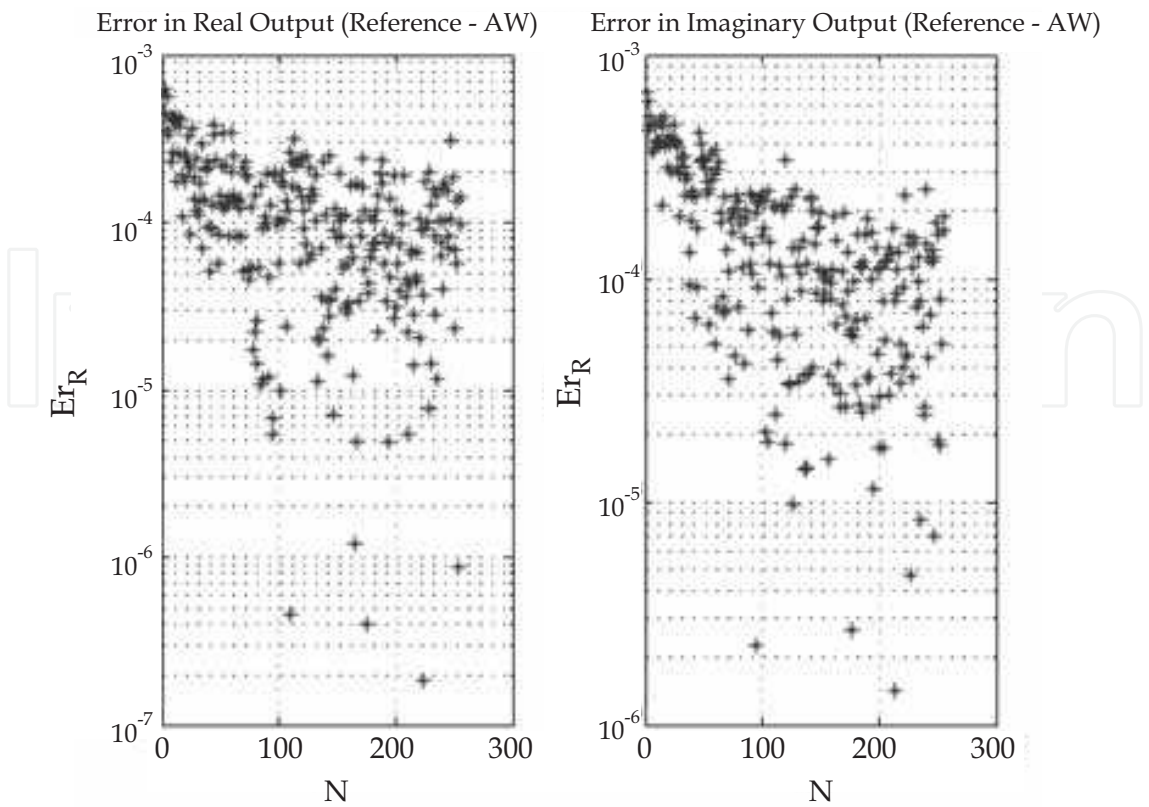Fig. 9. Real and imaginary signal verification of IFFT

Fig. 10. Error study between fixed point model and floating point model

xc5vfx30t-1ff665	Resources Used	Percentages of Consumption
Slices	252	4%
DSP48 Slices	4	6%
Number of fully used LUT-FF pairs	455	56%
IO Utilization	58	16%

Table 1. Hardware resource consumption of IFFT block with Radix-2 and N=256

Name	Power [W]	Resources		
		Used	Total Available	Utilization [%]
Logic	0.00006	538	20480	2.6
Signals	0.00057	1103	---	---
DSP	0.00026	4	64	6.3
Total Quiescent Power	0.61977	N/A		
Total Dynamic Power	0.01030			
Total Power	0.63008			

Table 2. Power consumption report for IFFT with Radix-2 and N=256

As mentioned before, one of main consideration in designing OFDM systems is the computational complexity which can be defined by the number of real additions and multiplications that is required for hardware implementation of a system.

According to [Baxely et al., 2007] Each IFFT requires $N/2logN+N/2$ complex multiplication and $NlogN$ complex addition. A complex multiplication takes four real multiplications and two real additions. Total number of real addition required for an IFFT, A_{IFFT} is presented in Eq. (1) and total number of real multipications for an IFFT, M_{IFFT} is presented in Eq. (2). Hence the total number of multiplication and addition of one IFFT can be given by Eq. (3)

$$A_{IFFT} = 2(\frac{N}{2}log N + \frac{N}{2}) + 2N log N \qquad (5)$$

$$M_{IFFT} = 4(\frac{N}{2}log N + \frac{N}{2}) \qquad (6)$$

$$T_{IFFT} = A_{IFFT} + M_{IFFT} = 5N log N + 3N \qquad (7)$$

where N is the number of subcarriers. When $N=256$, $T_{IFFT}=3850$. For $N=512$ and 1024, the value of T_{IFFT} is 8471 and 18484 respectively. It is obvious that by increasing the lenght of IFFT, the number of additions and multipication required for Implementing the IFFT is increased.

Design process of IFFT for higher number of subcarriers ($N=512$ and 1024) and Radix-4 is very similar to IFFT with Radix-2 and $N=256$. The Hardware resource Consumption and Power consumption for $N=512$ is presented in Table 3.

xc5vfx30t-1ff665	Resources Used	Percentages of Consumption
Slices	303	5%
DSP48 Slices	3	4%
Number of fully used LUT-FF pairs	554	64%
IO Utilization	58	16%

Table 3. Hardware resource consumption of IFFT block with Radix-2 and $N=512$

As shown in Table 3, the DSP48 and IO Utilization units of IFFT are used 4% and 16%, respectively.

According to ISE estimation, this IFFT processor consumes a total power of about 631 milliWatts and dynamic power of 11 milliWatts. Table 4 presents the details of this power report.

The Hardware Resource Consumption of IFFT processor with Radix-2 and $N=1024$ is presented in Table 5. It is shown that, the DSP48 and IO Utilization units of this IFFT block are used by 6% and 16%, respectively.

This IFFT processor consumes a total power of about 630 milliWatts and dynamic power of 10 milliWatts which are estimated by ISE tools. Table 6 presents the details of power report.

Name	Power [W]	Resources		
		Used	Total Available	Utilization [%]
Logic	0.00017	613	20480	3
Signals	0.00074	1198	---	---
DSP	0.00019	3	64	4.7
Total Quiescent Power	0.61993	N/A		
Total Dynamic Power	0.01197			
Total Power	0.63190			

Table 4. Power consumption report for IFFT with Radix-2 and *N*=512

xc5vfx30t-1ff665	Resources Used	Percentages of Consumption
Slices	330	6%
DSP48 Slices	4	6%
Number of fully used LUT-FF pairs	455	56%
IO Utilization	58	16%

Table 5. Hardware resource consumption of IFFT block with Radix-2 and *N*=1024

Name	Power [W]	Resources		
		Used	Total Available	Utilization [%]
Logic	0.00006	538	20480	2.6
Signals	0.00057	1103	---	---
DSP	0.00026	4	64	6.3
Total Quiescent Power	0.61977	N/A		
Total Dynamic Power	0.01030			
Total Power	0.63008			

Table 6. Power consumption report for IFFT with Radix-2 and *N*=1024

The Hardware Resource Consumption of IFFT processor with Radix-4 and *N*=256 is presented in Table 7. It is shown that, the DSP48 and IO Utilization units of this IFFT block are used by 18% and 16%, respectively.

xc5vfx30t-1ff665	Resources Used	Percentages of Consumption
Slices	696	13%
DSP48 Slices	12	18%
Number of fully used LUT-FF pairs	1064	49%
IO Utilization	58	16%

Table 7. Hardware resource consumption of IFFT block with Radix-4 and *N*=256

When comparing Table 7 and Table 1, it can be observed that the IO Utilization has no changes. However the consumption of DSP48 slices is increased by about 12%.

The IFFT processor with Radix-4 and N=256 consumes a total power of 0.65099 Watt and dynamic power of 0.02939 Watt which are estimated by ISE tools. Table 8 presents the details of power report. By Comparing Table 8 with Table 2, it is seen that power consumption of Radix-4 is increased compared to Radix-2 by about 0.02 Watt.

Name	Power [W]	Resources		
		Used	Total Available	Utilization [%]
Logic	0.00098	1364	20480	6.7
Signals	0.00322	2775	---	---
DSP	0.00078	12	64	18.8
Total Quiescent Power	0.62160	N/ A		
Total Dynamic Power	0.02939			
Total Power	0.65099			

Table 8. Power consumption report for IFFT with Radix-4 and N=256

xc5vfx30t-1ff665	Resources Used	Percentages of Consumption
Slices	629	12%
DSP48 Slices	12	18%
Number of fully used LUT-FF pairs	1001	51%
IO Utilization	58	16%

Table 9. Hardware resource consumption of IFFT block with Radix-4 and N=1024

The Hardware resource consumption of IFFT processor with Radix-4 and N=1024 is presented in Table 9. It is shown that, the DSP48 and IO Utilization units of this IFFT block are used by 18% and 16%, respectively.

Name	Power [W]	Resources		
		Used	Total Available	Utilization [%]
Logic	0.00080	1364	20480	6.7
Signals	0.00317	2775	---	---
DSP	0.00078	12	64	18.8
Total Quiescent Power	0.62125	N/ A		
Total Dynamic Power	0.02573			
Total Power	0.64698			

Table 10. Power consumption report for IFFT with Radix-4 and N=1024

The IFFT processor with Radix-4 and N=1024 consumes a total power of 0.64698 Watt and dynamic power of 0.02573 Watt which are estimated by ISE tools. Table 10 presents the details of power report.

5. Recent application of IFFT processor

Simple structure of an OFDM symbol consist of 4 sinusoids is shown in Fig. 11. The OFDM signal is created by the sum of multiple sinusoidal signals. Due to the constructive interference, as shown in Fig. 3 high peaks will be structured and as a result of destructive interference, the average power might be as low as zero. Hence, the ratio between peak and average will be high (Higashinaka et al., 2009).

Fig. 11. Sample of OFDM signal behavior

High Peak to Average Power Ratio (PAPR) is a major design challenge in OFDM systems (Krongold et al., 2003; Bauml et al., 1996; Wei et al., 2006).

The reason is that when OFDM signal with high PAPR is introduced to amplification stage, Power Amplifier (PA) which is usually peak power limited, is forced to operate in the non-linear region (Nieto, 2005). This will cause two impacts, out-of-band distortion or spreading the spectrum that can be measured by Adjacent Channel Power Ratio (ACPR) metric and in-band distortion, which can be measured by Error Vector Magnitude (EVM) metric.

There are some PAs with a wide dynamic linear region (Class AB), however they are generally expensive, consume more power, and less efficient (Cooper, 2008; Varahram et al., 2009; Sharma et al., 2010). Hence, in order to have high-efficiency OFDM signal and extended battery life, the PAPR must be reduced and the linearity of PA should be maximized.

The PAPR is calculated as the ratio of the maximum power and the average power of signal and can be defined by:

$$PAPR(A) = \frac{max\left[|s(t)|^2\right]}{E\left[|s(t)|^2\right]} \tag{8}$$

where $s(t)$ is the N carriers OFDM envelope presented as below (Ochiai, 2003):

$$s(t) = \sum_{n=0}^{N-1} A_n e^{j\omega_0 nt} \tag{9}$$

where $A = (A_0, A_1, ..., A_{(N-1)})$ is a modulated data sequence of length N in the time interval $(0, T)$, where A_i is a symbol from a signal constellation and T is the OFDM symbol duration.

where, $\omega_0 = 2\pi/T$ and $j = \sqrt{-1}$.

Basically the performance of a PAPR reduction is measured using Complementary Cumulative Distribution Function (CCDF) graph. It denotes the probability that the PAPR of a data symbol exceeds a predefined threshold as expressed by (Han et al., 2005; Heo et al., 2009):

$$
\begin{aligned}
probability(PAPR \rangle z) &= 1 - probability(PAPR \le z) \\
&= 1 - F(z)^N = 1 - (1 - exp(-z))^N \\
F(z) &= 1 - exp(z)
\end{aligned} \tag{10}
$$

where N is the number of subcarriers and z is the threshold. Basically, this probability function is used as a graph to determine the ability of an algorithm in reducing the PAPR of the OFDM signal and the PAPR is usually compared to unmodified OFDM signal at 0.01% CCDF which is shown by 10^{-4} CCDF in horizontal vector of graphs. A typical OFDM signal without any PAPR reduction technique has about 8dB to 13dB PAPR at 10^{-4} CCDF (Raab et al., 2011). Therefore, when a PAPR reduction technique is applied to the OFDM system, it is expected to reduce the 13dB PAPR to some lower value. According to the IEEE standard (IEEE STD 802.16e™-2005), the reduction should be at least 3dB.

Several techniques have been developed to reduce PAPR of the OFDM signal. There are two main categories for these techniques, distortion based methods (which means that applying these methods result in out-of-band distortion) and distortion less methods (there is no out-of-band distortion). First category includes Clipping (May et al., 1998), Windowing (Van et al., 1998), Envelope Scaling (Foomooljareon et al., 2002), Random Phase Updating (Nikookar et al., 2002), Peak Reduction Carrier (Tan et al., 2003), Companding (Hao et al., 2006; Hao et al., 2010; Cao et al., 2007; Chang et al, 2010; Hao et al., 2008; Kim et al., 2008) and other modified version of these methods.

Clipping is a simple technique for PAPR reduction, where in the transmitter, the signal is clipped to a desired level and the phase information remains unchanged. The clipping method applies distortion to the system; therefore normally clipping technique is integrated with filtering method in expense of additional IFFT and FFT blocks which increase the

complexity of the system. In windowing technique a large signal peak is multiplied with a certain frame. Envelope scaling method is an algorithm to reduce PAPR by scaling the input envelope for some subcarriers before they are sent to IFFT. In the random phase updating algorithm, some random phases are generated and assigned for each carrier. The process of updating is continued till the peak value of the OFDM signal is below the threshold. The peak reduction carrier involves the use of a higher order modulation scheme to represent a lower order modulation symbol (Vijayarangan et al., 2009). The Companding technique is used to compress and expand the OFDM signal in order to reduce PAPR. The speech processing is the main application of companding method as it has less frequent peaks problem.

The second category of PAPR reduction methods is named distortionless techniques. These methods have significant PAPR performance without causing nonlinear distortion. However, they typically incur large computational complexities and sometimes side information transmission. Moreover, these methods usually require receiver side modifications that may be incompatible to existing communication systems. Such approaches include Coding (Jones et al., 1994; Kwon et al., 2009), Partial Transmit Sequence (PTS) (Muller et al., 1997; Gao et al., 2009; Chen et al., 2010; Kang et al., 1999), Selected Mapping (SLM) (Bauml et al., 1996,), Dummy Signal Insertion (DSI) (Ryu et al., 2004; Qian et al., 2005), Tone Injection and Tone Reservation (Tellado, 2000), Interleaving (Jayalath et al., 2000), Active Constellation Extension (ACE) (Krongold et al., 2003).

Most of the recent researches are concentrating on modified SLM and PTS methods (Wang et al. 2011; Ghassemi et al. 2010; Naeiny et al., 2011; Kim et al., 2006; Jeon et al., 2011; Hong et al., 2010). According to the review, most of the modified methods reduce PAPR at the expense of complexity in the transmitter or degrading the spectrum efficiency of the system. It should be noted that improving the performance of SLM based techniques requires high number of IFFT processors which leads to high complexity. The PTS based methods also have drawback of complexity from another aspect. The improvement of these methods requires extra number of additions and multiplication to be implemented for finding optimum value which leads to high complexity. Hence, there is good scope to design a new method to overcome previous drawbacks and enhance the PAPR performance.

Here one of recently proposed methods for reducing PAPR of OFDM signal is presented (Mohammady et al., 2011). This method is named Optimum Phase Sequence insertion with Dummy Sequence Insertion (OPS-DSI). As shown in block diagram of OPS-DSI scheme in Fig. 13, there are two loops in OPS-DSI algorithm. If the PAPR is not less than the threshold, *Loop_a* with specific number of iterations is performed and the PAPR will be compared. If the PAPR is less than the threshold, the signal will be transmitted regardless of the second loop, otherwise the second loop *Loop_b* with predefined number of iterations is executed and the PAPR is calculated similarly. When *Loop_a* is performed, a new random dummy is generated and inserted to the signal, howeverthe phase sequence is the same as last iteration. It should be noted that the number of iterations is specified based on the PAPR reduction requirement and data rate. The value of the PAPR threshold is also based on each standard in wireless broadband.

It should be noted that when *Loop_b* is running, *Loop_a* is repeated. It means that in *Loop_b,* new random phase sequence will be selected and multiplied to the signal and then a new random dummy is inserted to the signal. When the threshold condition is passed, the signal

will be transmitted, however if the iterations for both loops are performed and still the PAPR is not less than the threshold, the signal with minimum PAPR among them will be transmitted.
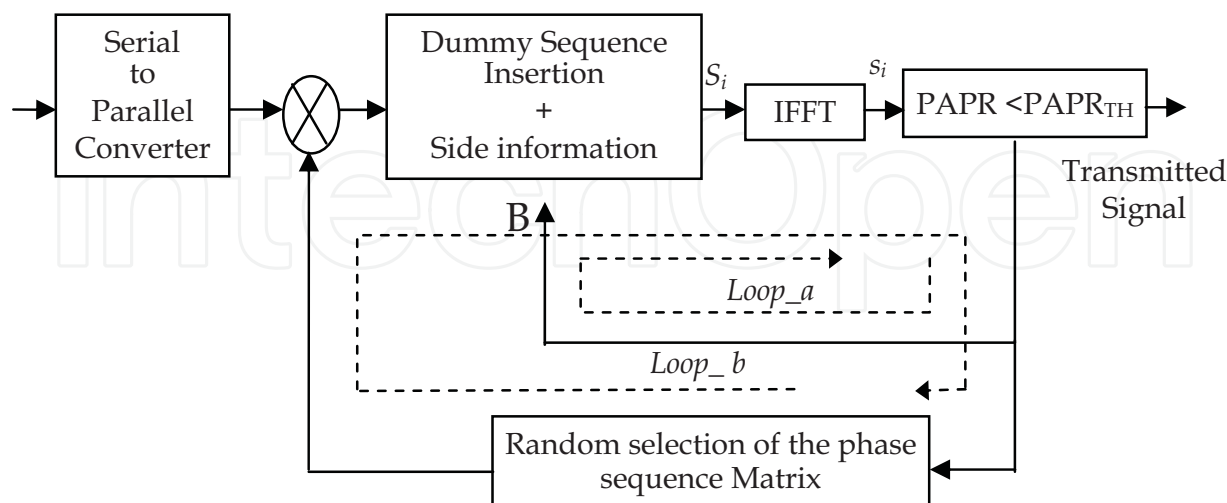

Fig. 12. Block diagram of the OPS-DSI scheme, transmitter

The CCDF result of a typical OFDM system with OPS-DSI scheme is compared with C-SLM and DSI methods. As shown in Fig. 13 (a), the PAPR of original OFDM signal is about 11.8dB at 10^{-4} CCDF or 0.01% CCDF. When DSI method is applied to this system, the PAPR is reduced to about 9.9dB shown by Fig. 13 (b) which means that the PAPR performance is enhanced by about 1.9dB compared to original OFDM signal.

When the C-SLM method with 8 IFFTs (number of candidate signals, M=8) is applied to the OFDM signal, the PAPR of 8.5dB is achieved which is shown by Fig. 13 (c). In this case, the PAPR is enhanced by about 3.4dB.

It is shown by Fig. 13 (d) that when OPS-DSI scheme is applied to the OFDM signal, the PAPR of about 7.7dB is achieved. In other words, the PAPR is enhanced by about 4.2dB compared to original signal. The PAPR performance of implemented OPS-DSI scheme is shown by Fig. 13 (e). The implemented system shows slightly degraded PAPR performance which is due to the Hardware input bit resolution. The ISE tol is able to generate total data path delay for OPS-DSI design which is 10.937 ns. This delay is within the accepted range according to Shannon-Hartly theorem (Hartley, 1928).

While comparing this result with recent works (Jeon et al., 2011; Naeiny et al., 2011; Hong et al., 2010; Wang et al., 2011; Kim et al., 2006), the face that 4.2dB reduction is achieved with only one IFFT and lowest complexity makes OPS-DSI method a very attractive method suitable for FPGA implementation.

In some literature papers, the PAPR performance is studied using time domain symbols. Fig. 14 presents 1024 samples of output signal with and without PAPR. Blue color samples are the output signal without PAPR reduction and the red color samples are the output signal when PAPR reduction is applied. It can be observed that the OFDM signal peaks are suppressed. However the reduction seems to be insignificant. The reason is that OPS-DSI scheme is a probabilistic method and the reduction is based on signal modification, therefore, time domain graph is not an accurate study tool for this case.
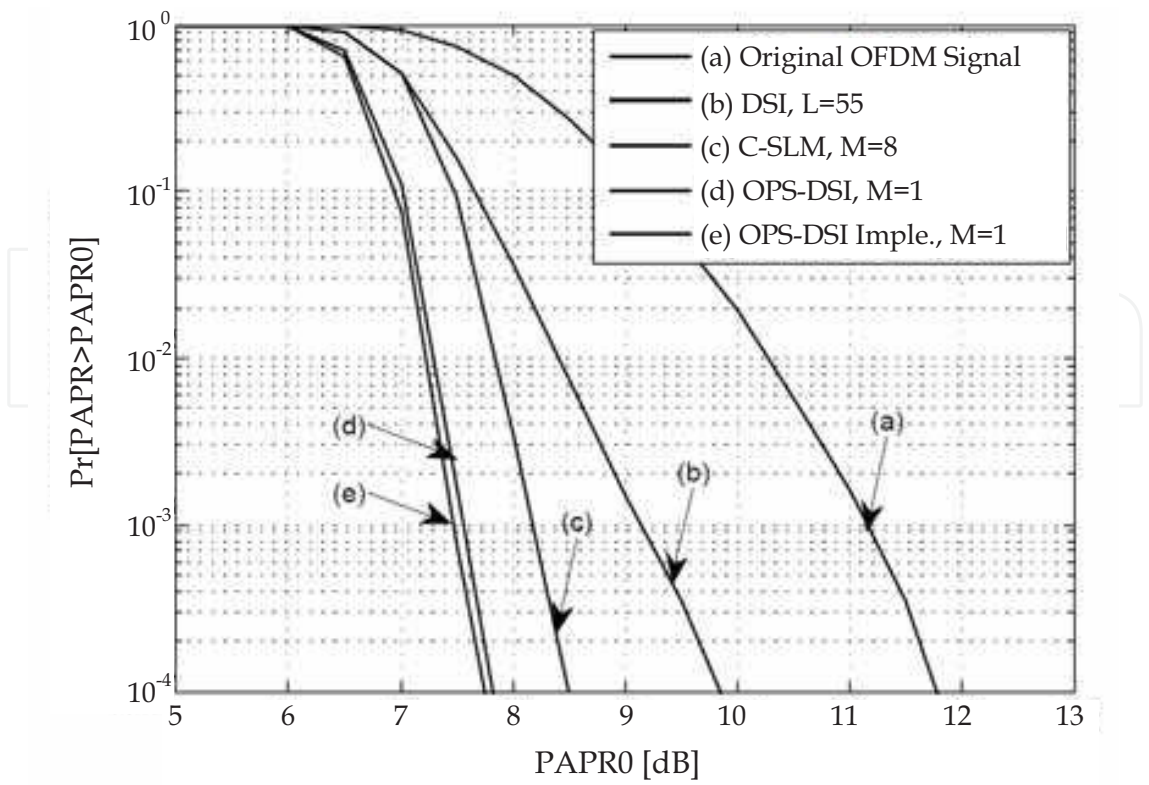
Fig. 13. Comparison of PAPR performance, (a) Original OFDM signal, (b) DSI method, (c) C-SLM method, (d) OPS-DSI method in simulation, (e) OPS-DSI in Implementation
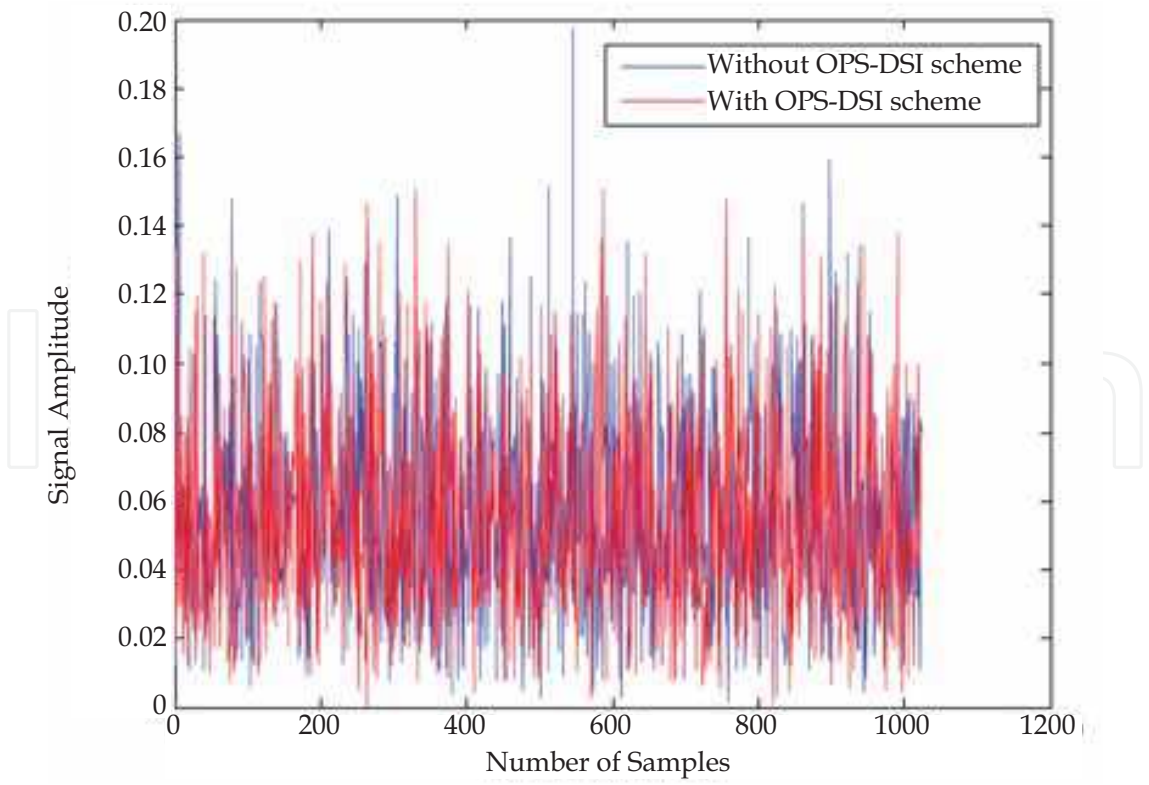

Fig. 14. OFDM signal in time domain, (Blue) without PAPR reduction technique, (Red) with PAPR reduction technique

6. Conclusion

In this chapter the OFDM transmition system is studied. The main component of IFFT processor is introduced. Hardware implementation of this block is performed and results are compared with the simulation. A very iportant application of IFFT in PAPR reduction scheme of OPS-DSI is reviewed. Different type of algorithms for IFFT are tested and Hardware resource consumption and power consumption are estimated using ISE tools. The complexity of implementing one IFFT block in the FPGA is mathematicaly computed.

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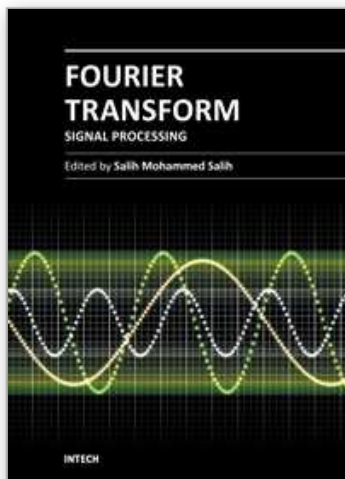
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Fourier Transform - Signal Processing

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The field of signal processing has seen explosive growth during the past decades; almost all textbooks on signal processing have a section devoted to the Fourier transform theory. For this reason, this book focuses on the Fourier transform applications in signal processing techniques. The book chapters are related to DFT, FFT, OFDM, estimation techniques and the image processing techqniques. It is hoped that this book will provide the background, references and the incentive to encourage further research and results in this area as well as provide tools for practical applications. It provides an applications-oriented to signal processing written primarily for electrical engineers, communication engineers, signal processing engineers, mathematicians and graduate students will also find it useful as a reference for their research activities.

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