18

SRAM Cells for Embedded Systems

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1. Introduction

Static Random Access Memories (SRAMs) continue to be critical components across a wide range of microelectronics applications from consumer wireless to high performance server processors, multimedia and System on Chip (SoC) applications. It is also projected that the percentage of embedded SRAM in SoC products will increase further from the current 84% to as high as 94% by the year 2014 according to the International Technology Roadmap for Semiconductors (ITRS). This trend has mainly grown due to ever increased demand of performance and higher memory bandwidth requirement to minimize the latency, therefore, larger L1, L2 and even L3 caches are being integrated on-die. Hence, it may not be an exaggeration to say that the SRAM is a good technology representative and a powerful workhorse for the realization of modern SoC applications and high performance processors.

This chapter covers following SRAM aspects, basic operations of a standard 6-transistor (6T) SRAM cells and design metrics, nano-regime challenges and conflicting read-write requirements, recent trends in SRAM designs, process variation and Negative Bias Temperature Instability (NBTI), and SRAM cells for emerging devices such as Tunnel-FET (TFET) and Fin-FET. The basic operation of a SRAM cell as a storage element includes reading and writing data from/into the cell. Success of these operations is mainly gauged by two design metrics: Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM). Apart from these metrics, an inline metric, N-curve is also used for measurement of read and write stability. The schematic diagrams and measurement process supported with HSPICE simulations results of different metrics will be presented in this chapter.

As standard 6T SRAM cell has failed to deliver the adequate read and write noise margins below 600mv for 65nm technology nodes, several new SRAM designs have been proposed in the recent past to meet the nano-regime challenges. In standard 6T, both read and write operations are performed via same pass-gate transistors, therefore, poses a conflicting sizing requirement. The recent SRAM cell designs which comprise of 7 to 10 transistor resolved the conflicting requirement by providing separate read and write ports.

SRAM cells are the first to suffer from the Process Variation (PV) induced side-effects. Because SRAM cells employ the minimum sized transistors to increase the device density into a die. PV significantly degrades the read and write noise margins and further exacerbates parametric yield when operating at low supply voltage. Furthermore, SRAM cells are particularly more susceptible to the NBTI effect because of their topologies. Since, one of the PMOS transistors is always negative bias if the cell contents are not flipped, it

introduces asymmetry in the standard 6T SRAM cell due to shift in threshold voltage in either of PMOS devices, as a result poor read and write noise margin. A brief discussion on the impact of PV and NBTI on the SRAM will be covered in this chapter.

Finally, SRAM architectures for emerging devices such as TFET and Fin-FET will be discussed in this chapter. Also issues related to uni-directional devices (TFET) for realization of SRAM cell will be highlighted as uni-directional devices poses severe restriction on the implementation of SRAM cell.

2. Random-Access Memories (RAMs)

A random-access memory is a class of semiconductor memory in which the stored data can be accessed in any fashion and its access time is uniform regardless of the physical location. Random-access memories in general classified as read-only memory (ROM) and read/write memory. Read/write random-access memories are generally referred to as RAM. RAM can also be classified based on the storage mode of the memory: volatile and non-volatile memory. Volatile memory retains its data as long as power is supplied, while non-volatile memory will hold data indefinitely. RAM is referred as volatile memory, while ROM is referred as nonvolatile memory.

Memory cells used in volatile memories can be further classified into static or dynamic structures. Static RAM (SRAM) cells use feedback (or cross coupled inverters) mechanism to maintain their state, while dynamic RAM (DRAM) cells use floating capacitor to hold charge as a data. The charged stored in the floating capacitor is leaky, so dynamic cells must be refreshed periodically to retain stored data. The positive feedback mechanism, between two cross coupled inverters in SRAM provides a stable data and facilitates high speed read and write operations. However, SRAMs are faster and it requires more area per bit than DRAMs.

2.1 SRAM architecture

An SRAM cache consists of an array of memory cells along with peripheral circuitries, such as address decoder, sense amplifiers and write drivers etc. those enable reading from and writing into the array. A classic SRAM memory architecture is shown in Figure 1. The memory array consists of 2^n words of 2^m bits each. Each bit of information is stored in one memory cell. They share a common word-line (WL) in each row and a bit-line pairs (BL, complement of BL) in each column. The dimensions of each SRAM array are limited by its electrical characteristics such as capacitances and resistances of the bit lines and word lines used to access cells in the array. Therefore, large size memories may be folded into multiple blocks with limited number of rows and columns. After folding, in order to meet the bit and word line capacitance requirement each row of the memory contains 2^k words, so the array is physically organized as 2^{n-k} rows and 2^{m+k} columns. Every cell can be randomly addressed by selecting the appropriate word-line (WL) and bit-line pairs (BL, complement of BL), respectively, activated by the row and the column decoders.

The basic static RAM cell is shown in inset of Figure 1. It consists of two cross-coupled inverters (M3, M1 and M4, M2) and two access transistors (M5 and M6). The access transistors are connected to the wordline at their respective gate terminals, and the bitlines at their source/drain terminals. The wordline is used to select the cell while the bitlines are

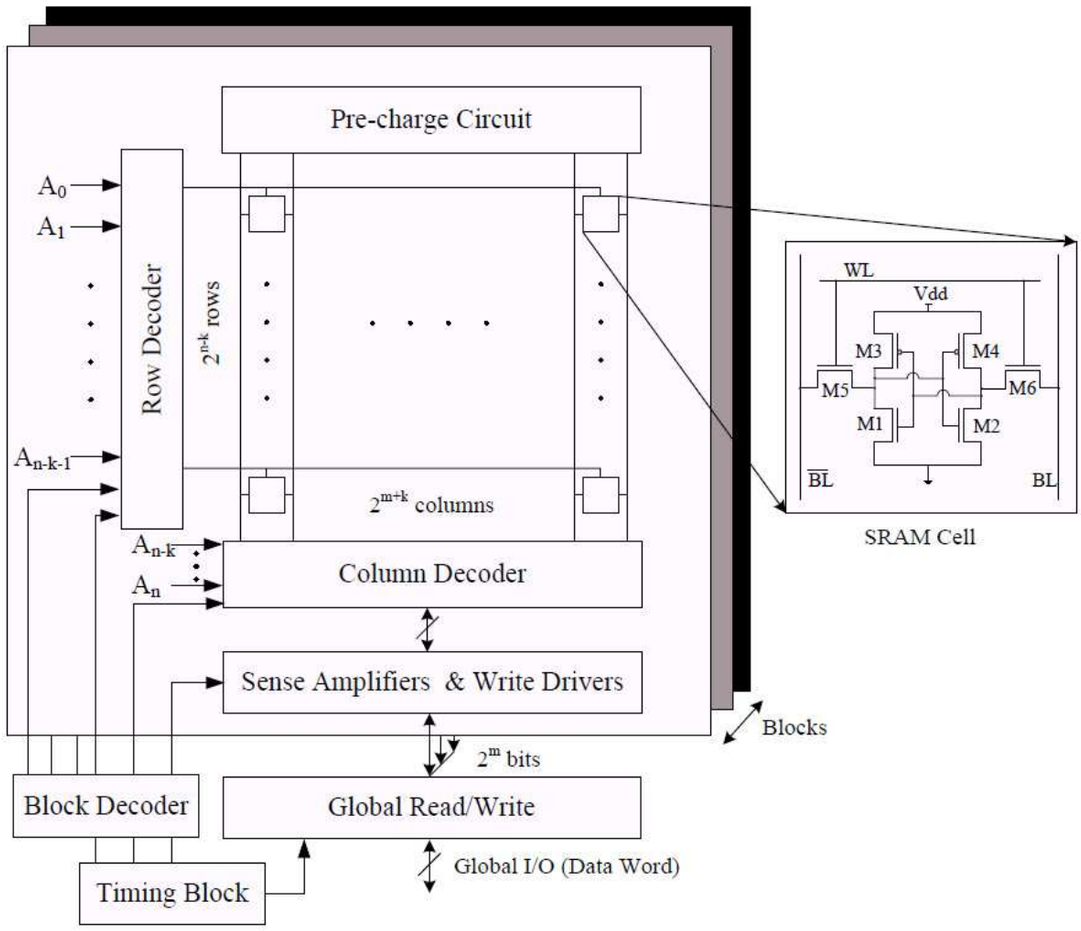

Fig. 1. SRAM architecture.

used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side. The two complementary bitlines are used to improve speed and noise rejection properties [D. A. Hodges, 2003; S. M. Kang, 2003].

The voltage transfer characteristics (VTC) of cross-coupled inverters are shown in Figure 2. The VTC conveys the key cell design considerations for read and write operations. In the cross-coupled configuration, the stored values are represented by the two stable states in the VTC. The cell will retain its current state until one of the internal nodes crosses the switching threshold, V_S. When this occurs, the cell will flip its internal state. Therefore, during a read operation, we must not disturb its current state, while during the write operation we must force the internal voltage to swing past V_S to change the state.

2.2 Standard six transistor (6T) SRAM

The standard six transistor (6T) static memory cell in CMOS technology is illustrated schematically in Figure 3. The cross-coupled inverters, M_1, M_3 and M_2, M_4, act as the storage element. Major design effort is directed at minimizing the cell area and power consumption

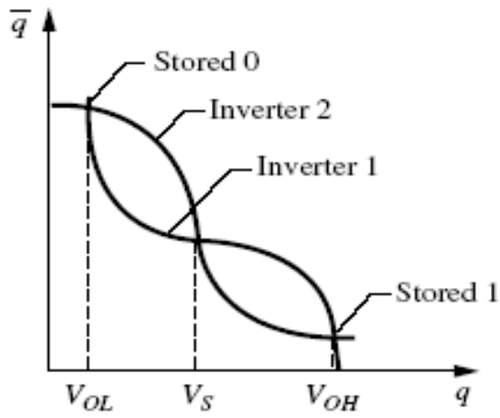

Fig. 2. Basic voltage transfer characteristics (VTC) of SRAM.

so that millions of cells can be placed on a chip. The steady state power consumption of the cell is controlled by sub-threshold leakage currents, so a larger threshold voltage is often used in memory circuits [J. Rabaey, 1999, J. P. Uyemura, 2002; A. S. Sedra 2003].

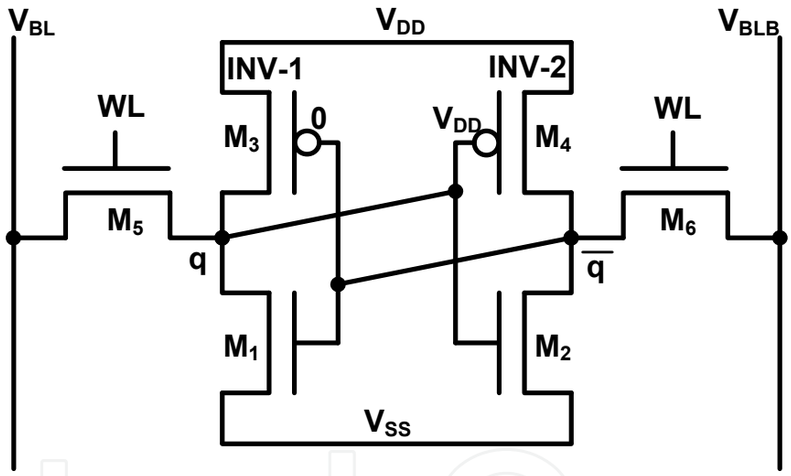

Fig. 3. Standard 6T SRAM cell.

3. Challenges in Bulk-Si SRAM scaling

Challenges for MOSFET scaling in the nanoscale regime including gate oxide leakage, control of short channel effects (SCE), contact resistance, ultra-shallow and abrupt junction technology apply to SRAM scaling as well. While it is possible to scale the classical bulk-Si MOSFET structure to sub-45 nm nodes [H. Wakabayashi *et al.*, 2003], effective control of SCE requires heavy channel doping (>5x10^{18} cm^{-3}) and heavy super-halo implants to suppress sub-surface leakage currents. As a result, carrier mobilities are severely degraded due to impurity scattering and a high transverse electric field in the ON-state. Further, more degraded SCE result in large leakage and larger subthreshold slope. Threshold voltage (V_{TH}) variability caused by random dopant fluctuations is another concern for nanoscale bulk-Si MOSFETs and is perceived as a fundamental roadblock for scaling SRAM. In addition to

statistical dopant fluctuations, line-edge roughness increases the spread in transistor threshold voltage (V_{TH}) and thus the on- and off- currents and can limit the size of the cache [A. J. Bhavnagarwala *et al.*, 2001; A. Asenov *et al.*, 2001].

3.1 Process variations

The study of process variations has greatly increased due to aggressive scaling of CMOS technology. The critical sources have variation including gate length and width, random dopant fluctuation, line-edge and line-width roughness, variation associated with oxide thickness, patterning proximity effect etc. These variations result in dramatic changes in device and circuit performance and characteristics in positive and negative directions. SRAM cells are especially susceptible to process variations due to the use of minimum sized transistors within the cell to increase the SRAM density. Furthermore, the transistors within a cell must be closely matched in order to maintain good noise margins. An individual SRAM cell does not benefit from the "averaging effect" observed in multi-stage logic circuits whereby random device variations along a path tend to partially cancel one another.

The stability of a 6T SRAM cell under process variation can be verified by examining its butterfly curves obtained by voltage transfer characteristics (VTC) and inverse voltage transfer characteristics (VTC^{-1}). Under process variation the read static noise margin (SNM) of a standard 6T SRAM cell is shown in Figure. 4 (a). One can observe that the SNM window has narrowed down due to process variation and this effect becomes severe at lower V_{DD} =0.3V, as shown in Figure. 5 (a). Therefore, process variation affects the reliability and performance severely at lower voltages. However, recently different SRAM cells have been proposed to circumvent the read SNM problem in SRAM cell. The most attracting cell in this direction is referred as read SNM free 8T SRAM cell. This cell provides 2-3X times better read SNM even at lower voltages as shown in Figure. 4 (b) and 5 (b).

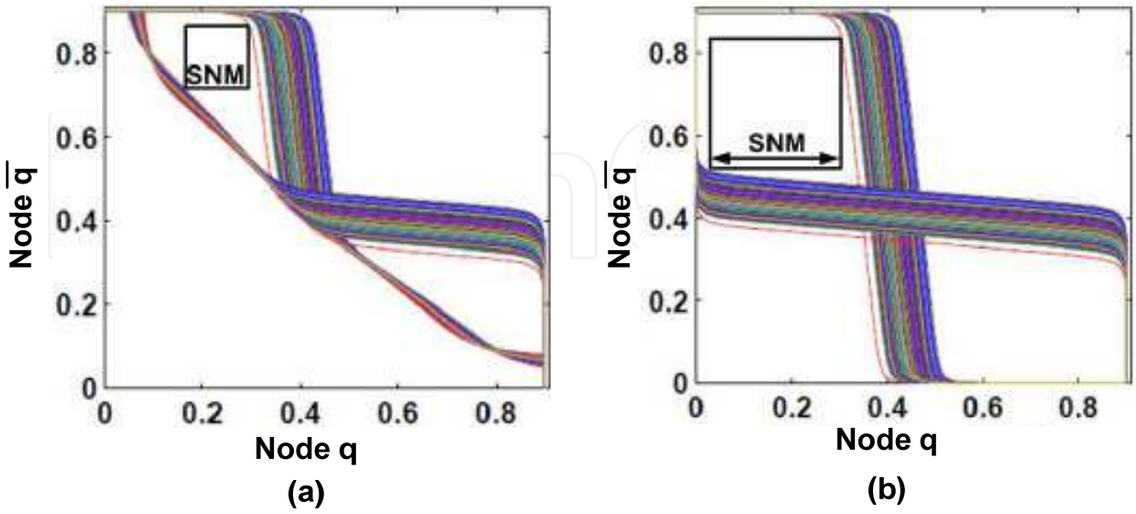

Fig. 4. Measurement of read static noise margin (SNM) at V_{DD}=0.9V for 45nm technology node (a) standard 6T SRAM cell, and (b) read SNM free 8T SRAM cell.

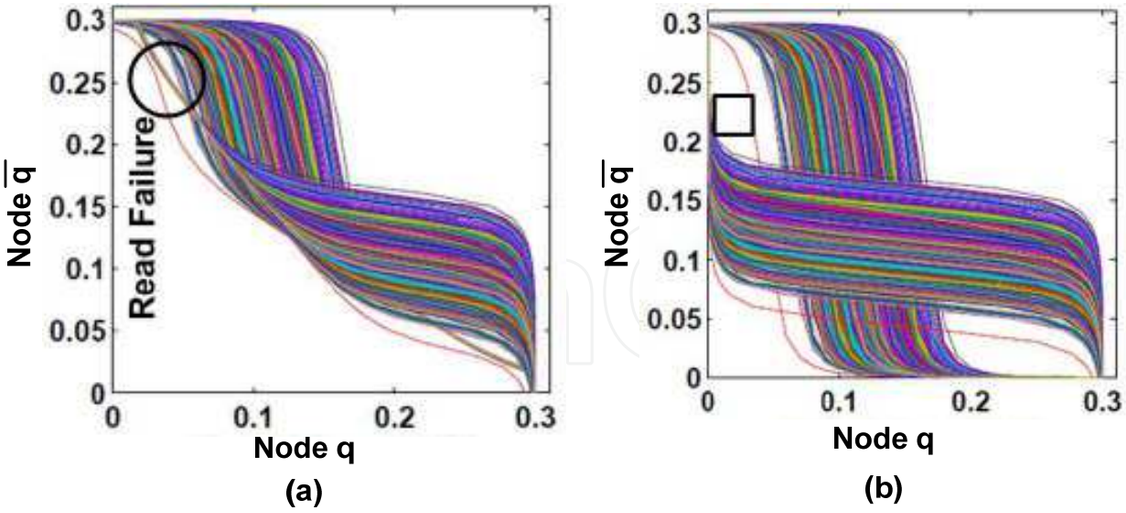

Fig. 5. Measurement of read static noise margin (SNM) at V_{DD}=0.3V for 45nm technology node (a) standard 6T SRAM cell, and (b) read SNM free 8T SRAM cell.

3.2 Device size requirements in SRAM cell

The standard 6T SRAM cell design space is continuously narrowing down due to lowering the supply voltage, shrinkage in device dimensions- attempting to achieve the high density and high performance objectives of on-chip caches. The SRAM cell stability, that is, read SNM and write-ability margins are further degraded by supply voltage scaling as shown above. The degradation in noise margins is mainly due to conflicting read and write requirements of the device size in the 6T cell. Both operations are performed via the same pass-gate (NMOS) devices, M5 and M6, as shown in Figure 3. For a better read stability (or read SNM), both pull down devices, M1 and M2 of the storage inverters must be stronger than the pass-gate devices, M5 and M6. While for write operation the opposite is desirable, that is, pass-gate devices, M5 and M6, must be stronger than pull up devices, M3 and M4, to achieve better write-ability, that is, weak storage inverters and strong pass-gate devices. Combining these constraints, yield the following relation.

strength (PMOS pull-up) < strength (NMOS access) < strength (NMOS pull-down)

The conflicting trend is also observed when read SNM and write noise margin (WNM) for different cell ratios and pull up ratios are simulated. Figure 6 shows the standard 6T SRAM cells' normalized read SNM and WNM measured for different cell ratio (CR), while the pull-up ratio is kept constant (PR=1). It can be seen from Figure 6 that the SNM is sharply increasing with increase in the cell ratio, while there is a gradual decrease in the WNM. For different pull-up ratio (PR), the normalized read SNM and WNM exhibit the similar trend. For example, there is a sharp increase in the read SNM and gradual decrease in WNM with increasing PR, while CR is kept constant to 2, as shown in Figure 7. In general, for a standard 6T cell the PR is kept to 1 while the CR is varied from 1.25 to 2.5 for a functional cell, in order to have a minimum sized cell for high density SRAM arrays. Therefore, in high density and high performance standard 6T SRAM cell, the recommended value for CR and PR are 2 and 1, respectively.

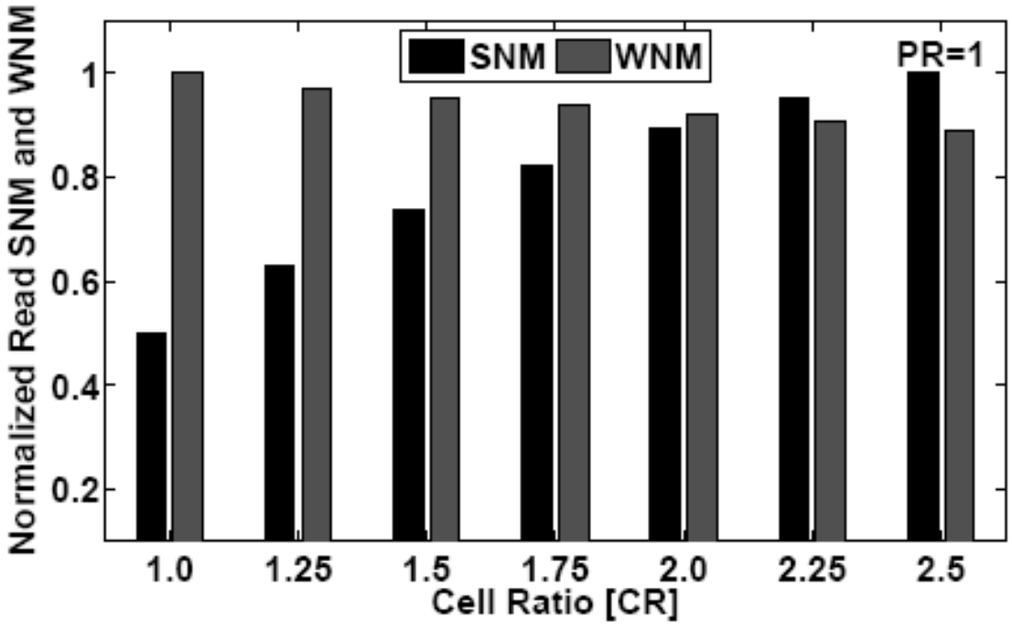

Fig. 6. Normalized read SNM and WNM of a standard 6T SRAM cell for different cell ratios (CR), while pull-up ratio (PR) was fixed to 1.

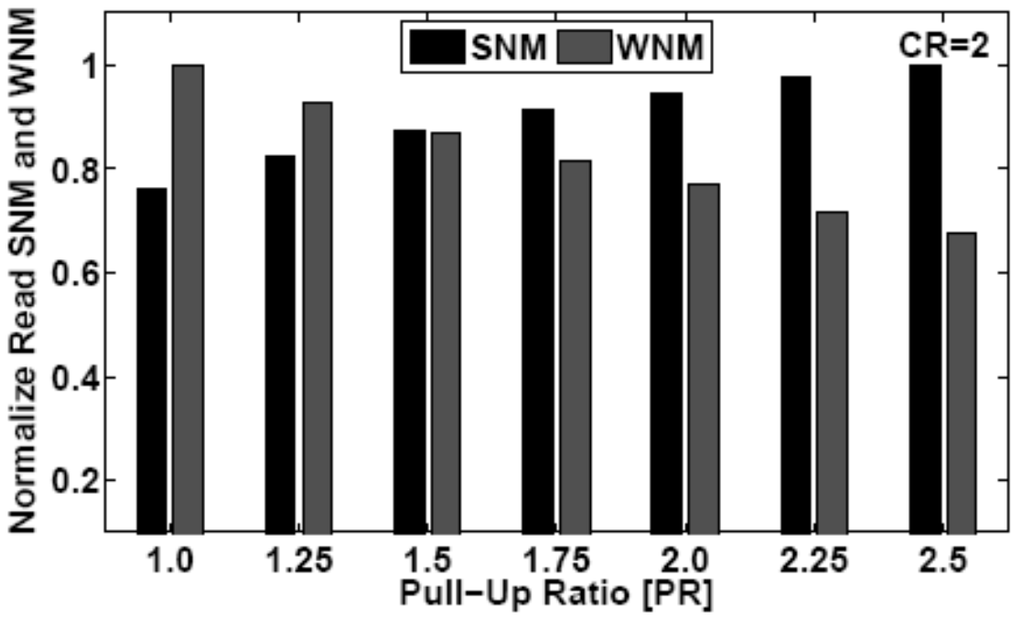

Fig. 7. Normalized read SNM and WNM of a standard 6T SRAM cell for different pull-up ratios (PR), while cell ratio (CR) is was fixed to 2.

3.3 Impact of NBTI on SRAM cells

A systematic shift in PMOS transistor parameters such as reduction in trans-conductance and drain current due to Negative Bias Temperature Instability (NBTI) over the life time of a system is becoming a significant reliability concern in nanometer regime. Particularly, sub-threshold devices and circuits which demand a high drive current for operation are hugely affected by threshold shifts and drive current losses due to NBTI. SRAM cells are particularly more susceptible to the NBTI effect because of their symmetric topologies. In other words, one of the PMOS transistor is always under stress if the SRAM cell contents are not periodically flipped. As a result, it introduces an asymmetric threshold shifts in both PMOS devices of a SRAM cell. The performance and reliability (noise margins) are significantly degraded in SRAM cells due to assymetric threshold voltage shift of PMOS devices. The degradation in read SNM of a standard 6T for different duty cycles (beta β) is shown in Figure 8. One can observe that there is a drastic reduction in read SNM of SRAM cell after five years of time span.

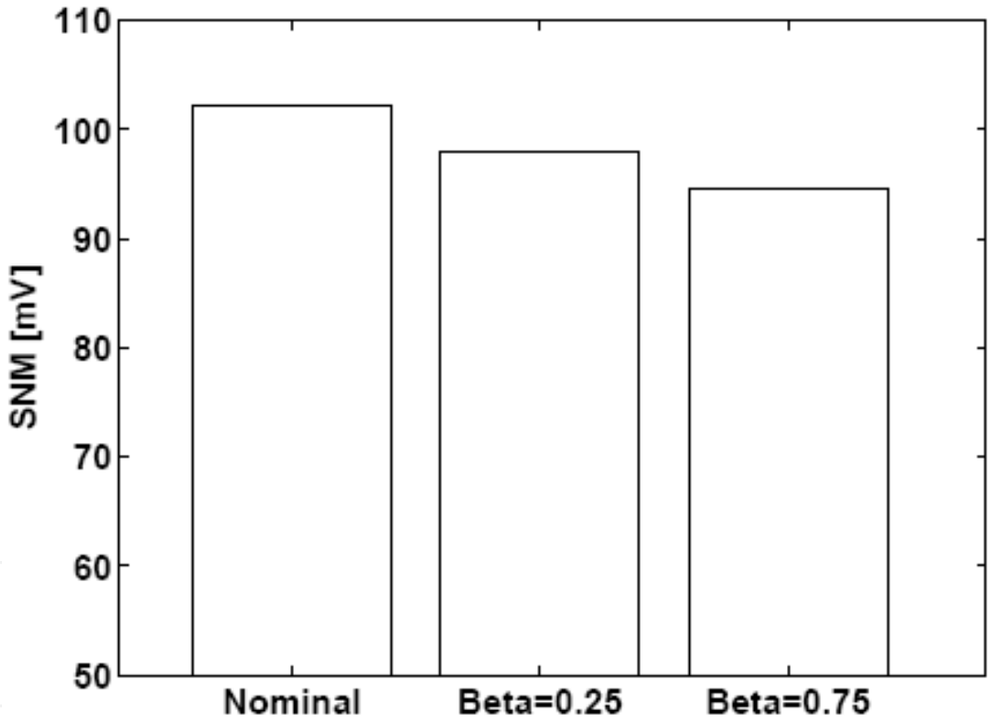

Fig. 8. Standard 6T SRAM cell read SNM degradation due to NBTI for different duty cycles.

3.4 SRAM scaling issues

Static Random Access Memory (SRAM) is by far the dominant form of embedded memory found in today's Integrated Circuits (ICs) occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products. The most commonly used memory cell design uses Six Transistors (6-T) to store a bit, so all of the issues associated with MOSFET scaling apply to scaling of SRAM [A. Bhavnagarwala, *et. al.,* 2005]. As memory will continue to consume a large fraction of the area in many future IC chips,

scaling of memory density must continue to track the scaling trends of logic. [Z. Guo *et al.*, 2005]. Statistical dopant fluctuations, variations in oxide thickness and line-edge roughness increase the spread in transistor threshold voltage and thus on- and off- currents as the MOSFET is scaled down in the nanoscale regime [A. Bhavnagarwala *et al.,* 2005]. Increased transistor leakage and parameter variations present the biggest challenges for the scaling of 6-T SRAM memory arrays [C. H. Kim, *et. al.,* 2005, H. Qin, *et. al.,* 2004].

The functionality and density of a memory array are its most important properties. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins (to be able to be read without changing the state, to hold the state, to be writable and to function within a specified timeframe), which are determined by device sizing (channel widths and lengths), the supply voltage and, marginally, by the selection of transistor threshold voltages. Increase in process-induced variations results in a decrease in SRAM read and write margins, which prevents the stable operation of the memory cell and is perceived as the biggest limiter to SRAM scaling [E. J. Nowak, *et. al.,* 2003].

The 6-T SRAM cell size, thus far, has been scaled aggressively by ~0.5x every generation (Figure 9), however it remains to be seen if that trend will continue. Since the control of process variables does not track the scaling of minimum features, design margins will need to be increased to achieve large functional memory arrays. Moving to more lithography friendly regular layouts with gate lines running in one direction, has helped in gate line printability [P. Bai *et al.,* 2005], and could be the beginning of more layout regularization in the future. Also, it might become necessary to slow down the scaling of transistor dimensions to increase noise margins and ensure functionality of large arrays, i.e., tradeoff cell area for SRAM robustness. [Z. Guo *et al.,* 2005].

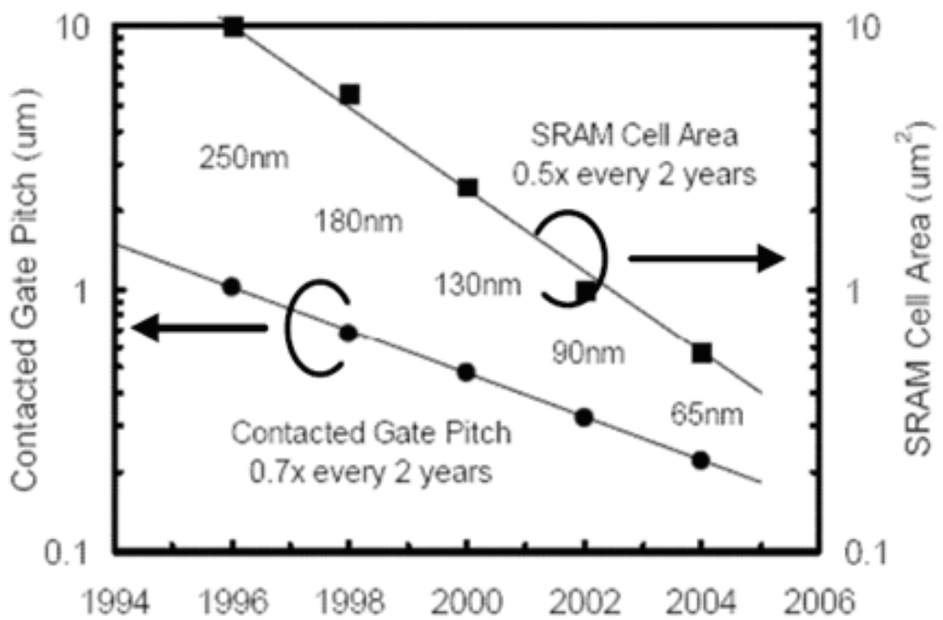

Fig. 9. SRAM cell size has been scaling at ~0.5 x per generation.

SRAM cells based on advanced transistor structures such as the planar UTB FETs and FinFETs have been demonstrated [E. J. Nowak *et al.,* 2003; T. Park *et al.,* 2003] to have excellent stability and leakage control. Some techniques to boost the SRAM cell stability, such as dynamic feedback [P. Bai *et al.,* 2005], are best implemented using FinFET technology, because there is no associated layout area or leakage penalty. FinFET-based SRAM are attractive for low-power, low voltage applications [K. Itoh, *et. al.,* 1998, M. Yamaoka, *et. al.,* 2005].

3.5 SRAM design Tradeoff's

a. Area vs. Yield

The functionality and density of a memory array are its most important properties. The area efficiency and the reliable printing of the SRAM cell which directly impacts yield are both reliant on lithography technology. Given lithography challenges, functionality for large memory arrays is guaranteed by providing sufficiently large design margins, which are determined by device sizing (channel widths and lengths), the supply voltage and, marginally, by the selection of transistor threshold voltages. Although upsizing the transistors increases the noise margins, it increases the cell area and thus lowers the density [Z. Guo *et al.,* 2005].

b. Hold Margin

In standby mode, when the memory is not being accessed, it still has to retain its state. The stored '1' bit is held by the PMOS load transistor (PL), which must be strong enough to compensate for the sub-threshold and gate leakage currents of all the NMOS transistors connected to the storage node V_L (Figure 8). This is becoming more of a concern due to the dramatic increase in gate leakage currents and degradation in I_{ON}/I_{OFF} ratio in recent technology nodes [H. Pilo *et al.,* 2005]. While hold stability was not of concern before, there has been a recent trend [H. Qin *et al.,* 2004] to decrease the cell supply voltage during standby to reduce static power consumption. The minimum supply voltage or the data retention voltage in standby is dictated by the hold margin. Degraded hold margins at low voltages make it increasingly more difficult to design robust low-power memory arrays. Hold stability is commonly quantified by the cell Static Noise Margin (SNM) in standby mode with the voltage on the word line V_{WL}=0 V. The SNM of an SRAM cell represents the minimum DC-voltage disturbance necessary to upset the cell state [E. Seevinck *et al.,* 1987], and can be quantified by the length of the side of the maximum square that can fit inside the lobes of the butterfly plot formed by the transfer characteristics of the cross-coupled inverters (Figure 10).

c. Read Margin

During a read operation, with the bit lines (BL and CBL) in their precharged state, the Word Line (WL) is turned on (i.e., biased at V_{DD}), causing the storage node voltage, V_R, to rise above 0V, to a voltage determined by the resistive voltage divider formed by the access transistor (AXR) and the pull-down transistor (NR) between BL and ground (Figure 8). The ratio of the strengths of the NR and AXR devices (ratio of width/length of the two devices) determines how high V_R will rise, and is commonly referred to as the cell β-ratio. If V_R exceeds the trip voltage of the inverter formed by PL and NL, the cell bit will flip during the

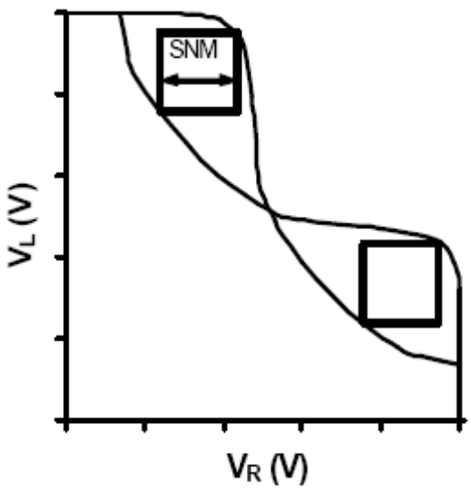

Fig. 10. Butterfly plot represents the voltage-transfer characteristics of the cross-coupled inverters in the SRAM cell.

read operation, causing a read upset. Read stability can be quantified by the cell SNM during a read access.

Since AXR operates in parallel to PR and raises V_R above 0V, the gain in the inverter transfer characteristic is decreased [A. J. Bhavnagarwala *et al.,* 2001], causing a reduction in the separation between the butterfly curves and thus in SNM. For this reason, the cell is considered most vulnerable to electrical disturbs during the read access. The read margin can be increased by upsizing the pull-down transistor, which results in an area penalty, and/or increasing the gate length of the access transistor, which increases the WL delay and also hurts the write margin. [J. M. Rabaey *et al.,* 2003] Process-induced variations result in a decrease in the SNM, which reduces the stability of the memory cell and have become a major problem for scaling SRAM. While circuit design techniques can be used to compensate for variability, it has been pointed out that these will be insufficient, and that development of new technologies, including new transistor structures, will be required [M. Yamaoka *et al.,* 2005].

d. Write Margin

The cell is written by applying appropriate voltages to be written to the bit lines, e.g. if a '1' is to be written, the voltage on the BL is set to V_{DD} while that on the BLC is set to 0V and then the WL is pulsed to V_{DD} to store the new bit. Careful sizing of the transistors in a SRAM cell is needed to ensure proper write operation. During a write operation, with the voltage on the WL set to V_{DD}, AXL and PL form a resistive voltage divider between the BLC biased at 0V and V_{DD} (Figure 8). If the voltage divider pulls V_L below the trip voltage of the inverter formed by PR and NR, a successful write operation occurs. The write margin can be measured as the maximum BLC voltage that is able to flip the cell state while the BL voltage is kept high. The write margin can be improved by keeping the pull-up device minimum sized and upsizing the access transistor W/L, at the cost of cell area and the cell read margin [Z. Guo *et al.,* 2005].

e. Access Time

During any read/write access, the WL voltage is raised only for a limited amount of time specified by the cell access time. If either the read or the write operation cannot be successfully carried out before the WL voltage is lowered, access failure occurs. A successful write access occurs when the voltage divider is able to pull voltage at V_L below the inverter trip voltage, after which the positive feedback in the cross-coupled inverters will cause the cell state to flip almost instantaneously. For the precharged bitline architecture that employs voltage-sensing amplifiers, a successful read access occurs if the pre-specified voltage difference, ΔV, between the bit-lines (required to trigger the sense amplifier) can be developed before the WL voltage is lowered [S. Mukhopadhyay *et al.*, 2004]. Access time is dependent on wire delays and the memory array column height. To speed up access time, segmentation of the memory into smaller blocks is commonly employed. With reductions in column height, the overhead area required for sense amplifiers can however become substantial.

4. Novel devices based SRAM design for Embedded Systems

4.1 FinFET based SRAM cell design

FinFETs have emerged as the most suitable candidate for DGFET structure as shown in figure 11 [E. Chin, et. al., 2006]. Proper optimization of the FinFET devices is necessary for reducing leakage and improving stability in FinFET based SRAM. The supply voltage (V_D), Fin height (H_{fin}) and threshold voltage (V_{th}) optimization can be used for reducing leakage in FinFET SRAMs by increasing Fin-height which allows reduction in V_D. [F. Sheikh, et. al., 2004]. However, reduction in V_D has a strong negative impact on the cell stability under parametric variations. We require a device optimization technique for FinFETs to reduce standby leakage and improve stability in an SRAM cell.

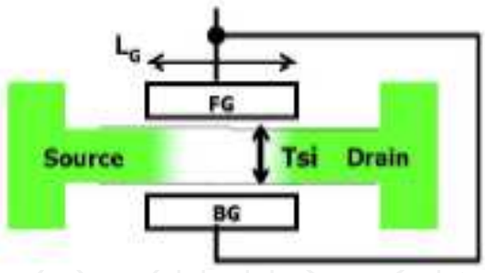

Fig. 11. Double Gate FinFET.

FinFET based SRAM cells are used to implement memories that require short access times, low power dissipation and tolerance to environmental conditions. FinFET based SRAM cells are most popular due to lowest static power dissipation among the various circuit configurations and compatibility with current logic processes. In addition, FinFET cell offers superior noise margins and switching speeds as well. Bulk MOSFET SRAM design at sub-45 nm node is challenged by increased short channel effects and sensitivity to process variations. Earlier works [Z. Guo, et. al., 2005; P. T. Su, et. al., 2006] have shown that FinFET based SRAM design shows improved performance compared to CMOS based design. Functionality and tolerance to process variation are the two important considerations for

design of FinFET based SRAM at 32nm technology. Proper functionality is guaranteed by designing the SRAM cell with adequate read, write, static noise margins and lower power consumption. SRAM cells are building blocks for Random Access Memories (RAM). The cells must be sized as small as possible to achieve high densities. However, correct read operation of the FinFET based SRAM cell is dependent on careful sizing of M1 and M5 in figure 12. Correct write operation is dependent on careful sizing of M4 and M6 as shown in the figure 12. As explained [F. Sheikh, et. al., 2004], the critical operation is reading from the cell. If M5 is made of minimum-size, then M1 must be made large enough to limit the voltage rise on Q' so that the M3-M4 inverter does not inadvertently switch and accidentally write a '1' into the FinFET based SRAM cell.

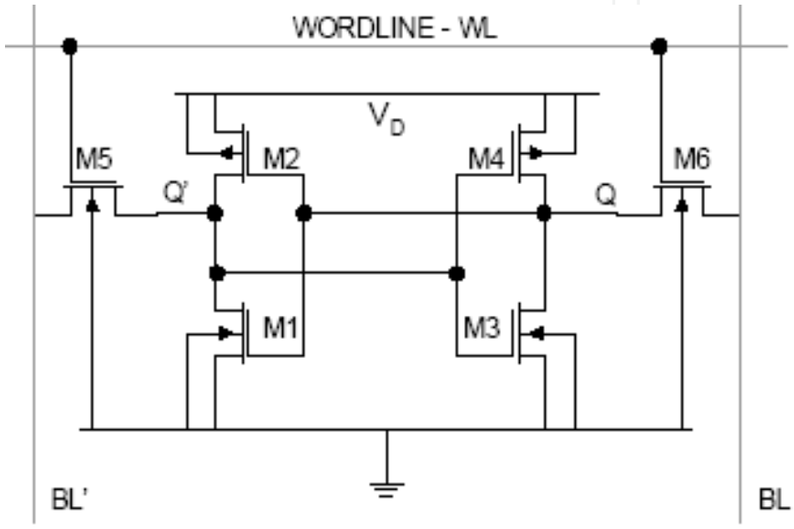

Fig. 12. 6T SRAM cell [F. Sheikh, et. al., 2004].

As explained [F. Sheikh, et. al., 2004], the sizing of the FinFET M5 and M6 is critical for correct operation once sizes for M1-M2 and M3-M4 inverters are chosen. The switching threshold for the ratioed inverter (M5-M6)-M2 must be below the switching threshold of the M3-M4 inverter to allow the flip-flop to switch from Q=0 to Q=1 state. The sizes for the FinFET can be determined through simulation, where M5 and M6 can be taken together to form a single transistor with twice the length of the individual transistors. It is well-understood that sizing affects noise margins, performance and power [Kiyoo Itoh, et. al., 1998; K. Zhang, et. al., 2005]. Therefore, sizes for pFinFET and nFinFET must be carefully selected to optimize the tradeoff between performance, reliability and power. We have studied FinFET based SRAM design issues such as: read and write cell margins, Static Noise Margin (SNM), power evaluation, performance and how they are affected by process induced variations [F. Sheikh, et. al., 2004].

4.2 Tunnel diode based SRAM cell design

As discussed in the previous sections, there is a fundamental limit to the scaling of the MOSFET threshold voltage, and hence the supply voltage. Scaling supply voltage limits the ON current (I_{ON}) and the I_{ON} - I_{OFF} ratio. This theoretical limit to threshold voltage scaling mainly arises from MOSFETs 60 mV/decade subthreshold swing at room temperature and

it significantly restricts low voltage operation. Therefore, it seems that quantum transistors such as Inter-Band Tunnel Field Effect Transistors (TFETs) may be promising candidates to replace the traditional MOSFETs because the quantum tunnelling transistor has smaller dimension and steep subthreshold slope. Compared to MOSFET, TFETs have several advantages:

- Ultra-low leakage current due to the higher barrier of the reverse p-i-n junction.
- The subthreshold swing is not limited by 60mV/dec at room temperature because of its distinct working principle.
- V_t roll-off is much smaller while scaling, since threshold voltage of TFET depends on the band bending in the small tunnel region, but not in the whole channel region.
- There is no punch-through effect because of reverse biased p-i-n structure.

One key difference between TFETs and traditional MOSFETs that should be considered in the design of circuits is uni-directionality. TFETs exhibit the asymmetric behavior of conductance. For instance, in MOSFETs the source and drain are inter-changeable, with the distinction only determined by the biasing during the operation. While in TFETs, the source and drain are determined at the time of fabrication, and the flow of current I_{ON} takes place only when $V_{DS} > 0$. For $V_{DS} < 0$ a substantially less amount of current flows, referred as I_{OFF} or leakage current. Hence, TFETs can be thought to operate uni-directionally. This uni-directionality or passing a logic value only in one direction has significant implication on logic and in particularly for SRAMs design.

5. SRAM bitcell topologies

Standard 6T SRAM cell has been widely used in the implementation of high performance microprocessors and on-chip caches. However, aggressive scaling of CMOS technology presents a number of distinct challenges for embedded memory fabrics. For instance, smaller feature sizes imply a greater impact of process and design variability, including random threshold voltage (V_{TH}) variations, originating from the fluctuation in number of dopants and poly-gate edge roughness [Mahmoodi et al., 2005; Takeuchi et al., 2007]. The process and design variability leads to a greater loss of parametric yield with respect to SRAM bitcell noise margins and bitcell read currents when a large number of devices are integrated into a single die. Predictions in [A.J.Bhavnagarwala et al., 2001] suggest the variability will limit the voltage scaling because of degradation in the SNM and write margin. Furthermore, increase in device mismatch that accompanies geometrical scaling may cause data destruction at normal V_{DD} [Calhoun et al., 2005]. Therefore, a sufficiently large read Static Noise Margin (SNM) and Write-Ability Margin (WAM) in a bitcell are needed to handle the tremendous loss of parametric yield.

Recently, several SRAM bitcell topologies have been proposed to achieve different objectives such as minimum bitcell area, low static and dynamic power dissipation, improved performance and better parametric yield in terms of static noise margins (SNM) and write ability margin (WAM). The prime concern in SRAM bitcell design is a trade-off among these design metrics. For example, in sub-threshold SRAMs, noise margin (robustness) is the key design parameter and not the speed [Wang & Chandrakasan, 2004, 2005]. Some of the attracting SRAM bitcell topologies having good noise margin are as follows.

5.1 8T SRAM bitcell topology

Figure 13 shows the read SNM free 8T bitcell [Chang et al., 2005, 2008; Suzuki et al., 2008; Takeda et al., 2006; Verma & Chandrakasan, 2008], a register file type of SRAM bitcell topology, which has separate read and write ports. These separate read and write ports are controlled by read (RWL) and write (WWL) wordlines and used for accessing the bitcell during read and write cycles, respectively. In 8T bitcell topology, read and write operations of a standard 6T SRAM bitcell are de-coupled by creating an isolated read-port or read buffer (comprised of two transistors, M7 and M8). De-coupling of read and write operations yields a non-destructive read operation or SNM-free read stability. The interdependence between stability and read-current is overcome, while dependence between density and read-current remains there. An additional leakage current path is introduced by the separate read-port which increases the leakage current as compared to standard 6T bitcell. Therefore, an increased area overhead and leakage power make this design rather unattractive, since leakage power is a critical SRAM design metric, particularly for highly energy constrained applications. The read bitline leakage current problem in the 8T bitcell is similar to the problem in the standard 6T bitcell, except that the leakage currents from the un-accessed bitcells and from the accessed bitcell affect the same node, RBL. So, the leakage currents can pull down RBL regardless of the accessed bitcells state. In [Verma & Chandrakasan, 2008] the bitline leakage current from the un-accessed bitcells is managed by adding a buffer-footer, shared by the all bitcells in that word.

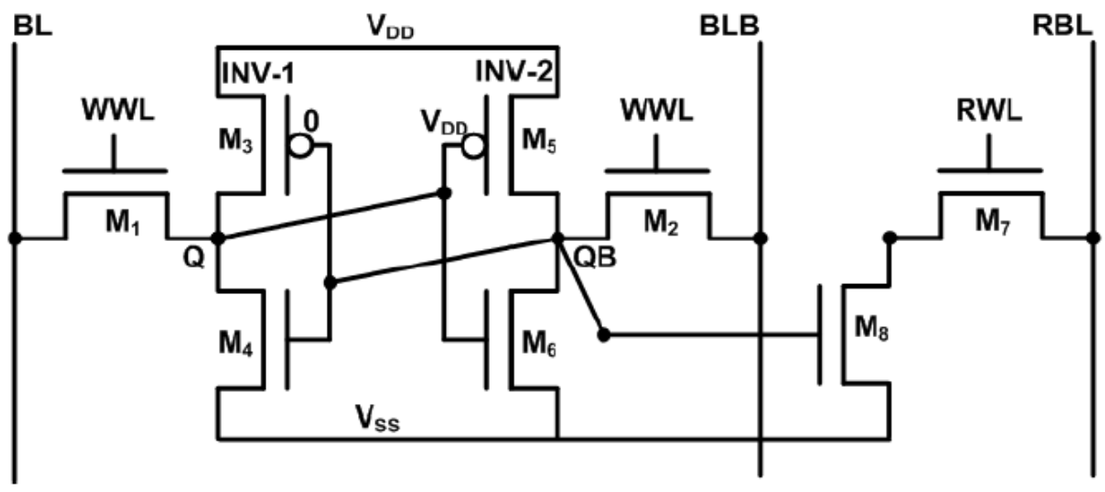

Fig. 13. Schematic diagram of read SNM free SRAM bitcell topology [Chang et al., 2005].

5.2 9T SRAM bitcell topology

Standard 6T bitcell along with three extra transistors were employed in nine-transistor (9T) SRAM bitcell [Liu & Kursun, 2008], to bypass read-current from the data storage nodes, as shown in Figure 14. This arrangement yields a non-destructive read operation or SNM-free read stability. However, it leads to 38% extra area overhead and a complex layout. Thin cell layout structure does not fit in this design and introduces jogs in the poly.

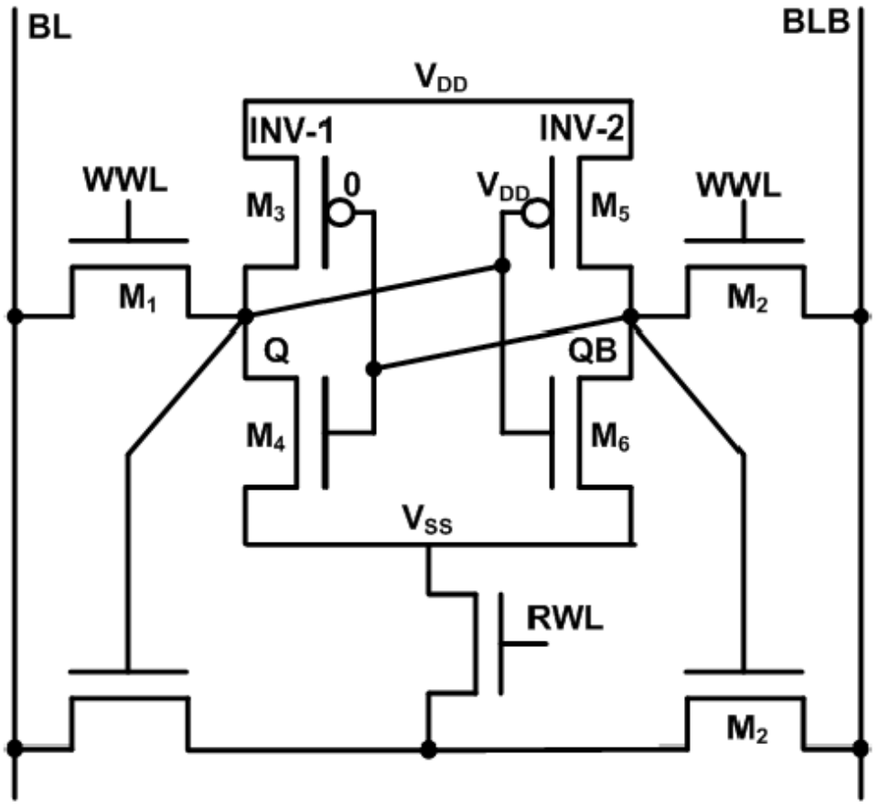

Fig. 14. Schematic diagram of 9T SRAM bitcell topology [Liu & Kursun, 2008].

5.3 10T SRAM bitcell topology

In the 10T bitcell [Calhoun & Chandrakasan, 2007], as shown in Figure 15, a separate read-port comprised of 4-transistors was used, while write access mechanism and basic data storage unit are similar to standard 6T bitcell. This bitcell also offers the same benefits as the 8T bitcell, such as a non-destructive read operation and ability to operate at ultra low voltages. But the 8T bitcell does not address the problem of read bitline leakage current, which degrades the ability to read data correctly. In particularly, the problem with the isolated read-port 8T cell is analogous to that with the standard (non-isolated read-port) 6T bitcell discussed. The only difference here is that the leakage currents from the un-accessed bitcells sharing the same read bit-line, RBL, affect the same node as the read-current from the accessed bitcell. As a result, the aggregated leakage current, which depends on the data stored in all of the unaccessed bitcells, can pull-down RBL even if the accessed bitcell based on its stored value should not do so. This problem is referred as an erroneous read. The erroneous read problem caused by the bitline leakage current from the un-accessed bitcells is managed by this 10T bitcell by providing two extra transistors in the read-port. These additional transistors help to cut-off the leakage current path from RBL when RWL is low and makes it independent of the data storage nodes content.

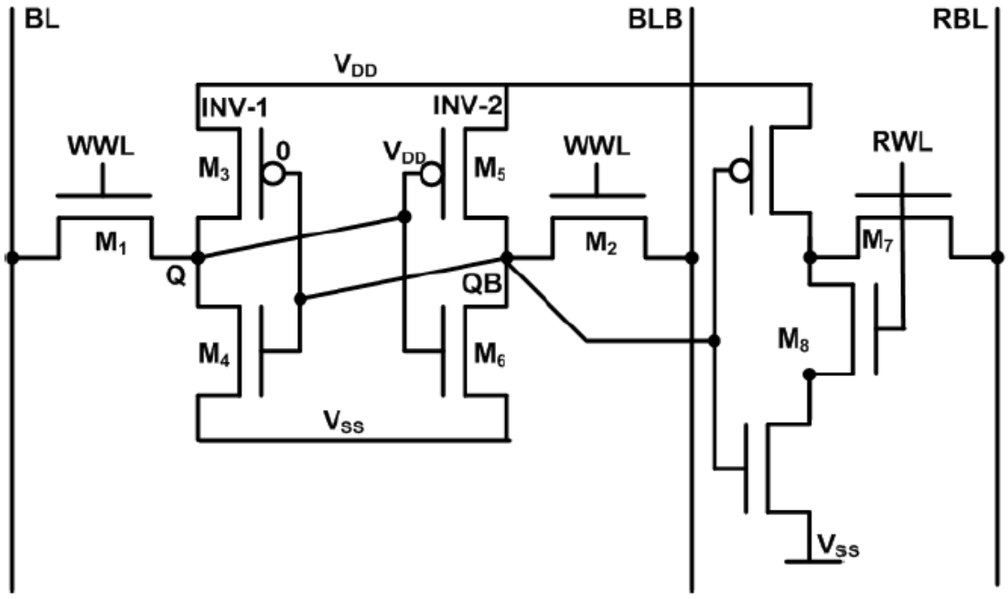

Fig. 15. Ultra-low voltage subthreshold 10T SRAM bitcell topology [Calhoun & Chandrakasan, 2007].

6. Summary

In this chapter, we have presented an existing review of bulk SRAM design and novel devices based embedded SRAM design. This literature survey has helped to identify various technical gaps in this area of research for embedded SRAM design. Through our work, we have tried to bridge these technical gaps in order to have better novel cells for low power applications in future embedded SRAM. Various research papers, books, monographic and articles have also been studied in the area of nanoscale device and memory circuits design. Articles on implementation of novel devices such as FinFET and Tunnel diode based 6T-SRAM cell for embedded system, which is having low leakage, high SNM and high speed were also incorporated.

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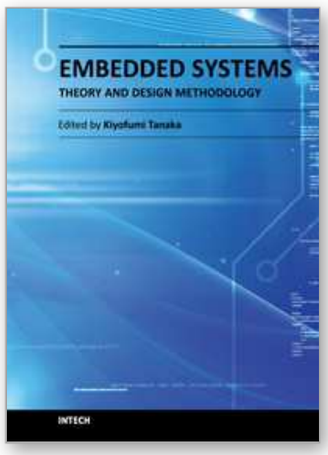

Embedded Systems - Theory and Design Methodology
Edited by Dr. Kiyofumi Tanaka

ISBN 978-953-51-0167-3
Hard cover, 430 pages
Publisher InTech
Published online 02, March, 2012
Published in print edition March, 2012

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