6

Active Matrix Driving and Circuit Simulation

Makoto Watanabe
Sony Mobile Display Corporation
Japan

1. Introduction

This chapter explains the principle of active matrix driving which is the most popular driving method used in current liquid crystal displays (LCDs). It then discusses issues that designers must overcome to avoid the malfunctioning and introduces a liquid crystal model for conducting circuit simulations to optimize the circuit parameters efficiently.

1.1 Equivalent circuit of a pixel in LCDs

The equivalent circuit of a pixel operated by active matrix driving is shown in Fig. 1.
Data lines are connected to a data driver for generating the signal pulses for the picture data. Scan lines are connected to a scan driver for generating the scan pulses which enable the addressing driving. Vsig and Vg are applied to the data lines and scan lines, respectively. The thin film transistor (TFT) has three terminals of MOS transistors, and each terminal gate, drain, and source is connected to a scan line, a data line, and a pixel electrode, respectively. Cgs means the parasitic capacitance between the gate and source terminal in the TFT. Liquid crystal is injected into the gap between the pixel electrode and the counter backplane electrode, and it forms a liquid crystal cell capacitance (Clc). Clc is a variable capacitor that changes value according to the applied voltage between the pixel electrode and a counter backplane electrode. The voltage of the pixel electrode and counter backplane electrode are denoted by Vpix and Vcom, respectively. The storage capacitor is denoted Csc, and it is connected in parallel to Clc. Its function is to hold charges on a pixel electrode while the TFT is switched off.

1.2 Timing chart for each signal pulse

Fig. 2 shows the wave forms applied to each bus line and electrode. The period during which the pixel electrode voltage (Vpix) is higher than the counter electrode voltage (Vcom) is called the “plus frame” (Fig.2 (a)), whereas the period during which Vpix is lower than Vcom is called the “minus frame” (Fig.2 (b)). The plus and minus frames are switched every frame period (Tf).
When the voltage of the gate terminal connecting to the scan line rise to a high level, the resistance between the drain and source terminals becomes very low (Ron). As a result, electrical charges flow into the pixel electrode from the data line till the voltage of the pixel electrode achieves the voltage of the data line during the writing time (Tw). This process is called the “Charge Process”. When the voltage of the scan line starts to drop, the pixel electrode voltage shows a negative shift ΔVfd because of the coupling with the gate terminal

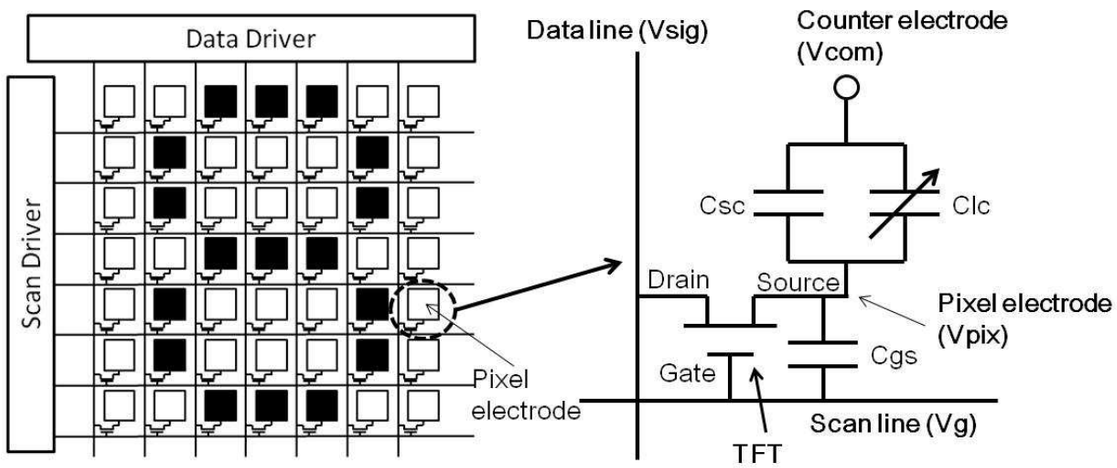


Fig. 1. Equivalent circuit of LCD panel operated with active matrix driving

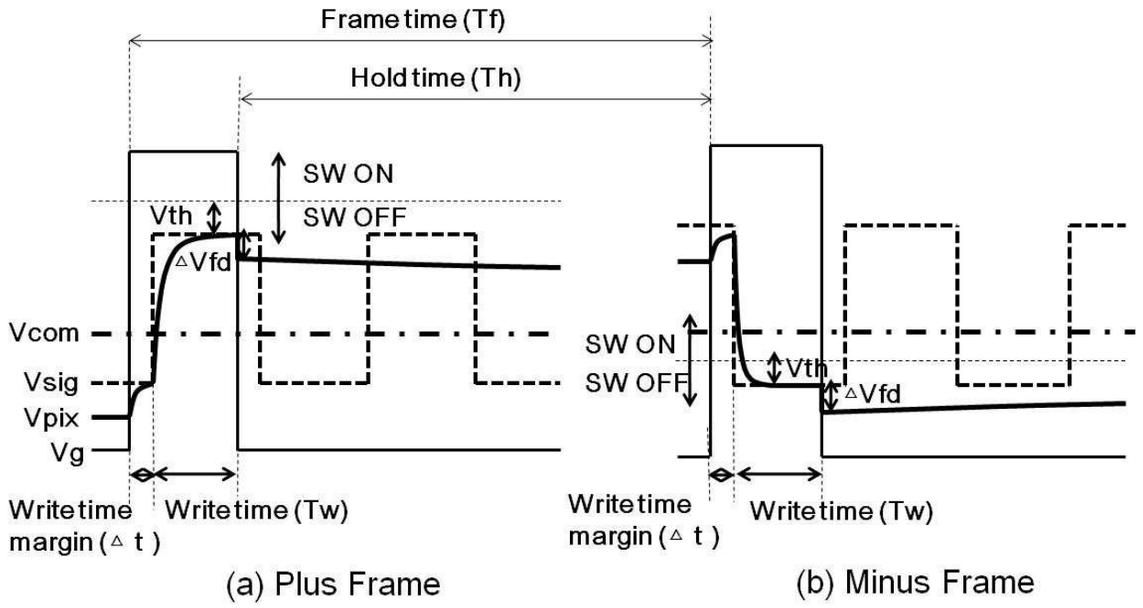


Fig. 2. Timing chart for each signal pulse applied to bus lines and electrodes

via the gate-source capacitance of TFT (Cgs) . This process is called the "Coupling Process". ΔVfd is generally called the feed-through voltage. When the voltage of the scan line becomes low, the resistance between the drain and source terminal becomes very high (Roff) . Ideally charges on the pixel electrode are kept for a hold time (Th) until TFT is switched on at the beginning of the next frame and the pixel electrode voltage keeps constant value. However some amount of current leaks out between the drain and source terminal, and in turn, the charges on the pixel electrode decreases gradually during the hold time (Th). This process is called the "Hold Process". The counter electrode voltage (Vcom) is just set to be the central value between the pixel electrode voltages in the plus and minus frames. By setting Vcom in this manner, we can obtain a constant transmittance that does not depend upon the frame; that is, we can get a flicker-free image since the applied voltages in both frames are the

same. As stated above, there are three stages (a) Charge Process (b) Hold Process (c) Coupling Process. In the following, the operation and key design points of the circuit are explained in detail.

Let us begin by explaining the relationships among the frame time (Tf), hold time (Th) and write time (Tw). The frame time (Tf) is generally taken to be 1/60 (sec) for historical reasons. For an application which cannot be allowed to have a flicker malfunction, however, the frame time is usually set to less than 1/60 (sec). The reason why flicker malfunction occurs will be explained later. In Fig. 2, Δt is called the "write time margin" and it means the offset time between the scan line pulse and the data line pulse. (Tw+Δt)=Tf/N is satisfied if there are N scan lines. For instance, Tw+Δt=7.3μ(sec) in the case of high-definition TVs which have 1125 scan lines with Tf=1/120(sec)≅8.3m(sec). The write time margin (Δt) is usually designed to be around 2μ(sec), although it depends on the expected amount of pulse decay. Consequently, Tw is about 5μ(sec). Strictly speaking, the hold time (Th) should be of the difference between the frame time (Tf) and (Tw+Δt). However, considering that Tw+Δt is on the order of microseconds, the hold time (Th) can be approximated to be the frame time (Tf).

1.2.1 Charge process

When TFT behaves just as an electrical switch, it operates in the linear region of the MOS transistor (Vds<Vgs-Vth). Vds is the voltage between the drain and source terminal, Vgs is the voltage between the gate and source terminal, and Vth is the threshold voltage of the TFT. In the linear region, the current between the drain and source terminal (Ids) can be described as (Sze, 1981)

$$I_{ds} = \mu C_{ox}\left(\frac{W}{L}\right)\left(V_{gs}-V_{th}\right)V_{ds} \tag{1}$$

Here μ is mobility, Cox is the gate insulator capacitance per unit, and L and W are the channel length and width. Therefore, the resistance while the TFT is switched on (Ron) can be expressed as

$$R_{on} = \frac{V_{ds}}{I_{ds}} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{gs}-V_{th}\right)} \tag{2}$$

As shown in Fig. 2, the source voltage of the TFT during a plus frame is higher than that during a minus frame. In other words, Vgs is smaller in a plus frame than in a minus frame. Therefore, according to Eq.(2), Ron becomes higher in a plus frame than in a minus frame. Referring to the equivalent circuit in Fig. 1, the time constant (τ_{on}) for charging to the pixel electrode can be described as

$$\tau_{on} = R_{on}(C_{gs} + C_{lc} + C_{sc}) \tag{3}$$

The charge time (Tw) should be sufficiently long compared with the time constant τ_{on} . In general, the TFT and the voltage applied to bus lines are designed so as to satisfy Tw=3 τ_{on} ~6 τ_{on} .

1.2.2 Hold process

The TFT switching-off resistance (Roff) cannot be expressed with a simple equation like Ron since it has complicated physical mechanisms (Jacunski, 1999). We note that ambient light dramatically decreases Roff. Referring to the equivalent circuit in Fig.1, the time constant (τ_{OFF}) for holding charges on the pixel electrode can be described as

$$\tau_{off} = R_{off}(C_{gs} + C_{lc} + C_{sc}) \tag{4}$$

The time constant τ_{OFF} should be sufficiently long compared with the hold time (Th).

1.2.3 Coupling process

When the voltage for the scan line falls from the high level (Vgon) to the low-level (Vgoff), the pixel electrode voltage shifts by the coupling with the parasitic capacitance (Cgs) between the gate and the source terminal of the TFT. This voltage shift of the pixel electrode is called the feed-through voltage (ΔVfd), and it can be expressed as

$$\Delta V_{fd} = \frac{C_{gs}}{C_{gs} + C_{lc} + C_{sc}}\left(V_{gon} - V_{goff}\right) \tag{5}$$

As discussed earlier, ΔVfd should be a constant independent of any conditions since it uniquely determines the voltage for the counter backplane electrode. This is important in that we can get high-quality flicker free images and get high reliability without residual DC voltages in the liquid crystal cell. ΔVfd, however, depends on various factors, such as Clc, Cgs, and pulse wave distortions.

The first factor is the liquid crystal capacitance (Clc) dependences on the voltage between the pixel and counter electrode. As this voltage increases, the electric field across the liquid crystal cell gets reinforced and the liquid crystal molecule tends to reorient itself along the electric field direction. Consequently, the capacitance of the liquid crystal cell (Clc) increases as shown in Fig. 3. From Eq.(5), ΔVfd changes in accordance with the value of Clc.

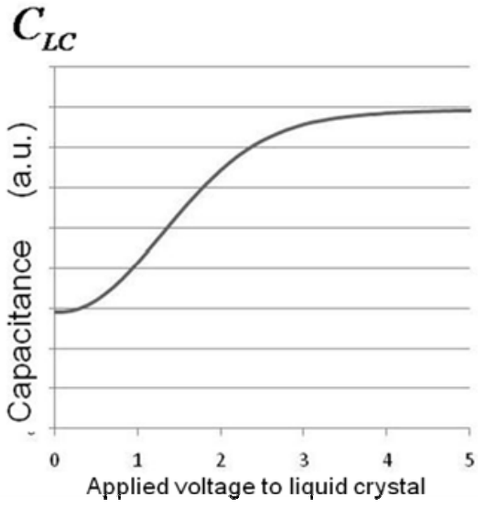


Fig. 3. Clc dependences on the applied voltage to liquid crystal

The second factor is the capacitance between the gate and source terminal (Cgs), which depends on the state (on or off) of the TFT. Fig. 4. shows a cross-sectional view of a general a-Si TFT. While TFT is the on-state (Fig.4 (a)), a conducting channel forms at the bottom of the a-Si layer and a capacitance between the channel and gate electrode (Con) has been generated. Half of Con can be regarded as Cgs in the on-state of TFT. A conducting channel does not form while TFT is the off-state (Fig.4 (b)). Therefore, Cgs during the off-state is the same as the capacitance between the source and gate electrode (Coff). Fig. 5 shows the dependence of Cgs on Vgs.

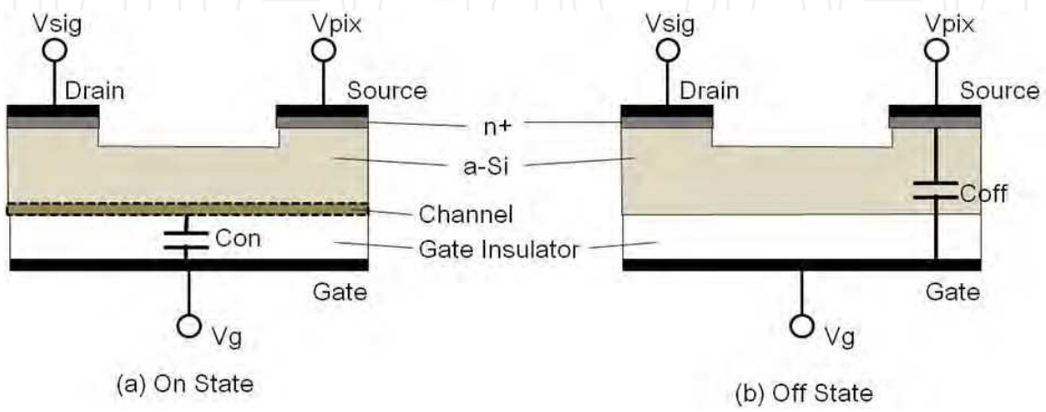


Fig. 4. Gate–source capacitance (On state / Off state)

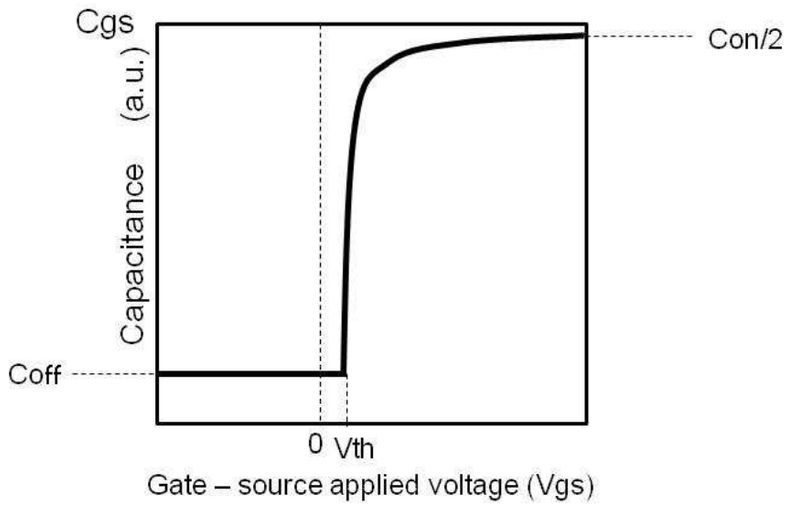


Fig. 5. Dependence of Cgs on the applied voltage

The cut-off voltage which TFT changes form on-state to off-state is Vgs=Vth.
The equation for ΔVfd is updated by taking this behavior into account. In Eq. (6), ΔVfd in a plus frame is smaller than it is in a minus frame since Con/2 is bigger than Coff.

$$\Delta V_{fd} = \frac{(C_{on}/2)(V_{gon} - (V_{PIX} + V_{th}))}{C_{on}/2 + C_{lc} + C_{sc}} + \frac{C_{off}((V_{PIX} + V_{th}) - V_{goff})}{C_{off} + C_{lc} + C_{sc}} \quad (6)$$

The third factor is the influence of a scan pulse distortion on ΔVfd. The scan pulse significantly decays at pixels farther away from the scan driver. Such a decay could cause problems especially in larger displays (Watanabe, 1996). Fig. 6(a) shows the feed through voltage (ΔVfd) under the condition that the scan pulse does not decay. Fig.6 (b) shows the feed through voltage (ΔVfd) under the condition that the scan pulse decays.

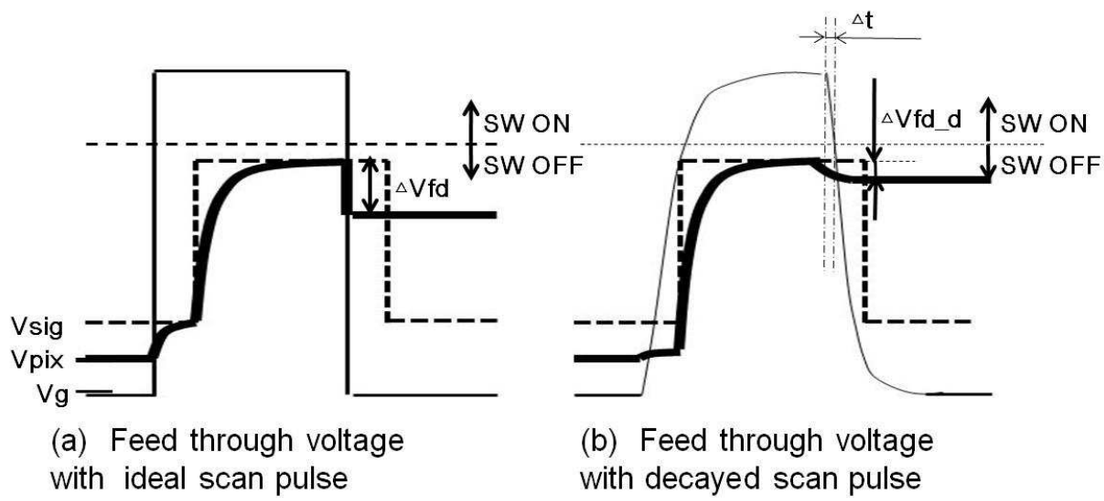


Fig. 6. Influence of a scan pulse distortion on the feed through voltage

When the scan pulse decays, it takes a finite amount of time Δt for the TFT to switch off. During Δt, current Ids(t) continues to flow from a data line to the pixel electrode. Therefore, ΔVfd is modified to Eq. (7).

$$\Delta V_{fd\_d} = \Delta V_{fd} - \frac{1}{C_{gs} + C_{lc} + C_{sc}} \int_0^{\Delta t} I_{ds}(t) dt \tag{7}$$

According to Eq.(7), the effective feed through voltage ΔVfd_d is smaller in a minus frame than in a plus frame because the cut-off voltage becomes lower and Δt becomes longer in a minus frame than in a plus frame.

2. Display quality problems

This section discusses some issues LCD designers must overcome in order to avoid such as shading, cross-talk (vertical / horizontal), flicker malfunctions, low response time and charge leakage in liquid crystal cells.

Even though active matrix driving is a dramatic improvement upon passive matrix driving (Pochi, 1999), the above malfunctions remains in the specific displayed patterns, so-called "killer pattern".

Here we explain what these modes of malfunction are, why they appear, and how to suppress them. This information would be very useful for designers not only in optimizing the design parameters but also in analyzing problems they may encounter. These problems tend to be apparent especially in large and high-resolution LCDs. In the example illustrated in the following explanation, we assume that the treated LCDs are of the dot inversion type

which same pixel polarities are aligned in a checker pattern (Fig.7 (a)) and normally white mode which has the maximum transmittance with no applied voltage (Fig.7 (b)). It will, however, be very easy for readers to apply them to other types of active matrix LCDs.

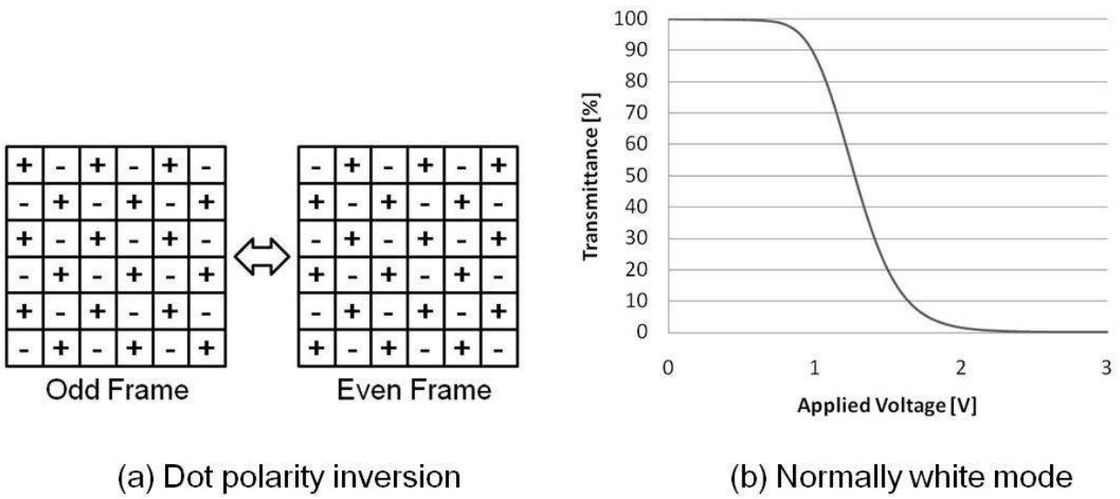


Fig. 7. Driving method assumed in the example

2.1 Shading

When a checker pattern of gray and black is displayed in background, as shown in Fig.8 (a), we see an unexpected gradational change vertically (Fig.8 (b)).

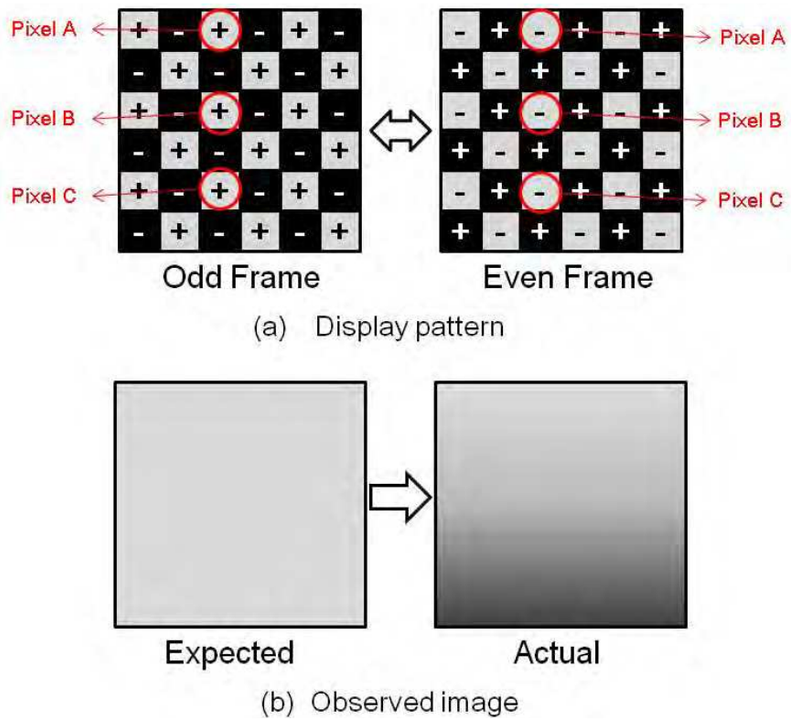


Fig. 8. Shading

The mechanism causing this phenomenon arises from the parasitic capacitance Cdp between the data line, or adjacent data line, and the pixel electrode (see Fig. 9). Here, we shall discuss the voltage modulation of a pixel electrode by the data line voltage (Vsig) and adjacent data line voltage (Vsiga) via the parasitic capacitance Cdp.

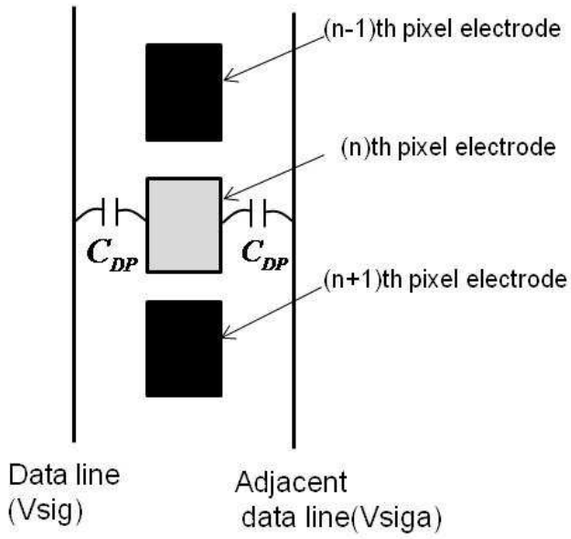


Fig. 9. Circuit model for the shading phenomenon

Fig.10 (a) shows the fluctuation in the data line voltage and Fig. 10 (b) shows the voltages of pixel electrodes located at A, B and C in Fig.8. At the moment when the frame changes from odd(even) to even(odd), the symmetry between the fluctuation in a data line and that of the adjacent data line is offset by the value of ΔVsig. Consequently, the voltage of the pixel electrode is modulated via Cdp. The modulated voltage of a pixel electrode δV can be expressed as

$$\delta V = \frac{2C_{dp}}{C_{tot}} \Delta V_{sig} \tag{8}$$

Here Ctot means the total of the capacitances connected to the pixel electrode. The voltages of the pixels in the upper area of display (such as Pixel A), is updated immediately after modulation at the moment of a frame switching. In contrast, pixels in the lower area of display (such as Pixel C) remain influenced by the modulation remains for a long time up to one frame. Therefore, the average voltage across a liquid crystal cell is higher in Pixel C than in Pixels A and B and a lower transmittance is obtained in the case of the normally white mode of LCDs. To reduce the shading level, designers should try to decrease the parasitic capacitance Cdp or to increase Ctot , for example, by using larger Csc in the pixel design process.

2.2 Vertical crosstalk

There is a variety of modes for a vertical crosstalk (Watanabe, 1997). Here we will describe the coupling mode between a pixel electrode and a data line: this sort of crosstalk will be a critical issue when very high-resolution LCDs become available.

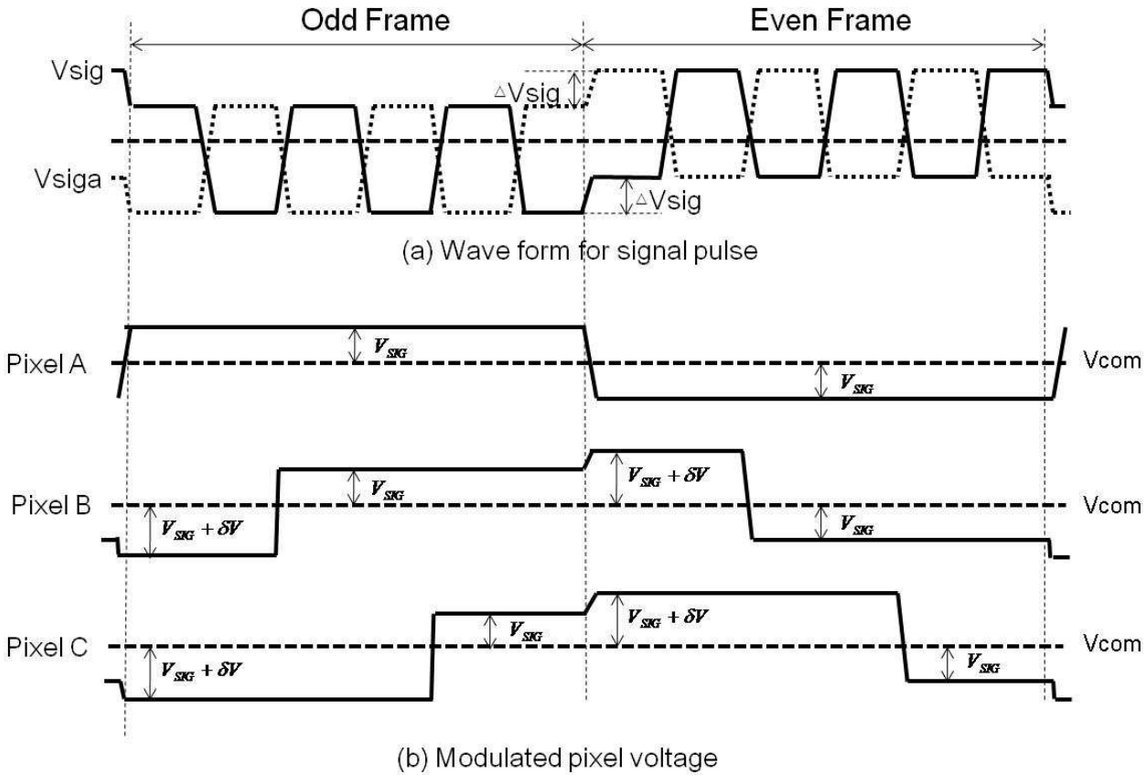


Fig. 10. Pixel voltage modulation by data lines via parasitic capacitances

When a white window is displayed in the middle of the display area on a background composes of a gray tone and black checker pattern as shown in Fig.11 (a), we see an unexpected brightness in the area above and below the window (Fig.11 (b)). The area above the window becomes darker and the area below the window becomes lighter than the tone of the background.

To explain the mechanism causing such vertical crosstalk, we will assume that the shading phenomenon discussed earlier can be ignored. However, readers should be aware that shading and vertical crosstalk can coexist on the same screen. The circuit model to explain vertical crosstalk is the same as that for the shading (Fig.9).

Fig. 12 (a) shows the voltage fluctuation in the data line and the pixel electrode voltage at point A in Fig. 11. Fig. 12 (b) shows the voltage fluctuation in the data line and the pixel electrode at points B and C in Fig. 11. Note that there is a white window below B and above C. In a pixel at B and C, the symmetrical relationship between the fluctuation of the data line and that of the adjacent data line disappears, when the period for drawing the widow starts or ends. Consequently, the pixel electrode voltage is modulated via the parasitic capacitance Cdp. The modulated voltage δV can be expressed by using the same equation as in the case of shading (Eq. (8)).

The brightness difference between pixels B and C can be explained as follows. The voltage of pixel B is affected by drawing the window after the charge process is completed in this frame. Meanwhile the voltage of the pixel C is affected before the charge process is completed in this frame. Therefore the voltage across the liquid crystal cell increases by δV in the pixel B and decreases by δV in the pixel C.

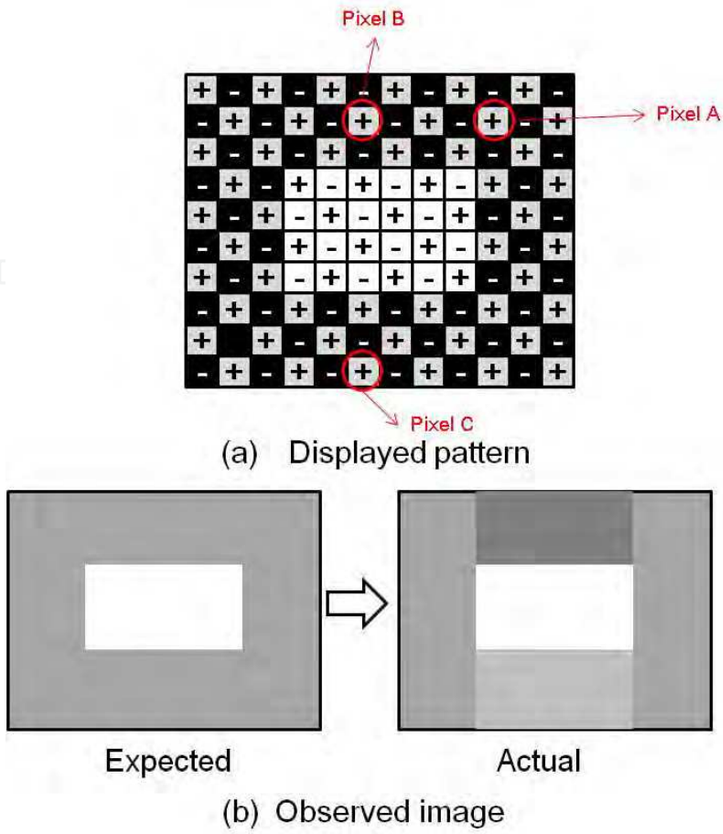


Fig. 11. Vertical crosstalk

To reduce vertical crosstalk, as is done in shading, designers should try to decrease the parasitic capacitance Cdp or increase Ctot, for example, by using a larger Csc in a pixel design process.

2.3 Horizontal crosstalk

When a white window is displayed in the middle of a display area with a background consisting of a striped pattern with gray tones and black as shown in Fig. 13(a), we see the brightness difference in the left and the right areas of the window compared with other area (Fig.13 (b)).

Here we should consider that the tones in the right and left area of the window are rather closed to the expected value compared with the tone in the other area.

Now let us explain the mechanism causing the horizontal crosstalk. Several models of the horizontal crosstalk have been proposed (Kimura, 1994). One of the circuit models is shown in Fig.14. The DC voltage Vcom is provided to a backplane counter electrode at the edge of the display area, which means there are no supply points for Vcom in the display area. Each node of this resistance network in the counter electrode is unintentionally connected to the data line via the parasitic capacitance Cd-com. The voltage of the counter electrode is thus modulated by the fluctuation of the data line voltage (Vsig).

Fig. 15 (a) shows the fluctuation in the voltage of all data lines in Fig. 13. The numbers on the left of the waves correspond to those assigned to the data lines in Fig. 13. The combination of the voltage fluctuations for all data lines modulates the counter electrode

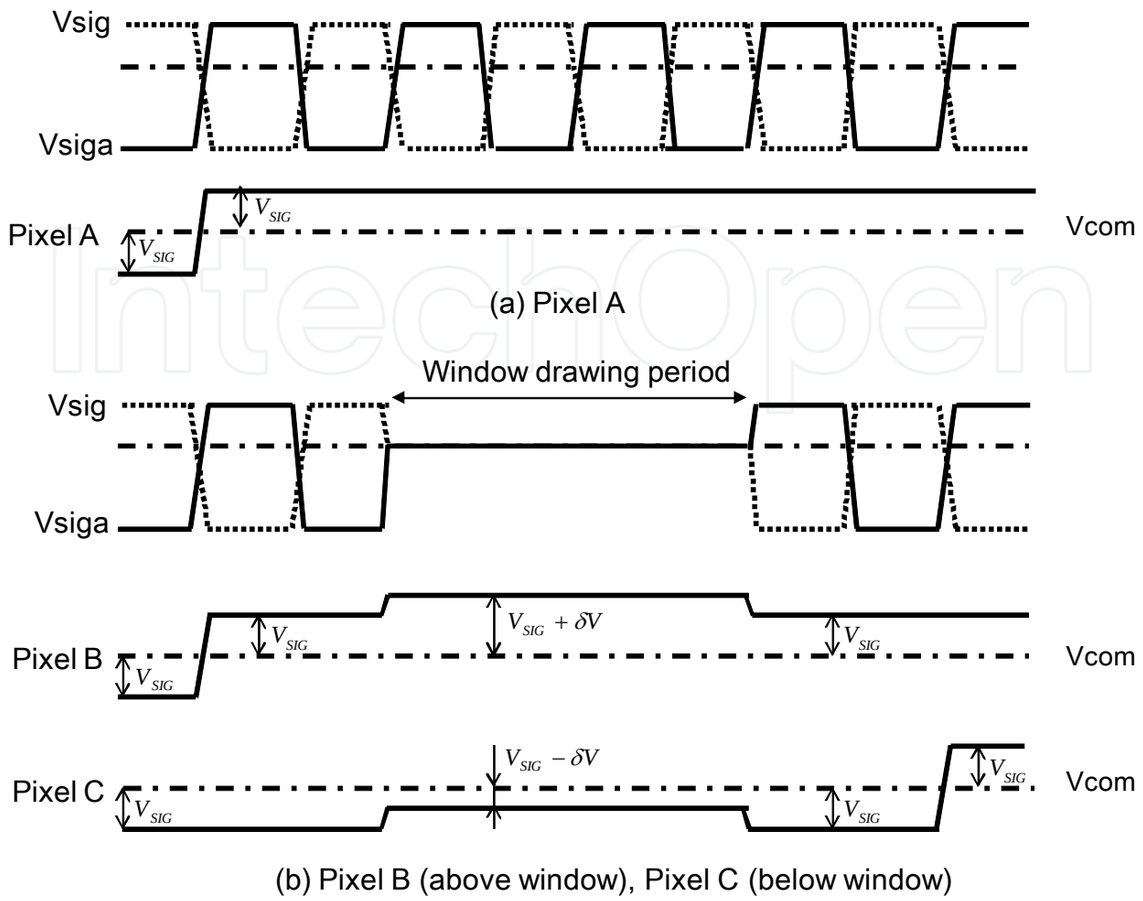


Fig. 12. Pixel voltage modulation by data lines via parasitic capacitances

voltage, as shown in Fig.15 (b). We can see the level of the modulation is lower in the period for drawing the window than in the other periods. ΔVcom and τ_{com} in Fig. 15(b) can be approximately expressed as

$$\Delta V_{com} = \frac{1}{C_{comtot}} \sum_i C_{d(i)-com} \Delta V_{sig(i)} \tag{9}$$

$$\tau_{com} = R_{com} C_{comtot} \tag{10}$$

Here Rcom means the total resistance of the counter electrode, and Ccomtot means the total capacitance connected to the counter electrode.

Referring to Fig. 16, if the wave for the counter electrode has not been restored to the DC level (Vcom) during the write time (Tw), an unexpected voltage will be applied to a liquid crystal cell Vlc' (>Vlc). The situation in pixel A is similar to Fig.16 (a) since the counter electrode voltage is not so modulated during pixel A's write time. Meanwhile the situation in a pixel B is similar to Fig.16 (b) since the counter electrode voltage is too modulated during pixel B's write time. As a result, we can see horizontal crosstalk since the effective voltage across the liquid crystal cell is bigger in pixel B than in pixel A. The best way to suppress the horizontal crosstalk is to decrease the counter electrode resistance. It is, however, difficult since optical properties such as transparency are often sacrificed.

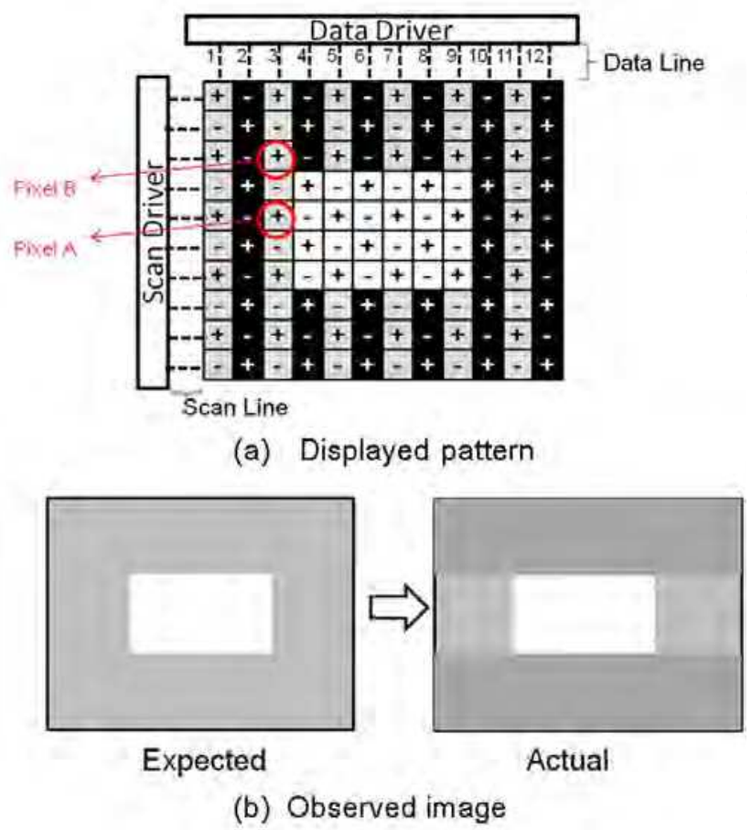


Fig. 13. Horizontal crosstalk

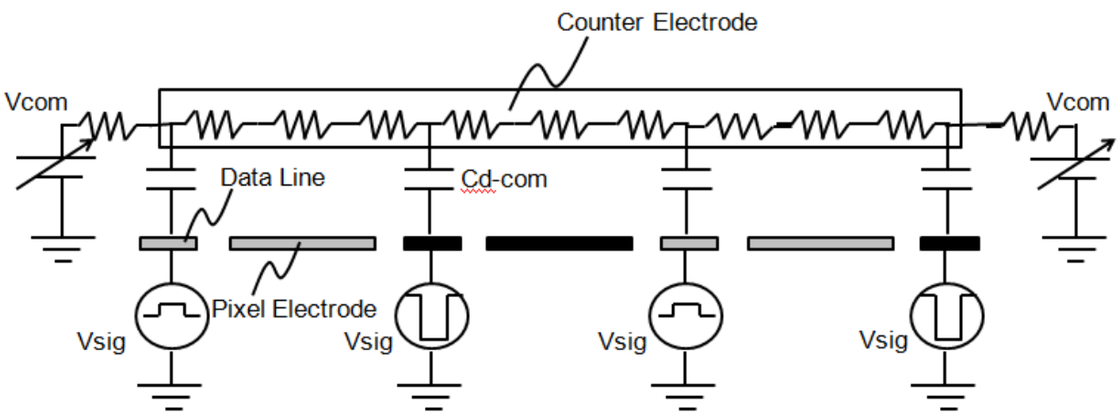


Fig. 14. Circuit model for horizontal crosstalk

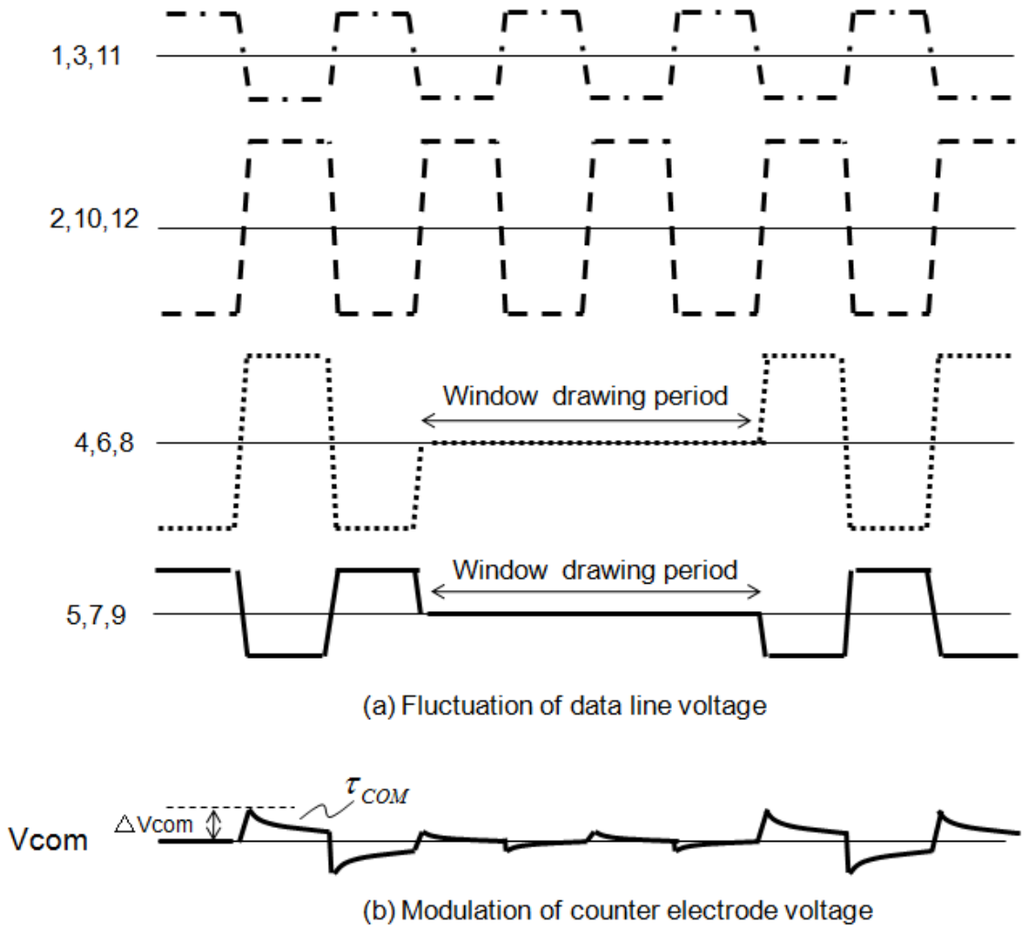


Fig. 15. Counter electrode voltage modulation by data lines via parasitic capacitances

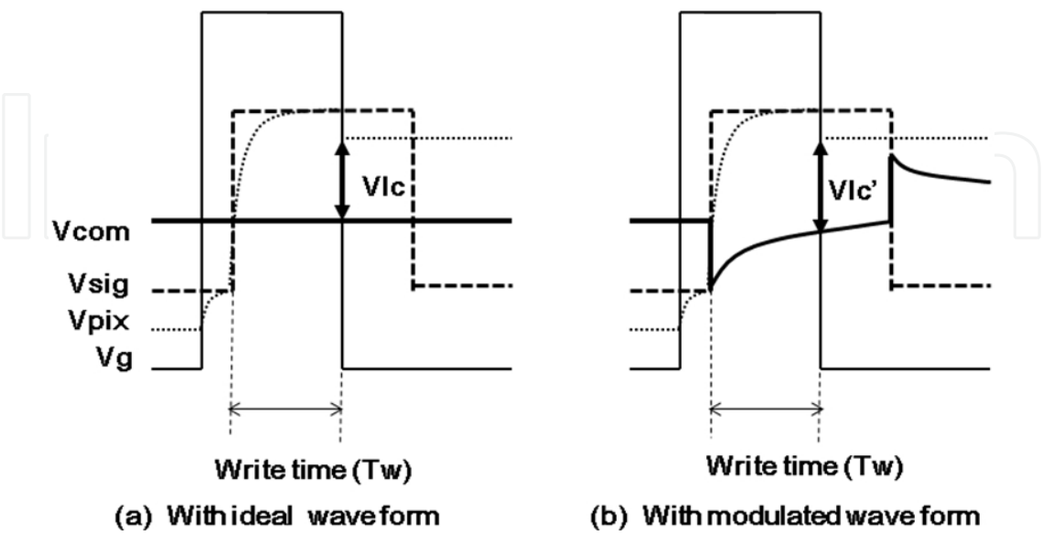


Fig. 16. Change in effective voltages across a liquid crystal cell resulting from counter electrode voltage modulation.

2.4 Flicker

When a gray tone and black checker pattern is displayed in the background as shown in Fig. 17 (a), we sometimes can see the flicker caused by the brightness differences between odd frames and even frames (Fig17 (b)). Note that all the gray tone dots with gray tone have the same polarity during one frame.

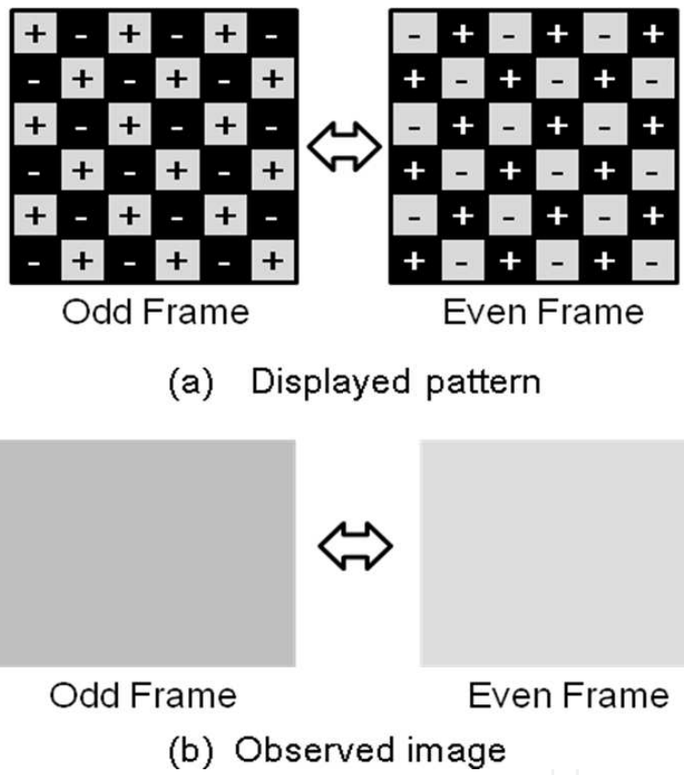


Fig. 17. Flicker

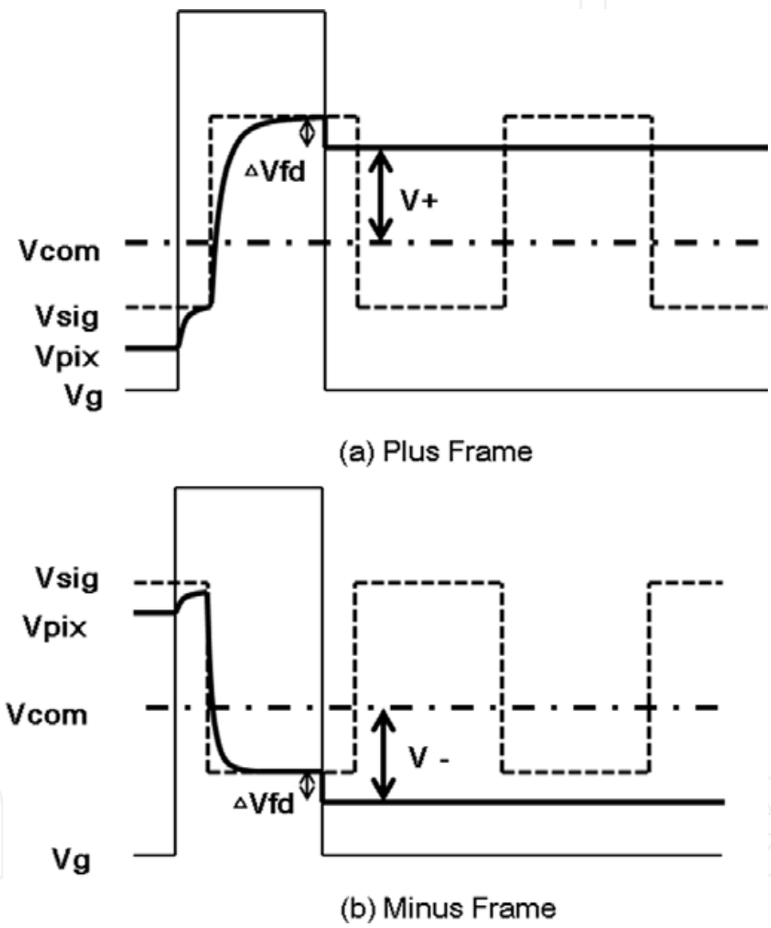


Fig. 18. Adjustment of the counter electrode voltage (Vcom) to suppress flicker (V+ = V-)

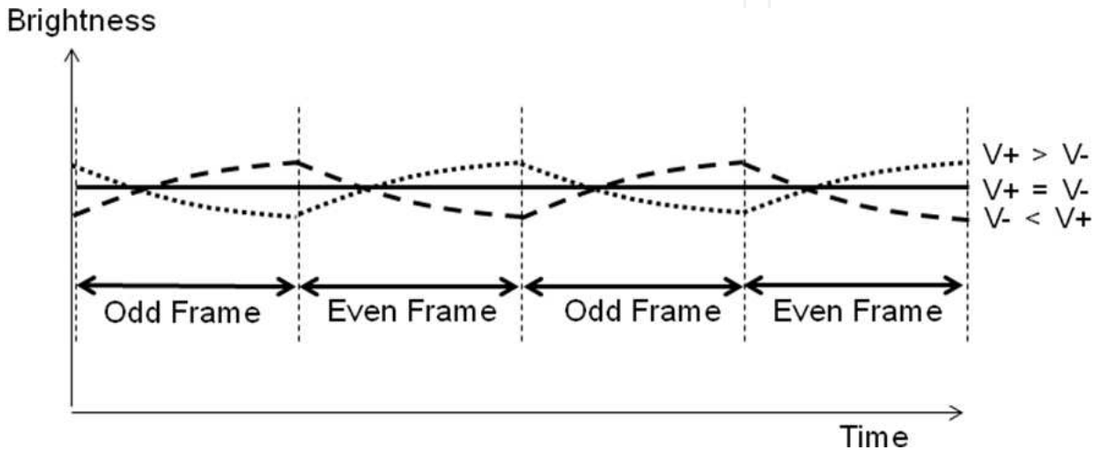


Fig. 19. Brightness fluctuation due to mis-adjustment of the counter electrode voltage(Vcom)

Ideally, the counter electrode voltage (Vcom) should be set so that the voltage between the pixel electrode and the counter electrode $|V_{pix} - V_{com}|$ is the same from one frame to the next (V+=V- in Fig.18). In so doing, we cannot see any flicker since the voltage across a liquid crystal cell stays constant value. However, as discussed earlier, it is too difficult to adjust Vcom such that V+=V- under any condition since the feed-through voltage ΔVfd depends on several factors: variation of Clc, Cgs, pulse distortion, and so on. If the voltage in each frame is not same (V+≠V-), a brightness fluctuation can be seen, as shown in Fig. 19. It is often said that the human eyes cannot perceive flicker of more than 50Hz. Therefore, making a frame rate much higher than 100Hz is one of the effective means to suppress flicker.

2.5 Low response time

If the response time of LCDs is not sufficiently short, the outline of the moving object on the screen blurs, as shown in Fig. 20. Although the properties of the liquid crystal material and cell structures are the dominant factors determining the response time （Wittek, 2008）, the influence of the circuit parameters is not negligible.

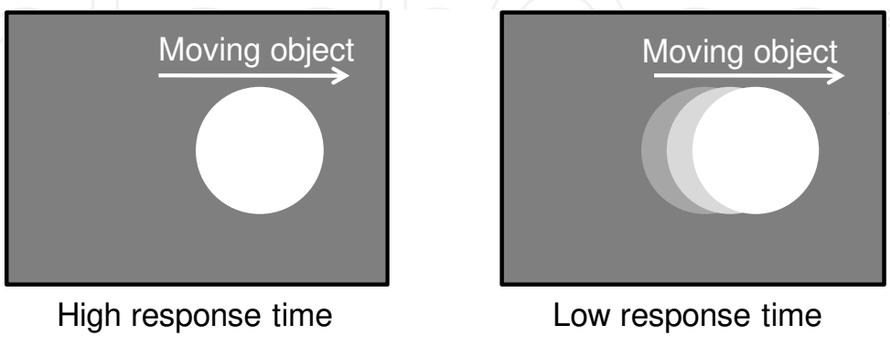


Fig. 20. Influence of response time on displayed image

Fig. 21 shows the effect of a storage capacitor (Csc) reducing the response time of LCDs.
If Csc is not sufficiently large (solid line), the response time is much longer than the case of the ideal operation (dashed line). In the worst case, the transmittance cannot achieve the expected level even in the saturated state.

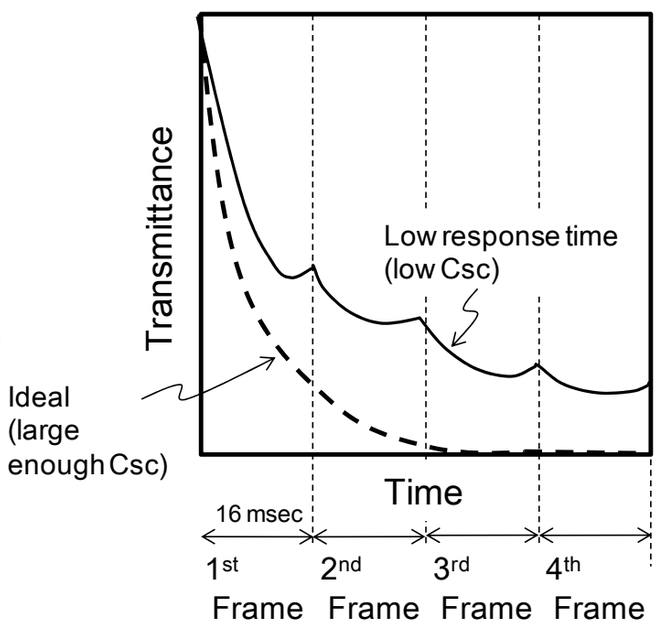


Fig. 21. Dependence of the response time on storage capacitance (Csc)

Now let us explain the mechanism of the low response time, as stated above using Fig. 22. In order to display the black pattern, V0 is applied to the liquid crystal capacitor and the storage capacitor (Csc). Here we should note that the liquid crystal capacitance (Clc0) is smaller just after the period of the charging process explained in section 1.2.1 because a white pattern was displayed in the previous frame and a finite amount of time is necessary to rotate the liquid crystal. The total accumulated charge (q0) on Csc and Clc0 can be described as

$$q_0 = (C_{SC} + C_{LC0})V_0 \tag{11}$$

After that, during the hold process, the liquid crystal tries to align itself parallel to the electric field and the liquid crystal capacitance becomes larger (Clc1), as shown in Fig. 3. Because the total charge on the electrodes is constant (q0), the applied voltage between the electrodes (V1) can be described as

$$V_1 = \frac{q_0}{C_{SC} + C_{LC1}} V_0 = \frac{C_{SC} + C_{LC0}}{C_{SC} + C_{LC1}} V_0 = \frac{1 + (C_{LC0} / C_{SC})}{1 + (C_{LC1} / C_{SC})} V_0 \tag{12}$$

In Eq. (12), we can see that V1 is smaller (larger) than V0 when Clc1 is larger (smaller) than Clc0. This means that the voltage applied to the liquid crystal cell drops (rises) until the pixel electrode is recharged in the next frame when the liquid crystal capacitance for the previous pattern is smaller (larger) than that for the latter pattern. Eq. (12) also shows that Csc should be sufficiently large compared with Clc0 and Clc1 in order to reduce the response time. This problem is especially evident in the ferroelectric liquid crystal, which has a large spontaneous polarization on its own.

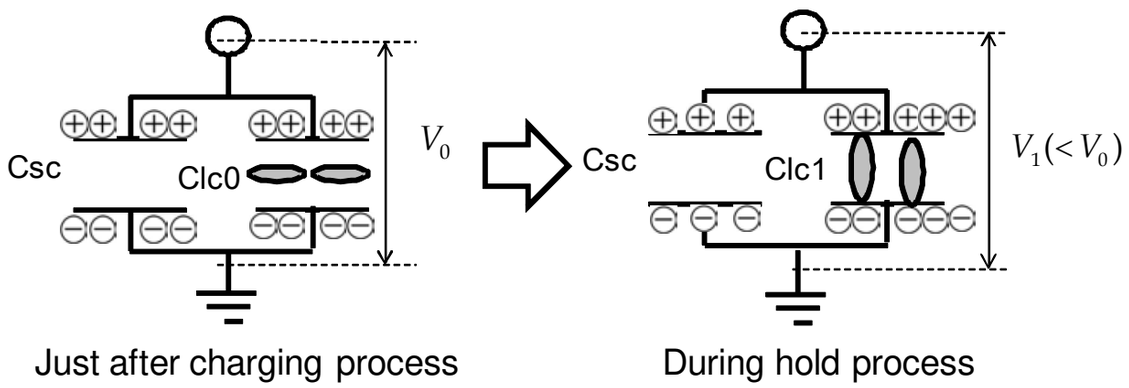


Fig. 22. Applied voltage drop caused by the liquid crystal response

2.6 Charge leakage in liquid crystal cells

An actual liquid crystal cell has a parasitic resistance because it includes many impurity ions. The resistivity of liquid crystal is normally on the order of 10^{10}~10^{13}(Ω • cm).

Therefore, even if the TFT works as an ideal switch, that is, the switching-off resistance (Roff) is infinite, the charge on the electrode cannot be kept during the hold process because of the parasitic resistance in the liquid crystal cell.

Here, we discuss the requirements of the circuit parameters in order to reduce the above influence. Fig. 23(a) shows the equivalent circuit for a pixel during the hold process with the assumption that the TFT is an ideal switch with an infinite resistance. The liquid crystal cell is composed of two electrodes with an area S and with a gap d, as shown in Fig. 23(b). The liquid crystal is injected into the gap between two electrodes. Clc, Rlc and Csc denote liquid crystal capacitance, parasitic resistance, and storage capacitance, respectively. Referring to Fig. 23(b), Rlc and Clc can be described as $R_{LC} = \rho(d/S)$, $C_{LC} = \varepsilon_0\varepsilon_r(S/d)$. Here, ρ and, εr mean the resistivity and, permittivity of the liquid crystal material, and ε0 means the vacuum permittivity.

The decay time constant (τ) for the voltage between two electrodes (Vcell) in Fig. 23(a) can be described as

$$\tau = R_{LC}\left(C_{LC} + C_{SC}\right) = R_{LC}C_{LC}\left(1 + \frac{C_{SC}}{C_{LC}}\right) = \varepsilon_0\varepsilon_r\rho\left(1 + \frac{C_{SC}}{C_{LC}}\right) \tag{13}$$

To keep the charge during the hold process, τ should be sufficiently long compared with the hold time (Th) in Fig. 2.

$$\tau = \varepsilon_0\varepsilon_r\rho\left(1 + \frac{C_{SC}}{C_{LC}}\right) \gg Th \tag{14}$$

Eq. (14) can be transformed into

$$\frac{C_{SC}}{C_{LC}} \gg \frac{Th}{\varepsilon_0\varepsilon_r\rho} - 1 \tag{15}$$

Given Th = 16 (msec), **ε0** = 8.854x10^{12}(F/m), **εr**=10, **ρ**=10^{10}(Ω • cm), we find that Csc/Clc should be designed to be more than 0.2.

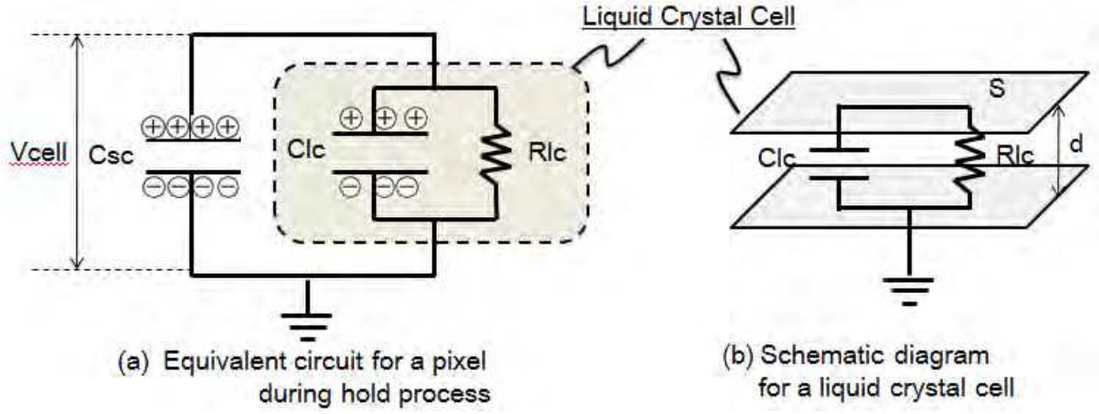


Fig. 23. Charge leakage model with a parasitic resistance in the liquid crystal cell

3. Design optimization by circuit simulation

A circuit simulation is a great tool for efficiently optimizing the design parameters given the complicated trade-off relationship among the electrical characteristics of displays. Although commercial circuit simulators can also be used for some design work, their device models are not detailed enough to have sufficient accuracy for liquid crystal capacitor and TFT since there are some important properties which are not considered in the implemented models into commercial simulator. To solve this problem, we have developed our own device models for a liquid crystal capacitor (Watanabe, 2007) and TFT (Ishihara, 2008) including the photo-leak effect. This section introduces the liquid crystal capacitor model as a representative. Moreover the Appendix provides codes written in VerilogA for implementing our device model into a circuit simulator.

3.1 Liquid crystal capacitor model

To make competitive products, the optical and electrical characteristics of LCDs should simultaneously be optimized to the highest level. Liquid crystal cells behave as a non-liner history-dependent capacitors from the electrical point of view, and as light valves, the transmittance of which can be varied with an applied voltage from the optical point of view. The following presents a macro-model for liquid crystal cells that includes these electrical and optical behaviors. We have enhanced Smet's approach (Smet, 2004) to improve the accuracy.

3.1.1 Modeling of a liquid crystal cell

The average orientation of liquid crystal molecule is assumed to be represented by one-dimensional variable 'x' as shown in Fig.24. In practice, three kinds of torques are in play (See Fig. 24).

1. The elastic torque $F_{elas} = Kx$ (K: constant)
   This torque pulls the molecules back to their resting position x=0 (parallel to the alignment layer). This torque is assumed to follow Hooke's law.
2. The electrical torque $F_{elec} = cE^2$ (c: constant)
   This torque aligns the molecules parallel to the field E. It is proportional to E^2.
3. The viscosity torque $F_{vis} = \gamma \frac{dx}{dt}$ (γ: constant)
   This torque hinders any movement and is proportional to the velocity at which the molecule move.

Since the moment of inertia of a liquid crystal molecule is small, it can be neglected. The equilibrium of torques in Fig. 24 states that:

$$cE^2 = Kx + \gamma \frac{dx}{dt} \tag{16}$$

This is well-known first-order system with time constant $\tau = \gamma / K$ and $x(t) \to \frac{c}{K}\left[\frac{V_{ext}}{d}\right]^2 (t \to \infty)$. Eq. (16) can be solved with the low pass filter circuit shown in Fig. 25. The resistance Rd and the capacitance Cd should be determined so that their product corresponds to the time constant $\tau = \gamma / K$. Note that the magnitude of the electric field E in the cell is described as Vext/d. Here, Vext and d are respectively the applied voltage

between two electrodes and the cell gap in Fig.24. After solving for x(t) from this circuit, the effective voltage Vi at time t is calculated as $V_i = \sqrt{\frac{Kd^2}{c}x(t)}$.

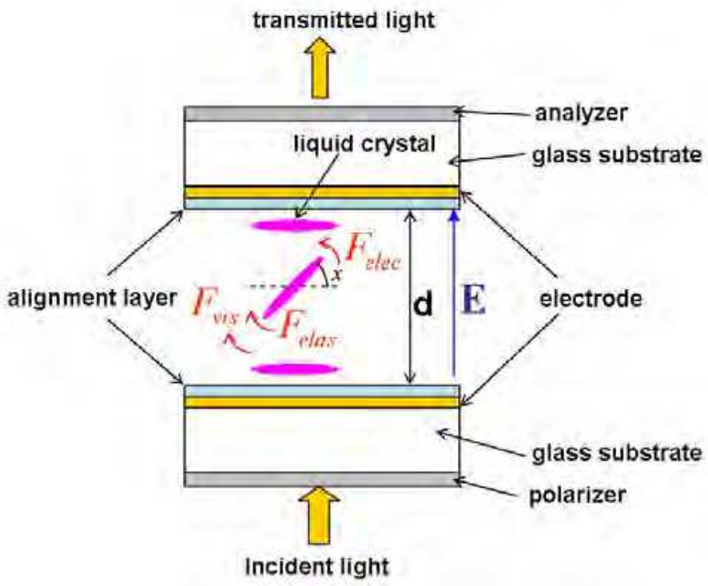


Fig. 24. Schematic diagram of liquid crystal cell

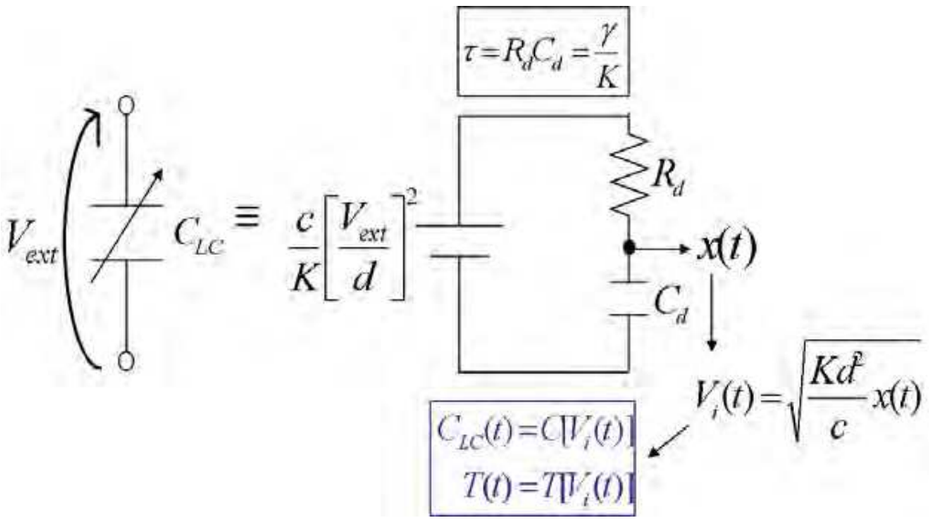


Fig. 25. Macro-model for liquid crystal cell

The static behaviors for the capacitance and transmittance of liquid crystal cells can be expressed empirically with Eq. (17) and Eq. (19) as function of the effective applied voltage Vi.

$$C(V_i) = C_{\perp} + \frac{2}{\pi}\left(C_{\parallel} - C_{\perp}\right) arctan\left[\frac{\alpha + \left(a^2 + \delta^2\right)^{1/2}}{2}\right] \tag{17}$$

$$\alpha = \frac{V_i - V_{tc}}{V_{mc}} \tag{18}$$

$$T(V_i) = T_{min} + (1 - T_{min}) tanh\left[\frac{\beta + \left(\beta^2 + \eta^2\right)^{1/2}}{2}\right] \tag{19}$$

$$\beta = \frac{V_i - V_{to}}{V_{mo}} \tag{20}$$

C∥, C⊥, δ, Vtc, Vmc, in Eq.(17) and Tmin, η, Vto, Vmo in Eq.(19) are treated as model parameters extracted from experimental results.

To improve accuracy, we have modified the form of the time constant (τ) in the equation proposed by Smet by considering the following points.

First, we should improve the accuracy for the external applied voltage dependency. Generally, the response time of liquid crystal depends on the external applied voltage (Vext). We got the following expression for time constant (τ) after further investigating of the relationship between the electric torque(Felec) and the applied voltage(Vext) (Watanabe, 2007).

$$\tau = \frac{1}{a_1 + a_2 V_{ext}^m} \tag{21}$$

Here a_1, a_2 and m are model parameters. Basically, m takes a value around 2.

The second point is to give the parameter to rise and fall process individualy. A rise (fall) process is defined as the case that the orientation angle x of the liquid crystal molecule is increasing (decreasing). The time constant for each process does not generally coincide. To implement this factor into our model, the parameters in Eq. (21) are selected after the voltage for both terminals of Rd are compared:

If

$$\frac{c}{K}\left(\frac{V_{ext}}{d}\right)^2 \geq x(t)$$

Then

$$a_1 = a1\_r, a_2 = a2\_r \quad \text{(for rise process)}$$

Else

$$a_1 = a1\_f, a_2 = a2\_f \quad \text{(for fall process)}$$

This additional routine enables individual control of the rise and fall behaviors. The VerilogA code for the above macro model is in Appendix.

3.1.2 Model evaluation

We verified the macro-model by comparing its results with experimental data. Fig. 26 compares modeled and experimental data for the static behavior. The experimental data is for a twisted-nematic liquid crystal cell with a 3.5μm gap. The model exhibits good agreement with the experimental data in both its transmittance and dielectric constant characteristics.

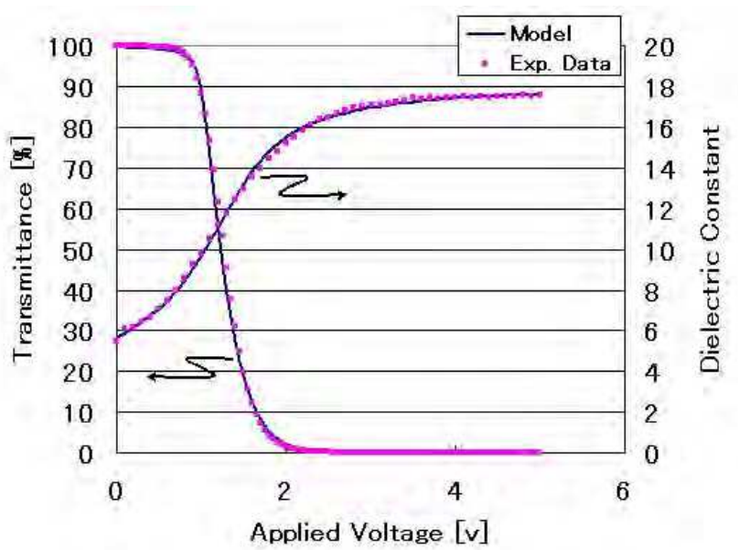


Fig. 26. Comparison of static behaviors of experimental data and model

Fig. 27 compares modelled and experimental data for the dynamic behavior for externally applied voltages. The transient behavior from low voltage to high voltage (rising process) is shown in Fig. 27 (a), and from high voltage to low voltage (falling process) in Fig. 27 (b). The transient behavior of the dielectric constant is not shown here because no measuring procedure has been established for it. We assumed that the dynamic parameters for the transmittance and dielectric constant are the same when this model is used in the actual design for the liquid crystal cell, though this assumption cannot be verified directly.

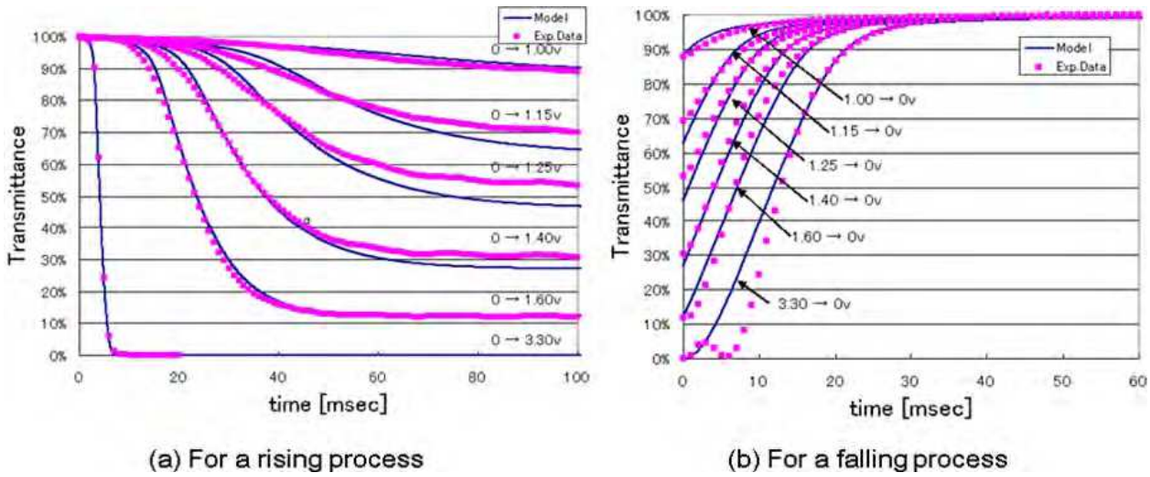


Fig. 27. Comparison of dynamic behaviors of experimental data and modelled

In Fig.27, the model exhibits good agreement with the experimental data except for the following points.

1. The bounce around 5msec in 3.30v → 0v in Fig.27 (b)
   This phenomenon is well known as the back-flow of liquid crystal molecule (Doom, 1975). This shape of the curve could not be expressed in principle since Eq.(19) is monotonous function. A new model supporting this phenomenon should be developed.
2. The disagreement between model and experiment after ample time elapses in Fig. 27(a) and in the initial state in Fig.27 (b)
   The origin of this disagreement is considered to be measurement error, since the modelled transmittances after an ample time has passed in Fig. 27(a) and at the initial time in Fig. 27(b) do not coincide with the static measurements ones in Fig. 26. It is hard to improve the measurement accuracy because the transmittance is very sensitive to the applied voltage around 1v, as can be seen in Fig.26.

4. Conclusion

Thanks to its individual control of each pixel, active matrix driving is definitely superior to passive driving in its capability to display higher quality pictures. Even in an active matrix driving, however, some malfunctions such as shading, crosstalk and flicker become apparent on screen when a specific picture pattern is displayed. In this chapter, we made the mechanism behind such malfunctions and some of the key design parameters. Readers may find the complicated trade-off relationship among key design parameters and a difficulty in optimizing the parameters simultaneously. A circuit simulator would be very useful for designers to optimize the design parameters more efficiently. However, general commercial circuit simulators often do not have enough device models such as liquid crystal cell capacitors, TFTs supporting the ambient light effects, and so on. Therefore, for the sake of accurate circuit simulations, LCD designers must aggressively develop device models and continuously improve them. In this chapter, we described a macro model for a liquid crystal cell capacitor as a representative model for making accurate designs. The current trend of developing larger and higher resolution of LCDs will spur a need for accurate circuit simulation technologies since there will be less margin for each design parameter.

5. Appendix

List 1. VerilogA code for Liquid Crystal Macro Model

```
// Liquid Crystal Cell Macro Model ver1.0
// M.Watanabe
//
`include "discipline.h"
`include "constants.h"
//
`define m_pi        (3.14159265358979323846)
//
module lccap(a,b);
inout a,b;
electrical a,b;
//
// Internal nodes
electrical vc, vt;
//
// Parameters for Static behavior
//
// For Capacitance
parameter real  cv = 8.82;
parameter real  cp = 27.1;
parameter real vtc = 0.88;
parameter real vmc = 0.88;
parameter real delta = 0.1;
//
// For Transmittance
parameter real tmin= 8.7e-4;
parameter real vto = 1.1;
parameter real vmo = 0.54;
parameter real eta = 0.24;
//
// Parameters for Dynamic behavior
//
// For Capacitance
parameter real  a1c_r = 0.014;
parameter real  a2c_r = 0.05;
parameter real  a1c_f = 0.014;
parameter real  a2c_f = 0.05;
parameter real  cdc   = 1e-3;
parameter real  mc_r  = 2.4;
parameter real  mc_f  = 2.05;
//
// For Transmittance
parameter real  a1t_r = 0.020;
parameter real  a2t_r = 0.02;
parameter real  a1t_f = 0.0205;
parameter real  a2t_f = 0.025;
parameter real  cdt   = 1e-3;
parameter real  mt_r  = 2.4;
parameter real  mt_f  = 2.05;
//
// Geometrical Parameters
//
parameter real area = 1;
parameter real vini = 0;
parameter real scale =1;
//
real a1c, a2c, a1t, a2t, cap, rdc, rdt;
real trans,alpha,beta;
real vi_c, vrms_c, vv, qi_c, vin, vi_t, vrms_t,  qi_t, mc,  mt ;
real qlc, cdiff;
//
```

```
analog
 begin
@(initial_step)
begin
cdiff = (2/`m_pi) * (cp - cv);
qlc = 0;
vi_c = vini * vini;
vi_t = vini * vini;
end

//
vin = V(a,b);
vv  = vin * vin;
//
// For Capacitance
//
if (vin >= vi_c)
  begin //rising
    a1c = a1c_r;
    a2c = a2c_r;
    mc  = mc_r;
  end
 else
  begin //falling
    a1c = a1c_f;
    a2c = a2c_f;
    mc  = mc_f;
  end

rdc = 1/(a1c + a2c * pow(vi_c, mc) );
I(vc) <+ ddt(cdc * V(vc));
I(vc) <+ (V(vc)-vv)/rdc;

vi_c = V(vc);
vrms_c = sqrt(vi_c + 0.01);
alpha = (vrms_c - vtc)/vmc;
cap = scale * area * (cv + cdiff * atan((alpha+sqrt(alpha * alpha + delta * delta ))/2));
//
// For Transmittance
//
if (vin >= vi_t)
  begin //rising
    a1t = a1t_r;
    a2t = a2t_r;
    mt  = mt_r;
  end
 else
  begin //falling
    a1t = a1t_f;
    a2t = a2t_f;
    mt  = mt_f;
  end

rdt = 1/(a1t + a2t * pow(vi_t, mt) );
I(vt) <+ ddt(cdt * V(vt));
I(vt) <+ (V(vt)-vv)/rdt;
vi_t = V(vt);
vrms_t = sqrt(vi_t + 0.01);
beta  = (vrms_t - vto)/vmo;

trans = 100*(1-(1-tmin)*tanh((beta+sqrt(beta * beta + eta * eta))/2));
//
// Description for device behavior
//
qlc = cap * vin;
I(a,b) <+ ddt(qlc);

end
endmodule
```

6. References

Doom, Z., Dynamic behavior of twisted nematic liquid-crystal layers in switched field, Journal of Applied Physics, Vol.46, No.9, September 1975, pp.3783-3745

Ishihara, K.(2008), Implementation of optical response of thin film transistor, *Proceedings of IEEE BMAS 2008 Conference*, pp.39-44, 2008.

Jacunski, M. D. (1999). A Short-Channel DC SPICE Model for Polysilicon Thin-Film Transistors Including Temperature Effects, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, Vol.46, No.6, June 1999, pp.1146-1158, ISSN 0018-9383

Kimura, M. (1994). Simulation Techniques for Horizontal Crosstalk in TFT-LCDs, *Proceedings of AM-LCD'94*, pp.228-231, ISBN 4-930813-62-10, Shinjuku, Tokyo, Japan, November 30 – December 1, 1994

Pochi, Y. (1999). *Optics of Liquid Crystal Displays*, pp.248-252, John Wiley & Sons, ISBN 0-471-18201-X, the United States of America

Smet, H.D., Electrical model of a liquid crystal pixel with dynamic, voltage history-dependent capacitance value, *Liquid Crystal*, Vol.31, No.5, May 2004, pp.705-711

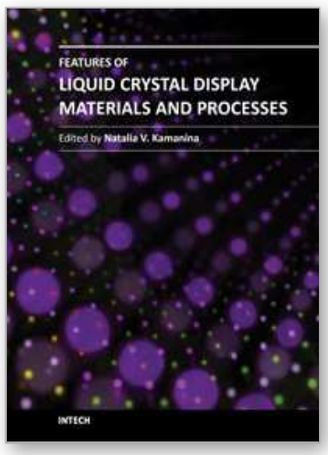
Sze, S. M. (1981). *Physics of Semiconductor Devices Second Edition*, pp.440, John Wiley & Sons, ISBN 0-471-05661-8, the United States of America

Watanabe, M.(1996), Development of a 20.1 Diagonal Super Fine TFT LCD, *Proceedings of Euro Display'96*, pp.587-590, 1996.

Watanabe, M.(1997), Novel pixel structre for IPS TFT-LCD with color-shift free,*Proceedings of International Display Research Conference'97*, pp.L-9, 1997.

Watanabe, M.(2007), Macro modeling of liquid crystal cell with VerilogA, *Proceedings of IEEE BMAS 2007 Conference*, pp.132-137, 2007.

Wittek,M. (2008), Advanced LC Materials for Ultra-Fast Switching for Active-Matrix-Device (AMD) Applications, Proceedings of IDRC '08 Conference, pp.253-255, 2008



Features of Liquid Crystal Display Materials and Processes
Edited by Dr. Natalia Kamanina

ISBN 978-953-307-899-1
Hard cover, 210 pages
Publisher InTech
Published online 30, November, 2011
Published in print edition November, 2011

Following the targeted word direction of Opto- and Nanoelectronics, the field of science and technology related to the development of new display technology and organic materials based on liquid crystals ones is meeting the task of replacing volume inorganic electro-optical matrices and devices. An important way in this direction is the study of promising photorefractive materials, conducting coatings, alignment layers, as well as electric schemes that allow the control of liquid crystal mesophase with good advantage. This book includes advanced and revised contributions and covers theoretical modeling for optoelectronics and nonlinear optics, as well as includes experimental methods, new schemes, new approach and explanation which extends the display technology for laser, semiconductor device technology, medicine, biotechnology, etc. The advanced idea, approach, and information described here will be fruitful for the readers to find a sustainable solution in a fundamental study and in the industry.

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen