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An Optimization of 16-Point Discrete Cosine Transform Implemented into a FPGA as a Design for a Spectral First Level Surface Detector Trigger in Extensive Air Shower Experiments

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1. Introduction

The Pierre Auger Observatory is a ground based detector located in Malargue (Argentina) (Auger South) at 1400 m above the sea level and dedicated to the detection of ultra high-energy cosmic rays with energies above 10^{18} eV with unprecedented statistical and systematic accuracy. The main goal of cosmic rays investigation in this energy range is to determine the origin and nature of particles produced at these enormous energies as well as their energy spectrum. These cosmic particles carry information complementary to neutrinos and photons and even gravitational waves. They also provide an extremely energetic stream for the study of particle interactions at energies orders of magnitude above energies reached at terrestrial accelerators (Abraham J. et al., 2004).

The flux of cosmic rays above 10^{19} eV is extraordinarily low: on the order of one event per square-kilometer per century. Only detectors of exceptional size, thousands of square-kilometers, may acquire a significant number of events. The nature of the primary particles must be inferred from properties of the associated extensive air showers (EAS).

The Pierre Auger Observatory consists of a surface detectors (SD) array spread over 3000 km² for measuring the charged particles of EAS and their lateral density profile of muon and electromagnetic components in the shower front at ground, and of 24 wide-angle Schmidt telescopes installed at 4 locations at the boundary of the ground array measuring the fluorescence light associated with the evolution of air showers: the growth and subsequent deterioration during a development. Such a "hybrid" measurements allow cross-calibrations between different experimental techniques, controlling and reducing the systematic uncertainties.

Very inclined showers are different from the ordinary vertical ones. At large zenith angles the slant atmospheric depth to ground level is enough to absorb the part of the shower that follows from the standard cascading interactions, both of electromagnetic and hadronic type. Only penetrating particles such as muons and neutrinos can traverse the atmosphere at large zenith angles to reach the ground or to induce secondary showers deep in the atmosphere and close to an air shower detector.

The ability to analyze inclined showers with zenith angles larger than 60° induced by neutrinos or photons essentially increases the acceptance of the surface array and opens a part of the sky that was previously inaccessible to the detector. These showers provide a new tool for ultra high energy cosmic rays interpretation because they are probing muons of significantly higher energies than vertical showers. Spectral triggers offering a pattern recognition in a frequency domain may improve a standard detection technique based on the signal coincidences from many PMT channels above some thresholds in the time domain. The "old" muon shower fronts have only a small longitudinal extension, which is leading to short detector signals also in time. To identify these showers at the presence of "young" showers with a large electromagnetic component one may need a very good spectral sensitivity to the fast muon component in the trigger.

The main advantage of the spectral trigger is the scaling feature. The set of the DCT coefficients depends only on the shape of signals, not on their amplitudes. Triggers sensitive on the shape of FADC traces may detect events with expected characteristics i.e. the fast attenuated, very short peaks related to the muonic, flat fronts coming from very inclined showers. Independence of the amplitude is especially promising for the Auger North, where due to a single PMT in the surface detectors the coincidence technique cannot be used. In order to keep reasonable trigger rate for the 1st level trigger (ca. 100 Hz), the threshold for the 1st trigger should be much higher than for example in the Pierre Auger Observatory, where 3-fold coincidences attenuated a noise.

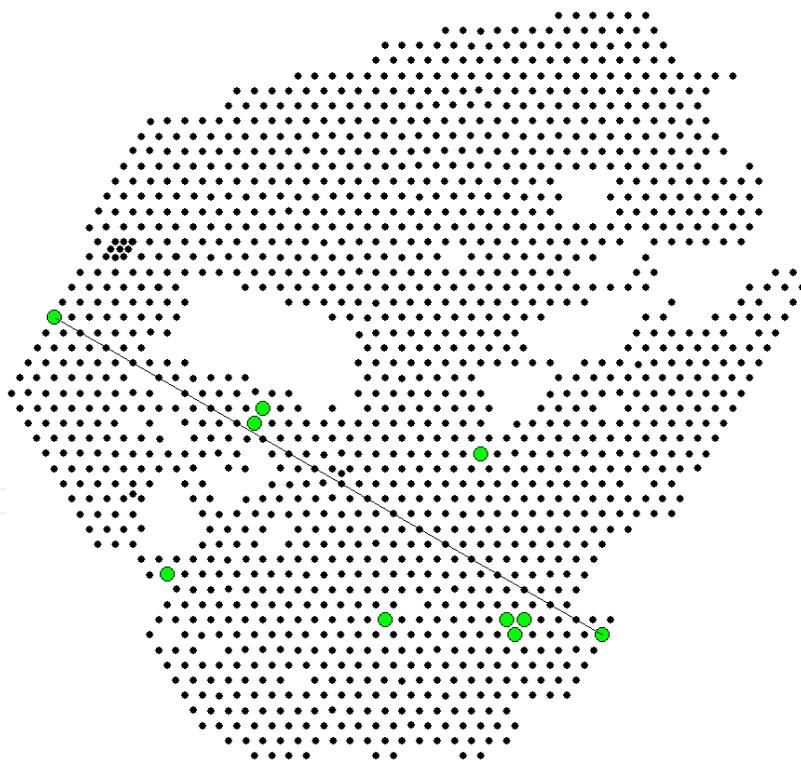


Fig. 1. Position of triggered surface detectors on the Auger array for the very inclined shower ($\theta = 83.5^\circ$) nr 1155555. Muons triggered only few surface detectors, although they crossed several hundred detectors. A distance between opposite detectors is 54 km.

2. Triggers

Two different triggers are currently implemented at the 1st level. The first is a single-bin trigger generated as 3-fold coincidence of the 3 PMTs at a threshold equivalent to 1.75 vertical emitted muons. The estimated current for a Vertical Equivalent Muon (I_{VEM}) is the reference unit for the calibration of FADC traces signals and corresponds to ca. 50 ADC-counts. This trigger has a rate of about 100 Hz. It is used mainly to detect fast signals, which correspond also to the muonic component generated by horizontal showers. The single bin trigger is generated when the input signal is above the fixed thresholds calculated in the micro-controller during the calibration process. It is the simplest trigger useful for high-level signals. The second trigger is the Time over Threshold (ToT) trigger that requires at least 13 time bins above a threshold of $0.2 I_{VEM}$. A pre-trigger ("fired" time bin) is generated if in a sliding time window of 120×25 ns length a coincidence of any two channels appears. This trigger has a relatively low rate of about 1.6 Hz, which is the expected rate for two muons crossing the Auger surface detector. It is designed mainly for selecting small but spread-in-time signals, typical for high energy distant EAS or for low energy showers, while ignoring the single muon background (Abraham J. et al., 2010).

Cherenkov light generated by very inclined showers crossing the Auger surface detector can reach the PMT directly without reflections on Tyvec liners. Especially for "old" showers the muonic front is very flat. This together corresponds to very short direct light pulse falling on the PMT and in consequence very short rise time of the PMT response. For vertical or weakly inclined showers, where the geometry does not allow reaching the Cherenkov light directly on the PMT, the light pulse is collected from many reflections on the tank walls. Additionally, the shower developed for not so high slant depth are relatively thick. These give a signal from a PMT as spread in time and relatively slow increasing.

Hadron induced showers with dominant muon component give an early peak with a typical rise time mostly from 1 to 2 time bins (by 40 MHz sampling) and decay time of the order of 80 ns (Aglietta et al., 2005). The estimation of the rise time for the front on the base of one or two time bins is rather rough. The rise time calculated as for two time bins may be overestimated due to a low sampling rate and an error in a quantization in time. Higher time resolution would be favorable. The expected shape of FADC traces suggests to use a spectral trigger, instead of a pure threshold analysis in order to recognize the shape of the FADC traces characteristic for the traces of very inclined showers. The monitoring of the shape would include both the analysis of the rising edge and the exponentially attenuated tail. A very short rise time together with a relatively fast attenuated tail could be a signature of very inclined showers. We observe numerous very inclined showers crossing the full array but which "fire" only few surface detectors (Fig. 1). For that showers much more detectors should have been hit. Muonic front probably produces PMT signals not high enough to generate 3-fold coincidences, some of signals are below of thresholds (see Fig. 2). This may be a reason of "gaps" in the array of activated surface detectors.

3. Discrete Fourier Transform vs. Discrete Cosine Transform

There are several variants of the DCT with slightly modified definitions. The DCT-I is exactly equivalent (up to an overall scale factor of 2), to a DFT of $2N - 2$ real numbers with even symmetry. The most commonly used form of the Discrete Cosine Transform is DCT-II.

$$\tilde{X}_k = \alpha_k \sum_{n=0}^{N-1} x_n \cos \left(\frac{\pi}{N} \left(n + \frac{1}{2} \right) k \right) \quad (1)$$

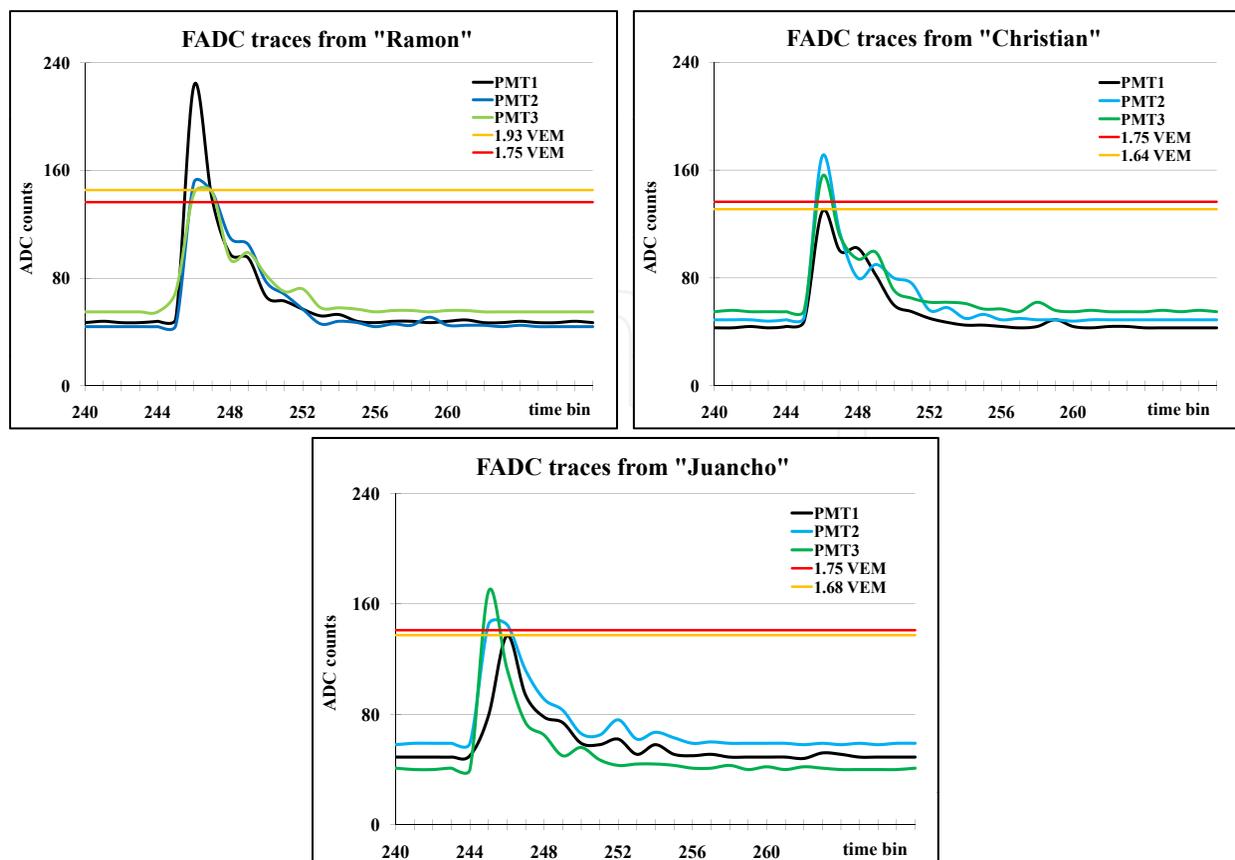


Fig. 2. FADC traces (in ADC-counts) of a horizontal shower (no. 01145055: $\theta = 83.3^\circ$) registered in three detectors: Ramon, Christian and Juancho, respectively, and shown for the range of (240 - 265) time bins. Only the signal in the Ramon detector ($1.93 I_{VEM}$) is above the standard threshold of $1.75 I_{VEM}$. Signals in Cristian ($1.64 I_{VEM}$) and Juancho ($1.68 I_{VEM}$) detectors are below the standard thresholds and they are detected by chance (compare a registration efficiency for a similar event shown in Fig. 1). For all very inclined showers the rising edge corresponds to one or two time bins.

where $\alpha_0 = \frac{1}{\sqrt{N}}$ and $\alpha_k = \frac{2}{\sqrt{N}}$ for $k \geq 1$.

The DCT-III form is sometimes simply referred to as "the inverse DCT" (IDCT). A variant of the DCT-IV, where data from different transforms are overlapped, is called the Modified Discrete Cosine Transform (MDCT). The DCT is a Fourier-related transform similar to the DFT, but using only real numbers. DCT are equivalent to DFT of roughly twice the length, operating on real data with even symmetry (since the Fourier transform of a real and even function is real and even), where in some variants the input and/or output data are shifted by half a sample. The DCT-II and DCT-IV are considered as the alternative approach to the FFT. In fact, the FFT routine can be supplied in an interleaving mode, even samples treated as real data, odd samples as imaginary data. A trigger based on Discrete Fourier Transform (DFT) (Radix-2 FFT) (Szadkowski, 2006) has already been implemented in the 3rd generation of the Front FEB based on Cyclone™ Altera® chip (Szadkowski, 2005b). However, for real signal x_n

$$\bar{X}_{\frac{N}{2}+k} = \sum_{n=0}^{N-1} x_n e^{-j\frac{2\pi}{N}(\frac{N}{2}+k)n} = \sum_{n=0}^{N-1} x_n (-1)^n \left[e^{j\frac{2\pi}{N}kn} \right]^* = \bar{X}_{\frac{N}{2}-k}^* \quad (2)$$

and $\left(\frac{N}{2}\right)^{th}$ spectral line of \bar{X}_k , $k = 0,1,\dots,N-1$ is lying on a symmetry axis: the real part is symmetric, the imaginary part is asymmetric. The useful information is contained only in 1^{st} $\left(\frac{N}{2} + 1\right)$ spectral lines for $k = 0,1,\dots,N/2$ corresponding to frequencies $f_k = k \cdot f_0 = k \frac{1}{N\Delta t}$, changing from zero to $\frac{f_{smp}}{2}$ with $\frac{f_{smp}}{N}$ grid.

3.1 Pedestal independence

The analog section of the FEB has been designed to have a pedestal of ca. 10 % of the full FADC range in order to investigate undershoots. However, the pedestal is relatively sensitive on the temperature. Daily variation of the pedestal may reach 5 ADC-counts. The trigger pedestal-independent is very welcome. Let us consider signal with a constant pedestal:

$$\bar{X}_k(ped) = \sum_{n=0}^{N-1} (x_n + ped)F(k, n) = \bar{X}_k + ped \sum_{n=0}^{N-1} F(k, n) = \bar{X}_k + ped \times W \quad (3)$$

$$F(k, n) = \cos\left(\frac{k\pi}{N}\left(n + \frac{1}{2}\right)\right) \quad (4)$$

Due to symmetry and parity of the cosine, we get for odd and even indices respectively:

$$W = 2 \sum_{n=0}^{\frac{N}{2}-1} \left\{ \cos\left(\frac{k\pi}{2}\right) \cos\left[\frac{\pi}{N}\left(n + \frac{1}{2}\right)k - \frac{k\pi}{2}\right] \right\} = \begin{cases} 0, & k - odd \\ 2 \sum_{n=0}^{\frac{N}{2}-1} F(k, n), & k - even \end{cases} \quad (5)$$

By a recursion, repeating (5) we get finally $\frac{N}{2} = 2$ and $k = 0, \frac{N}{2}$. For $k = \frac{N}{2}$

$$\sum_{n=0}^1 \cos\left(\frac{\pi}{2}\left(n + \frac{1}{2}\right)\right) = 0 \quad (6)$$

In a consequence for $k > 0$ the DCT coefficients are independent of the pedestal.

3.2 Scaling

The DCT algorithm has a significant advantage in comparison to the FFT one. The structure of DCT coefficients is much simpler for interpretation and for a trigger implementation than the structure of the FFT real and imaginary coefficients (compare 4th of the FFT data vs. 2nd row for the DCT coefficients in Fig. 3). For the exponentially attenuated signals from the PMTs higher DCT coefficients (scaled to the 1st harmonics)

$$\xi_k = \frac{\bar{X}_k}{\bar{X}_1} \quad (7)$$

are almost negligible, while both real and imaginary parts of the FFT (scaled to the module of the 1st harmonics) give relatively significant contributions and are not relevant for triggering. When a peak appears in the pure attenuated signal (last column in Fig. 3) the structure of the DCT dramatically changes and trigger condition immediately expires, while modules of FFT components almost do not change. The structure of FFT harmonics for the last graph in Fig. 3 would be more suitable for a trigger (almost negligible imaginary part for higher harmonics and also relatively low real harmonics), however it corresponds just to situation, when the

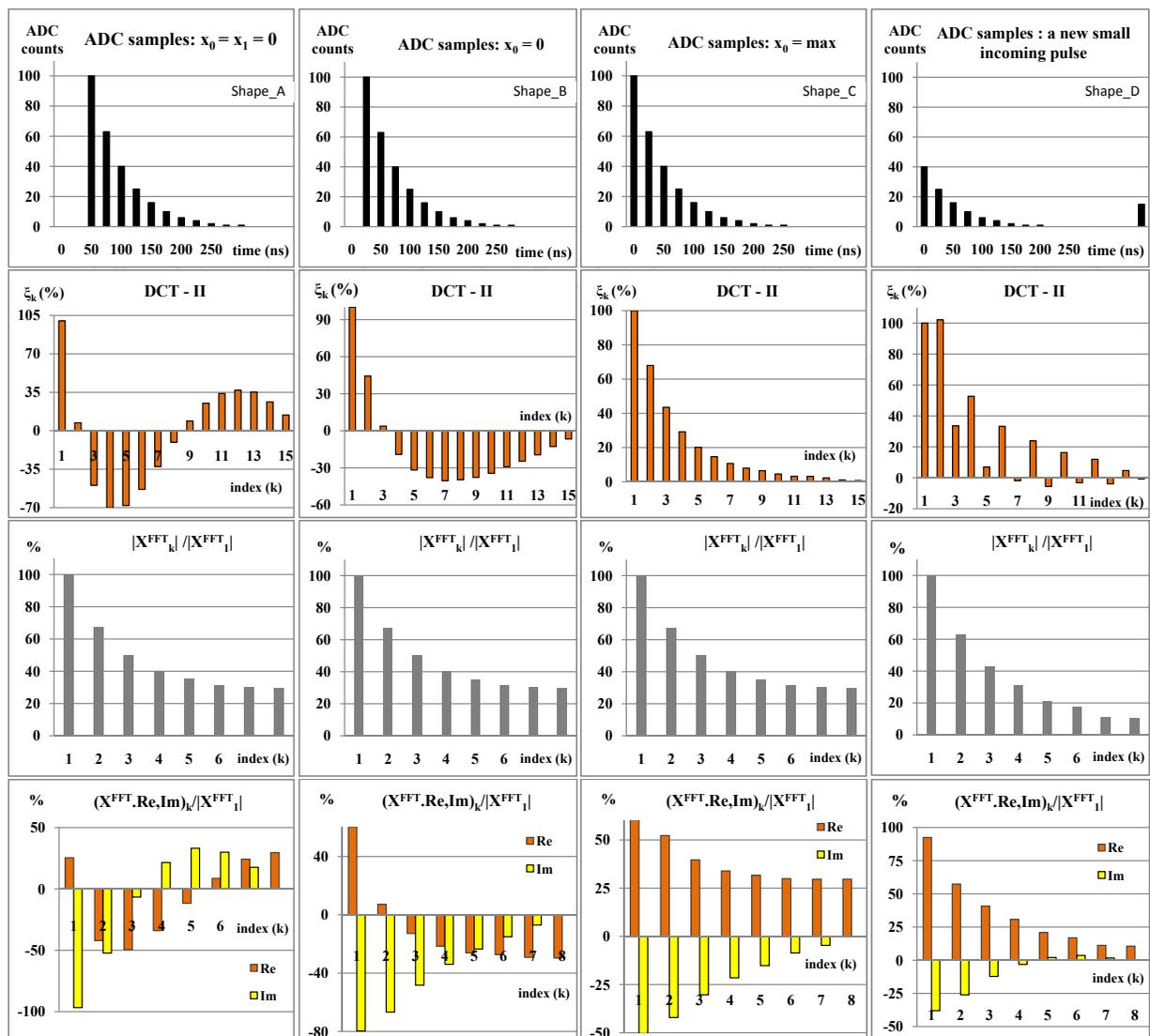


Fig. 3. A propagation of the pulse (1st row) through the shift register, DCT-II coefficients (2nd row), absolute values of the DFT (3rd row) and corresponding real (Re), imaginary parts (Im) (4th row). The 1st column shows the pulse (shape A), when two time bins are on the pedestal level, the 2nd one (shape B), when only the one time bin is still on the pedestal level, while the 3rd one (shape C) shows the pulse fully fulfilled the range of investigating shift registers. For a signal shape related to the exponential attenuation (shape C), the contribution of higher DCT coefficients is small and suitable for a trigger. When a peak appears in the declining signal (last column - shape D), the DCT coefficients immediately exceeds assumed relatively narrow acceptance range for triggers. The DFT coefficients (Re and Im in 4th row) have similar structure as the DCT, however for the pure exponentially declining signal the higher real DFT harmonics have relatively high values and they are not suitable for triggering. Absolute values of DFT components (3rd row) are clearly insensitive on discussed conditions.

pure attenuated signal is distorted by some peak on the tail and a trigger condition has been violated.

The plot in the 4th row and 3rd column on Fig. 3 shows a contribution of the DFT vs. the absolute value of the 1st harmonic. For an exponential attenuated signal (with the attenuation factor = β) the contribution of both real and imaginary coefficients decreases monotonically with a significant value for all real coefficients. From the DFT definition we get:

$$\bar{X}_k = A \sum_{n=0}^{N-1} e^{\beta n} e^{-j\frac{2\pi k}{N}n} = A \frac{1 - e^{-N\beta}}{1 - e^{\beta + j\frac{2\pi k}{N}}} \quad (8)$$

$$\zeta = \frac{Re(\bar{X}_k)}{\|\bar{X}_1\|} = \frac{(1 + e^{-\beta N})}{\sqrt{(1 - e^{-\beta} \cos\phi)^2 + e^{-2\beta} \sin^2\phi}} \quad (9)$$

where $\phi = \frac{2\pi k}{N}$.

Calculating (8) for boundary factors $\beta = (0.28, 0.42)$ (from the Auger database) and for $k = N/2$ (as the lowest in a monotonically decreasing chain), we obtain for $N = 16$: $\zeta = 24\%$ and 28% , respectively. These values are too large to be use for triggering. Even an extension of the DFT size does not help very much. For $N = 32$: we get still large values: $\zeta = 17\%$ and 23% . Almost vanishing higher DCT coefficients provide much natural trigger conditions. 32-point FFT (roughly equivalent to 16-point DCT) does not offer better stability.

4. General DCT algorithm

The DCT for real signal x_n gives independent spectral coefficients for $k = 0, 1, \dots, N-1$, changing f_k also from zero to $\frac{f_{\text{sampl}}}{2}$ but with $\frac{f_{\text{sampl}}}{2N}$ grid. DCT vs. DFT gives twice better resolution. Splitting the sum (1) and redefine the indices we get:

$$\bar{X}_k = \alpha_k \left\{ \sum_{n=0}^{\frac{N}{2}-1} \left(x_n \cos \left[\frac{\pi}{N} \left(n + \frac{1}{2} \right) k \right] - x_{N-1-n} \cos \left[\frac{\pi}{N} \left(N - \left(n + \frac{1}{2} \right) \right) k \right] \right) \right\} \quad (10)$$

Due to symmetry of the cosine function

$$\bar{X}_k = \alpha_k \sum_{n=0}^{\frac{N}{2}-1} \cos \left[\frac{\pi}{N} \left(n + \frac{1}{2} \right) k \right] \times \left(x_n + (-1)^k x_{N-1-n} \right) \quad (11)$$

We can introduce the new set of variables:

$$A_n = \begin{cases} x_n + x_{N-1-n} & (n = 0, \dots, \frac{N}{2} - 1) \\ x_{N-1-n} - x_n & (n = \frac{N}{2}, \dots, N - 1) \end{cases} \quad (12)$$

DCT coefficients can be separated for even and odd indices respectively:

$$\bar{X}_{\text{odd}}^{(\text{even})} = \alpha_k \sum_{n=\binom{0}{N-1}}^{\frac{N}{2}-\binom{1}{0}} A_n \cos \left[\frac{\pi}{N} \left(n + \frac{1}{2} \right) k \right] \quad (13)$$

Let us notice that (13) for even indices has the same structure as (1) with only shorter range of indices. Recurrently we can introduce new sets of variables for the set of indices $k = 2p$, where

p is integer, till $k < N$. In order to use symmetry of trigonometric functions in a maximal way, N should be a power of 2, similarly to Radix-2 approach used in FFT algorithm. If $N = 2q$, recurrent minimization is possible till $p = q$. The twiddle factors for successive minimization steps m equal to $\cos\left(\frac{2\pi}{2^q} \frac{2^{p+m}}{2}\right) = -1$, because the sum of step index m and range factor p is constant and equals to q . For the rest of indices twiddle factor depends on fractional angle $\alpha = \frac{\pi 2^{q-m-1}}{N}$.

After the 1st step of minimization, the terms of the sum (13) for odd indices depends only on the odd multiplicity of the fractional angle

$$\bar{X}_k = \alpha_k \sum_{n=N-1}^{\frac{N}{2}-1} A_n \cos\left[\frac{\pi}{2N} (2n+1)k\right] \quad (14)$$

Using a following trigonometric identity

$$\cos\alpha = \frac{1}{2\cos\beta} (\cos(\alpha + \beta) + \cos(\alpha - \beta)) \quad (15)$$

the fractional angles can be increased by the factor of 2 for $\beta = \frac{k\pi}{2N}$. Thus:

$$\bar{X}_k = \frac{\alpha_k}{2\cos\left(\frac{k\pi}{2N}\right)} \sum_{n=N-1}^{N/2} A_n \times \left[\cos\left(\frac{k\pi}{N}(n+1)\right) + \cos\left(\frac{k\pi}{N}n\right) \right] \quad (16)$$

Let us notice that:

- 1). $\cos(k\pi) = (-1)^k$, for $n = N-1$, hence pure A_n coefficient survives,
- 2). $\cos\left(\frac{k\pi}{2}\right) = 0$, for $n = \frac{N}{2}$ because of odd k ,
- 3). the rest of indices appear in cosine terms twice in A_{n+1} and A_n coefficients, which allows introducing the new set of variables

$$\begin{aligned} B_{N-1} &= A_{N-1} \\ B_{N-1-n} &= A_{N-n} + A_{N-1-n} \end{aligned} \quad (17)$$

The range of B_n indices is continuous and can be split again on even and odd parts. The above procedure can be repeated in recurrence.

5. 8-point DCT algorithm

For $N = 8$ according to formulae (12) and (17) we get :

$$A_{0,1,2,3} = x_{0,1,2,3} + x_{7,6,5,4} \quad A_{7,6,5,4} = x_{0,1,2,3} - x_{7,6,5,4} \quad (18)$$

$$B_{0,1} = A_{0,1} + A_{3,2} \quad B_{2,3} = A_{0,1} - A_{3,2} \quad B_{6,5,4} = A_{7,6,5} + A_{6,5,4} \quad B_7 = A_7 \quad (19)$$

For even indices the DCT coefficients are expressed as follows:

$$2\sqrt{2} \begin{bmatrix} \bar{X}_0 \\ \bar{X}_4 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \end{bmatrix} \quad 4 \begin{bmatrix} S_2 \bar{X}_2 \\ S_6 \bar{X}_6 \end{bmatrix} = B_3 + S_4 \begin{bmatrix} 1 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} B_3 \\ B_2 \end{bmatrix} \quad (20)$$

where

$$S_k = \cos\left(\frac{k\pi}{16}\right) \quad (21)$$

For odd indices with a support of (15) we get:

$$4 \begin{bmatrix} S_1 \bar{X}_1 \\ S_7 \bar{X}_7 \\ S_3 \bar{X}_3 \\ S_5 \bar{X}_5 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & -1 & 1 & -1 & 0 \\ 1 & -1 & 0 & -1 & 0 & 1 \\ 1 & 1 & 0 & -1 & 0 & -1 \end{bmatrix} \begin{bmatrix} B_7 \\ S_2 B_4 \\ S_6 B_4 \\ S_4 B_5 \\ S_2 B_6 \\ S_6 B_6 \end{bmatrix} \quad (22)$$

A direct approach from the classical definition requires: a single multiplication for even indices (20) and 5 multiplications for odd indices (22). The scaled coefficients $S_{1,7,3,5} \bar{X}_{1,7,3,5}$ in (22) can be expressed in an equivalent way introduced by Arai, Agui, Nakajima (AAN, 1988), which allows reducing an amount of multiplications from 5 to 4 only.

$$4 \begin{bmatrix} S_1 \bar{X}_1 \\ S_7 \bar{X}_7 \\ S_3 \bar{X}_3 \\ S_5 \bar{X}_5 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & -1 \\ 1 & 1 & -1 & 0 & 1 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & -1 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} B_7 \\ S_4 B_5 \\ (S_2 + S_6) B_6 \\ (S_2 - S_6) B_4 \\ S_6 (B_6 - B_4) \end{bmatrix} \quad (23)$$

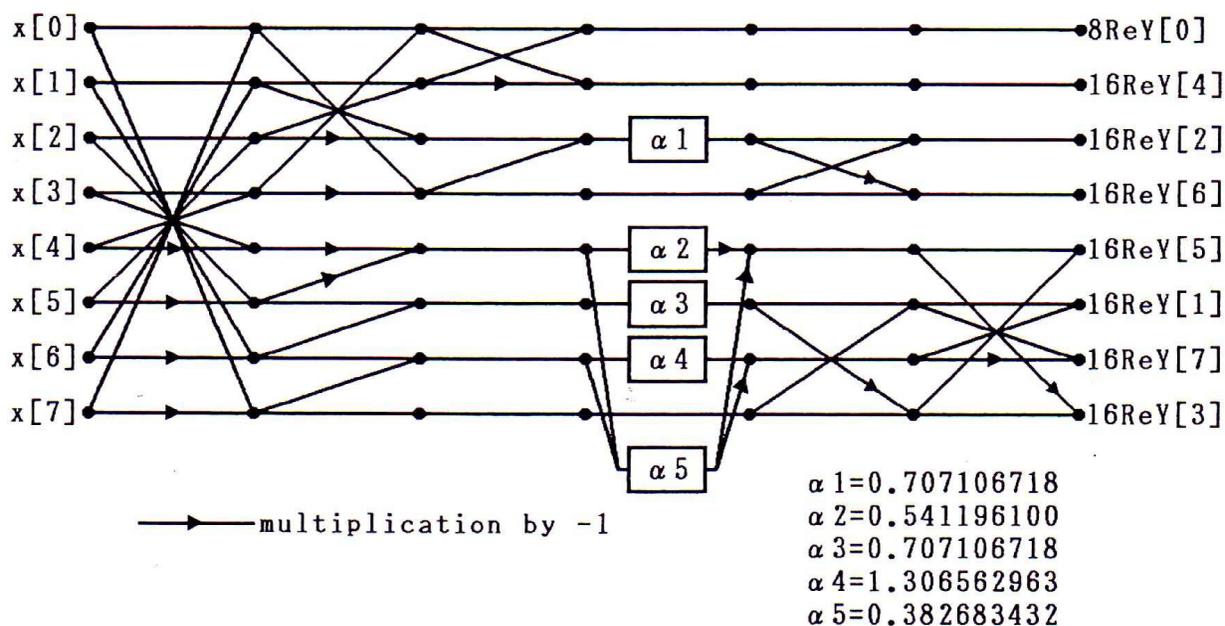


Fig. 4. A fast DCT algorithm developed in 1988 by Arai, Agui and Nakajima

A minimization of multiplications amounts is one of a fundamental goal in long-term numerical calculations. Reduction of product terms significantly speed up sophisticated calculations, because a single multiplication requires several clock cycles of processor. Multiplications in powerful FPGA chips can be however performed in very fast dedicated DSP blocks in a single clock cycle. Signals processed in parallel threads in a hardware implementation of a pipeline design have to be synchronized to each other. Pipeline approach requires additional shift registers for synchronization also for signal currently not being processed. However, such synchronization needs additional resources. Fig. 5 shows the part of pipeline chain corresponding to odd indices of DCT coefficients (lower part in Fig. 4).

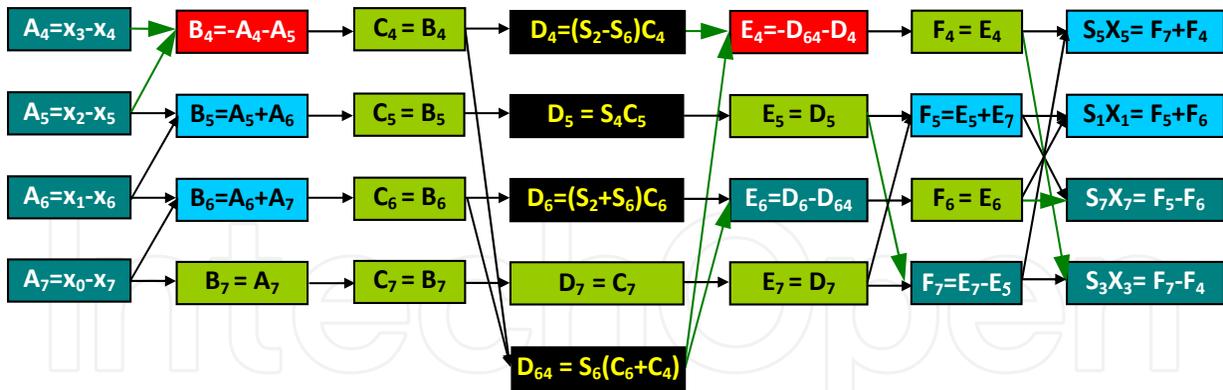


Fig. 5. The AAN algorithm limited to indices 4 - 7 only with a time-oriented structure. Adders, sub-tractors, multipliers and shift registers are marked by the following colours: blue, gray, black and green, respectively. Red colour corresponds to routines requiring a cascade processes.

A direct implementation of the pure AAN algorithm requires 7 pipeline stages, which utilize additional resources of shift registers for synchronization for operations like: $X(t+1) = X(t)$. In a numerical calculation in processors data are simply waiting for a next performance cycle. The D_{64} block contains a cascade of the sum and the multiplication. An implementation of the cascade in a single clock FPGA logic block significantly reduce a speed. Additionally, the *lpm_add_sub* mega-function from the Altera® library of parameterized modules (LPM) does not support an inversion of a sum i.e. $B_4 = -(A_4 + A_5)$ or $E_4 = -(D_{64} + D_4)$. These operations would have to be performed in a cascade way by an adder and a sign inversion. Cascade operations performed in the same clock cycle significantly slow down a global registered performance.

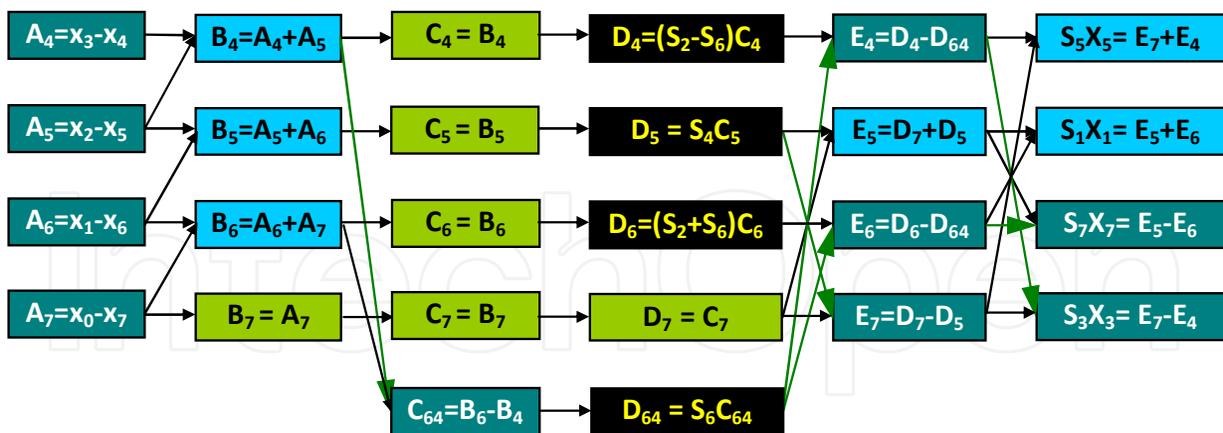


Fig. 6. Optimized AAN algorithm for indices 4 - 7. A redefinition and splitting of variables allowed a reduction of the chain length.

A simple redefinition of nodes removes difficulties mentioned above. The B_4 node defined as the sum of $A_{4,5}$ nodes requires a simple *lpm_add_sub* mega-function. The D_4 node with currently inverted sign allows using *lpm_add_sub* in E_4 performing a subtraction. The D_{64} node from Fig. 5 can be split into the subtraction C_{64} and the multiplication D_{64} in the next clock cycle (Fig. 6).

Routines E and F from Fig. 5 have been merged into single routine E (Fig. 6) to short an amount of pipeline stages and remove unnecessary shift registers.

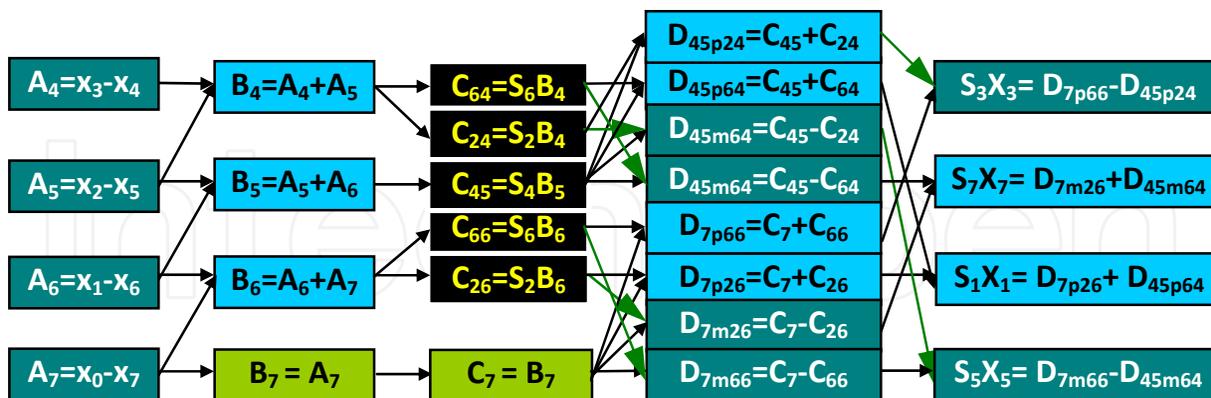


Fig. 7. Optimized, shorter pipeline chain based on the classical approach. The reduction of the length of the chain at the cost of an additional multiplier.

A classical approach reduces a length of the chain from 6 to 5 stages only, at the cost of one additional multipliers. An abridgement of the pipeline chain and in a consequence a reduction of the shift registers needed for synchronization allows saving significant amount of logic blocks, especially for wide data bus. In order to reduce an approximation errors, the data bus in the intermediate stages is enlarged.

6. 16-point DCT algorithm

The 16-point DCT algorithm will be implemented according to the classical approach with an optimization of the number of pipeline stages at the cost of an utilization of embedded multipliers (Szadkowski, 2009). The 1st and the 2nd pipeline stages utilize the set of variables (12) and (17) respectively. For $N = 16$ the fractional angle of the twiddle factor in the 1st step of minimization equals to $\beta = \pi$. The same fractional angle corresponds to the 2nd step of minimization for even indices corresponded to A_n .

$$B_{0,1,2,3} = A_{0,1,2,3} + A_{7,6,5,4} \quad B_{4,5,6,7} = A_{3,2,1,0} - A_{4,5,6,7} \tag{24}$$

The scaling procedure used for odd indices of \bar{X}_k with the fractional angles $\beta = \frac{k\pi}{32}$ gives:

$$B_{15} = A_{15} \quad B_{14,\dots,8} = A_{15,\dots,9} + A_{14,\dots,8} \tag{25}$$

Coefficients \bar{X}_k for even indices can be expressed by variables (24) and scaling factor (21)

$$\begin{bmatrix} \bar{X}_0 \\ \bar{X}_8 \\ \bar{X}_4 \\ \bar{X}_{12} \end{bmatrix} = \frac{1}{2\sqrt{2}} \begin{bmatrix} S_4 & S_4 & S_4 & S_4 \\ S_4 & -S_4 & -S_4 & S_4 \\ S_2 & S_6 & -S_6 & -S_2 \\ S_6 & -S_2 & S_2 & -S_6 \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} \bar{X}_2 \\ \bar{X}_{14} \\ \bar{X}_6 \\ \bar{X}_{10} \end{bmatrix} = \frac{1}{2\sqrt{2}} \begin{bmatrix} S_7 & S_5 & S_3 & S_1 \\ -S_1 & S_3 & -S_5 & S_7 \\ -S_5 & -S_1 & -S_7 & S_3 \\ S_3 & S_7 & -S_1 & S_5 \end{bmatrix} \begin{bmatrix} B_4 \\ B_5 \\ B_6 \\ B_7 \end{bmatrix} \tag{27}$$

After a scaling according to (15) we can introduce the new set of variables for the 3rd pipeline stage:

$$4 \begin{bmatrix} \bar{X}_0 \\ \bar{X}_8 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} C_0 \\ C_1 \end{bmatrix} \quad 4\sqrt{2} \begin{bmatrix} S_2 \bar{X}_4 \\ S_6 \bar{X}_{12} \end{bmatrix} = \begin{bmatrix} 1 + S_4 & S_4 \\ 1 - S_4 & -S_4 \end{bmatrix} \begin{bmatrix} C_3 \\ C_2 \end{bmatrix} \quad (28)$$

$$4\sqrt{2} \begin{bmatrix} S_1 \bar{X}_2 \\ S_7 \bar{X}_{14} \\ S_3 \bar{X}_6 \\ S_5 \bar{X}_{10} \end{bmatrix} = \begin{bmatrix} 1 & S_4 & S_2 & S_6 \\ 1 - S_4 & S_6 & -S_2 & \\ 1 - S_4 & -S_6 & S_2 & \\ 1 & S_4 & -S_2 & -S_6 \end{bmatrix} \begin{bmatrix} C_7 \\ C_5 \\ C_6 \\ C_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 1 & 1 & 0 \\ 1 - 1 & 0 & -1 & 0 & 1 & \\ 1 & 1 & 0 & -1 & 0 & -1 \\ 1 & 0 & -1 & 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} C_7 \\ S_2 C_4 \\ S_6 C_4 \\ S_4 C_5 \\ S_2 C_6 \\ S_6 C_6 \end{bmatrix} \quad (29)$$

$$\begin{aligned} C_{0,1} &= B_{0,1} + B_{3,2} & C_{3,2} &= B_{0,1} - B_{3,2} \\ C_{4,5,6} &= B_{4,5,6} + B_{5,6,7} & C_7 &= B_7 \end{aligned} \quad (30)$$

Let us notice that the structure of the right vector in (29) is exactly the same as in (22), but the structures of the 6x4 matrices are different. In (22) the matrix comes from a transformation for the odd indices supported by (21), while in (29) the matrix comes from a transformation of even indices.

Scaled coefficients corresponding to odd indices

$$\bar{Z}_k = 4\sqrt{2} \bar{X}_k \cos\left(\frac{k\pi}{32}\right) \quad (31)$$

can be expressed by variables (25) and scaling factors (21) as follows:

$$\begin{bmatrix} \bar{Z}_{1,15} \\ \bar{Z}_{3,13} \\ \bar{Z}_{5,11} \\ \bar{Z}_{7,9} \end{bmatrix} = \begin{bmatrix} 1 & S_4 & S_2 & S_6 \\ 1 - S_4 & S_6 & -S_2 & \\ 1 - S_4 & -S_6 & S_2 & \\ 1 & S_4 & -S_2 & -S_6 \end{bmatrix} \begin{bmatrix} B_{15} \\ B_{11} \\ B_{13} \\ B_9 \end{bmatrix} \pm \begin{bmatrix} S_1 & S_3 & S_5 & S_7 \\ S_3 & -S_7 & -S_1 & -S_5 \\ S_5 & -S_1 & S_7 & S_3 \\ S_7 & -S_5 & S_3 & -S_1 \end{bmatrix} \begin{bmatrix} B_{14} \\ B_{12} \\ B_{10} \\ B_8 \end{bmatrix} \quad (32)$$

Matrix (32) can be factorized as follows:

$$\begin{bmatrix} \bar{Z}_{1,15} \\ \bar{Z}_{7,9} \\ \bar{Z}_{5,11} \\ \bar{Z}_{3,13} \end{bmatrix} = \begin{bmatrix} (C_{15} + C_{11}) + (C_{13}^2 + C_9^6) \\ (C_{15} + C_{11}) - (C_{13}^2 + C_9^6) \\ (C_{15} - C_{11}) - (C_{13}^6 - C_9^2) \\ (C_{15} - C_{11}) + (C_{13}^6 - C_9^2) \end{bmatrix} \pm \begin{bmatrix} \frac{1}{2S_1} & 0 & 0 & 0 \\ 0 & \frac{1}{2S_3} & 0 & 0 \\ 0 & 0 & \frac{1}{2S_5} & 0 \\ 0 & 0 & 0 & \frac{1}{2S_7} \end{bmatrix} \begin{bmatrix} 1 & S_4 & S_2 & S_6 \\ 1 - S_4 & S_6 & -S_2 & \\ 1 - S_4 & -S_6 & S_2 & \\ 1 & S_4 & -S_2 & -S_6 \end{bmatrix} \begin{bmatrix} C_{14} \\ C_{10} \\ C_{12} \\ C_8 \end{bmatrix} \quad (33)$$

where:

$$C_{8,10,12} = B_{8,10,12} + B_{10,12,14} \quad C_{14,15} = B_{14,15} \quad C_{9,13}^{2,6} = B_{9,13} S_{2,6} \quad C_{11} = B_{11} S_4 \quad (34)$$

In the 4th pipeline step directly from (32) we can introduce new variables:

$$D_{15,11} = C_{15} \pm C_{11} \quad D_{13} = C_{13}^2 + C_9^6 \quad D_9 = C_{13}^6 - C_9^2 \quad (35)$$

The rest of variables require 10 next multipliers, 3 adders/subtractors and 3 shift registers:

$$D_{5,10} = S_4 C_{5,10} \quad D_{4,6,8,12}^{2,6} = S_{2,6} C_{4,6,8,12} \quad D_{3,7,14} = C_{3,7,14}$$

$$D_{0,1} = C_0 \pm C_1 \quad D_2 = C_2 + C_3 \quad (36)$$

However, the 5th pipeline stage requires only a single multiplier for the E_2 variable:

$$E_2 = S_4 D_2 \quad E_{0,1,3} = D_{0,1,3} \quad E_4 = D_6^6 - D_4^2 \quad E_6 = D_6^2 + D_4^6 \quad (37)$$

$$E_{7,11,15} = D_{7,11,15} \pm D_{5,9,13} \quad E_{14,10} = D_{14} \pm D_{10} \quad E_{12} = D_{12}^2 + D_8^6 \quad E_8 = D_{12}^6 - D_8^2 \quad (38)$$

The 6th stage does not require any multiplier, only 10 adders/subtractors and 6 shift registers for synchronization:

$$F_{3,5,7,9,13} = E_{3,5,7,9,13} \pm E_{2,4,6,8,12} \quad F_{0,1,9,11,13,15} = E_{0,1,9,11,13,15} \quad (39)$$

In the 7th pipeline stage 12 signals are delayed only for synchronization and 4 are scaled for the following (n,k) pairs: (14,1),(12,7),(10,3),(8,5):

$$G_n = \frac{F_n}{2S_k} \quad (40)$$

In the 8th pipeline stage pure registers for synchronization only are implemented for even indices of $\bar{X}_{0,2,4,6,8,10,12,14}$ and

$$H_{9,11,13,15} = G_{9,11,13,15} \pm G_{8,10,12,14} \quad (41)$$

The last stage contains all scaling multipliers:

$$\bar{X}_k = \frac{H_m}{4\sqrt{2}\cos\left(\frac{k\pi}{32}\right)} \quad (42)$$

for the following (k,m) pairs: (1,15), (15,14), (7,13), (9,12), (3,11), (13,10), (5,9), (11,8), (14,7), (2,6), (6,5), (10,4), (4,3), (12,2).

7. Implementation of the code into a FPGA

The spectral trigger should be generated if DCT coefficients normalized to the 1st harmonics are in an arbitrary narrow range:

$$Thr_k^L \leq \zeta_k = \frac{\bar{X}_k}{\bar{X}_1} = \frac{\eta_k * H_{f(k)}}{\eta_1 * H_{15}} \leq Thr_k^H \quad (43)$$

where Thr_k^L and Thr_k^H are lower and upper thresholds for each spectral index k, respectively. Altera® Library of Parameterized Modules (LPM) contains the lpm_divide routine supporting a division of fixed-point variables. However, this routine needs huge amount of logic elements and it is slow (calculation requires 14 clock cycles in order to keep sufficiently high registered performance). DSP blocks also do not support this routine. A simple conversion to

$$H_{15} \times \theta_k^L = H_{15} \left(\frac{\eta_1}{\eta_k} Thr_k^L \right) \leq H_{f(k)} \leq H_{15} \left(\frac{\eta_1}{\eta_k} Thr_k^H \right) = H_{15} \times \theta_k^H \quad (44)$$

allows implementation of fast multipliers from the DSP blocks and calculation of products in a single clock cycle. θ_k^L and θ_k^H are lower and upper scaled thresholds respectively, which are set as external parameters.

According to (44) the calculation of a sub-trigger needs two multipliers, two comparators and an AND gate. The multiplier stage of an embedded multiplier block supports 9×9 or 18×18 bit multipliers. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel. Due to wide data busses embedded multiplier blocks do not use the 9×9 mode in any multiplication. Each multiplier utilizes two embedded multiplier 9-bit elements. The full DCT procedure needs the calculation of all coefficients 70 DSP blocks. However, the scaling of \bar{X}_k in the last pipeline chain is no longer needed. It is moved to the thresholds according to (44). Removing last pipeline chain reduces amount of DSP blocks to 40. Sub-triggers routines (Fig. 9) need 2 DSP blocks each. The chip EP3C40F324I7 selected for the 4th generation of the 1st level SD trigger contains 252 DSP 9-bit multipliers. So, for 3-fold coincidences and an implementation of 3 "engines" the single DCT "engine" can support only 11 independent DCT coefficients (Szadkowski, 2011). Sub-triggers $A_k^{0,1,2,3}$, $B_k^{0,1,2}$, $C_k^{0,1}$ and D_k^0 are generated for the patterns A_k , B_k , C_k and D_k ($k = 2,4,6$) from Fig. 3, respectively. Sub-triggers are synchronized to each other in shift registers in order to put simultaneously on an AND gate (Fig. 11). In order to keep a trigger rate below the boundary deriving from the limited radio bandwidth, additionally the amplitude of the jump is verified. If the jump is too weak, a veto comparator disables the AND gate. Thus, if spectral coefficients ζ_k match pattern ranges for each time bins selected by multiplexer totally in 4 consecutive time bins and if veto circuit is enabled the final trigger is generated. A delay time for the veto signal depends on the type of shape, which is an interest of an investigation. For the single time bin of the rising edge the veto is delayed on 3 clock cycles, for the investigated pattern corresponding to the three time bins of the rising edge the maximal ADC value appears 2 clock cycles later in comparison to the previous case, so the veto should be delayed on a single clock cycle only.

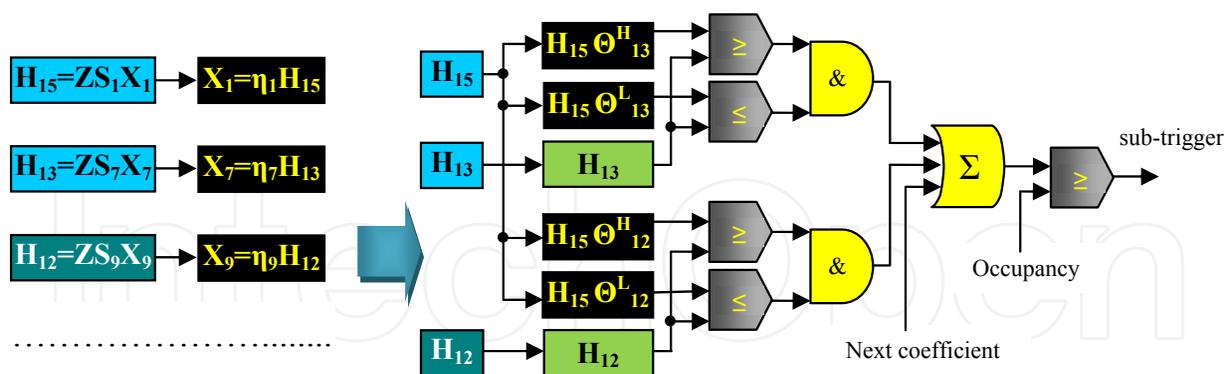


Fig. 9. The structure of sub-triggers. The DCT coefficients \bar{X}_k are not directly calculated. They have been replaced by a boundary of the acceptance lane: upper and lower thresholds $H_{15} \times \theta_k^H$ and $H_{15} \times \theta_k^L$, respectively. Signals between that thresholds (two comparators + AND gate) generate preliminary sub-triggers, which are next summed and compared with the arbitrary Occupancy level. If an amount of "fired" preliminary sub-triggers is above the selected Occupancy, the final sub-trigger is generated for the next processes. It is enabled/disabled depending on the veto variable, verifying the minimal amplitude of the input signals to keep the trigger rate on the reasonable level and to prevent the saturation of the transmission channel.

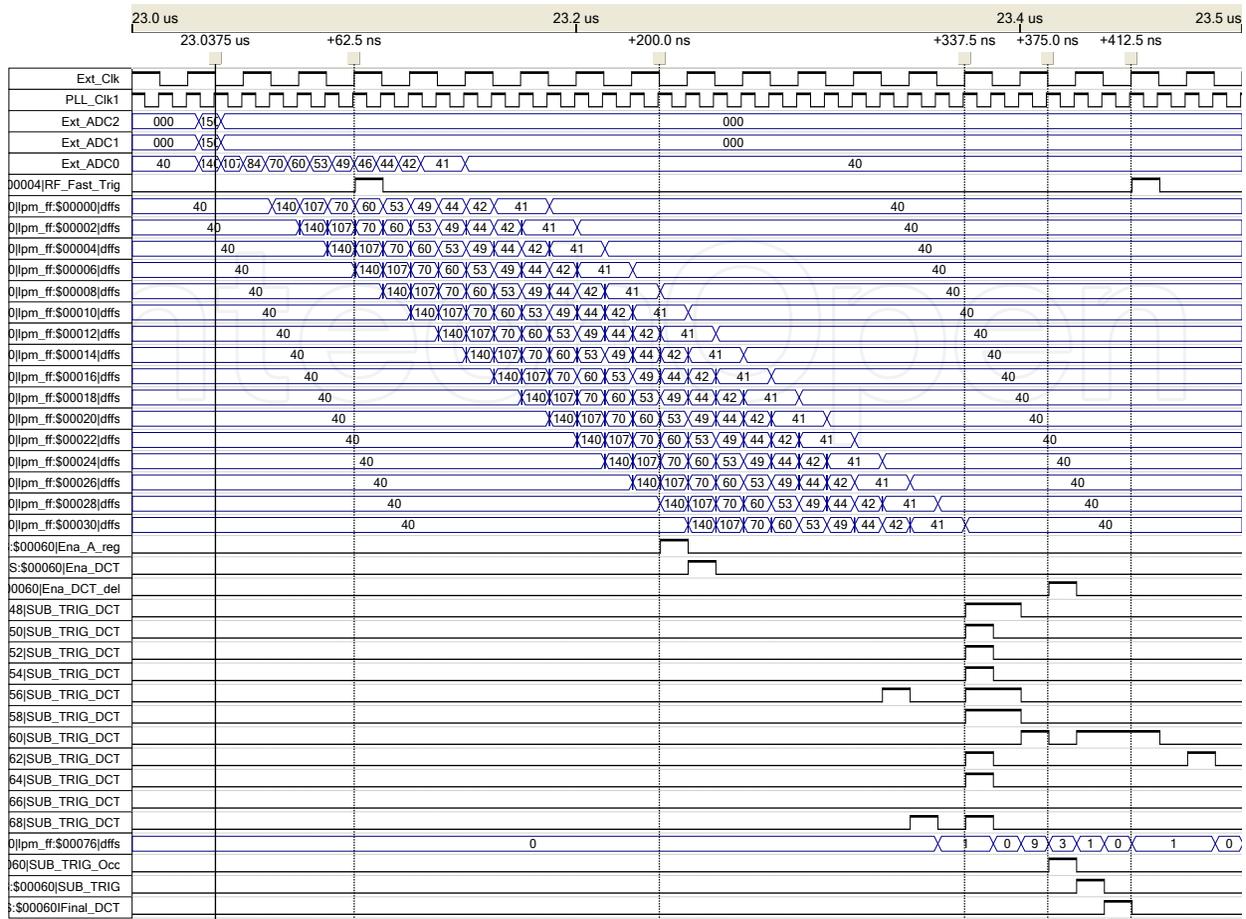


Fig. 10. Simulation of the 1-fold spectral trigger simultaneously with the 3-fold threshold trigger. The length of the shift registers = 16. Data in the Ext_ADC0 channel corresponds to a muon signal with a 1-time-bin rising edge, 11-time-bins attenuation tail and with a constant pedestal = 40 ADC-counts. Together with the begin of the muon peak (at 23.075 μ s), two neighboring channels Ext_ADC1,2 are driven artificially to 150 ADC-counts to generate the standard threshold trigger based on the 3-fold coincidence. The internal PLL clock = 80 MHz. The internal standard threshold trigger appears 5 clock cycles later (+62.5 ns). The nodes lpm_ff:\$00000 | dffs - lpm_ff:\$00030 | dffs correspond to the shift register x_{15}, \dots, x_0 . The system is tuned for the Shape_A recognition (two 1st time bins on the pedestal level). Ena_A_reg is generated (+200 ns = 16 clock cycles) due to the amplitude of the signal (140 ADC-counts) is above the veto threshold. It is delayed next 15 cycles to be synchronized with SUB_TRIG_OCC. Sub-triggers are generated 27 clock cycles (+337.5 ns) after the rising edge. A calculation of the Occupancy takes next two clock cycles. 29 clock cycles after the rising edge due to a coincidence of the Occupancy and Ena_DCT_del (inversion of the veto) the SUB_TRIG is generated. Finally it appears in the same position as 3-fold coincidence threshold trigger 31 clock cycles later. Final_DCT trigger corresponds to the possible coincidence with a neighboring DCT "engines". If the standard threshold trigger (based on 3-fold coincidence) appears next any triggers are ignored though 768 clock cycles.

The 16-point DCT with 16-stage shift register for 100 MHz sampling can cover 150 ns time window. For the horizontal or very inclined showers this interval is sufficient for the analysis. However, for the higher sampling frequency, when the time window may turn out too short, the shift register may be extended from 16 to 24 stages and the eight samples for the higher

indices may be taken from the last 16 shift register nodes according to the Fig. 11. The samples with higher indices correspond to the exponentially attenuated tail and the analysis of the tail is less critical than the rising edge, where samples are analyzed with a full speed.

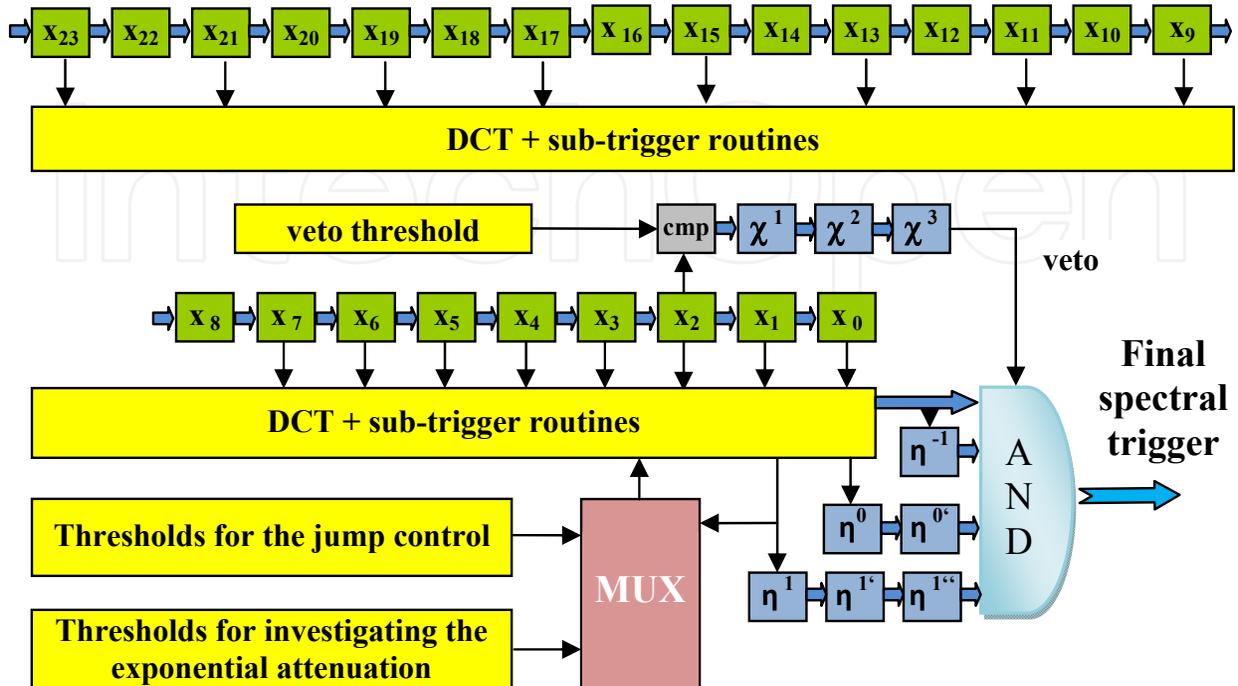


Fig. 11. A scheme of the final spectral trigger. The shift register presented here has an extended length = 24 stages to cover longer time window. However, for a sampling frequencies $f_s \leq 100$ MHz 16 stages and $T \geq 150$ ns the window is wide enough for an analysis of horizontal showers. If signal shifted in the register chain matches the expected patterns for 4 consecutive time bins i.e. corresponding to ADC shapes in Fig. 3 (1st row, 3 first graphs). The 4th pattern is exactly the same as the 3rd one. The amplitude of the signal decreases, but the DCT coefficients remain the same (still an exponential attenuation).

3 DCT trigger "engines" have been successfully merged with the Auger code working with 100 MHz sampling. The final code utilizes only 38 gives an opportunity to add new, sophisticated algorithms. The slack reported by the compiler corresponds to a maximal sampling frequency 112 MHz, which gives a sufficient safety margin for a stable operation of the system. For sufficiently high amplitudes of the ADC samples the Threshold trigger will be generated 32 clock cycles earlier than the spectral trigger (24 clock cycles of propagation in the shift registers + 8 clock cycles of performance in the DCT chain). If the Threshold trigger has been already generated, the next triggers are inhibited for 768 time bins necessary to fulfill memory buffers (see Fig. 7 in (Szadkowski, 2005a)). Because the Threshold trigger (sensitive to bigger signals) has a higher priority than the spectral trigger, ADC samples will not be delayed for the Threshold trigger in order to synchronize it with the spectral one. The system uses 10-bit resolution (standard Auger one). A compilation for the 12-bit resolution for the current chip EP3C40F324I7 failed, due to a lack of the DSP blocks. 12-bit system requires bigger chip EP3C55. The slack times are on the same level as for EP3C40. All pipeline routines shown in Fig. 8 are implemented in a direct mode (no pipeline mode - like i.e. in the 2nd generation of the FEB based on the ACEX family (see Fig. 2 in (Szadkowski, 2005a)) or for the FFT implementation in the Cyclone family (Fig. 2 in (Szadkowski, 2005b)). So, a performance

of a signal requires a single clock cycle only. All routines are fast enough to work with 100 MHz sampling without an additional pipeline stages and they do not introduce an additional latency.

8. Accuracy

10-bit resolution of FADC in the high-gain channels (responsible for a trigger generation) implies the ranges of \bar{X}_k coefficients given in the 2nd column of Table 1. Multiplications of integer values N by real scaling factors sf give floating-point results. In order to keep possible high speed of calculation and not to utilize resources spendthrift the fixed-point algorithm of processing has been chosen. $N \times sf$ were approximated on each pipeline stage again to the integer value. For almost all scaling factors: $sf \leq 1$, $N \times sf$ has a representation of the same or less amount of bits. For $sf \geq 1$, $N \times sf$ extends the representation on 1 or 2 bits. This approximation introduces errors. However, the width of the data in the internal pipeline stages is extended from the N at the shift register x_{15}, \dots, x_0 , to $N+1, N+2, N+3, N+4, N+5, N+7, N+8$ in routines A, B, C, D, E, F, G, respectively (Fig. 8). This reduces approximation errors mostly to the LSB, apart the \bar{X}_{15} . This coefficient will not be used for a trigger.

k	range of \bar{X}_k	LSB	2 nd bit	3 rd and more	k	range of \bar{X}_k	LSB	2 nd bit	3 rd and more
0	0...4092	0.0%	0.00%	0.00%	8	± 2041	0.0%	0.00%	0.00%
1	± 2521	13.1%	0.00%	0.00%	9	± 12224	23.8%	1.55%	0.00%
2	± 2581	8.7%	0.00%	0.00%	10	± 4557	12.8%	0.00%	0.00%
3	± 2914	13.1%	0.00%	0.00%	11	± 7519	17.7%	0.00%	0.00%
4	± 2348	4.8%	0.00%	0.00%	12	± 5671	11.5%	0.00%	0.00%
5	± 4019	15.1%	0.00%	0.00%	13	± 9605	24.3%	2.00%	0.00%
6	± 3045	8.6%	0.00%	0.00%	14	± 12978	26.9%	2.86%	0.00%
7	± 10032	23.1%	1.10%	0.00%	15	± 25597	30.9%	25.08%	6.83%

Table 1. Ranges of \bar{X}_k coefficients and relative errors for least significant bits of \bar{X}_k . For $k \leq 14$ the errors appear practically only in the LSB.

According to above estimations, the configuration with 3 "engines" does not support all ξ_k sub-triggers due to limited amount of DSP blocks. However, for the next generation of the water Cherenkov detectors array, where probably only a single PMT will be used, 3 "engines" will be implemented to investigate and to detect 3 different shapes of FADC traces corresponding to i.e. different rise times of the rising edge.

9. Preliminary tests

Analysis of Auger ADC traces of very inclined showers shows that the maximum of the signal is mostly reach in a single time bin. The attenuation factor for a tail is in the range of $\beta = (0.2 - 0.5)$. Fig. 12 shows shapes of signals with various attenuation factors with two first time bins on a pedestal level. For simplicity it has been set on zero. It does not reduce the generality of analysis, because the pedestal is irrelevant for DCT ($k \geq 1$). The corresponding DCT coefficients are shown in upper Fig. 3 (Shape_A). After a single clock cycle, when data is shifted in the registers chain, shifted signal with only one time bin on the pedestal level determines a new set of the DCT coefficients shown in lower Fig. 3 (Shape_B). Pattern, which is going to be recognized, can be selected by a setting of DCT coefficient in the DCT engines.

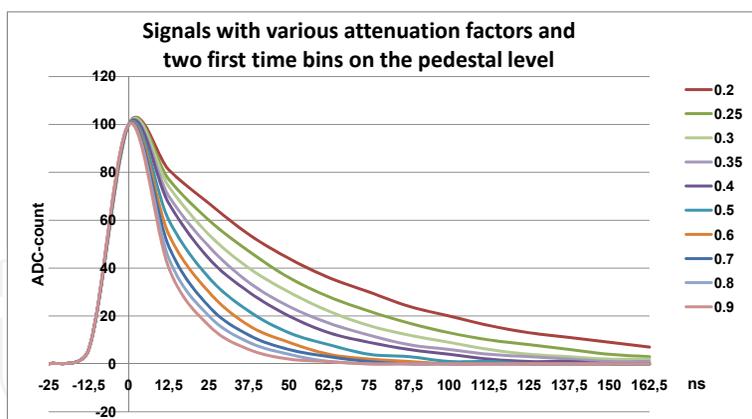


Fig. 12. Shapes of signals with various attenuation factors and two first time bins on the pedestal level

All signals with first two time bins on the pedestal level for sure will be with only one time bin on the pedestal level in the next clock cycle. But, not vice versa. A signal with only a single time bin on the pedestal level before sharp rising edge can have significant contribution in the 2nd time bin before rising edge and it will not be recognized by a pattern recognition procedure tuned on the Shape_A. A procedure recognizing Shape_A is more restrictive and gives lower trigger rate than for the Shape_B. Due to limited amount of the DSP blocks only 11 DCT coefficients can be analyzed simultaneously. For the Shape_A the \bar{X}_4 and \bar{X}_{10} are ignored and for the Shape_B : \bar{X}_6 and \bar{X}_{14} , respectively, as weakly sensitive on changes of signal shapes. The trigger based only on the DCT pattern recognition gives too high rate, due to a contribution of very weak signals with also appropriate shape, but usually treated as noise. In order to reduce and control the trigger rate, the veto threshold has been introduced. The calculation of the DCT coefficients in the pipeline chain and next the calculation of sub-triggers in multipliers and comparators block takes 12 clock cycles. The signal is synchronized with the DCT sub-triggers delayed the same time to be compared with the veto threshold, simultaneously with a generated DCT sub-triggers. If the signal is above the sum of the veto threshold and the pedestal, the sub-triggers are enabled to generate a final spectral trigger. The condition that all 11 DCT coefficients were inside the acceptance lane is too strong. The shapes are not ideal, noise introduces additional shape distortions. Similarly as in the ToT trigger only a part of "fired" sub-triggers (Occupancy $\leq 11 = \text{max. number of sub-triggers}$) is enough to generate the final spectral trigger.

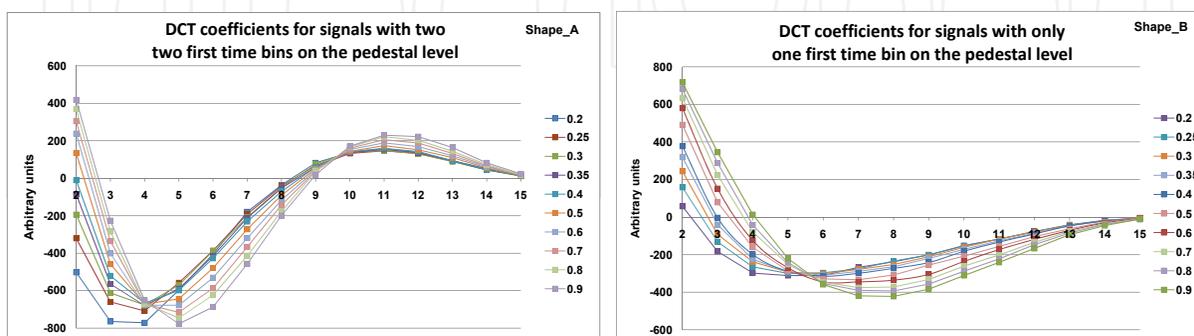


Fig. 13. Coefficients for signals with various attenuation factors and two first time bins (left) and only one time bin (right) on the pedestal level

Although the spectral trigger is being developed for the future and for a single detection channel (a single PMT), the DCT trigger in the Auger surface detector has been tested in a 2-fold coincidences of any 3 PMTs, to be close as possible for a comparison of the results with the standard Auger data.

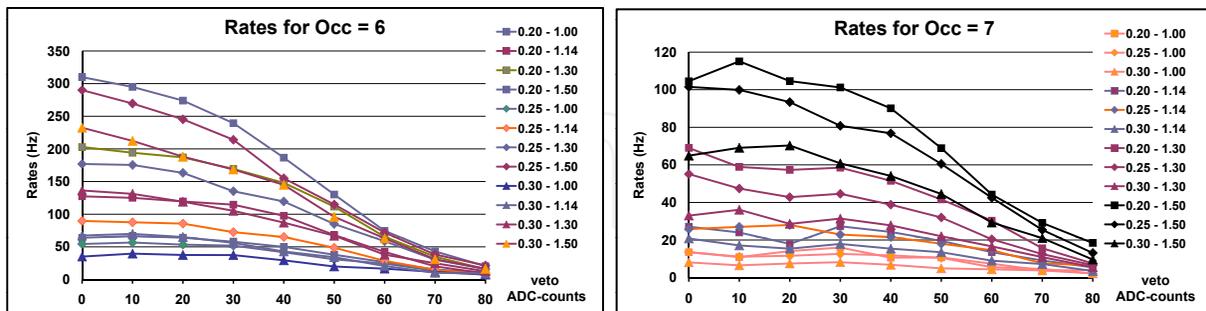


Fig. 14. Rates for various acceptance lanes (from 0.20 - 1.00 till 0.30 - 1.50) and the veto threshold (0 - 80 ADC-counts) for the Occupancy = 6 (left) and 7 (right), respectively. Due to a possible saturation of a transmission channel, the rate of the spectral trigger should not exceed ca. 40 Hz.

Fig. 14 show the trigger rate for the Occupancy = 6 and 7, respectively. The T1 trigger rate is calibrated to ca. 100 Hz. Generally, the trigger rate for Occ = 6 is too high. In order not to saturate the microcontroller and the transmission chain the total (standard Auger + spectral) trigger rate should not exceed 150 Hz. This gives max. 40 - 50 Hz for the spectral trigger only. The Occupancy = 7 with a range of attenuation factors limited to $\beta = (0.20 - 1.14)$ gives a trigger range on the reasonable level. The Occupancy = 8 reduces the trigger rate below 1 Hz and seems to be too restrictive. The FPGA contains internal counters counting the trigger rate and a contribution of DCT sub-triggers to the final trigger. The required trigger rate range can be set remotely from the Central Data Acquisition System (CDAS). The FPGA automatically tunes the veto threshold to get the required trigger rate. If the veto threshold is above 60 ADC-counts (ca. 1.2 VEM) the acceptance lane is modified. The attenuation factor β from the left side of the range is increased/decreased in the range of (0.20 - 0.40) by the fixed right boundary $\beta = 1.3$.

Fig. 15 show three calibration processes, when either initial parameters has been set ideally (B) or they have to be tuned to get required trigger rate (A and C). The tuning process typically does not exceed 3 minutes. In contrary to the standard Auger tuning procedure, when the thresholds for the Threshold trigger are calculated by the external microcontroller located on the Unified Board (UB), the thresholds for the acceptance DCT lane are initially calculated and next stored in the ROM inside the FPGA and they are only multiplexed. This allows a full autonomous FPGA calibration process without a support by any external microcontroller. The new Front-End Board samples analog signals with 80 MHz. Data is written via a left port in the dual-port RAM. Stored data are next read via the right port with 40 MHz. The new board is seen by the rest of electronics as the standard one. Only a additional flag informs the system on the type of the trigger. Internal FPGA counters allow counting a contribution of the DCT coefficients to the final spectral trigger. Fig. 15d shows a relative contribution of the DCT coefficients for the Shape_A. The contribution of the \bar{X}_5 and \bar{X}_9 is a little bit lower than the rest ones. For the \bar{X}_9 the acceptance lane (compare Fig. 13A) is relatively narrow, so the lower contribution is not strange. \bar{X}_5 is probably more sensitive on signal noise and possible signal distortions. The graph A (Fig. 15) shows a process when the trigger rate is initially too

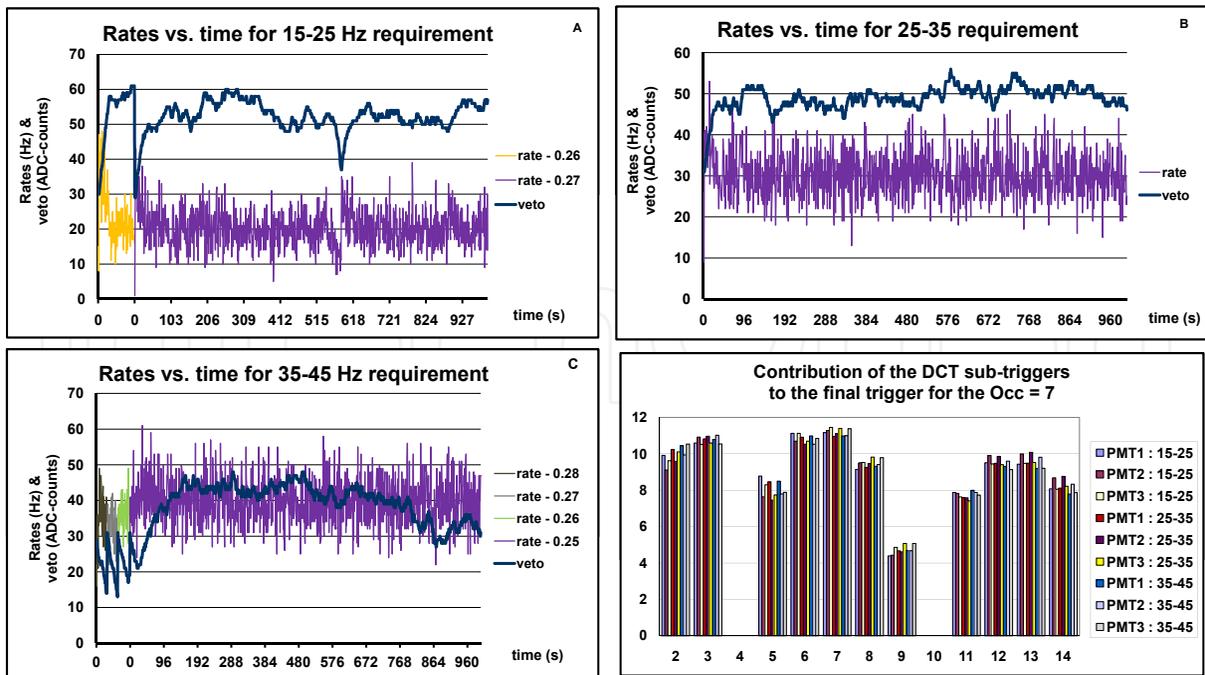


Fig. 15. Rates obtained in the test detector during an auto-calibration process (graphs A, B and C). A comparison of a contribution of "fired" DCT coefficients generating the sub-triggers for all three PMT channels and for various trigger rates requirements (right-down). There are no significant differences in a contribution of a fixed coefficients for different PMT and various configuration of trigger rate requirements

high and the attenuation factor has to be increased (the acceptance lane is narrowed down). The graph B shows the process, when the initial parameters are optimal and the acceptance lane is not modified (only the veto threshold is tuned). The graph C shows the process when the initial parameters give too low trigger rate and the acceptance lane is changed three times.

10. Conclusion

The pattern recognition technique implemented parallel with the standard threshold detection may improve an efficiency of a registration of rare events, especially for a single PMT in the surface detector, when the coincidence technique cannot be longer used.

The optimized algorithm of the spectral trigger based on the Discrete Cosine Transform with veto and auto-calibration procedure has been successfully implemented into the FPGA and showed the perfect stability in the real detector. Measurements in the test detector confirmed assumption for a selection of limited amount of DCT coefficients and a stability of algorithm for arbitrarily selected acceptance lane of the spectral trigger rate.

Although 6 surface detectors from the Pierre Auger Observatory have been used for the tests, the spectral trigger is being developed more generally for future ground EAS arrays using - other than the present Pierre Auger Observatory - only one PMT per station.

11. Acknowledgement

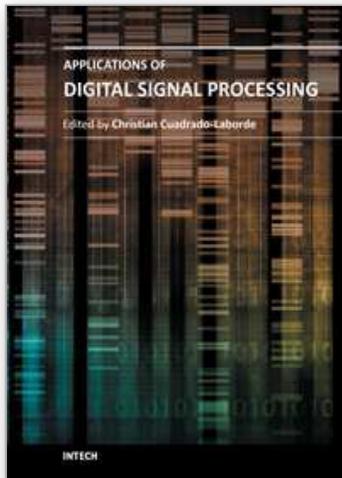
The author would like to thank the Pierre Auger Collaboration for being allowed to use a PAO infrastructure and a test-hexagon and for getting the data made available. The successful installation and preliminary tests of the new Front End Boards with the DCT trigger would

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12. References

- Abraham J., et al., [Pierre Auger Collaboration] (2004). Properties and Performance of the Prototype Instrument for the Pierre Auger Observatory. *Nucl. Instr. Meth.*, Vol. A523, (May 2004) pp. (50-95) ISSN: 0168-9002
- Abraham J. et al., [Pierre Auger Collaboration] (2010). Trigger and aperture of the surface detector array of the Pierre Auger Observatory *Nucl. Instr. Meth.*, Vol. A613, (Jan. 2010) pp. (29-39) ISSN: 0168-9002
- Aglietta M., et. al, (2005). Response of the Pierre Auger Observatory Water Cherenkov Detectors to Muons, *Proceedings of 29th Int. Cosmic Rays Conference*, pp. 100-104, ISBN, Pune, India, Aug. 2005
- Arai Y.; Agui T. & Nakajima M. (1988). A fast DCT-SQ scheme for images. *Trans. IEICE*, Vol. E-71, (Nov. 1988) pp. (1095-1097)
- Szadkowski Z. (2005). The concept of an ACEX[®] cost-effective first level surface detector trigger in the Pierre Auger Observatory *Nucl. Instr. Meth*, Vol. A551, (Oct. 2005) pp. (477-486) ISSN: 0168-9002
- Szadkowski Z.; Becker K-H. & Kampert K-H. (2005). Development of a New First Level Trigger for the Surface Array in the Pierre Auger Observatory based on the Cyclone[™] Altera[®] FPGA. *Nucl. Instr. Meth*, Vol. A545, (June 2005) pp. (793-802) ISSN: 0168-9002
- Szadkowski Z. (2006). 16-point Discrete Fourier Transform based on the Radix-2 FFT algorithm implemented into Cyclone[™] FPGA as the UHECR trigger for horizontal air showers. *Nucl. Instr. Meth*, Vol. A560, (May 2006) pp. (309-316) ISSN: 0168-9002
- Szadkowski Z. (2009). A spectral 1st level FPGA trigger for detection of very inclined showers based on a 16-point Discrete Cosine Transform for the Pierre Auger Experiments. *Nucl. Instr. Meth*, Vol. A606, (July 2009) pp. (330-343) ISSN: 0168-9002
- Szadkowski Z. (2011). Trigger Board for the Auger Surface Detector with 100 MHz Sampling and Discrete Cosine Transform. *IEEE Trans. Nucl. Science*, Vol. PP 99, (March 2011) pp. (1-9) ISSN: 0018-9499



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In this book the reader will find a collection of chapters authored/co-authored by a large number of experts around the world, covering the broad field of digital signal processing. This book intends to provide highlights of the current research in the digital signal processing area, showing the recent advances in this field. This work is mainly destined to researchers in the digital signal processing and related areas but it is also accessible to anyone with a scientific background desiring to have an up-to-date overview of this domain. Each chapter is self-contained and can be read independently of the others. These nineteenth chapters present methodological advances and recent applications of digital signal processing in various domains as communications, filtering, medicine, astronomy, and image processing.

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