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MATLAB Co-Simulation Tools for Power Supply Systems Design

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1. Introduction

Modern electronic devices could be thought as the collection of elementary subsystems, each one requiring a regulated supply voltage in order to perform the desired function. Actually, in a system board you can find as many as ten separate voltage rails, each one rated for a maximum current and current slew-rate. If the available energy source is not suitable for the specific application, a power supply system is required to convert energy from the available input form to the desired output. Since power-up, power-down sequences and recovery from multiple fault conditions are usually offered, monitoring and sequencing the voltage rails is quite complex and a central power management controller is used. The design of the power management system is a key step for a successful conclusion of the overall design. The cost, size and volume of the electronic device are heavily affected by the power supply performances. The proliferation of switching converters throughout the electronic industry is a matter of fact. Unlike linear regulators, switching converters are suitable for both reducing and increasing the unregulated input voltage and efficiency can be as high as 97%. Classification of switching power supplies is mainly based on the available input energy form and the desired output: AC-AC cycle conversion: alternate input, alternate output; AC-DC rectification: alternate input, continuous output; DC-AC inversion: continuous input, alternate output; DC-DC conversion: continuous input, continuous output. Several topologies are well suited to perform the required conversion (Erikson et al., 2001; Pressman et al., 2009). Independently of the specific topology, the architecture of a power supply system can be generalized as shown in Fig.1. A power section and a control section are highlighted. The switching converter is included in the power section while the feedback network and protection circuits for safe operation are collected in the control system. Mainly because of the growing interest in digital controllers, a power supply system can be modelled as a complex system, quite often involving both digital and analog subsystems. If compared to their analog counterparts, digital controllers offer lower power consumption, higher immunity to components aging and higher and higher design flexibility. The control algorithm is often described at a functional level using hardware description language, as VHDL or Verilog. ASICs or FPGA based controllers are usually integrated by the means of sophisticated simulation, synthesis and verification tools. Time to market is heavily reduced by the means of powerful simulation environments and accurate system modelling. Achieving high accuracy models for mixed-mode systems is quite difficult. Specific simulation tools are available on the market, each one oriented to a specific

abstraction level. Circuit simulation software as *Powersim PSIM* and *Orcad Pspice* are the most common choice for circuit modelling. In (Basso, 2008), the design and simulation of switch-mode power supplies is deeply analyzed and simulation tips in several environments are proposed. ASIC simulation and verification tools as Xilinx ISE/Modelsim or Aldec Active-HDL are available to implement the digital controller by the VHDL or VERILOG source code. Since the interaction between subsystems is the most common source of faults, testing separately analog and digital subsystems by the means of different verification tools is a severe mistake. Matlab is a powerful simulation environment for mixed-mode systems modelling and simulation, providing several tools for system co-simulation (Pop, 2010; Kaichun et al., 2010). The Matlab suite offers co-simulation tools for *PSIM*, *Modelsim* and *Active-HDL* simulation environments. Ideally, modelling the power converter by a circuit implementation in PSIM environment and the digital controller by the VHDL code in *Xilinx ISE* or *Active-HDL* environment allows the designer to test the composite system in Matlab environment using co-simulation procedures. Unfortunately, the use of several co-simulation tools in the same Simulink model heavily reduces the processing speed. As an example, in this chapter the Simulink model of a multiphase dc-dc converter for VRMs applications is described. The control system is described by VHDL language and the controller model is implemented in *Active-HDL* environment. For the highest processing speed, an alternative modelling technique for the power section is proposed by the means of elementary library blocks, avoiding *PSIM* co-simulation and not affecting the accuracy of behavioural simulations. As shown by simulation results, the high accuracy relies in the opportunity to match the system behaviour both within the switching event and during long-time events such as load transients and start-up. The great potential of the co-simulation procedure for mixed-mode systems is highlighted by the comparison between simulation and experimental results.
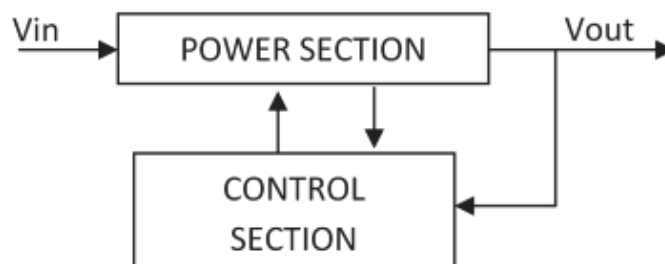

Fig. 1. Power supply system architecture.

2. Multiphase dc-dc converters for VRM applications

The evolution in microprocessor technology poses new challenges for power supply design. The end of 2009 marked the birth of 32nm technology for semiconductor devices, and 22nm is expected to be reached in the 2011-2012 timeframe. The next generation of computer microprocessors will operate at significantly lower voltages and higher currents than today's generation in order to decrease the power consumption and increase the processing speed. Within several years, Intel cores are expected to operate on a 0.8V supply voltage. High-quality power is delivered to the microprocessor by a point-of-load (POL) converter, also known as voltage regulator module (VRM), which is located on the motherboard next to the load. Embedded POL converters are designed to supply a tight regulated output voltage in the 0.8 – 1.2V range. Due to integration advances and increasing clock frequencies, high current

values, often higher than 100A, are required. VRMs supply highly dynamic loads exhibiting current slew rates as high as 1000A/µs. Today, in distributed power architectures, individual POL converters usually draw power from a 12V intermediate power bus. Lowering the core voltage results in a very narrow duty cycle of the 12V-input converter, worsening the converter efficiency and load transient response. The best topology for VRM applications features tight voltage regulation, very fast transient response, high-current handling capabilities and high efficiency. Modern technology advances constantly prompt electronics researchers to meet all requirements investigating innovative solutions. The evolution from a classical buck topology to multiphase architectures is described to better understand the great advantages brought by multiphase architectures.

The buck topology and the MOSFET gate drive signal are shown in Fig.2. The gate signal period is always referred to as the converter switching period T. The duty-cycle D is defined as the ratio between the MOSFET on-time and the switching period. Since one terminal of the power MOSFET is tied to the high-side of the input voltage rail, the MOSFET is also called high-side MOSFET. The steady-state analysis is here performed assuming constant the input voltage and the output voltage during a switching period.
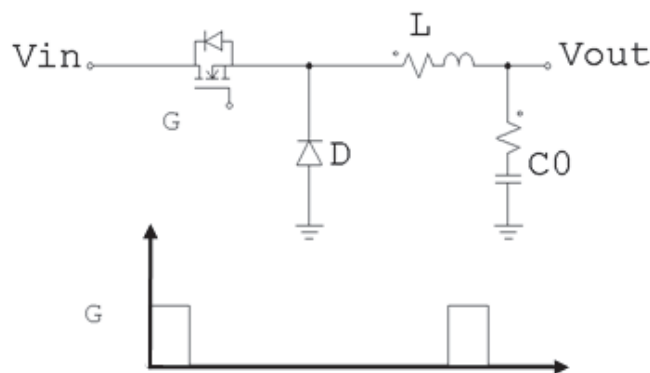

Fig. 2. The buck converter topology and gate drive signal.

On the rising edge of the gate drive signal, the high-side MOSFET is turned on. The inductor is now series connected between the input and output rails and the diode is reverse biased. During the MOSFET on-time, the inductor current slope is constant and it can be expressed as:

$$s_{on} = \frac{Vin - Vout}{L} \tag{1}$$

On the falling edge of the gate drive signal, the MOSFET is turned off. The inductor opposes the current break trying to maintain the previously established current. The voltage polarity across it immediately reverses. Since the right terminal of the inductor is tied to the output rail, the cathode voltage of the diode D is driven toward negative values. When zero crossing occurs, the diode D is forced into conduction clamping the cathode node to ground. The inductor voltage is now reversed and full inductor current flows through the diode D.

The inductor is now connected in parallel to the output voltage rail. During the OFF-time, the slope of the inductor current is given by:

$$s_{off} = \frac{-Vout}{L} \tag{2}$$

Under steady-state conditions, the average inductor voltage over a switching period is zero, resulting in the expression:

$$(Vin - Vout) \cdot T_{on} = -Vout \cdot T_{off} \tag{3}$$

Or

$$Vout = Vin \cdot \frac{T_{on}}{T_{on} + T_{off}} \tag{4}$$

where Ton is the MOSFET conduction time and Toff the MOSFET off-time.

As shown in Fig.3 the inductor undergoes a magnetizing cycle over the entire switching period. The inductor current ripple could be expressed as:

$$\Delta I_L = \frac{Vin - Vout}{L} \cdot T_{on} = \frac{-Vout}{L} \cdot T_{off} = \frac{Vin(1 - D)D}{L} T \tag{5}$$

where D is the duty cycle and T the switching period.
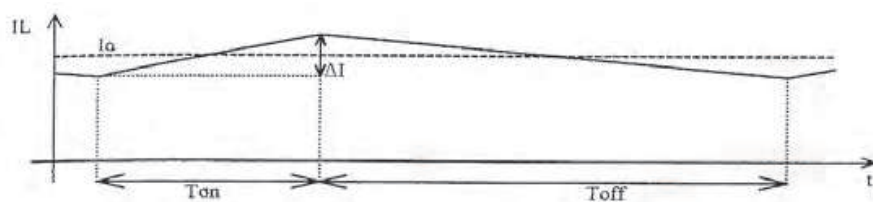
Fig. 3. The inductor current waveform over the switching period under steady-state conditions.

Since at steady-state the average capacitor current is null, the average inductor current is equal to the load current. The ac component of the inductor current flows through the parallel connection between load and capacitor. Commonly, the capacitor is large enough to assume that its impedance at the switching frequency is much smaller than the load resistance. Hence nearly all the inductor current ripple flows through the capacitor. The ac current flowing into the load could be reasonably neglected. A continuous conduction mode is assumed. The inductor is sufficiently large to assume:

$$\frac{\Delta IL}{2} \ll I_{out} \tag{6}$$

The inductor current never crosses zero during the switching period. A continuous conduction mode is preferred in high-current applications since lower and lower conduction power losses are involved.

The capacitor current waveform is shown in Fig.4. When the capacitor current is positive, the stored charge as well as the capacitor voltage will increase. Vice versa, when the capacitor current goes negative, stored charge will be released and the output voltage will decrease as well.

The total voltage change occurs between two consecutive zero-crossings of the capacitor current. Evaluating the total charge q as the grey-coloured area in Fig.4 yields:

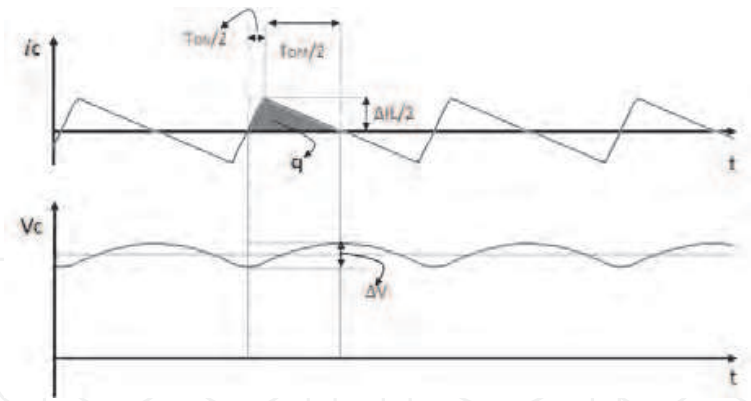$$q = \frac{1}{2} \frac{\Delta I_L}{2} \frac{T}{2} \tag{7}$$

Fig. 4. At the top, the output capacitor current. At the bottom, the output voltage.

The voltage ripple across the output capacitor is given by:

$$\Delta V = \frac{q}{C} = \frac{\Delta I_L T}{8C}$$

(8)

Increasing the output capacitor value or the switching frequency directly improves the output voltage regulation. If a larger inductor is selected, the ripple current would decrease as well as the output voltage ripple. Yet, by increasing the inductor value the load transient response is worsened. A load transient could be modelled by the equivalent circuit shown in Fig.5.
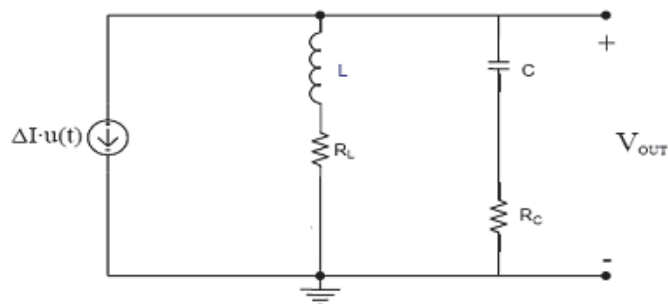
Fig. 5. The equivalent circuit under large-signal load transients.

The load transient is modelled as an ideal current step. Since the input voltage is assumed constant, the switching node is dynamically tied to ground. The inductor is thus parallel connected to the output capacitor filter. If the loop response is sluggish, the peak output voltage deviation $\Delta V_{out,max}$ tends to approach the open-loop value which is given by:

$$\Delta V_{out,max} = \Delta I \cdot \sqrt{\frac{L}{C}} + Rc \cdot \Delta I$$

(9)

where ΔI is the current step width and Rc the equivalent series resistor of the output capacitor.

In Fig.6 the load current *Iload*, the inductor current *IL*, the capacitor current *Ic* and the output voltage V*out* under a load transient are shown. By increasing the output capacitor value, the dynamic response could be further improved. Yet, in high-current applications a too large capacitance will be obtained affecting the system cost and size.
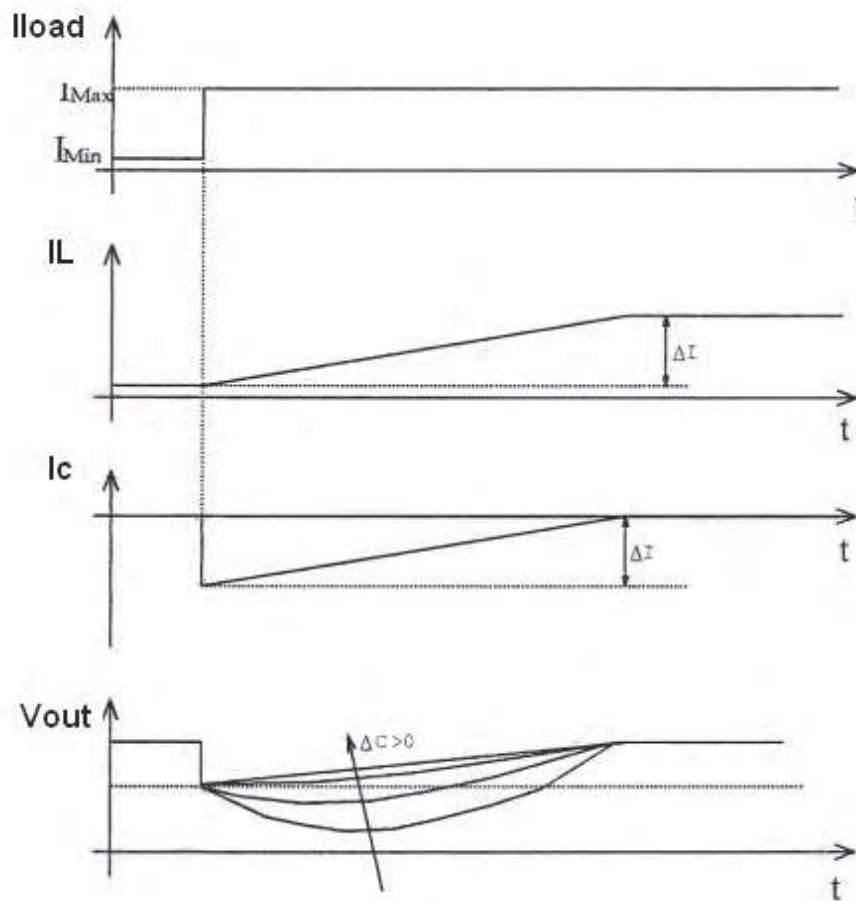
Fig. 6. The converter waveforms under a large-signal transient.

The optimization of steady-state and dynamic performances leads to a trade-off in the choice of the inductor value. As will be further discussed, the inductor value is usually chosen to meet steady-state requirements and dynamic performances are improved by the control algorithm.

As shown by (4), the buck converter reduces the dc input voltage by the means of switching elements. Power loss due to switches is ideally zero. Yet, switches are not ideal. Further, switching losses cannot be neglected. The inductor current flows through the MOSFET during the on-time and through the diode during the OFF time. Conduction losses are proportional to the forward voltage drop across the active elements. The MOSFET forward voltage drop is lower than the diode threshold voltage. In a buck converter, conduction losses are mainly due to the freewheeling diode.

In high-current low-voltage applications, synchronous rectification is widely used to improve efficiency. As shown in Fig.7, the diode D is replaced by a MOSFET featuring a very low forward voltage drop. The rectification function, typically performed by diodes, is now achieved by the means of a MOSFET which is driven synchronously with the high-side MOSFET. For this reason, the added MOSFET is sometimes referred to as the synchronous rectifier MOSFET. Since the rectifier MOSFET source terminal is tied to the low-side of the input voltage rail, the MOSFET is also called low-side MOSFET. If compared with classical topology, synchronous rectification heavily reduces conduction losses improving efficiency. During the conduction time of the high-side (on time) the low-side is off and vice versa.
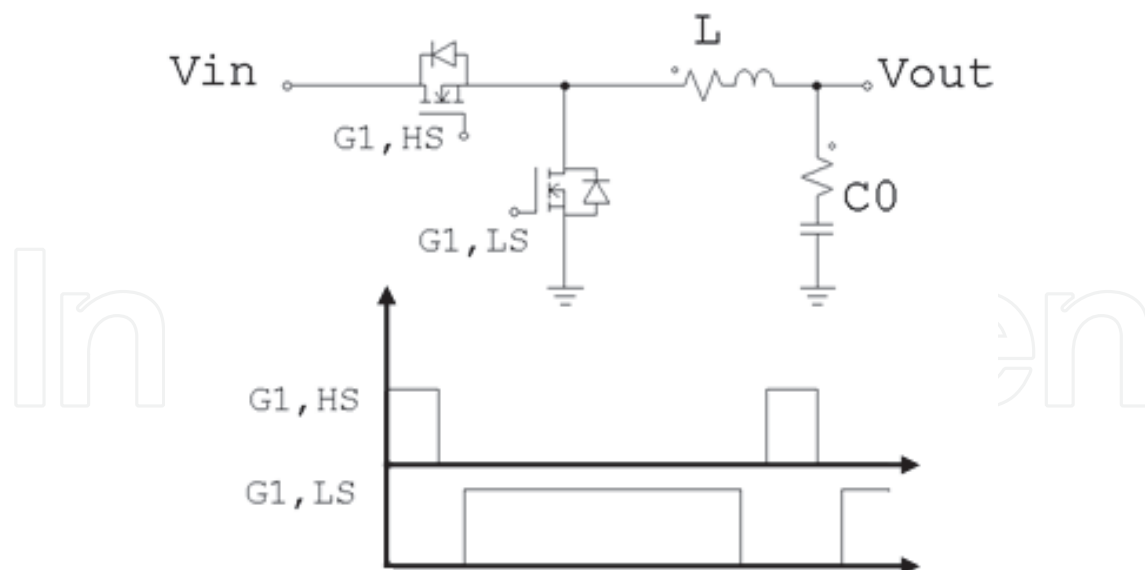
Fig. 7. The synchronous buck topology and MOSFETs gate drive signals.

A dead-time is required to avoid the simultaneous conduction of high-side and low-side MOSFETs. During the dead time, neither the low-side nor the high side MOSFET is on. When the high-side MOSFET is turned off, the inductor opposes the current break forcing the low-side MOSFET body-diode into conduction. Over the entire dead time the full inductor current flows through the body diode itself. At the end of the dead time, the low-side MOSFET is turned on, the body diode is bypassed by the active MOSFET channel and the inductor current flows through the low-side MOSFET channel. During the dead time, classical and synchronous topologies are exactly alike. It would be advisable a further reduction of both the diode threshold voltage and the dead time in order to limit power losses. A Schottky diode is often integrated in parallel to power MOSFET: the body diode will be bypassed by the Schottky diode over the entire dead time lowering the effective threshold voltage. A minimization of the low-side body-diode conduction time is required to take advantage from synchronous rectification. Sophisticated dead-time control algorithms are usually implemented by synchronous MOSFET drivers. If a single buck converter topology were employed in high-current applications, a large amount of output-filter and on-board decoupling capacitance would be required to achieve the expected transient response. The size and cost of the voltage regulator would increase as well. Multi-phase converters are widely used. Ripple cancellation and improved transient response are only a few advantages of multi-phase architectures. A detailed analysis of multiphase converters is reported in (Miftakhutdinov, 2001). In N-modules architecture, N identical buck converters are connected in parallel to the load resulting in a heavy reduction of the output ripple. Smaller inductances are allowed thus improving the transient response. Note that increasing the number of modules emphasizes the advantages of a multiphase architecture. Gate drive signals are interleaved to take full advantage from the multiphase architecture. Assume that each channel operates at a switching frequency f_{sw}. Under steady-state conditions, the phase shift between gate drive signals of each module depend on the number of interleaved channels. If an N-channels architecture is considered, assume that the control signal sequence is Phase 1, 2,.., N. The interleaved technique requires a 360°/N phase shift between two following channels. The maximum number of channel is limited by the relationship:

$$(1 - D) > N \cdot D \qquad (10)$$

where N is the number of channel and D is the duty-cycle. A key feature of multiphase architecture is now highlighted: the ripple frequency of the output voltage is N-times the switching frequency of each power module. The equivalent switching frequency is higher and higher than the effective switching frequency of each module. The designed multiphase converter features a 4-modules architecture, as shown in Fig.8. Inductors and capacitors are modelled including the parasitic equivalent series resistance. Assume that the control sequence is Phase 1,2,3,4. Interleaved gate drive signals are shown in Fig.9. Fig.10 shows the inductor current waveforms for each buck channel. As shown in Fig.11, the equivalent current is defined as:

$$IL_{eq} = \sum_{i=1}^{n} IL_i = IL_1 + IL_2 + IL_3 + IL_4 \qquad (11)$$

Ripple cancellation derives from the interleaving technique. The steady-state analysis is carried on within a fundamental Tsw/4 time interval. Within a Tsw/4 period, only one module could be driven in the ON state, the others are constantly OFF. For example, from 0 to Tsw/4 modules 2, 3 and 4 are constantly OFF while the first module (phase 1) is driven in the ON state during the subinterval [0, DTsw/4]. No matter which phase is active in the ON state, the fundamental period of the output waveforms is Tsw/4 since we have assumed identical modules.
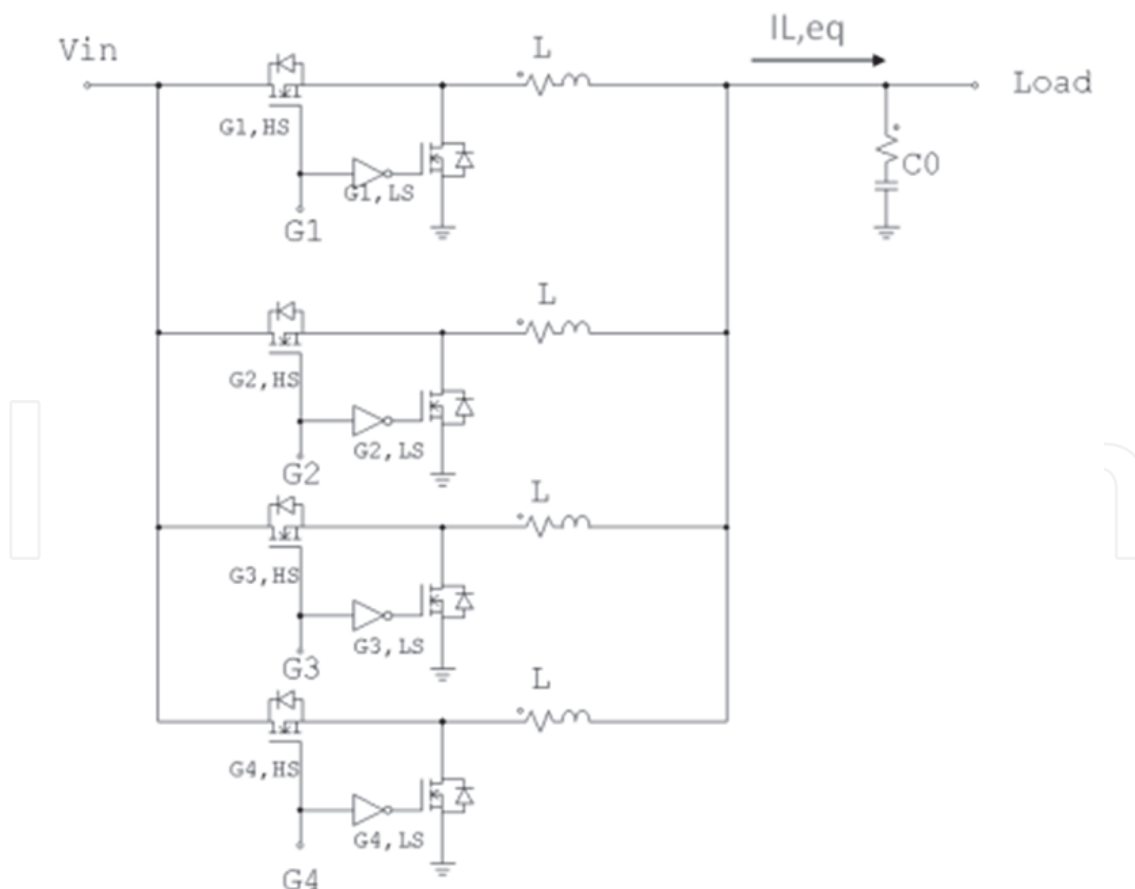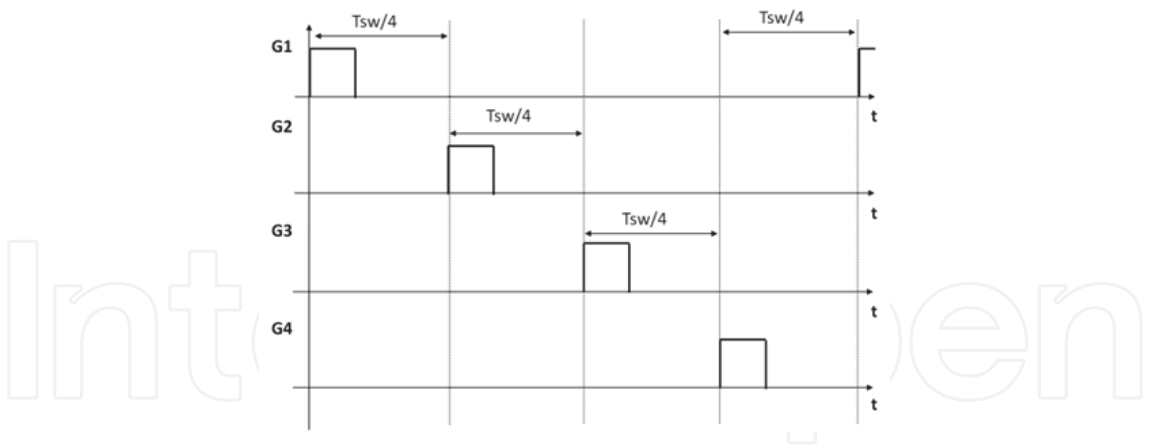

Fig. 8. Multiphase architecture.

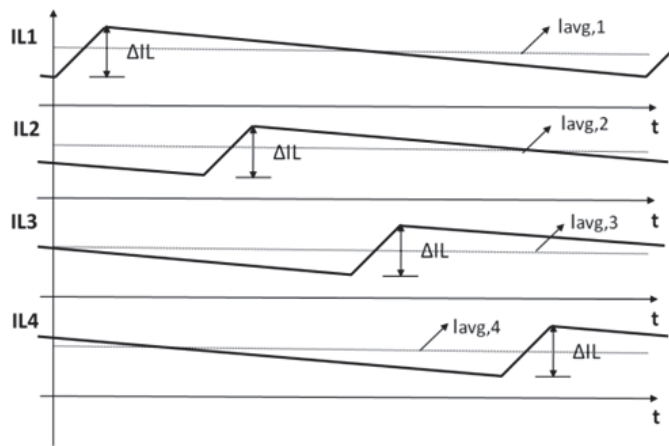Fig. 9. High-side MOSFETs gate drive signals.

Fig. 10. Inductor current waveforms under steady-state conditions.
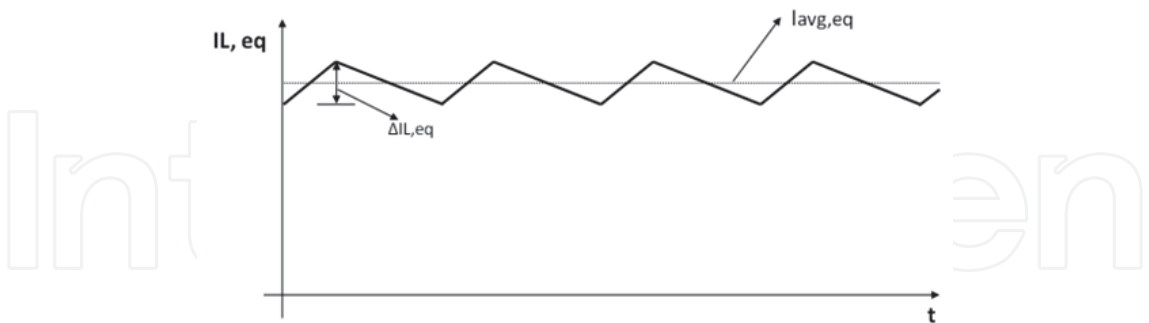

Fig. 11. Equivalent inductor current under steady-state conditions.

Within the time interval [0, DTsw/4] the slope of the equivalent current is given by:

$$s_{eq,on} = \frac{Vin - Vout}{L} - (N-1)\frac{Vout}{L} = \frac{Vin(1 - ND)}{L} \qquad (12)$$

The equivalent slope is positive during the first subinterval. During the second subinterval [DTsw/4,Tsw/4] all modules are driven OFF. The equivalent current slope is negative according to the equation:

$$s_{eq,off} = -N\frac{Vout}{L} \tag{13}$$

The equivalent current ripple is given by:

$$\Delta I_{L,eq} = \frac{Vin(1-ND)D}{L}T_{sw} = \frac{\Delta IL\,(1-ND)}{(1-D)} \tag{14}$$

As (14) states, in a multiphase architecture the current ripple is cancelled. If compared with classical buck converters, the current ripple is reduced by (1-ND)/(1-D). Moreover, the equivalent switching frequency as seen by the power load is N times the operating switching frequency of each power module.

Note that (14) could be expressed as:

$$\Delta I_{L,eq} = \frac{Vin(1-ND)D}{L}T_{sw} = \frac{Vin(1-ND)DN \cdot N}{N \cdot N\,L}T_{sw} = \frac{Vin,eq(1-Deq)Deq}{Leq}T_{sw,eq} \tag{15}$$

where N is the number of modules and $Deq = N \cdot D$, $fsw,eq = N \cdot fsw$, $Leq = \frac{L}{N}$, $Vin,eq = \frac{Vin}{N}$.

By comparing (15) and (5), conclusions are drawn: a N-modules architecture is equivalent to a buck converter operating at $f_{sw,eq}$ switching frequency, D_{eq} duty-cycle, supplied by $V_{in,eq}$ input voltage and featuring L_{eq} inductance. Then, if compared with a buck converter fed by the same input voltage rail and supplying the same voltage bus, the multiphase architecture features higher switching frequency, higher duty-cycle and lower inductance. Both steady-state and dynamic performances of the switching regulator take a great advantage from these interesting properties. With regards to steady-state performances, tight voltage regulation could be achieved thanks to the ripple cancellation effect. Dynamic performances are greatly improved by the reduction of the equivalent inductor under load transients. The steady-state and dynamic performances of multiphase converters are affected by the duty cycle value. A narrow duty cycle results in a poor ripple cancellation. Hence, a larger inductance should be selected to keep tight voltage regulation worsening the transient response. If a wide input-output voltage range is considered, a proper design of passive components is not yet suitable for speeding up the system performances. Multiphase architectures achieving a duty cycle extension by the means of coupled inductors are frequently proposed in literature.

Otherwise, unconventional control algorithms are proposed to speed up the transient response not affecting the passive components design.

3. The control system

A survey of the control algorithm is given to highlight the system complexity and high accuracy of simulation results. Authors suggest (Boscaino et al., 2009) for further details. A linear-non-linear digital controller oriented to IC implementation, improving both steady-state and transient response is presented. A schematic block diagram of the linear loop is shown in Fig.12.

A Pulse Width Modulation (PWM) current-mode control is implemented. Two 10 bits/2V ADCs and a 12 bits /5V DAC are included in the analog-digital interface. The output voltage is converted to digital and compared to a reference voltage V_{ref}. The error signal

COMP_OUT is generated by the error amplifier which includes the adder and the *COMP* block. A type-2 compensation action is digitally implemented to ensure system stability. The error signal is then converted to analog and compared to the current sense signal of each power module Vc2,i.
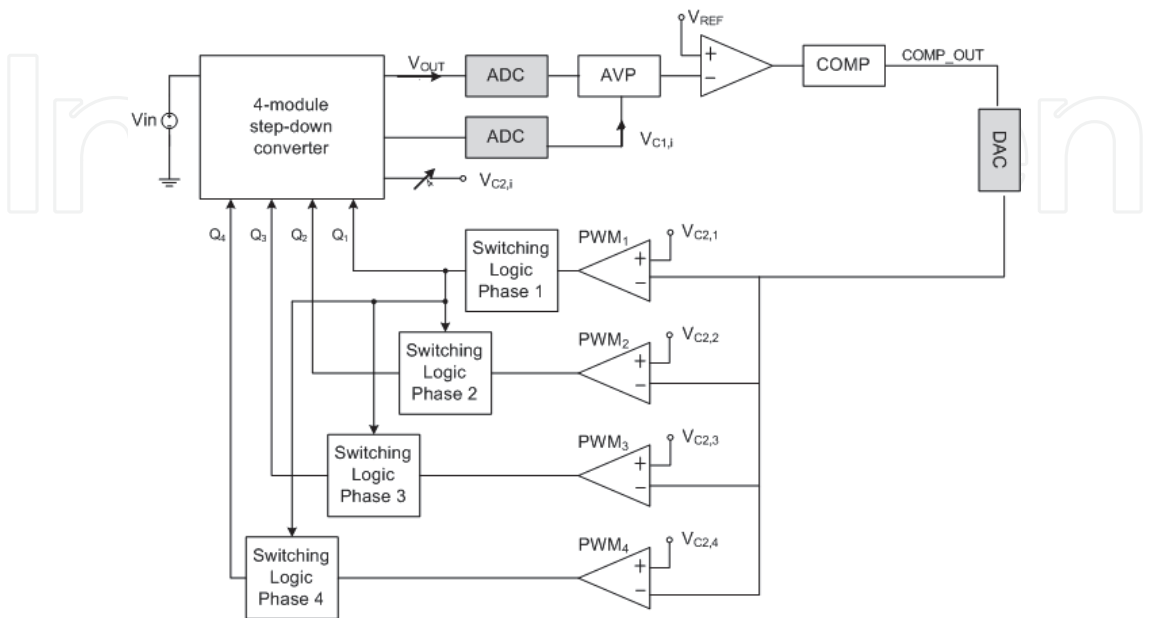

Fig. 12. Schematic block diagram of the linear controller.

The gate drive interleaved technique is digitally implemented by the *Switching logic* subsystems. The master module is the Phase 1, the others slave. Fig.13 shows the switching logic algorithm for the master power module. A clock signal at the switching frequency is synchronously derived from the system clock. The switch-on of the high-side MOSFET is triggered by the rising-edge of the switching clock Ck1. The high-side MOSFET switch-off is triggered by the rising-edge of the corresponding PWM signal.
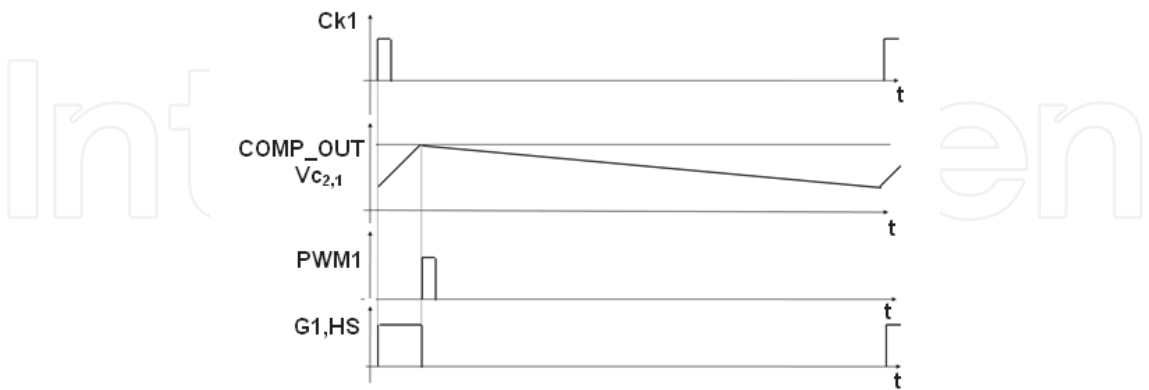
Fig. 13. Switching logic for the master module.

A digital counter generates a switching clock for each slave module which is synchronous with the master switching clock and phase-shifted according to the interleaved technique.
The sense signal $V_{c2,i}$ reproduces the instantaneous inductor current of the *i-th* power module. RC networks are used to sense the instantaneous inductor current of each power

module. As shown in Fig.14, a RC filter is connected across the low-side MOSFET of each power module. The capacitor voltage V_{c2} is the sense signal for current-mode control implementation.
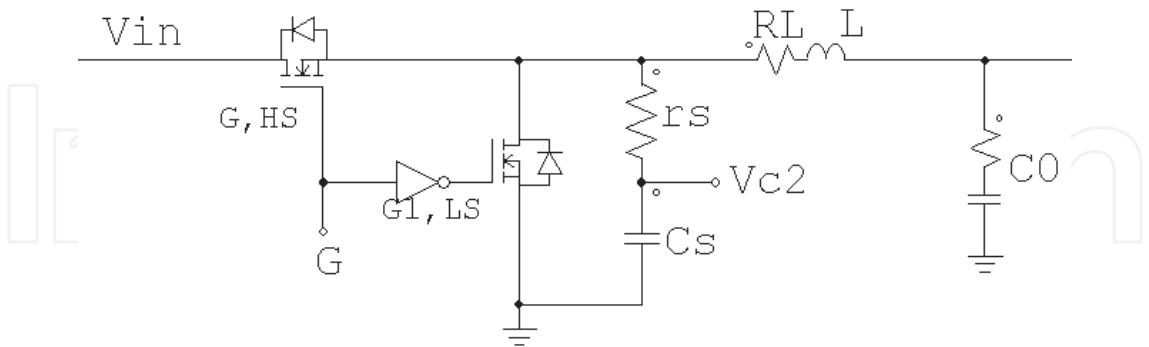

Fig. 14. Current sense network.

The period $T=r_sC_s$ is fixed according to the equation:

$$D_{max}T_{sw} \ll T \tag{16}$$

where T_{sw} is the switching period and D_{max} the maximum operating duty-cycle. The charge and discharge of the capacitor C_2 within the switching period reproduces the charge and discharge of the inductor L. The average value of the sense signal is given by:

$$\overline{V_{c2}} = Vout + \overline{I_L}R_L \tag{17}$$

where $\overline{I_L}$ is the average inductor current and R_L the ESR of the inductor L.
The superimposed ripple is given by:

$$\Delta V_{c2} = R_v\Delta I_L \tag{18}$$

where ΔI_L is the inductor current ripple and R_v the virtual sensing resistor which is given by:

$$R_v = \frac{L}{r_sC_s} \tag{19}$$

The current-mode control is implemented by the Vc2 sense signal. A detailed analysis of the proposed current-sensing technique, including design guidelines is reported in (Boscaino et al., 2008).
Another RC network featuring a lower cut-off frequency is connected across the switching node of the master phase. The sense capacitor voltage V_{c1} reproduces the average inductor current. V_{c1} is converted to digital and feeds the *AVP* subsystem which implements the well-known Adaptive Voltage Positioning (AVP) technique. Fig.15 shows the output voltage and the load current waveforms under a load current step without AVP. The maximum tolerance window on the output voltage is given by:

$$\Delta V_{out,max} = 2 \cdot \Delta I_{o,max}Rc \tag{20}$$

With the AVP technique, the reference voltage becomes a function of the load current according to the following equation.
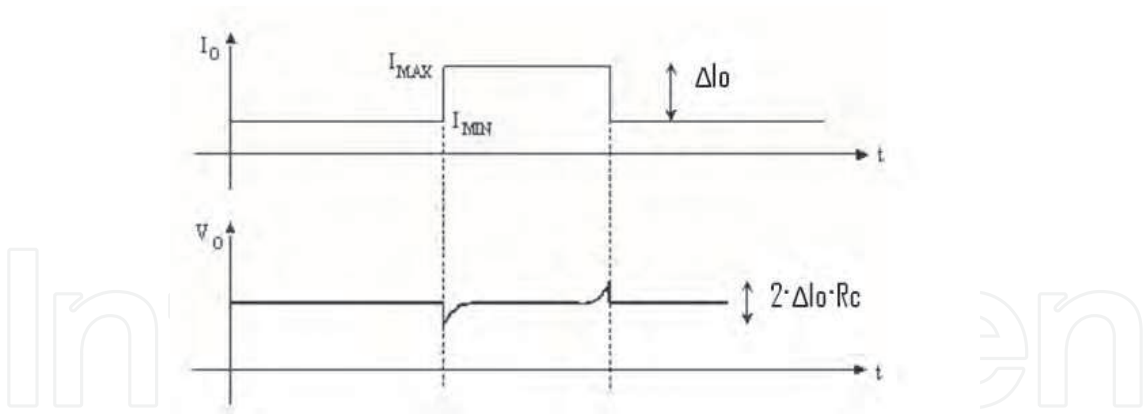
Fig. 15. Dynamic response under load transients. At the top the load current step, at the bottom, the output voltage waveforms are shown.

$$v'_{ref} = V_{ref} - I_o Rc \tag{21}$$

where, v'_{ref} is the variable reference voltage, V_{ref} is a fixed reference voltage, I_o is the load current and R_c is the equivalent series resistor of the output capacitor. The DC set point of the output voltage changes accordingly to the output current, as shown in Fig.16. At steady-state, the output voltage is forced by the AVP technique to the variable reference voltage, instead of a fixed value V_{ref} . Under high-load conditions, the DC set point drops in the lower part of the allowable tolerance window. The maximum tolerance window is now given by:

$$\Delta V_{out,max} = \Delta I_{o,max} Rc \tag{22}$$

The technique results in added margin to handle load transients. Since the load current is equal to the average inductor current, the AVP technique is implemented by sensing the average inductor current of the master phase.
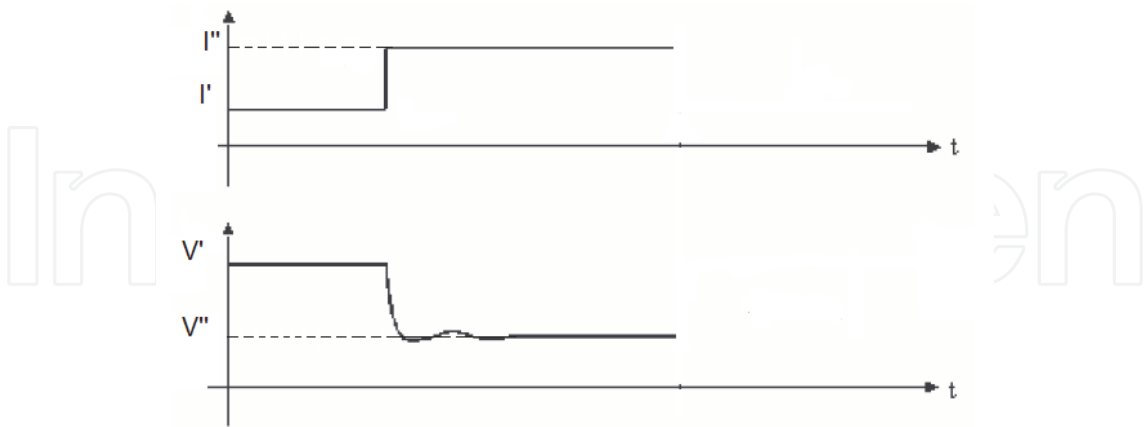

Fig. 16. The dynamic response to a load current step with Adaptive Voltage Positioning.

A non-linear control is introduced to speed-up the transient response not affecting steady-state performances. During transients, the non-linear control modifies a few linear loop parameters, as the reference voltage or the duty-cycle. Since the converter output voltage is the only non-linear loop input, the proposed technique can be efficiently applied to each power supply

system independently of the specific converter topology and linear loop architecture. Thanks to the AVP technique, load transients are detected by an instantaneous drop of the output voltage, and the increasing or decreasing load current transient is detected by monitoring the output voltage drop in terms of sign and width. Two different non-linear control actions are implemented: under a load current increase (*case a*) or decrease (*case b*). The reference voltage (*case a*) or the duty-cycle (*case b*) is modified by the non-linear control loop. Under increasing load current steps, the non-linear control loop acts on the reference voltage advancing the linear loop action. Two auxiliary signals, V_{VAR} and V_{LOOP}, are defined: V_{VAR} is the output voltage value related to the new steady-state condition while V_{LOOP} is the output voltage ripple during transient referred to V_{VAR} value, as shown in Fig.17.

$$V_{LOOP} = Vout - V_{VAR} \tag{23}$$

$$v'_{ref} = V_{ref} - V_{LOOP} \tag{24}$$

In order to achieve the fastest transient response, the gain factor K_{NL} is introduced. Hence, v'_{REF} is given by:

$$v'_{ref} = V_{ref} - K_{NL}V_{LOOP} \tag{25}$$

The K_{NL} value is designed by the frequency response analysis to ensure the fastest effective gain under transients avoiding loop instabilities. Under transients, the difference between the output voltage and V_{VAR} is monitored and compared with the maximum steady-state output voltage ripple V_{OUT_STEADY}. If the condition (26) is continuously verified over T_{STEADY} time, the non-linear control action ends.

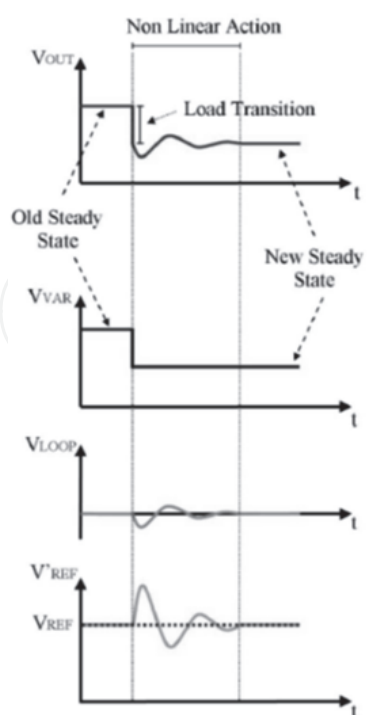$$Vout - V_{VAR} < \Delta V_{OUT\_STEADY} \tag{26}$$

Fig. 17. Non linear control signals under a load current increase.

Under a load current decrease, the non-linear control loop modifies the duty-cycle signal, as shown in Fig.18. All modules are simultaneously turned off to allow the inductor current to decrease as fast as possible. Turning off all modules allows the fastest transient response. Unfortunately, the system is driven towards a loop upsetting and thus to an increase, instead of a reduction, of the output voltage over-and-under shoots. Then, a fixed duty-cycle is forced to all modules according to the interleaved technique. Known the V_{VAR} value, the new steady-state duty-cycle is evaluated and forced by the non-linear subsystem to maintain a regulated output voltage during linear loop resettling. The false steady-state period is a tunable parameter to achieve high design flexibility.

$$D_{NL} = \frac{Vout + \overline{I_L}R_L}{Vin} \tag{27}$$

where Vout is the regulated output voltage, $\overline{I_L}$ is the average inductor current of a single module, R_L the inductor parasitic resistance and Vin the converter input voltage.
From (27), defining the K_R constant as:

$$K_R = \frac{4R_L}{Rc} \tag{28}$$

the forced D_{NL} value is obtained:

$$D_{NL} = \frac{V_{VAR} + (Vout_{I=0} - V_{VAR})K_R}{Vin} \tag{29}$$

The duty-cycle value is evaluated by the non linear controller by the means of fixed parameters and the V_{VAR} value which is obtained by monitoring the output voltage. The difference between the output voltage and V_{VAR} is monitored and compared to the maximum steady-state output voltage ripple V_{OUT_STEADY}. If the condition (30) is continuously verified over a fixed T_{FSS} time, the non-linear control action ends.

$$Vout - V_{VAR} < \Delta V_{OUT\_STEADY} \tag{30}$$

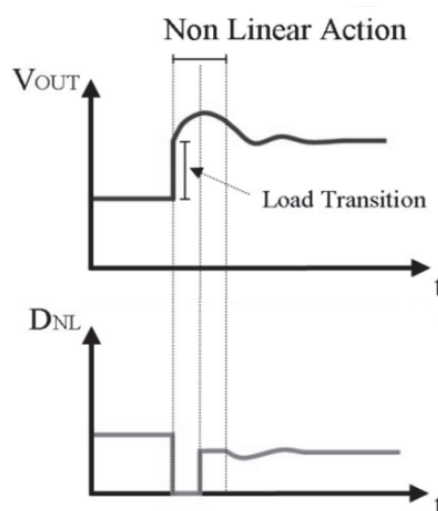Further design guidelines could be found in (Boscaino et al. 2009, 2010).

Fig. 18. The output voltage and the forced duty-cycle value under a load current decrease.

4. Co-simulation set-up

Active-HDL provides an interface to MATLAB/Simulink simulation environment which allows co-simulation of functional blocks described by using hardware description languages. The digital controller is tested on a FPGA device. A specific co-simulation procedure should be activated in order to make each VHDL design unit available in Simulink libraries. The VHDL code and signal timing are tested as well. High-accuracy simulation results are obtained heavily reducing experimental fault conditions. The co-simulation procedure features automatic data type conversion between Simulink and Active HDL and simulation results could be displayed in both simulation environments. All VHDL entities are collected in an Active HDL workspace. A MATLAB m-file is generated for each VHDL entity. By right clicking on a VHDL entity, select the option "Generate Block Description for Simulink". The procedure is repeated for each VHDL entity of current Workspace. After generating the m-files, the *Active-HDL Blockset* is available in the Simulink library browser. The *Active-HDL Co-Sim* and *HDL Black-Box* elements are used for system co-simulation. The *Active-HDL Co-Sim* element must be included in the Simulink top level model. The block allows the designer to fix co-simulation parameters. In order to simulate a VHDL entity as an integral part of the current model, a *HDL Black-Box* block should be added and associated to the corresponding m-file by the configuration box. When the model is completed, running simulation from Simulink starts the co-simulation. The connection to the Active-HDL server will be opened and all *HDL Black-Boxes* simulated with the Active-HDL simulator. Input and output waveforms can be analyzed both in Simulink and Aldec environment while internal signal waveforms can be analyzed in Aldec environment only.

5. MATLAB/Simulink model

The top level model is shown in Fig.19. The power section includes the *Multiphase converter* and the *Current-sense* subsystems. In the *A/D converter* subsystem, the Analog-to-Digital interface is modelled by Simulink library elements. The controller is modelled in Aldec Active-HDL environment and each design unit is included in the *Controller* subsystem. The *Active-HDL Co-Sim* block is added to the top level model.

5.1 The power section model

The power section includes the multiphase converter and current-sense filters. A four-module interleaved synchronous buck converter is connected to the power load. The power section is modelled by Simulink library elements in order to achieve the highest processing speed. The use of several co-simulation tools is avoided, keeping at the same time the highest accuracy. In this paragraph, the Simulink model of the multiphase converter based on a continuous-time large-signal model is described. The proposed modelling technique could be efficiently extended to each switching converter.

In Simulink environment, the State-Space block models a system by its own state-space equations:

$$\dot{x} = Ax + Bu$$
$$y = Cx + Du \tag{31}$$

where **x** is the state vector, **u** the input vector and **y** the output vector.

According to (31), the block is fed by the input vector *u* and the output vector *y* is generated. As shown in Fig.20, the designer could enter the matrix coefficients in the parameter box.
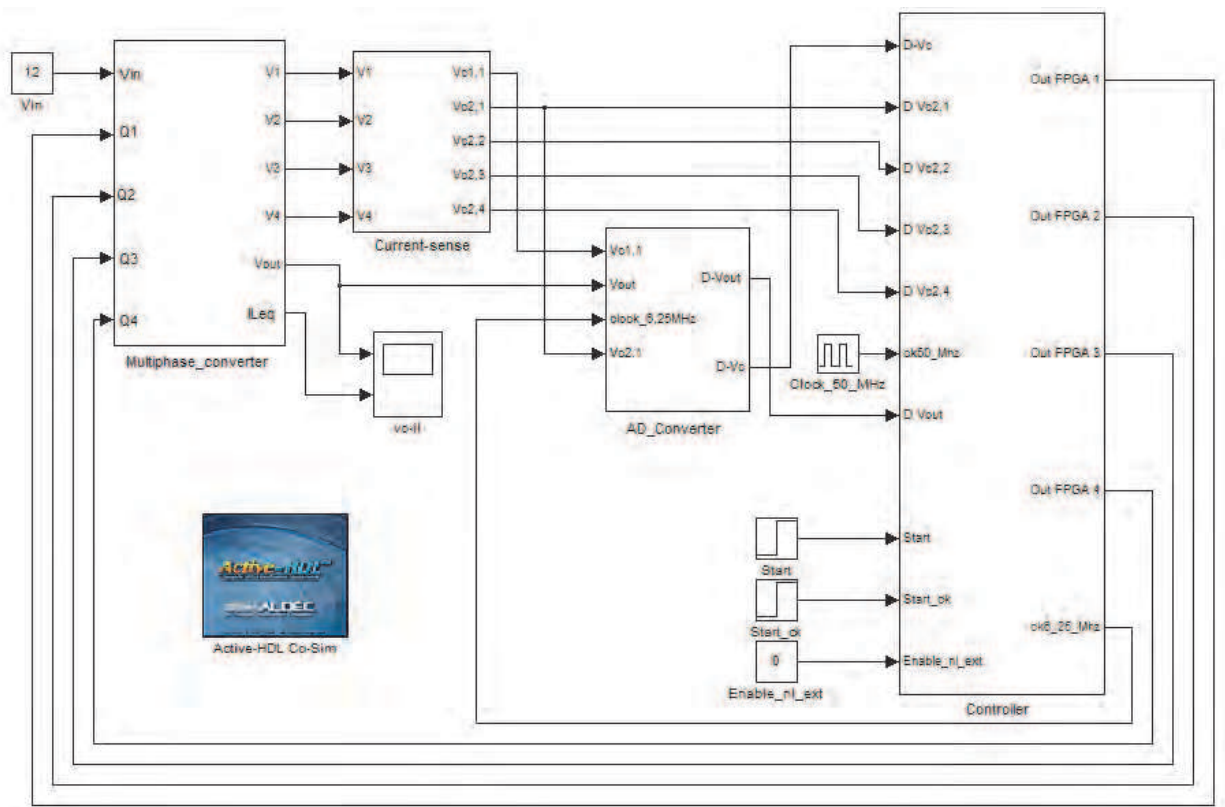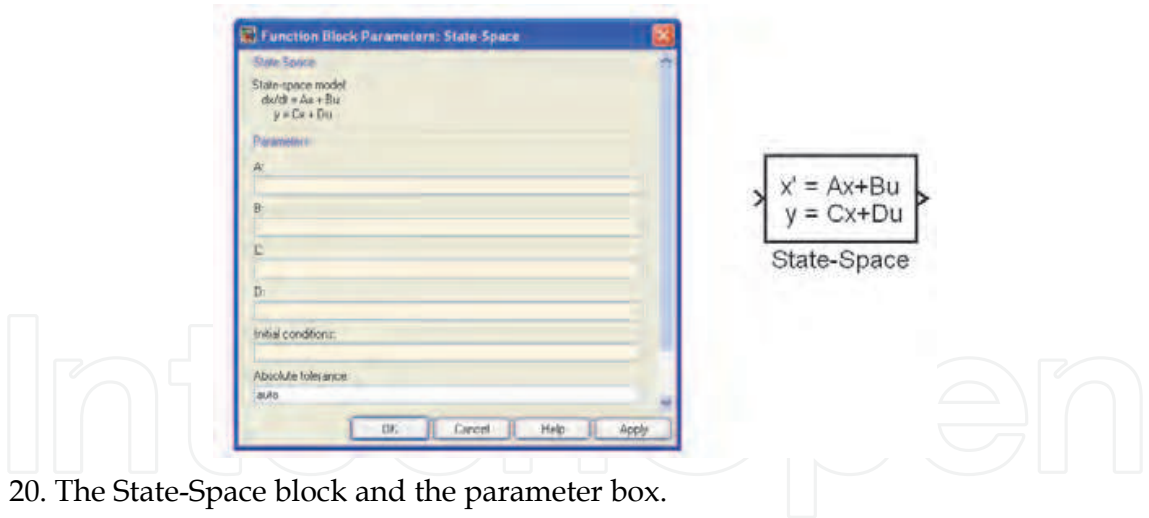
Fig. 19. Top level model

Fig. 20. The State-Space block and the parameter box.

A continuous large-signal model of the buck converter is derived and implemented by the state-space block. The Parasitic components of passive elements as the DC resistance of the inductor (DCR) and the capacitor equivalent series resistor (Rc) are included. Assuming identical MOSFETs, the model accounts for the MOSFET equivalent resistance $R_{ds,on}$. Define a state vector as:

$$\boldsymbol{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{32}$$

where $i_L(t)$ is the inductor current and $v_c(t)$ is the voltage across the output capacitor.
In the proposed model, the output vector is defined as:

$$\boldsymbol{y}(t) = \begin{bmatrix} y_1(t) \\ y_2(t) \end{bmatrix} = \begin{bmatrix} i_L(t) \\ v_{out}(t) \end{bmatrix} \tag{33}$$

where $v_{out}(t)$ is the output voltage and $i_L(t)$ the inductor current.
During the on-time, the buck converter is equivalent to the circuit shown in Fig.21.
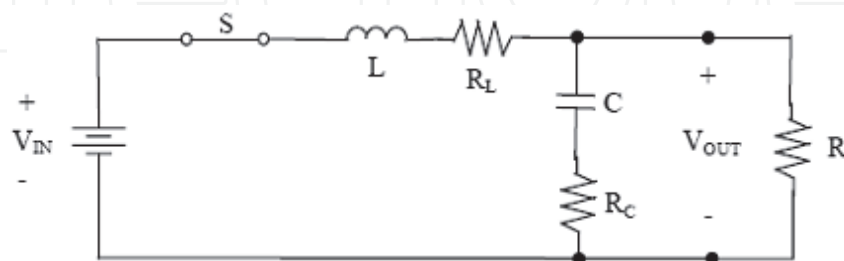
Fig. 21. On-time equivalent circuit.

Both the inductor DCR and the high-side $R_{ds,on}$ are included in the resistance R_L. The analysis of the on-time circuits yields:

$$\begin{cases} L\dot{x}_1(t) + R_cC\dot{x}_2(t) = -R_Lx_1(t) - x_2(t) + Vin \\[2mm] (R_c + R)C\dot{x}_2(t) = Rx_1(t) - x_2(t) \end{cases} \tag{34}$$

The corresponding matrix equation is given by:

$$\begin{bmatrix} L & R_cC \\ 0 & (R_c + R)C \end{bmatrix} \dot{\boldsymbol{x}}(t) = \begin{bmatrix} R_L & -1 \\ R & -1 \end{bmatrix} \boldsymbol{x}(t) + \begin{bmatrix} 1 \\ 0 \end{bmatrix} Vin \tag{35}$$

From (35), the (36) is obtained:

$$\dot{\boldsymbol{x}}(t) = \begin{bmatrix} \dfrac{R_LR_c + R(R_L + R_c)}{(R_c + R)L} & -\dfrac{R}{(R_c + R)L} \\[4mm] \dfrac{R}{(R_c + R)C} & -\dfrac{1}{(R_c + R)C} \end{bmatrix} \boldsymbol{x}(t) + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} Vin \tag{36}$$

The OFF-time equivalent circuit is shown in Fig.22. Both inductor DCR and low-side $R_{ds,on}$ are included in R_L resistance.
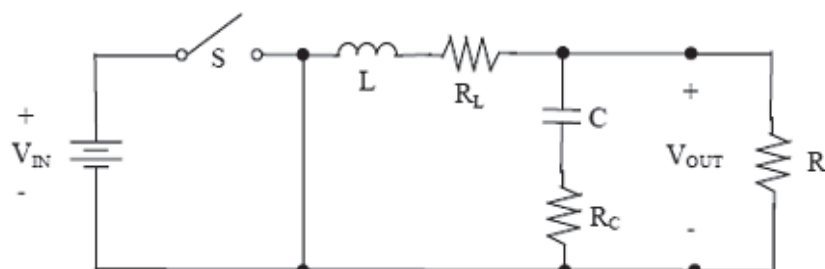

Fig. 22. OFF-time equivalent circuit

The analysis yields:

$$\begin{cases} L\dot{x}_1(t) + RcC\dot{x}_2(t) \doteq -R_L x_1(t) - x_2(t) \\ \\ (Rc + R)C\dot{x}_2(t) = Rx_1(t) - x_2(t) \end{cases} \tag{37}$$

The corresponding matrix equation is given by:

$$\begin{bmatrix} L & RcC \\ 0 & (Rc + R)C \end{bmatrix} \dot{x}(t) = \begin{bmatrix} R_L & -1 \\ R & -1 \end{bmatrix} x(t) \tag{38}$$

Manipulating (38) the (39) is obtained:

$$\dot{x}(t) = \begin{bmatrix} \dfrac{R_L Rc + R(R_L + Rc)}{(Rc + R)L} & -\dfrac{R}{(Rc + R)L} \\ \dfrac{R}{(Rc + R)C} & -\dfrac{1}{(Rc + R)C} \end{bmatrix} x(t) \tag{39}$$

With regard to the output vector, the analysis of both circuits yields:

$$\begin{cases} y_1(t) = x_1(t) \\ y_2(t) = \dfrac{RcR}{R + Rc} x_1(t) + \dfrac{R}{R + Rc} x_2(t) \end{cases} \tag{40}$$

The corresponding matrix equation is given by:

$$y(t) = \begin{bmatrix} 1 & 0 \\ \dfrac{RRc}{R + Rc} & \dfrac{R}{R + Rc} \end{bmatrix} x(t) \tag{41}$$

The analysis of equivalent circuits results in two linear state-space models. During the on-time, the converter is modelled by state-space equations (42):

$$\dot{x}(t) = \mathbf{A_{on}} \cdot x(t) + \mathbf{b_{on}} \cdot u(t)$$

$$y(t) = \mathbf{C_{on}} \cdot \dot{x}(t) + \mathbf{d_{on}} \cdot u(t) \tag{42}$$

where:

$$A_{on} = \begin{bmatrix} \dfrac{R_L Rc + R(R_L + Rc)}{(Rc + R)L} & -\dfrac{R}{(Rc + R)L} \\ \dfrac{R}{(Rc + R)C} & -\dfrac{1}{(Rc + R)C} \end{bmatrix} \tag{43}$$

$$\mathbf{b_{on}} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \tag{44}$$

$$\mathbf{C_{on}} = \begin{bmatrix} 1 & 0 \\ \dfrac{1}{RRc} & \dfrac{R}{R + Rc} \\ \dfrac{R + Rc}{} & \end{bmatrix} \tag{45}$$

$$\mathbf{d_{on}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{46}$$

During the OFF-time, the converter is modelled as:

$$\mathbf{x}(\dot{\mathbf{t}}) = \mathbf{A_{off}} \cdot \mathbf{x}(\dot{\mathbf{t}}) + \mathbf{b_{off}} \cdot u(\mathrm{t})$$

$$\mathbf{y}(\mathrm{t}) = \mathbf{C_{off}} \cdot \mathbf{x}(\dot{\mathbf{t}}) + \mathbf{d_{off}} \cdot u(\mathrm{t}) \tag{47}$$

where

$$\boldsymbol{A}_{on} = \begin{bmatrix} \dfrac{R_L Rc + R(R_L + Rc)}{(Rc + R)L} & -\dfrac{R}{(Rc + R)L} \\ \dfrac{R}{(Rc + R)C} & -\dfrac{1}{(Rc + R)C} \end{bmatrix} \tag{48}$$

$$\mathbf{b_{off}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{49}$$

$$\mathbf{C_{off}} = \begin{bmatrix} \dfrac{1}{RRc} & 0 \\ \dfrac{RRc}{R + Rc} & \dfrac{R}{R + Rc} \end{bmatrix} \tag{50}$$

$$\mathbf{d_{off}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{51}$$

Note that:

$$\mathbf{A} = \mathbf{A_{ON}} = \mathbf{A_{OFF}}$$

$$\mathbf{C} = \mathbf{C_{ON}} = \mathbf{C_{OFF}}$$

$$\mathbf{b_{OFF}} = \mathbf{0}$$

$$\mathbf{d_{ON}} = \mathbf{d_{OFF}} = \mathbf{0} \tag{52}$$

Define the gate drive signal q(t) as:

$$q(t) = \begin{cases} 1 \ during \ the \ ON \ time \\ 0 \ during \ the \ OFF \ time \end{cases} \tag{53}$$

With the aid of q signal, a new input signal is defined as:

$$u(t) = q(t) \cdot Vin \tag{54}$$

A unique state-space model is thus obtained:

$$\mathbf{x}(\dot{\mathbf{t}}) = \mathbf{A} \cdot \mathbf{x}(\dot{\mathbf{t}}) + \mathbf{b} \cdot Vin \cdot q(t)$$

$$\mathbf{y}(\mathbf{t}) = \dot{\mathbf{C}} \cdot \mathbf{x}(\mathbf{t}) \tag{55}$$

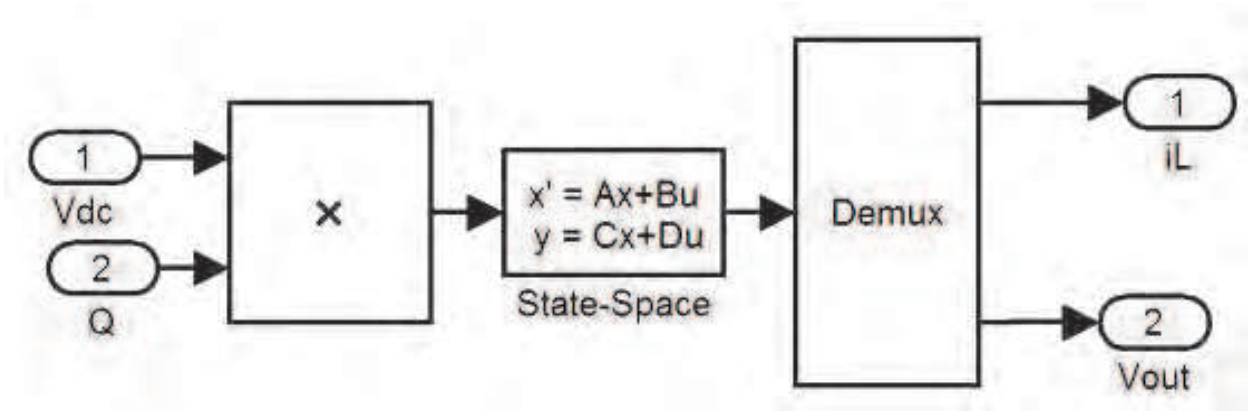The Simulink model of the buck converter is shown in Fig.23.

Fig. 23. The buck converter model.

In the state space block, matrix coefficients are entered. The input voltage V_{dc} and the gate drive logic signal Q are the subsystem inputs. The scalar components of the output vector are obtained by the *Demux* block.

The modelling technique is extended to the four-modules architecture which is shown in Fig.24.
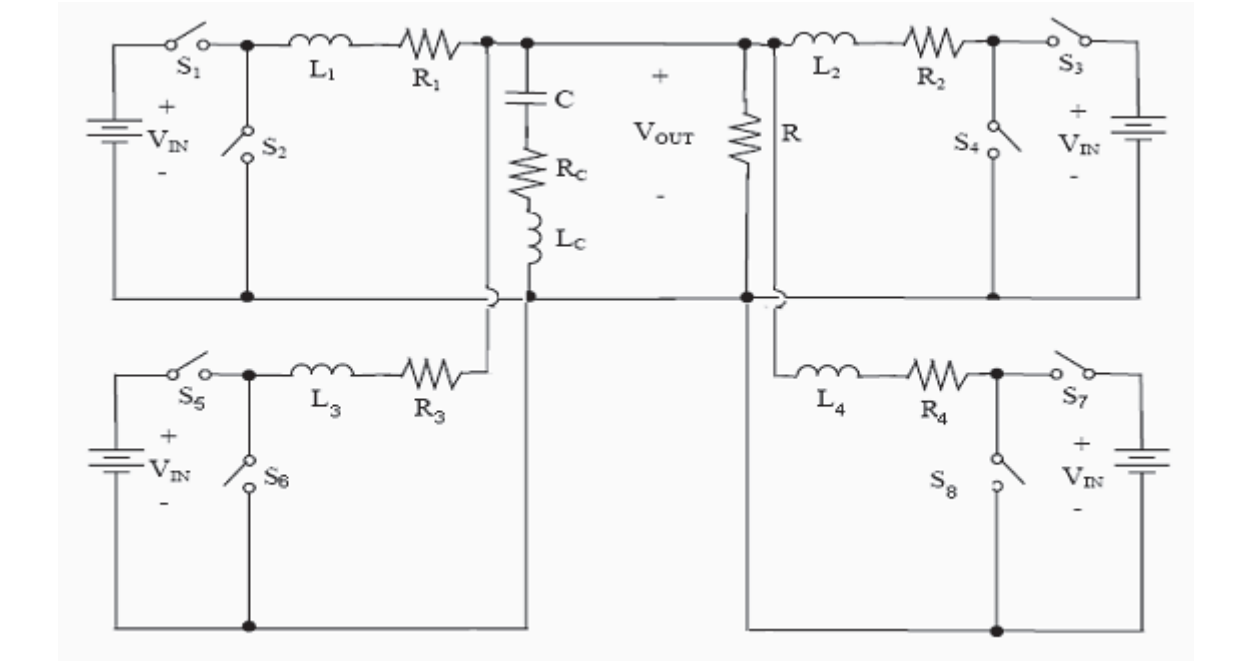

Fig. 24. A four-modules buck converter.

The state-vector is defined as:

$$x(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ i_{L4}(t) \\ v_c(t) \end{bmatrix} \tag{56}$$

The output vector is defined as:

$$\mathbf{y}(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ i_{L4}(t) \\ v_{out}(t) \end{bmatrix} \tag{57}$$

The state-space model is obtained:

$$\dot{\mathbf{x}}(t) = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{b} \cdot Vin \cdot \mathbf{q}(t)$$

$$\mathbf{y}(t) = \mathbf{C} \cdot \mathbf{x}(t) \tag{58}$$

where:

$$A = \begin{bmatrix} \dfrac{RR_1 + RR_C + R_C R_1}{L_1(R+R_C)} & -\dfrac{RR_C}{L_1(R+R_C)} & -\dfrac{RR_C}{L_1(R+R_C)} & -\dfrac{RR_C}{L_1(R+R_C)} & -\dfrac{R}{L_1(R+R_C)} \\ -\dfrac{RR_C}{L_2(R+R_C)} & -\dfrac{RR_2 + RR_C + R_C R_2}{L_2(R+R_C)} & -\dfrac{RR_C}{L_2(R+R_C)} & -\dfrac{RR_C}{L_2(R+R_C)} & -\dfrac{R}{L_2(R+R_C)} \\ -\dfrac{RR_C}{L_3(R+R_C)} & -\dfrac{RR_C}{L_3(R+R_C)} & -\dfrac{RR_3 + RR_C + R_C R_3}{L_3(R+R_C)} & -\dfrac{RR_C}{L_3(R+R_C)} & -\dfrac{R}{L_3(R+R_C)} \\ \dfrac{RR_C}{L_4(R+R_C)} & \dfrac{RR_C}{L_4(R+R_C)} & \dfrac{RR_C}{L_4(R+R_C)} & -\dfrac{RR_4 + RR_C + R_C R_4}{L_4(R+R_C)} & -\dfrac{R}{L_4(R+R_C)} \\ \dfrac{R}{C(R+R_C)} & \dfrac{R}{C(R+R_C)} & \dfrac{R}{C(R+R_C)} & \dfrac{R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix} \tag{59}$$

$$B = \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 & 0 \\ 0 & \dfrac{1}{L_2} & 0 & 0 \\ 0 & 0 & \dfrac{1}{L_3} & 0 \\ 0 & 0 & 0 & \dfrac{1}{L_4} \end{bmatrix} \tag{60}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ \dfrac{RR_C}{R+R_C} & \dfrac{RR_C}{R+R_C} & \dfrac{RR_C}{R+R_C} & \dfrac{RR_C}{R+R_C} & \dfrac{R}{R+R_C} \end{bmatrix} \tag{61}$$

$$\mathbf{q}(t) = \begin{bmatrix} q_1(t) \\ q_2(t) \\ q_3(t) \\ q_4(t) \end{bmatrix} \tag{62}$$

Fig. 25 shows the Simulink model of the multiphase converter. The input voltage and scalar components of the q vector are the model inputs. The *Mux* block multiplexes scalar components into the input vector **u**. The *Demux* block generates the scalar components of the output vector **y**(t).
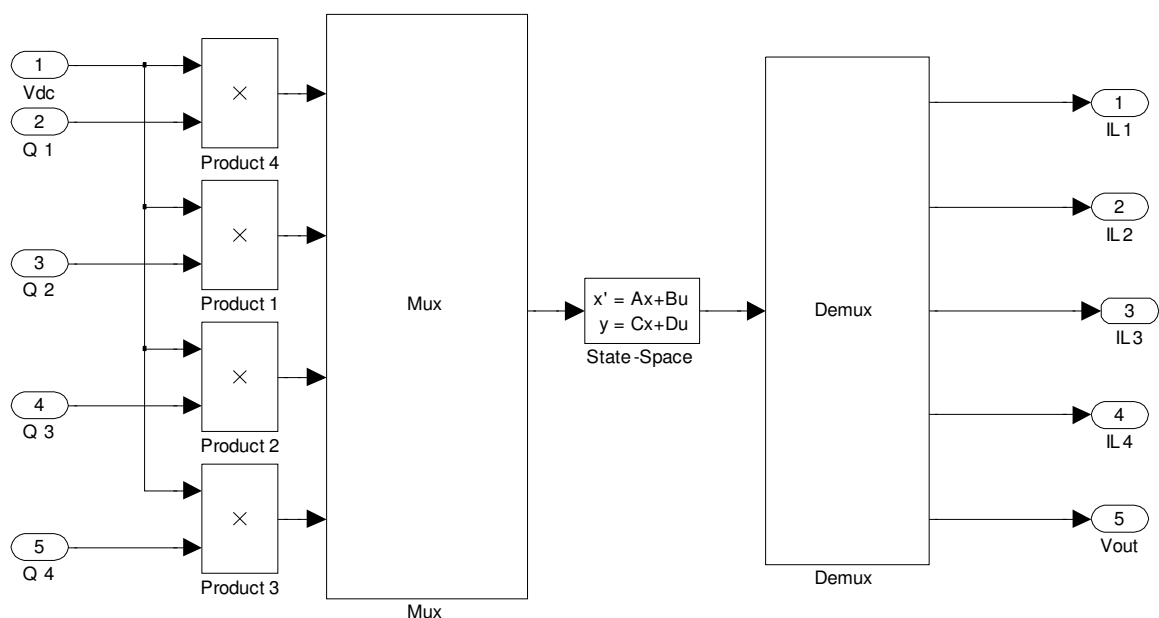

Fig. 25. Simulink model of a four-module buck converter. Inductor currents are the output vector components.

The proposed model could be adapted to the designer requirements. For example, in Fig.26 another implementation is shown. Besides the inductor current signals and the output voltage, the switching node voltages V_{sw} of each module are also included in the output vector. Further, the equivalent inductor current instead of the inductor currents as well as switching node voltages are available outside the subsystem. The equivalent current is obtained as the sum of inductor currents by the means of *Adder* blocks.
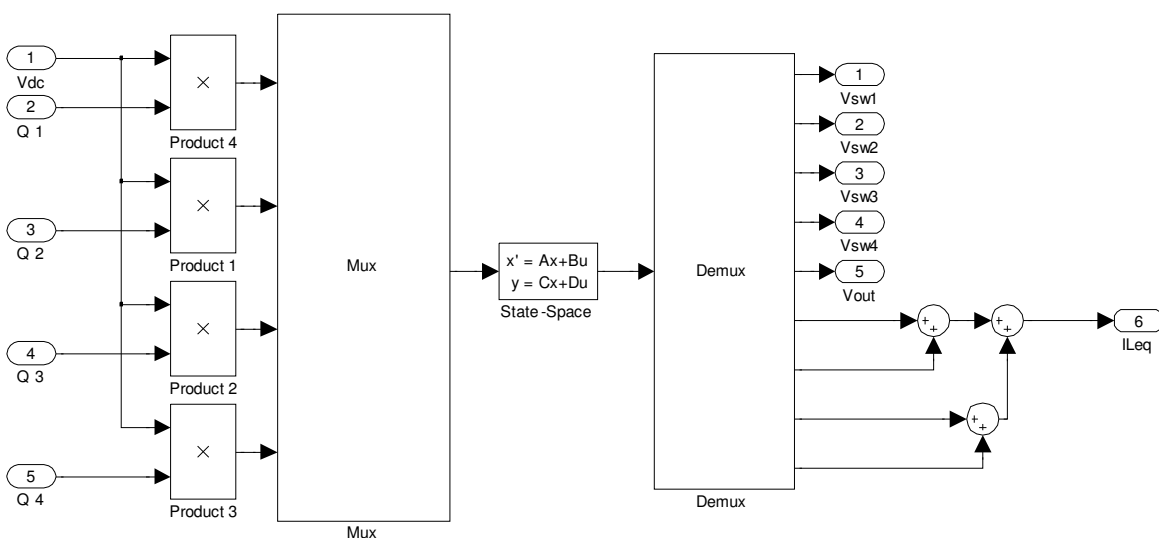
Fig. 26. Simulink model of the multiphase converter.

5.2 The sense network

Current sense filters are modelled by their own Laplace transfer function using the *Transfer Function* block. In the parameter box the coefficients of the Laplace function are entered. The *low-pass filter* subsystem of the master phase is shown in Fig.27. Low-pass filter subsystems are fed by the switching node voltage of the corresponding power module.
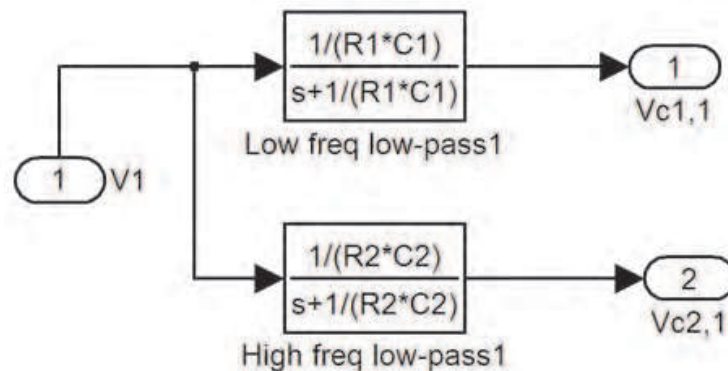

Fig. 27. Current-sense filters of the master module.

5.3 The digital controller model

The digital controller is modelled as the collection of VHDL entities, each one described by the VHDL code in Active-HDL environment. By the co-simulation procedure, each design unit is added to the Simulink model and simulated among the others. The Simulink model of the *Controller* subsystem is shown in Fig.28. Two subsystems are highlighted: the *Non_linear_controller* and the *Linear_Controller*. VHDL entities are collected in the *Controller* subsystem. The 6.25MHz system clock is derived from the 50MHz clock signal available from the FPGA device by the means of a digital clock divider, described in the *clock_div* entity. VHDL entities are linked in Simulink environment. Note that modelling the digital controller by multiple entities is a unique choice of the designer. Instead of modelling the controller by a unique VHDL entity, authors suggest a multiple entities approach to monitor internal signal of the FPGA controller in Simulink environment. The co-simulation procedure allows the designer to test the VHDL code, including timing between entities. The digital controller is thus tested as closely as possible to the effective FPGA implementation.

Each VHDL entity accomplishes a specific task of the digital controller: soft-start, protection circuits for safe operation, adaptive voltage positioning and the strictly-named controller implementing the sophisticated control algorithm, as shown in Fig.29. The co-simulation procedure as well as the proposed modelling approach allows the designer to test each available function by behavioural simulations, thus reducing the risk of experimental fault conditions.

In the *Linear Controller*, the error signal is converted to analog by the DAC subsystem and then compared to the analog saw-tooth within the PWM generator. The interleaved technique is digitally implemented. Fig.30 shows the switching logic subsystem of the master phase. The *f1_sim* VHDL entity is fed by the master phase PWM signal and non-linear control signals. The unit generates the q-signal for the master module. The digital counter which generates the switching clocks (*SwCk*) of all slave modules is modelled by the *acc_sint* VHDL unit.
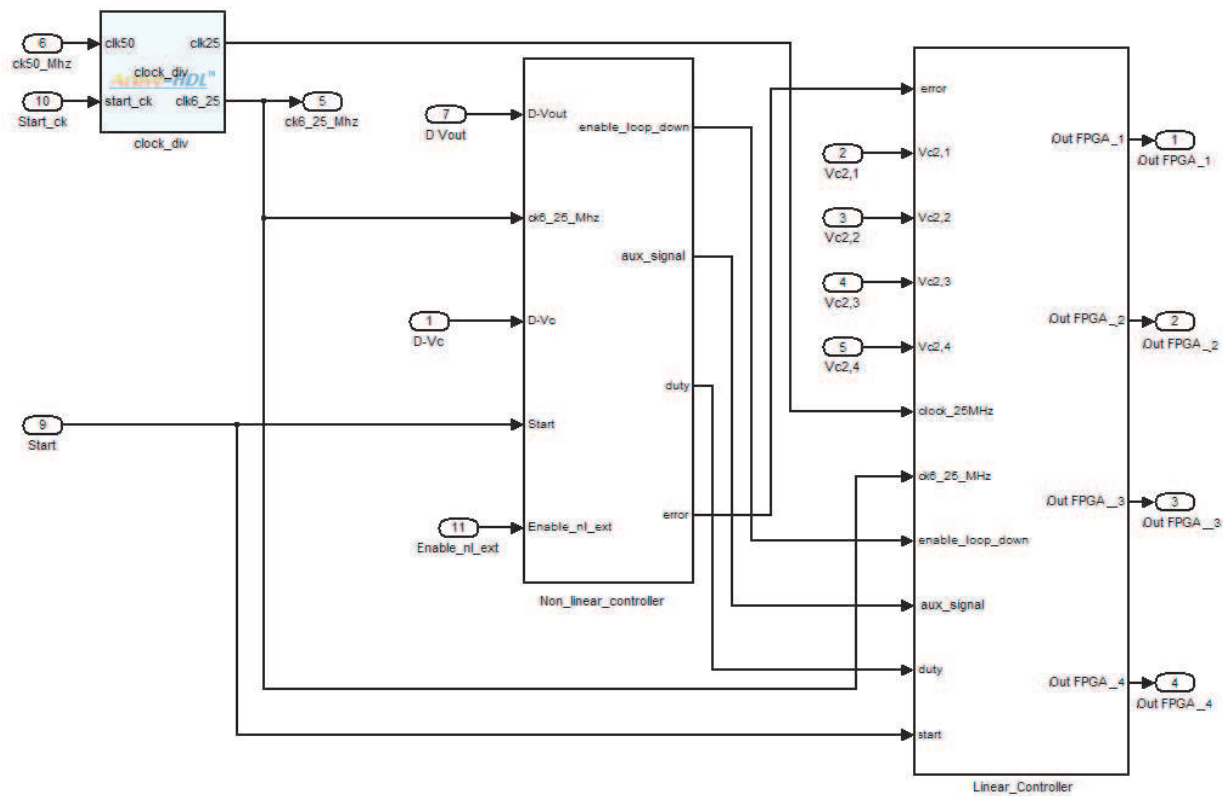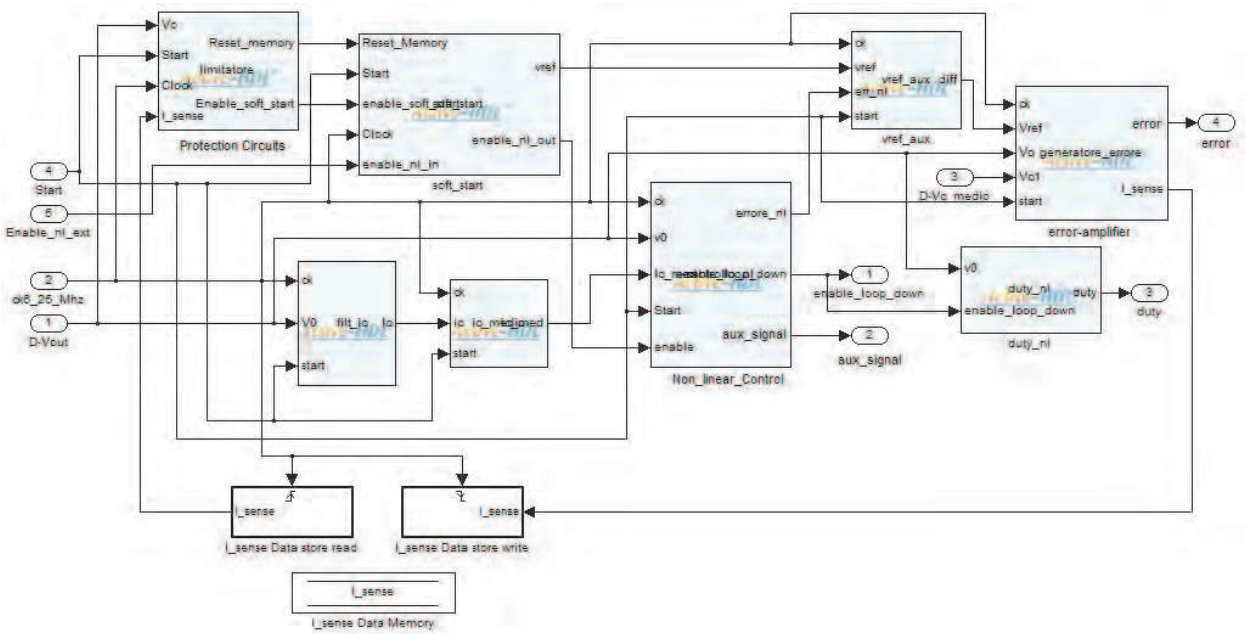
Fig. 28. The Controller subsystem.
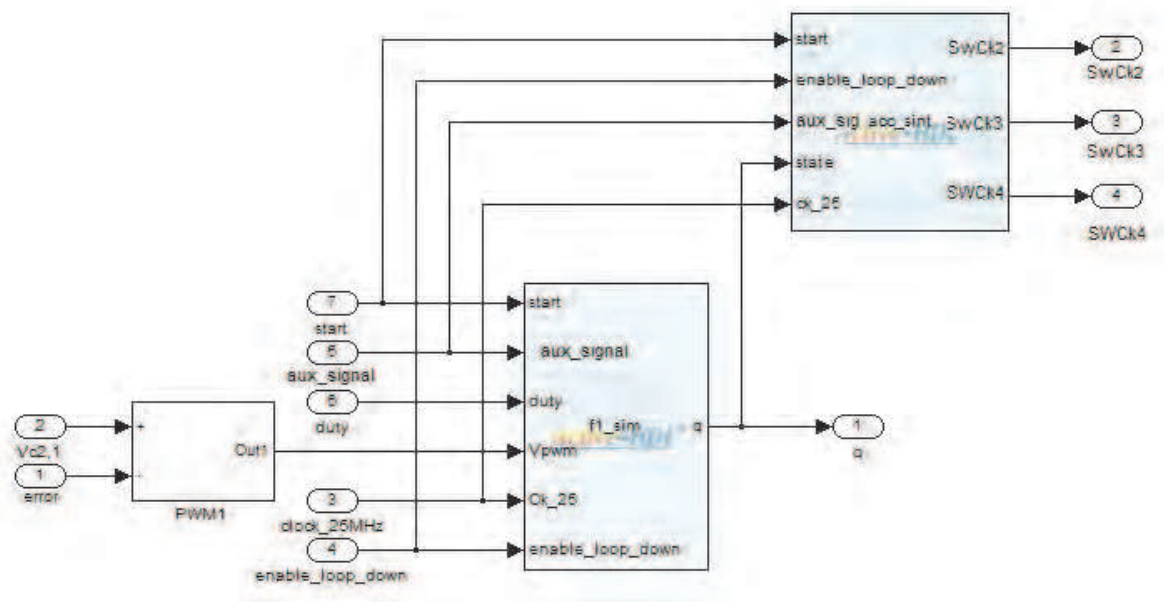

Fig. 29. The non-linear controller.

Fig. 30. The Switching Logic model of the master module.

5.4 Analog-digital interface

Co-simulation features are to be well-understood before implementing a mixed-mode model. ALDEC and Simulink automatically code common signals. In ALDEC environment signals are coded as signed binary vectors. The output of each HDL block is thus a binary vector. Simulink automatically codes binary vectors by the equivalent decimal number. HDL block inputs are Simulink signals thus coded as decimal numbers. ALDEC environment codes decimal numbers as the equivalent signed binary vector. The Simulink model should account for binary-decimal data conversion. Digital to analog converters and analog to digital converters are introduced in the Simulink model.

The A/D converter section includes two A/D converters, each modelled as shown in Fig.31 by the means of elementary blocks of Simulink libraries.
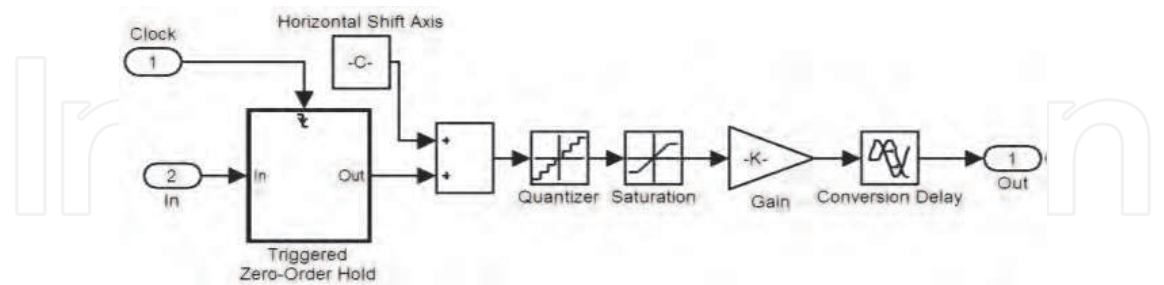
Fig. 31. The A/D converter model

The input signal is sampled at the clock frequency by the *Triggered Zero-Order Hold* block. Since in the Simulink library browser only an ideal symmetrical *Quantizer* block is provided, a non-ideal A/D converter model is achieved by adding the horizontal shift. The horizontal shift constant is given by:

$$C = \frac{FS}{2^{Nbit+1}} \tag{63}$$

where N_{bit} is the bit resolution and FS the full scale voltage.

The available *Quantizer* block allows the user to set the voltage resolution while the number of levels is yet unlimited.

The S*aturation* block is thus cascaded to the *Quantizer* in order to set the full scale range. The high-level saturation limit is given by:

$$\text{High} = V_{res} \cdot N_{lev} = \frac{FS}{2^{Nbit}} \cdot (2^{Nbit} - 1) \tag{64}$$

where V_{res} is the voltage resolution and N_{lev} the number of levels. The discrete output of the *Saturation* block should be coded. In order to simulate the ADC coding, the *Gain* block is cascaded to the saturation block. The output of the ADC model is the equivalent decimal number of the binary vector. The conversion gain is given by:

$$K = \frac{FS}{2^{Nbit}} \tag{65}$$

The *Conversion Delay* block accounts for the input-output delay of the modelled A/D converter.

The Simulink model of the digital-to-analog converter is shown in Fig.32. The subsystem is fed by a digital signal and generates a discrete analog signal. The maximum value of the input signal is given by:

$$Vmax = 2^{N_{bit,dac}} - 1 \tag{66}$$

where $N_{bit,dac}$ is the converter bit resolution. The maximum value of the output voltage is equal to the DAC full scale voltage. The digital-to-analog converter is modelled by a gain factor K_{dac}:

$$K_{dac} = \frac{FS_{dac}}{2^{N_{bit,dac}}} \tag{67}$$

In order to model the full scale range of the converter, a *Saturation* block is cascaded with the gain block. Saturation levels are equal to the full scale range.
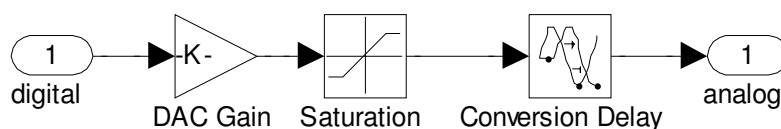

Fig. 32. The Simulink model of a digital-to-analog converter.

5.5 PWM comparator model

The PWM comparator is fed by the analog error signal and the analog current sense signal. The analog comparator model is shown in Fig.33. An adder block is used as the input stage of the comparator. The *Relay* block models the non-linearity of the comparator. The Relay block allows its output to switch between two specified values. The state of the relay is obtained by comparing the input signal to the specified thresholds, the *Switch-off point and the Switch-on point* parameters. When the relay is on, it remains on until the input drops below the value of the *Switch-off point* parameter. When the relay is off, it remains off until the input exceeds the value of the *Switch-on point* parameter. The parameter box allows the

end user to set a specified value for both on and off conditions. In this model, the output value is equal to "1" in the on-state, "0" in the off-state.
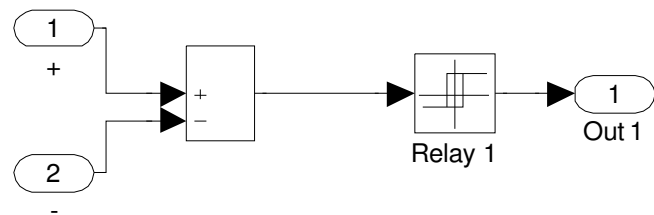

Fig. 33. The Simulink model of the PWM comparator.

6. Simulation results

A 12V/1V@120A four-module buck converter has been designed and modelled in Simulink-Aldec mixed environment. Each power module operates at 250kHz switching frequency. Simulation results are shown to highlight the high accuracy of the modelling approach. Steady-state waveforms under 1A load are shown in Fig.34. At the top the output voltage waveform, at the bottom the equivalent inductor current is shown. The proposed modelling approach allows the designer to simulate the system behaviour within the switching period achieving high accuracy results. The output voltage ripple and the current ripple are accurately modelled. The DC set point of the output voltage is fixed at the nominal value. The output voltage, at the top, and the equivalent current, at the bottom, under 115A load are shown in Fig.35. The DC set point is fixed at 0.96V at full load due to the implemented AVP technique.

The system is tested under load current transients to evaluate the non-linear control performances. Under a 0-120A load current step, if the non linear controller is disabled the system behaviour shown in Fig.36 is obtained. Under a 120A -0 load current step, if the non linear controller is disabled the system behaviour shown in Fig.37 is obtained. The output voltage, at the top, and the equivalent current, at the bottom, are shown. Note that the proposed design approach accurately models the system behaviour within the switching period as well as under large-signal transients.
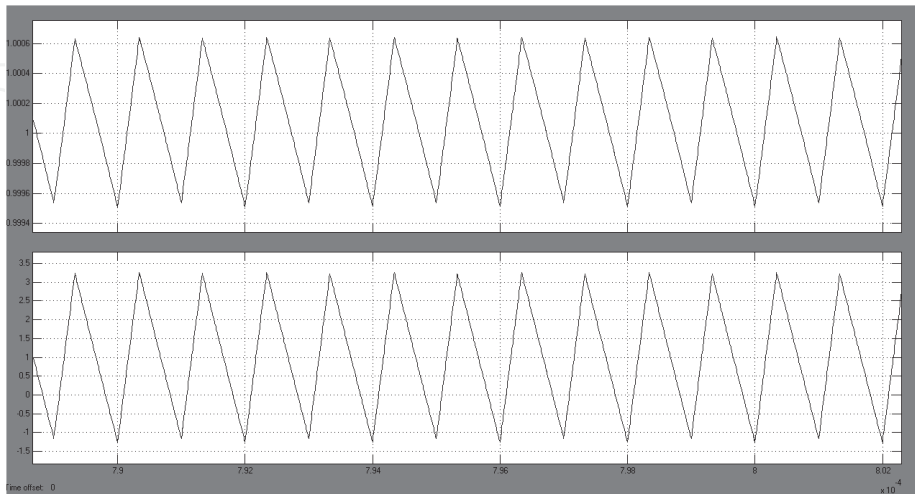

Fig. 34. Steady-state waveforms under 1A load current. At the top the output voltage, at the bottom the equivalent current waveforms are shown.
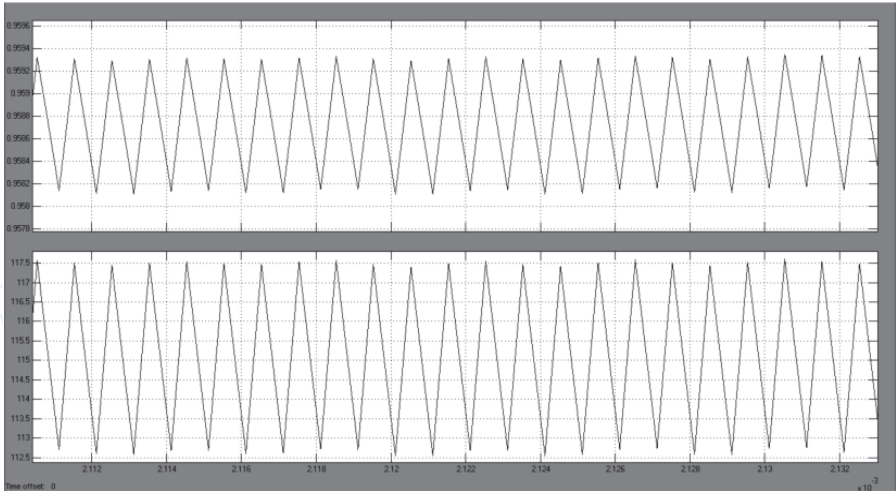
Fig. 35. Steady-state waveforms under 115A load current. At the top the output voltage, at the bottom the equivalent current waveforms are shown.
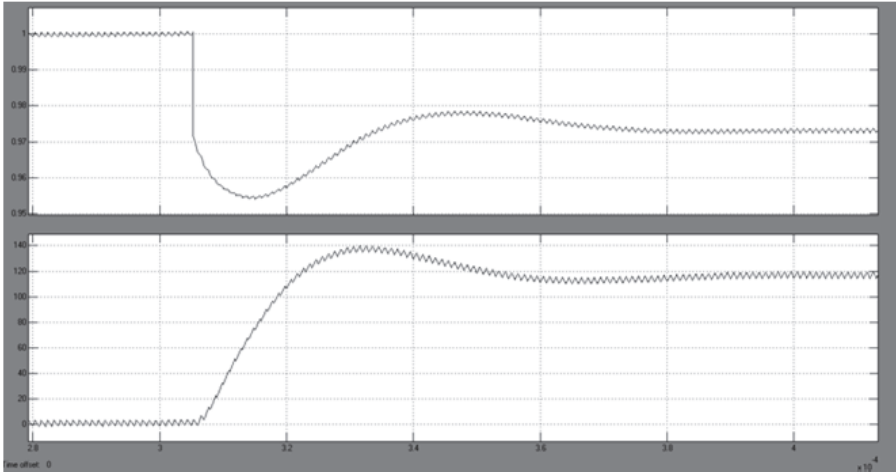

Fig. 36. Dynamic response to a 0-120A load current step without the non-linear control. At the top the output voltage, at the bottom the equivalent current waveforms are shown.
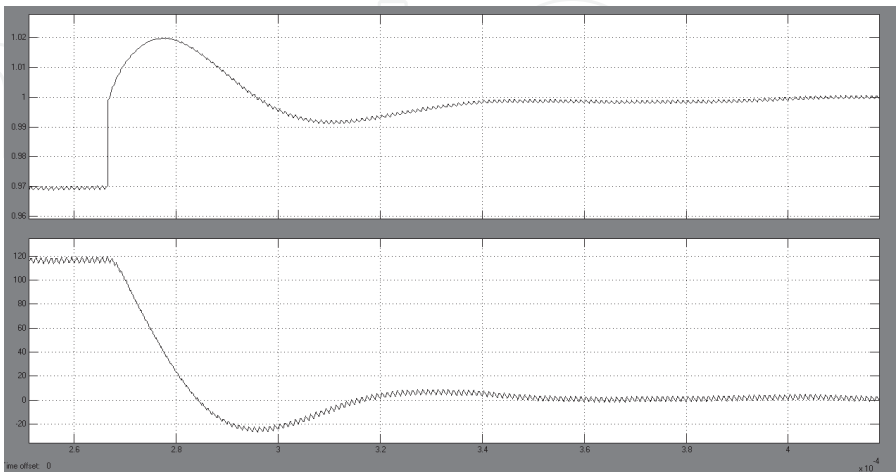

Fig. 37. Dynamic response to a 120A-0 load current step without the non-linear control. At the top the output voltage, at the bottom the equivalent current waveforms are shown.

Fig.38 and 39 show the dynamic response to a 0-120A and 120A-0 load current step, respectively, obtained by enabling the non-linear controller.
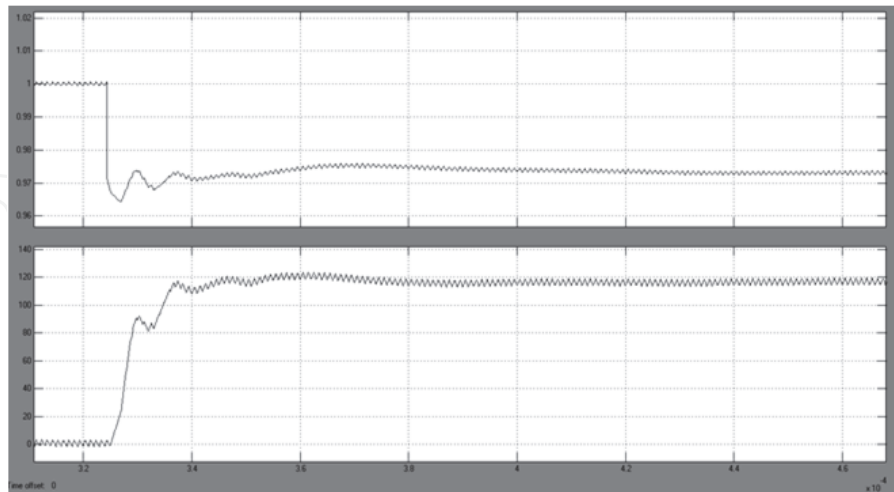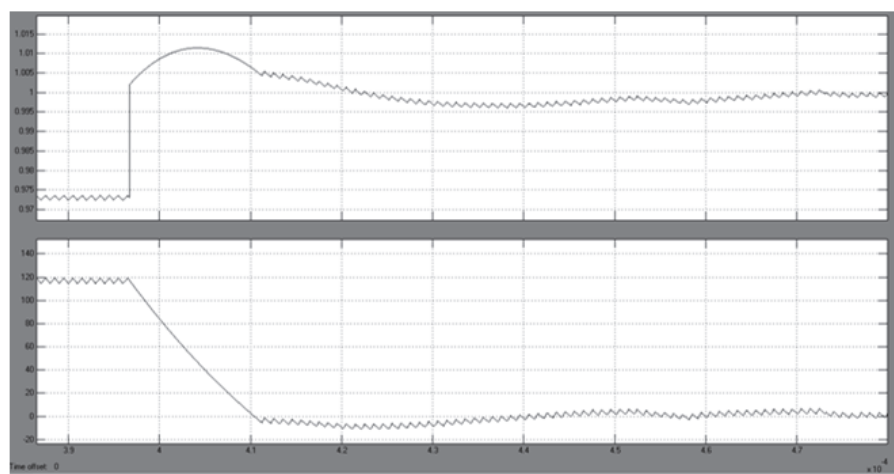

Fig. 38. Dynamic response to a 0-120A load current step with the non-linear control. At the top, the output voltage. At the top the output voltage, at the bottom the equivalent current waveforms are shown.

Fig. 39. Dynamic response to a 120A-0 load current step with the non-linear control. At the top the output voltage, at the bottom the equivalent current waveforms are shown.

As shown by simulation results, the non linear controller ensures a reduction of the output voltage over- and-under-shoots during large-signal transients. Under the rising edge of the load current step, the output voltage under-shoot is reduced by 22%. Under the falling edge of the load current step, the output voltage over-shoot is reduced by 26%. The recovery time is reduced by 24%. The instantaneous output voltage change due to the capacitor ESR is included. Note that the instantaneous drop is not affected by the non-linear control.

7. Experimental results

A laboratory prototype has been realized to test the efficiency of the non-linear control algorithm. Experimental validation of the non linear control algorithm has been proposed in

(Boscaino et al., 2010). The high accuracy of the proposed design approach is here discussed by the comparison of simulation and experimental results. Experimental waveforms in Fig.40 show the system behaviour under 120A load current square-wave obtained by disabling the non-linear control (a), and by enabling the non-linear control (b). Ch1 shows the output voltage (200mV/div), Ch3 shows the master module inductor current (10A/div) and Ch4 shows the load current (60A/div).

The great potential of the proposed design approach relies in the performance evaluation of the designed controller. Under load transients, the recovery time as well as the percentage of drop reduction due to the non linear control accurately matches experimental results. The system behaviour is perfectly matched by simulation results. Evaluating system performances by simulation or experimental results leads to the same conclusions. A detail of Fig.40 under the rising edge of the load current square wave is shown in Fig.41: (a) the linear controller response, (b) the non-linear controller response. As shown by experimental results, under the load current rising-edge, the under-shoot of the output voltage is reduced by 29%.

A detail of Fig.40 under the falling edge of the load current square wave is shown in Fig.42: at the left the linear controller response, at the right the non-linear controller response. By comparing experimental waveforms in Fig.42 the output voltage over-shoot under a load current falling edge is reduced by 28%. Under both transients, the recovery time is reduced by 25%.
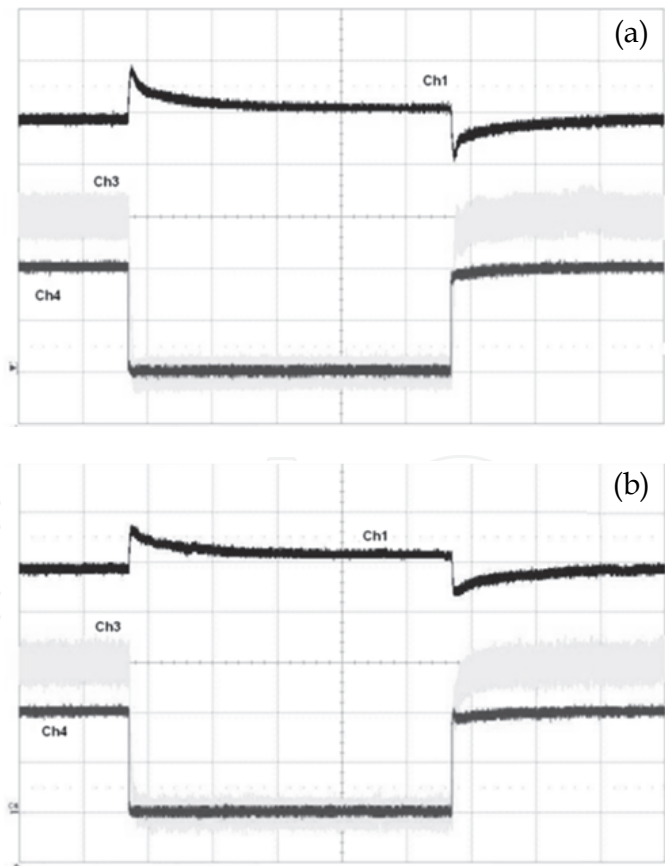

Fig. 40. System behaviour under a 115A width load current square wave. Ch1 shows the output voltage (200mV/div), Ch3 shows the master module inductor current (10A/div) and Ch4 shows the load current (60A/div). (a) The non-linear control is disabled. (b) The non-linear controller is enabled.
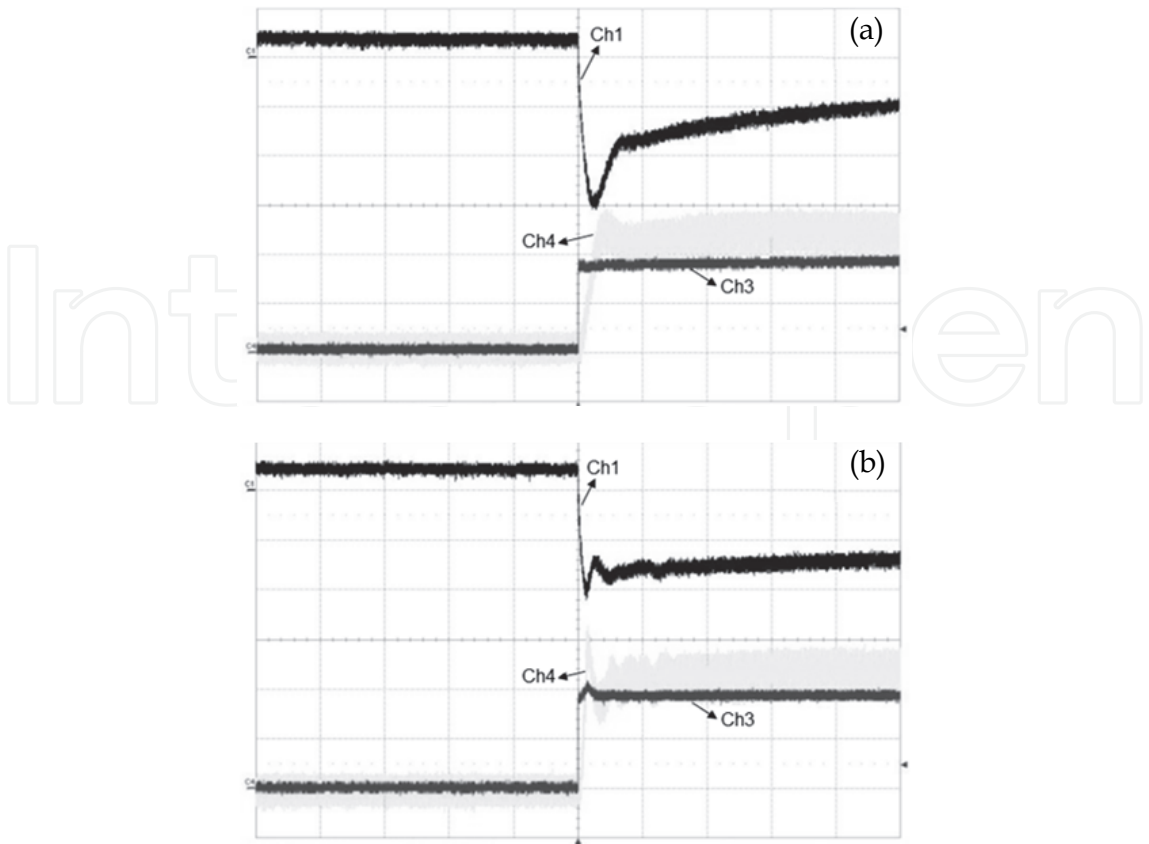
Fig. 41. System behaviour under the load current rising-edge. Ch1 shows the output voltage (50mV/div, AC coupling), Ch3 shows the master module inductor current (10A/div) and Ch4 shows the load current (60A/div). At the left, the non-linear control is disabled. At the right, the non-linear controller is enabled.
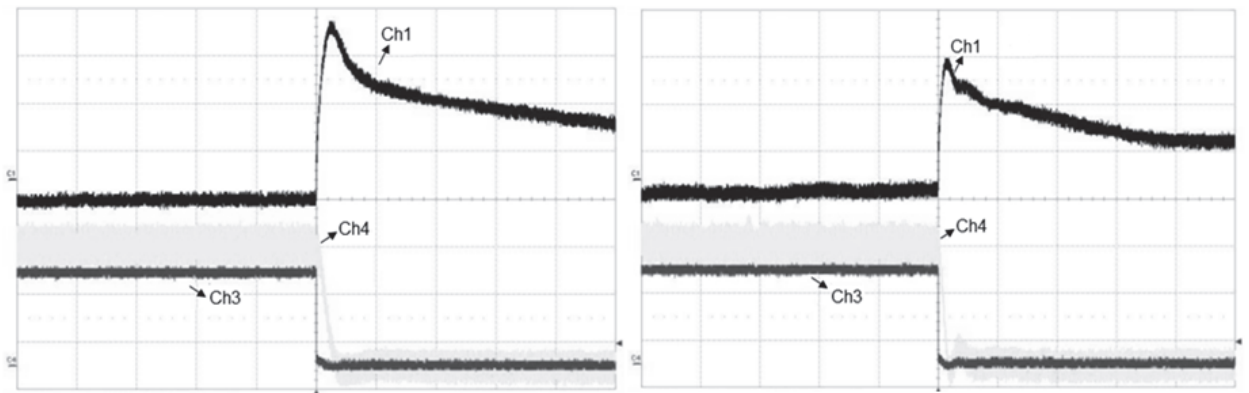

Fig. 42. System behaviour under the load current falling-edge. Ch1 shows the output voltage (50mV/div, AC coupling), Ch3 shows the master module inductor current (10A/div) and Ch4 shows the load current (60A/div). At the left, the non-linear control is disabled. At the right, the non-linear controller is enabled.

8. Conclusion

In this chapter, a high-accuracy design approach for power supply systems is proposed. Mixed-mode systems are modelled in Simulink environment using powerful co-simulation

tools. For the highest processing speed, a modelling technique for the power section is proposed. The digital subsystems are described by VHDL source code and verified by Aldec/Simulink co-simulation tool, allowing the test of the VHDL code and timing between separate entities. As an application, the model of a multiphase dc-dc converter for VRM applications is described. Thanks to the available co-simulation tool, all provided functions such as soft-start, protection algorithms for safe operation and adaptive voltage positioning are accurately modelled and verified during behavioural simulations. As shown by simulation results, the proposed model matches the system behaviour both within the switching period and during load transients. The design approach allows the designer to simulate the system behaviour as closely as possible to the effective behaviour, modelling and testing the "effective" controller. The controller performances are evaluated by simulation and experimental results leading to the same conclusions. Authors suggest the co-simulation tool for mixed-mode system and complex architectures. Actually, the IC implementation of the proposed controller in BCD6S technology is carried on. A central unit for signal processing is introduced. Mathematical operations are time-multiplexed in order to speed up the input-output delay in the control loop. The co-simulation tool is already used to test the efficiency of the implemented solution.

9. Acknowledgements

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