4

Importance of Simulation Studies in Analysis of Thin Film Transistors Based on Organic and Metal Oxide Semiconductors

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1. Introduction

Organic semiconductors and metal oxides (such as ZnO) have recently been recognized as a new class of electronic materials for thin film transistor (TFT) applications such as active matrix displays, identification tags, sensors and other low end consumer applications (Campbell et al, 2007; Fortunato et al, 2008; Masuda et al, 2003; Nelson et al, 1998; Sandberg et al, 2002). Owing to their low cost, large area coverage, and at par or better performance, these materials are also considered to have enormous potential to replace amorphous silicon for use in existing and new electronic device applications. From the device technology and fabrication point of view, there have been rapid developments in this area over the past decade, but the field is still very much nascent in gaining the fundamental understanding, both, at the material and the device physics level. For example, whereas, vanderwal bonded organic semiconductors often suffers from spatial and energetic disorder (Pope et al, 1999), ZnO has very rich defect chemistry (Özgür et al, 2005; McCluskey et al 2009). Additionally, they tend to have complex interaction with several surfaces, which often results in phenomenon difficult to explain by classical theories. It is therefore critical that the research in this area is necessarily be coupled with theoretical perspective in order to resolve several of the important issues, which will help in further enhancing its progress. In traditional electronics, device modelling and simulation has proven to be of great help in not only understanding the detailed device operation but has also served as a powerful tool to design and improve devices. The physics based device simulation is also becoming beneficial to the research area of organic and metal oxide semiconductors TFTs, where it is effectively predicting the device behaviour, giving insight into the underlying microscopic mechanisms and providing intuitive information about the performance of a new material (Bolognesi, 2002; Gupta et al, 2008, 2009, 2010; Hill, 2007; Hossain, 2003; Scheinert, 2004). Its continued involvement for explaining various device phenomenons will certainly be of great use for future developments.

In this chapter, we show the importance of two dimensional simulations in both the classes of materials by addressing several common issues which are often vaguely explained by experimental means or by analytical equations. Pentacene and tris-isopropylsilyl (TIPS) – pentacene are taken as examples in the class of organic semiconductors, while solution processed ZnO and Li- doped ZnO served as illustrations in the metal- oxide category. Pentacene is a small molecule organic semiconductor and has unarguably been considered as a high mobility material for TFT applications (Jackson). (TIPS) – pentacene, on the other hand is a novel functionalized derivative of pentacene that incorporates the best properties of pentacene moiety together with the solution processibility, which pentacene lacks (Anthony). We begin with modelling of TFTs based on tris-isopropylsilyl (TIPS) – pentacene to provide a baseline for describing the charge transport in any new material. We completely model its electrical characteristics by considering all the aspects of contact barrier effect, field-dependent mobility, and traps/ interface trapped charges (Gupta et al, 2008). We then highlighted the role of metal – semiconductor contacts and the effect of dielectric- semiconductor interface structure on the device characteristics of pentacene based TFTs, which are two of the major concerns in organic TFT (OTFT) operation. Next we consider the stability issue in solution processible zinc oxide (ZnO) TFTs, in which we investigated the problem of change in device characteristics when subjected to electrical stress or exposed to air for a prolonged time. ZnO has several merits like substantially high mobility as compared to amorphous silicon or organic semiconductors, better structural homogeneity than polycrystalline silicon, high transparency, low cost, and ease of processing by wet chemical routes. However, its device degradation with respect to electrical stress and air exposure may inhibit its full exploitation due to instability and reliability problems. We deal with this issue by considering the rich and undefined defect states in pure and Li-doped ZnO [10], and build a physical degradation model based on the changes in density of states (DOS) of active layers, which effectively explains the degradation phenomenon in ZnO. In each of the examples, by providing a detailed description of the modelling scheme, we systematically approach the problem underhand and verify the simulated results with the experimentally obtained device characteristics.

2. Device simulation procedure

The simulator used for device modeling in this chapter is Silvaco's ATLAS (Silvaco). ATLAS is a two-dimensional semiconductor device simulator which incorporates the physics that govern charge carrier transport and applies it to the dimensions of the device being studied. For simulation, the commercial device simulator Silvaco-Atlas® is used, which predicts the electrical characteristics associated with a specified physical structure and bias conditions by solving systems of Poisson's equation and continuity equation that are a set of coupled, partial differential equations as shown by Eqs. 1 and 2 below:

$$\varepsilon\nabla^2\psi = -q(p - n + N_D^+ - N_A^-) \tag{1}$$

$$-\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot J_p + G_p - R_p \tag{2a}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G_n - R_n \tag{2b}$$

where ε is the dielectric constant, ψ is the potential, p is hole density, n is electron density, p refers to holes, n refers to electrons, q is the fundamental electronic charge, G is the charge generation rate, R is the charge recombination rate, and J is the current density which is given considering its drift and diffusion components by Eq.3:

$$J_p = qp\mu_p F + qD_p \nabla p \tag{3a}$$

$$J_n = qp\mu_n F + qD_n \nabla n \tag{3b}$$

where μ is mobility, F is the local electric field, and D is the diffusion coefficient. This simulator was primarily developed for silicon devices and, therefore, its applicability to organic materials is limited. However, the simulator can still predict the qualitative device characteristics correctly, as demonstrated by available literature [18, 26-29] on simulation of organic devices.

To account for the trapped charge, Poisson's equations are modified by adding an additional term Q_T, representing trapped charge. The trapped charge may consist of both donor - like and acceptor-like states across the forbidden energy gap, where the acceptor-like states act as electron traps and donor-like states act as hole traps. The density of defect states, g(E), is defined as a combination of four components. Two tail bands with an exponentially decreasing function are specified to contain large numbers of defect states at the conduction band (acceptor-like traps) and valence band (donor-like traps) edges, respectively. In addition, two deep-level bands for acceptor-and donor-like defects are defined that are modeled using a Gaussian distribution. The equations describing these terms are given as follows:

$$g_{TA}(E) = N_{TA} \exp\left(\frac{E - E_C}{W_{TA}}\right) \tag{4a}$$

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_V - E}{W_{TD}}\right) \tag{4b}$$

$$g_{GA}(E) = N_{GA} \exp\left[-\left(\frac{E - E_{GA}}{W_{GA}}\right)^2\right] \tag{4c}$$

$$g_{GD}(E) = N_{GD} \exp\left[-\left(\frac{E - E_{GD}}{W_{GD}}\right)^2\right] \tag{4d}$$

where E is the trap energy , E_C is conduction band energy, E_V is valence band energy, and the subscripts T, G,A, D stand for tail, Gaussian (deep level), acceptor and donor states respectively. The exponential distribution of DOS is described by conduction and valence band intercept densities (N_{TA} and N_{TD}), and by its characteristic decay energy (W_{TA} and W_{TD}). For Gaussian distributions, the DOS is described by its total density of states (N_{GA} and N_{GD}), its characteristic decay energy (W_{GA} and W_{GD}), and its peak energy/peak distribution (E_{GA} and E_{GD}).

2.1 Material parameters

In order to perform the simulations, it is necessary to define the required parameters for a particular material. The important material parameters required for a semiconductor as an input for the device simulation are band gap (E_g), electron affinity (E_A), effective density of states (N_C for conduction band and N_V for valence band) and permittivity. Table 1 summarizes the selected values of these parameters for pentacene, TIPS-pentacene and ZnO, as reported in the literature, including both theoretically calculated and experimentally measured values. Figure 1 shows the chemical structure of pentacene and TIPS-pentacene.

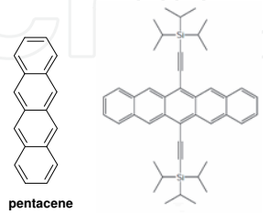


Fig. 1. Chemical structure of (a) pentacene and (b) TIPS- pentacene molecule.

Parameter	Pentacene	TIPS-Pentacene	ZnO	Ref.
Band Gap (eV)	2.2	2.2	3.4	Gupta et al, 2009; Hossain et al 2003
Electron Affinity (eV)	2.8	2.8	4.29	‘’
N_C (cm^{-3})	$2x10^{21}$	$2x10^{21}$	$4.5x10^{24}$	‘’
N_V (cm^{-3})	$2x10^{21}$	$2x10^{21}$	$9x10^{24}$	‘’
Permittivity	4	4	8.5	‘’

Table 1. Material parameters for pentacene, TIPS- pentacene and ZnO.

3. Device modelling of TFTs made of TIPS-pentacene

TIPS- pentacence based OTFTs were fabricated in bottom contact geometry on a 100 nm thick SiO_2 layer thermally grown on heavily doped n-Si wafers that also function as the gate (G) electrode (Gupta et al, 2008). The source (S) and drain (D) electrodes consist of 5 nm titanium adhesion layer and 100 nm gold layer onto which a solution of 2 wt% TIPS-pentacene in toluene was drop-cast. The solution was then allowed to dry slowly in a solvent-rich environment at 50°C to promote ordered molecular arrangement. The morphology of TIPS-pentacene films typically consist of platelet-like structures each of which may be regarded crystalline. The channel width W is 1.5 mm and length L is 50 µm, respectively.

Figure 2 shows the experimental output characteristics (dotted lines) in the forward sweep (off to on) at gate voltage (V_G) from 0 to -40 V in a step of -10 V. The curves exhibit saturation behavior at high drain voltages (V_D), but one can easily observe a non-ohmic behavior of the drain current (I_D) in the linear region at low V_D, which is often called as “current crowding”. This may be explained mainly by a limited carrier injection from metal contacts to semiconductors due to an existing contact barrier Φ_B (Hill, 2007; Tessler et al, 2001). Φ_B is defined as the difference between the metal workfunction (Φ_S) and valence band maximum (E_v) of the semiconductor. Theoretically, Ti/Au contacts provide a proper energy level alignment with TIPS-pentacene, as the workfunction of gold lies between 4.7-5.0 eV.

However, in literature, it is many times quoted that an interfacial electrical dipole may be formed which can effectively change the work-function of the metal in the close proximity of the organic semiconductor. The reasons for the formation of this interfacial dipole is often debatable, but is believed to be the result of charge transfer, screening, or hybridization effects caused by the complex chemical interaction between the organic semiconductor and metal (Ishii et al, 1999; Kahn et al, 2003).

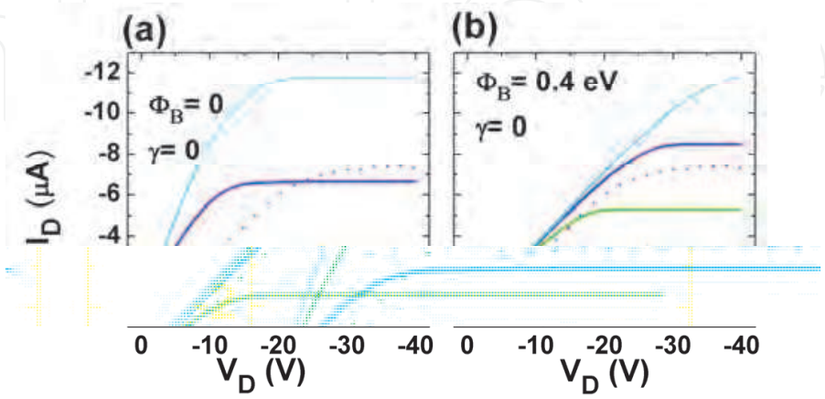


Fig. 2. Output characteristics of TIPS-pentacene TFTs: experimental (dotted) vs. numerical simulation (solid) results. (a) Simulated characteristics with Φ_B = 0 and γ =0 (no field-dependence) and (b) Simulated characteristics with Φ_B = 0.4 eV and γ=0. In (a) and (b), the mobility value is scaled to match the value of I_D(V_D=-40V) for V_G=-40V. V_{GS} in (a) and (b) is varied from 0 to -40V in -10V steps. (Reprinted from *Organic Electronics*, vol.9, D.Gupta, N. Jeon, S. Yoo, "Modeling the electrical characteristics of TIPS-pentacene thin-film transistors: Effect of contact barrier, field-dependent mobility, and traps", p.1026, 2008, *with permission from Elsevier)*

On the basis of the above discussion, we investigated several values of effective contact barrier (Φ_B=0 to 0.4eV) to reproduce the output characteristics at low drain voltages in the output curves. However, we found that none of the values of Φ_B can reproduce the whole output characteristics in both linear and saturation regions over the range of V_{GS} used in this study. For example, the simulated device characteristics with Φ_B=0 (Fig. 2a) resulted in an ohmic behavior in the linear region, while Φ_B=0.4 eV (Fig. 2b) causes large reduction in drain current and requires adjustment of mobility towards a larger value. Therefore, field dependence of mobility in addition to contact barrier which has previously been shown to result in non-linear characteristics of the output curves is invoked. The presence of field-dependent mobility in TIPS-pentacene OTFTs is shown by extracting field-effect mobility of devices with L of 10, 20, and 50 μm at several values of V_{DS} in linear region and plotted it as a function of $(V_D/L)^{0.5}$, as shown in Figure 3a (Cherian et al, 2004; Wang et al, 2003). The logarithmic variation of mobility with $(V_D/L)^{0.5}$ for a series of channel lengths suggests that it follows the Poole-Frenkel (PF)-type field-dependence given by:

$$\mu = \mu_o \exp\left(\gamma\sqrt{F}\right) \tag{4}$$

where μ_0 is the zero-field mobility, F is the electric field and γ is the characteristic parameter for the field-dependence. A linear fit [dashed line in Fig. 4] to the data yielded field-

dependent parameters of μ_o= 0.035 cm²/Vs and γ =1.7×10^{-3} (cm/V)$^{0.5}$. It is noted that this PF field-dependence is often observed in disordered organic semiconductors. In this respect, the field-dependence of mobility given by Eq.4 is incorporated, in addition to the contact barrier effect, into the numerical simulation. Line curves in Fig. 3b shows the simulated output curves which take into account both the PF mobility and contact barriers. The best fit to the experimental data was obtained with Φ_B of 0.38 eV, μ_o of 0.061 cm²/Vs, and γ of 1.8×10^{-3} (cm/V)$^{0.5}$, respectively.

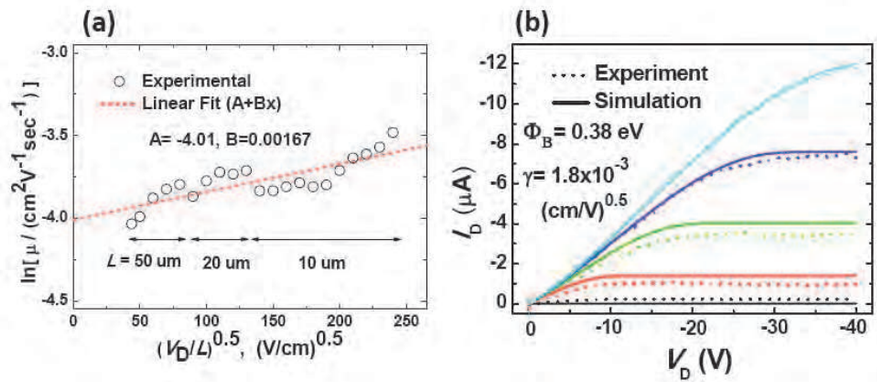


Fig. 3. (a) Natural logarithm of field-effect mobility as a function of $(V_D/L)^{0.5}$. Dashed line is a linear fit with which the field-dependent parameters are estimated to be μ_o= 0.035 cm²/Vs and γ=1.7×10^{-3} (cm/V)$^{0.5}$. (b) Output characteristics of TIPS-pentacene TFTs: experimental (dotted) vs. numerical simulation (solid) results. Simulation was done in consideration of both a contact barrier height Φ_B of 0.38 eV, μ_o= 0.061 cm²/Vs and γ=1.8×10^{-3} (cm/V)$^{0.5}$. V_G is varied from 0 to -40V in -10V steps. (Reprinted from *Organic Electronics*, vol.9, D.Gupta, N. Jeon, S. Yoo, "Modeling the electrical characteristics of TIPS-pentacene thin-film transistors: Effect of contact barrier, field-dependent mobility, and traps", p.1026, 2008, *with permission from Elsevier)*

The incorporation of contact barrier and PF dependence of mobility show a reasonable match to the output curves, but transfer curves still suffers from a significant deviation at low $|V_G|$ (curve 1 in Fig. 4a), which signifies include additional factors based on traps to complete the TFT model. Moreover, a hysteresis loop in the I_{DS}-V_{GS} transfer curve shown in Fig. 4(a), when scanned V_{GS} from 0 to -40 V and then back from -40 to 0 V again indicate about the existence of traps, which may come from dielectric-semiconductor interface or from structural defects in TIPS-pentacene films (Alam et al, 1997; Scheinert et al, 2004). This trap-related phenomenon is simulated by assuming a spatially uniform density of trap states in TIPS-pentacene films that is modeled by an exponential distribution of acceptor-like traps as in Eq. 4a and 4b. It was previously discussed that oxygen is the chemical origin of acceptor-like traps in pentacene and that acceptor-like traps provide extra hole current in the subthreshold region in pentacene OTFTs (Alam et al, 1997; Knipp et al, 2003; Scheinert et al, 2004; Street et al, 2002). Additionally, a positive interface trapped charge (N_{it}) is included, which may arise due to impurities such as moisture, oxygen or mobile charges in the dielectric. It was observed that the forward sweep (curve 2) can be better reproduced with N_{TA} = 1.0×10^{18} cm^{-3}eV^{-1}, W_{TA} = 0.55 eV and N_{it} = 8.0×10^{11} cm^{-2}, while reverse sweep (curve 3) requires N_{TA} = 8.0×10^{17} cm^{-3}eV^{-1}, W_{TA} = 0.55 eV, N_{it} = 2.0×10^{12} cm^{-2}, and μ_o = 0.058

cm²/Vs. The increase in N_{it} in the reverse sweep is a result of discharging of the trap states that is relatively slow when compared to the sweep speed (= 5V/sec) used in this study and is mainly responsible for the shift in threshold voltage. The output curves were also well simulated with the additional incorporation of traps in TIPS- pentacene films, as shown in Fig. 4b. Thus, this work is helpful in building an integral picture of injection, transport, and traps in TIPS-pentacene in a context of OTFT operation, and will serve as a starting point for further performance optimization and baseline for simulation of TFT made of any new semiconductor.

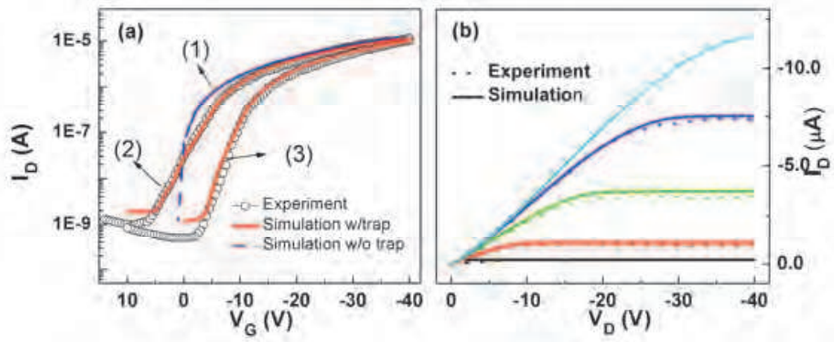


Fig. 4. (a) Numerical fit to the transfer curves (curve 1 is without traps, while curves 2 and 3 are plotted using trap distribution given by Eq. 4 and interface charges in forward (2) and reverse (3) bias sweep. (b) Output curves with DOS distribution and contact barrier height of 0.38 eV, μ_o= 0.052 cm²/Vs and γ=1.8×10^{-3} (cm/V)$^{0.5}$ (Reprinted from *Organic Electronics*, vol.9, D.Gupta, N. Jeon, S. Yoo, "Modeling the electrical characteristics of TIPS-pentacene thin-film transistors: Effect of contact barrier, field-dependent mobility, and traps", p.1026, 2008, *with permission from Elsevier)*

4. Effect of device design of OTFT

In OTFTs, there is a common issue of difference in device performance of OTFTs fabricated in top contact and bottom contact device configurations (Gundlach et al, 2006; Gupta et al 2009; Roichman et al, 2002; Street et al, 2002). The process difference between the two device designs is that in top contact OTFT, semiconductor is deposited prior to depositing source and drain electrodes, while this is vice versa in bottom contact OTFT. From fabrication point of view, bottom contact OTFT is preferred because in this design the soft organic semiconductor can be protected from harsh chemicals, high temperatures and metal penetration. However, usually bottom contact OTFT show inferior performance, the reasons for which is provided on the basis of large metal-semiconductor contact resistance, irregular deposition or poor morphology of the semiconductor films around the source and drain contacts (Kang et al, 2003; Kymissis et al, 2001; Koch et al, 2002; Lee et al 2006, Schroeder et al, 2003). In the bottom contact OTFT, it is possible that both the contact barrier and the structural inhomogenities in the semiconductor play important role in affecting the charge injection and transport characteristics. However, separating one from the other and finding the dominant role of one of the effects is necessary to properly understand the device operation mechanisms.

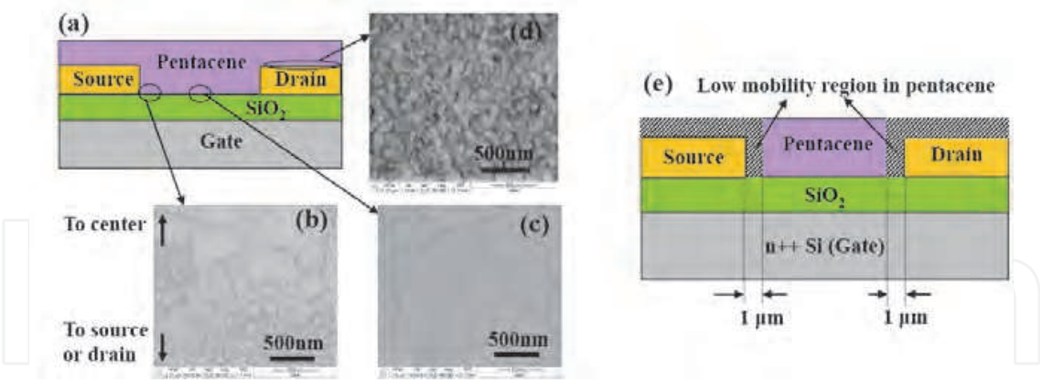


Fig. 5. (a) Schematic of the bottom contact device showing different region of pentacene morphology. Scanning electron micrograph of pentacene on gold contact (b) near gold contact edge on SiO_2, (c) far away from gold contact edge on SiO_2, (d) on gold contacts, and (e) Schematic of the 1μm wide low-mobility-region near the source and drain contact edges and above the contacts in bottom contact devices. (Reprinted from *Organic Electronics, Vol. 10, No. 1,* D. Gupta, M.Katiyar, Deepak**,** "An analysis of difference in device behavior of top and bottom contact devices using device simulation", *pp. 775-784, 2009, with permission from Elsevier)*

The experimental devices consist of n+ Si as gate, 40 nm gold as source and drain electrodes, 200 nm SiO_2 as gate insulator, and pentacene as the organic semiconductor. Pentacene films with thicknesses of 50 nm are deposited by thermal evaporation at the rate of 0.03-0.04 nm/sec at substrate temperature of 65^{o}C. The channel length (L) for both top and bottom contact devices is 30 μm and their widths (W) are 1mm and 3.6mm, respectively. The experimentally obtained data in the output curves were also corrected in order to remove the effects of gate leakage and contact resistances (Gupta et al, 2009). To correct for the gate leakage, half of the gate current is added to the obtained drain current at each gate voltage. In order to correct the device characteristics for the metal-semiconductor contact resistance, device parasitic resistance (R_P) is calculated as a function of gate voltage following the procedures provided in the well- known transmission line method (TLM). R_P estimated by TLM method is then used to correct the drain currents to their equivalent values in a device with no metal-semiconductor contact resistance. From the as measured curves, the extracted field effect mobility for top and bottom contact devices are 0.125 cm^2/Vs and 1.74x10^{-3} cm^2/Vs, respectively, in the saturation region. After the gate leakage and contact resistance correction, an effective mobility of 0.14 cm^2/Vs and 3.2x10^{-3} cm^2/Vs is obtained for the top and bottom contact devices, respectively.

The simulation data obtained from the top and bottom contact device structures overlay on each other, which implies that device structure by itself is not responsible for causing any difference in the two device structures. The other factors then must lay down to the differences in the manner that two devices are fabricated. In bottom contact devices, it is possible that a shadow cast by metal during evaporation of pentacene could lead to unfilled corners at the source/drain contacts, which in turn could result in lower effective device mobility. This kind of situation in the simulation is incorporated by adding a vacuum layer of dimensions 50 nm x 40 nm adjacent to the source and drain electrodes. However, the resultant drain currents are only slightly affected by the unfilled corners, as the current find

a way of charge injection/extraction through the top surface of the source and drain electrodes, respectively. The next possibility, i.e. the effect of morphology of pentacene is then deeply investigated in order to find out the reasons for inferior performance of bottom contact devices. The investigation of pentacene morphology in the different regions of the bottom contact device showed a marked variation in grain sizes. From the scanning electron micrograph of the device in Fig. 5, one can clearly see that the large grain structure far away from the source/drain contact edges changes into a small grain structure as one move closer to the edge of the channel, near the gold electrodes. On SiO_2, the average grain size is 0.57 µm and on the source and drain contacts, the grain size is 0.15 µm. The reason for such a difference in morphology is attributed to the difference in surface energies of metal and dielectric layers.

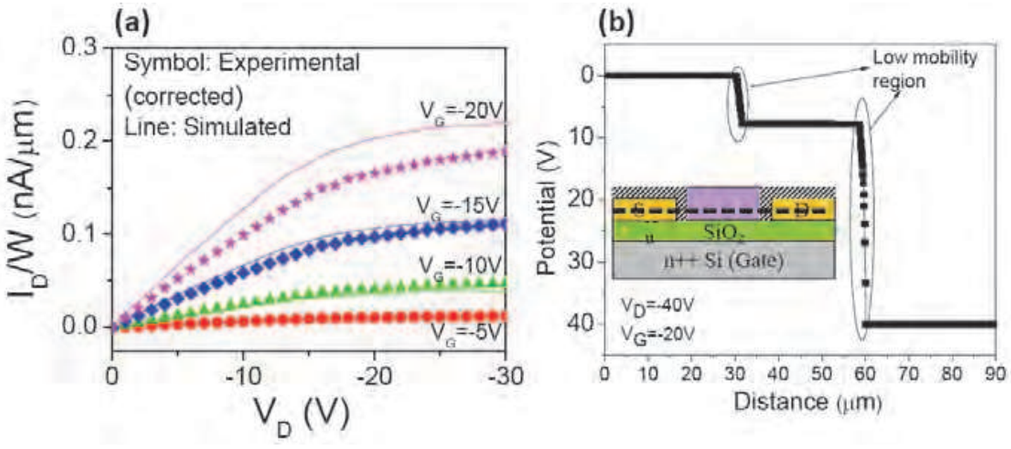


Fig. 6. (a) Comparison of the experimental (gate leakage and contact corrected) and the simulated output curves. The mobility of the low-mobility-region is 1.5x10-4 cm/#/Vs and bulk mobility of pentacene is 0.14 cm^2/Vs. (b) Surface potential profile 1 nm above the dielectric surface (source, drain and channel lie between 0-30 µm, 60-90 µm and 30-60 µm, respectively). (Reprinted from *Organic Electronics, Vol. 10, No. 1,* D. Gupta, M.Katiyar, Deepak, "An analysis of difference in device behavior of top and bottom contact devices using device simulation", *pp. 775-784, 2009, with permission from Elsevier)*

The above mentioned structural features are then incorporated in the simulation model (as depicted in Fig. 5) where a low-mobility-region near the source and drain contact edges and above the contacts is defined in the bottom contact device. The low-mobility-region has lower mobility as compared to the rest of the pentancene, and the reason for such an assignment is attributed to the significantly lower grain size as compared to the bulk film. Keeping the bulk mobility as 0.14 cm^2/Vs, several values of mobility of the low-mobility-region are tried and a mobility value of $1.5x10^{-4}$ cm^2/Vs yields a good comparison with the measured data, as shown in Fig. 6a. The effective mobility calculated from this structure is $1.8x10^{-4}$ cm^2/Vs, which closely matches with the experimental value. In order to analyze the effects of low-mobility-region, potential profiles between the source and drain contacts at 1 nm above the dielectric interface (along a horizontal dashed line in the inset of Fig. 7b) are taken. Figure 6b shows that almost all the applied potential is accommodated in the low-mobility-region, forcing its effect on the overall device characteristics. The current density profiles (Fig. 7a) taken across the bottom contact device depicts that charge injection and

extraction takes place from the lower region of metal contacts (within 5 nm region from the insulator) forcing the current to pass through the low-mobility region and causing a large potential drop. As an analogy, the low-mobility-region in the top contact devices is also introduced below the source and drain electrodes, which spans across the full thickness of pentacene. As an example, a mobility value of $1x10^{-3}cm^2/Vs$ for the low mobility region is taken, but no significant change in the device behaviour could be observed. The reason for this can be understood from the current density profile in Fig. 7b, which clearly indicates that charge is injected from the side/corner of the contacts, bypassing the low-mobility-region. Thus top contact devices would be less susceptible to morphological variations. Therefore, the simulation determines that the possible cause of differences observed in bottom and top contact devices could be due to differences in pentacene morphology leading to low mobility regions near the contacts.

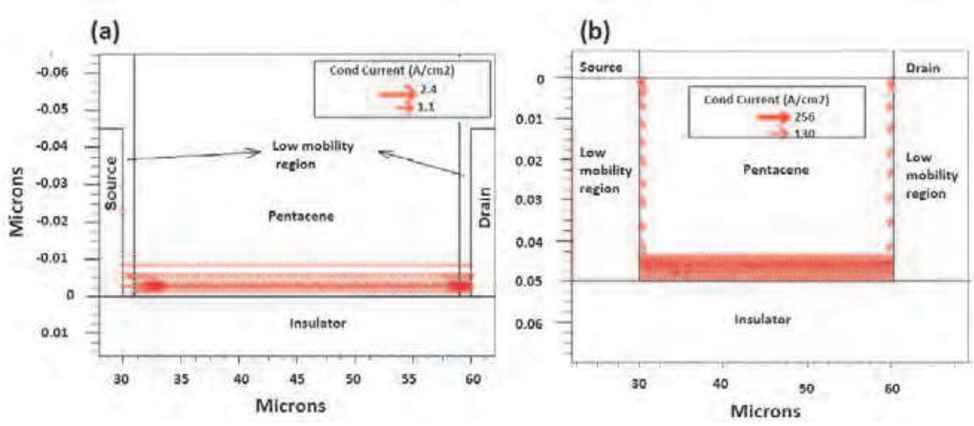


Fig. 7. Schematic diagram for the path of the current flow in pentacene film (line with the arrow) in a (a) bottom contact device having a low-mobility region adjacent to and above the source and drain contacts and in a (b) top contact device having a low-mobility-region under the source and drain contacts. (Reprinted from *Organic Electronics, Vol. 10, No. 1,* D. Gupta, M.Katiyar, Deepak**,** "An analysis of difference in device behavior of top and bottom contact devices using device simulation", *pp. 775-784, 2009, with permission from Elsevier)*

5. Effect of pentacene thickness

The next issue of interest is dependence of device performance on the semiconductor thickness. Theoretically, the device mobility should be independent of semiconductor thickness in TFTs, because the field effect causes all the charges to be accumulated in few nanometers of the semiconductor near the insulator, thus nullifying the effect of the rest of the film (Dinelli et al, 2004; Horowitz et al 2003). However, practically, this is a common observation and the reasons for such an occurrence are explained in terms of organic semiconductor morphology, semiconductor-insulator interfaces, and access resistances (Dodabalapur et al, 2005; Granstrom et al, 1999; Kiguchi et al, 2005; Schroeder et al 2003). Figure 8 shows the mobility dependence of top contact OTFTs based on pentacene for pentacene thicknesses of 10, 20, 35, 50, 80 and 100 nm, respectively. The source and drain electrodes are made of gold, gate is n+ silicon, insulator is 200 nm thick SiO_2, channel width *W* is 1.5 mm and length *L* is 30 µm, respectively. According to the experiments, the mobility

increases until a pentacene thickness of 35 nm, and then it decreases. However, the simulated device characteristics are only very slightly affected by pentacene thickness (Fig. 8a), and not to the extent of experimental observations. Since there is a sufficient mobility variation with pentacene thickness experimentally, it is imperative to incorporate additional features in the simulation in order to model the device characteristics accurately. In the simulation, the physical behavior related to charge transport in the first few layers adjacent to the dielectric is not modeled. However, it is important to note that the first few layers, where most of the charge transport occurs, may have different electronic properties as compared to the bulk film. In literature, it has been demonstrated that the pentacene film near the dielectric may have several structural defects, discontinuities, low surface coverage and may also be affected by charge-surface phonon interaction caused by the polar oxide dielectric (Houilli et al 2006; Kiroval et al, 2003; Puntambekar et al, 2005; Sandberg et al, 2002; Stassen et al, 2004; Steudel et al, 2004; Ruiz et al 2005; Veres et al, 2002). Apart from this, inter layer surface potential between the pentacene layers and polarization interaction energy of the charge in the dielectric may force the mobile carriers more towards the vicinity of the dielectric (Houilli et al 2006; Kiroval et al, 2003; Puntambekar et al, 2005). Based on this discussion, following two points emerge (Gupta et al, 2009):

a. A monolayer of pentacene may have low mobility in comparison to the bulk pentacene. Hereafter this layer is referred as low mobility layer.
b. Mobile charge, for reasons not precisely understood, is preferentially forced to this low mobility region.

These effects are then systematically introduced in the simulation model for a better match with the experimental data. To evaluate the effect of the low mobility layer at the insulator surface, 1.5 nm thick layer (roughly the thickness of a monolayer of pentacene) at the dielectric interface is incorporated, as depicted in the inset of Fig. 8b. The simulations were performed while keeping the bulk mobility value of 0.28 cm^2/Vs, and lowering the mobility of the low-mobility-layer down to several decades. However, the extracted mobility from the simulation increases until pentacene thickness of 35 nm and then becomes almost constant (Fig. 8b). This simulated behaviour is significantly different than the experimental results and thus the second effect, ie charge confinement towards dielectric is investigated subsequently.

Since the commercial simulator in use here does not contain any models to physically simulate the carrier confinement, an energy band offset between the low mobility layer and bulk pentacene is intentionally introduced in the simulation model in such a way that it facilitates the charge migration towards the low mobility layer. Figure 9a shows the energy band diagram of pentacene film depicting the energy band offset between the low mobility layer and the bulk pentacene. To force the mobile charge towards the low mobility layer, the electron affinity (E_A) value of the low mobility layer (E_{A1}) is reduced in comparison to its value in the bulk pentacene (E_{A2}), while keeping the band gap (E_g) value same for both the regions. The combined effect of low-mobility-layer and the charge confinement induced by the above mentioned method is such that the effective mobility of the device reduces significantly as compared to the bulk mobility value. For example, for a pentacene thickness of 50nm, a bulk mobility value of 0.28 cm^2/Vs, a low-mobility-value of 0.014 cm^2/Vs and an energy band-offset of 0.1 eV produce an effective mobility value of 0.09 cm^2/Vs. With several trials and errors, it was observed that the quantitative behavior of mobility up to 35

nm is better matched for an energy band offset value of 0.11 eV, the mobility of low mobility layer as ~1x10^{-4} cm^2/Vs and bulk mobility as 1.3 cm^2/Vs (Fig. 9b). However, as shown in Fig. 9b, after 35 nm, no match could be obtained, which is discussed based on the pentacene morphology variation with thickness, in the next paragraph.

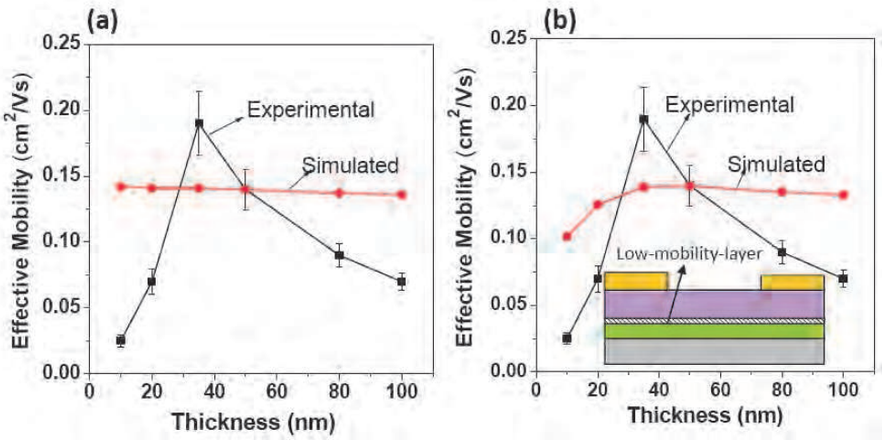


Fig. 8. (a) A comparison of the mobility values for the experimental and the simulated devices and (b) between experimental and simulated devices on incorporating the low-mobility-layer as a function of pentacene thickness. (Reprinted from *Organic Electronics, Vol. 11,* D. Gupta, Y. Hong, "Understanding the effect of semiconductor thickness on device characteristics in organic thin film transistors by way of two dimensional simulations", *pp. 127-136, 2010, with permission from Elsevier)*

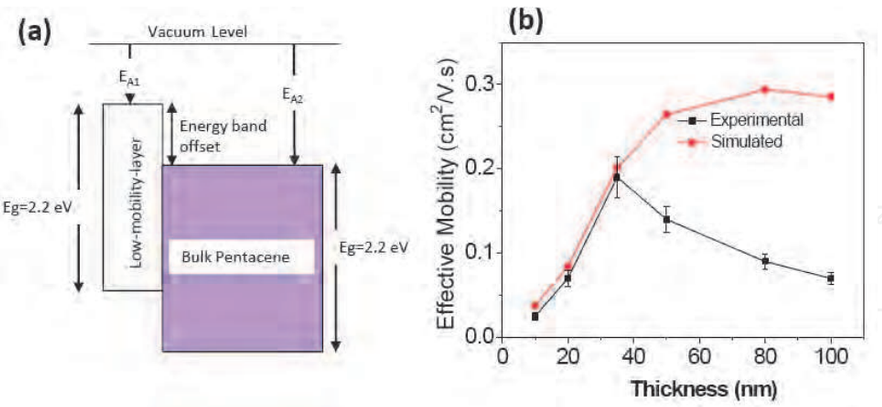


Fig. 9. (a) Schematic diagram of the energy levels in the low mobility layer and bulk of the pentacene film (b) Comparison of experimental and simulated mobility value as a function of pentacene thickness. The mobility of the low-mobility-layer is 1x10^{-4} cm^2/Vs and bulk mobility is 1.3 cm^2/Vs. The energy band offset value is 0.11 eV. (Reprinted from *Organic Electronics, Vol. 11,* D. Gupta, Y. Hong, "Understanding the effect of semiconductor thickness on device characteristics in organic thin film transistors by way of two dimensional simulations", *pp. 127-136, 2010, with permission from Elsevier)*

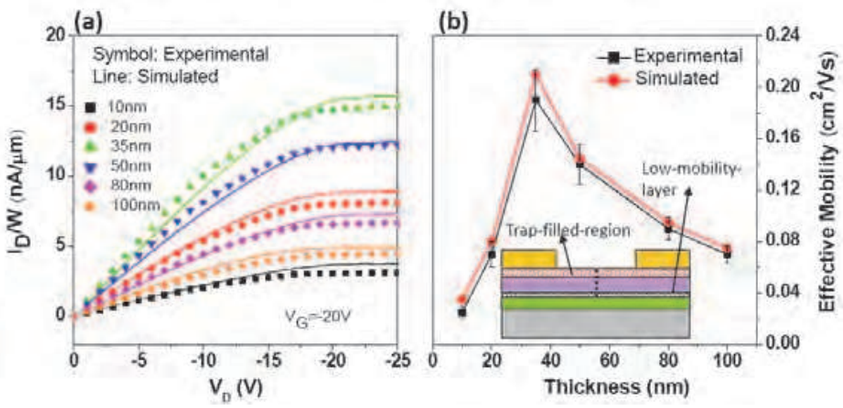


Fig. 10. A comparison of simulated and experimental (a) output curves and (b) mobility value as a function of pentacene thickness. The mobility of the low-mobility-layer and bulk pentacene is taken as $1x10^{-4}$ cm^2/Vs and 1.3 cm^2/Vs, respectively. The energy band offset value is 0.11 eV. The trap concentration is taken as $4x10^{16}$ cm^{-3} for 50 nm thick film and $6x10^{16}$ cm^{-3} for 80 and 100 nm thick films, respectively. (Reprinted from *Organic Electronics, Vol. 11,* D. Gupta, Y. Hong, "Understanding the effect of semiconductor thickness on device characteristics in organic thin film transistors by way of two dimensional simulations", *pp. 127-136, 2010, with permission from Elsevier)*

The investigation of morphology of pentacene films revealed that grain size and crystal structure varies as a function of thickness. It is found that until pentacene thickness of 35 nm, the average grain size remains ~0.85 μm. After further increasing the film thickness, the grain size reduces and reaches to 0.15 μm for the 100 nm thick pentacene films. The reduction in grain size causes more grain boundaries to appear, which acts as trapping centers for the mobile charge. The bulk traps in the region above 35 nm of pentacene thickness are then introduced, as illustrated in the inset of Fig. 10b. It was found that the donor type traps with a trap level of 0.4eV, produces a reasonable match between the experimental and simulated curves, if bulk donor trap concentration of $4x10^{16}$ cm^{-3} for 50 nm thick film and $6x10^{16}$ cm^{-3} for 80 and 100 nm thick films, respectively, are chosen. Figure 10a and 10b show the superimposed experimental and simulated results of the output curves and mobility values, respectively. Therefore, this study indicates that OTFT devices face several non-regularities, which are expressed in the form of low-mobility of the pentacene layers that are associated with the dielectric, existence of energy band offset between the interface layers and the bulk, and the bulk traps due to the structural defects like grain boundaries. The combined effect of these features causes the extracted mobility to depend on the film thickness, which in an ideal case should have been absent. It also signifies the importance of optimizing the thickness of organic semiconductor in order to have enhanced as well as reliable device performance.

6. Device stability of solution processed ZnO TFTs under electrical stress

Device stability of TFTs under electrical stress is highly important in view of practicality, which is not only important in estimating the device lifetime but also in understanding the instability mechanisms. Electrical instability in TFTs is typically measured by threshold voltage (V_T) shift that occurs when the device is subjected to constant voltage or drain current

for certain duration (Wehrspon et 2003, Jahinuzzaman et al, 2005). During constant gate bias, the channel charge and hence the on current continuously decreases to eventually saturate the V_T shift. On the other hand, during constant current stress the applied gate bias continually adjusts itself in time to keep the drain current constant. Also important is the post-stress relaxation characteristics of the device, where V_T shift occurring during the stress state is recovered in the off-state. From a practical point of view, this situation occurs in displays or integrated circuits where the device is temporarily switched on, and then switched off.

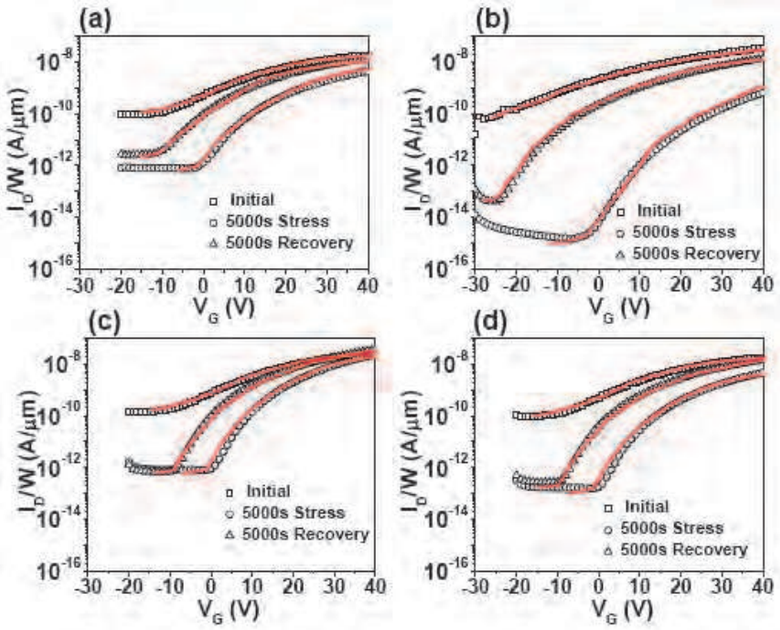


Fig. 11. Measured (symbol) and simulated (line) transfer characteristics showing initial curve, after stressing for 5000 sec and after relaxation for 5000 sec for stress values of (a) 20 V of gate bias, (b) 50 V of gate bias and (c) $5x10^{-6}$ A of drain current and (d) $3x10^{-5}$ A of drain current.

The ZnO-TFT is fabricated in a simple bottom-gate top-contact configuration. In this device, n++ silicon wafer served as gate electrode, Al as source and drain electrode, 100 nm-thick SiO_2 film as gate insulator onto which sol-gel processed ZnO films are spin-coated. The sol is prepared by making a 0.5 M solution of zinc acetate in the solvent mixture of DMF and methoxy-ethanol (volume ratio=3:2) (Gupta et al, 2008) and then spin-coated twice on the wafer. The films were pyrolyzed at 500°C for 1 hour, yielding polycrystalline films with an average grain size of 300 nm. The channel width is 1.0 mm and channel length is 50 μm, respectively. During electrical stress measurements in bias stress mode, a voltage is applied only to the gate while keeping the source and drain grounded in order to create a uniform electric field across the channel interface. During the current stressing, a constant current was applied to the drain keeping the gate and drain connected in a diode-connected configuration, while keeping the source grounded. This measurement configuration allows automatic adjustment of the gate/drain to source voltage (V_{GS}=V_{DS}) to achieve a constant drain current. The relaxation characteristics are measured soon after the stressing period of 5000 sec, while keeping all three terminals grounded. Figure 11a – 11d shows the obtained

stress- recovery characteristics of the device in the gate bias (gate bias value = 20V and 50V) and current stress (current stress value= $5x10^{-6}$ A and $3x10^{-5}$ A) mode, respectively. As shown in Fig. 11, for both the gate bias and current stress, the on- current decreases and transfer curves shift to more positive gate voltages leading to a positive threshold voltage shift. Additionally, off- currents (V_G = -30 V) are reduced to a greater extent than the on current (V_G = 40V) in the stressing period of 5000 sec, which causes an improvement in the on/off ratio of the device. Also, to be noted is that in the first $2x10^3$ sec of the stressing period approximately, the change in the off current and subthreshold slope (S) is maximum, after which this variation is not that significant. However, under both the voltage and current stress conditions, the transfer curves keep on shifting to the higher positive gate voltage values without change in S value. The mobility values, on the other hand, continue to decrease for the whole stress period. During the recovery period, the transfer curves shift in a parallel way towards negative value for approximately 2000 s, and then S/off-current values increase slowly on relaxing the devices subsequently. However, the initial on drain-current values could not be fully recovered in the measured period of 5000 sec.

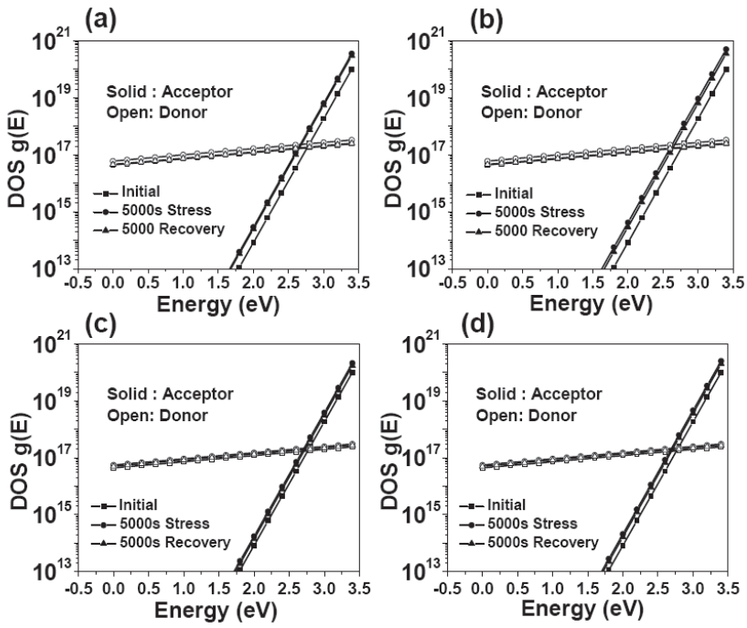


Fig. 12. Variation in density of states (DOS) during stress and recovery period for stress values of (a) 20 V of gate bias, (b) 50 V of gate bias and (c) $5x10^{-6}$ A of drain current and (d) $3x10^{-5}$ A of drain current.

In order to investigate deeply into the microscopic details of the instability mechanisms, we performed two dimensional device simulations by modelling ZnO films with a continuous and spatially uniform density of states (DOS) throughout its volume. This assumption is based on the fine grain structure of sol-gel ZnO films, which can be considered as composed of small crystalline grains embedded in an amorphous matrix. This kind of structure may produce a large defect density within the grain boundaries as well as in the grains. The total density of states g(E) is assumed to have exponential distribution of donor (D) like and acceptor (A) like defects that follow the equations 4a and 4c, respectively. This DOS model is attractive because of its simplicity and accuracy and has been used as the basis for many

studies on metal oxide based TFTs (Hossain et al, 2003, 2004; Fung et al, 2009; Ming et al, 2009) . Additionally, traps at the semiconductor – dielectric interface are assumed, which are defined by their concentration (N_{it}) and energy level (E_{it}). Also shown in Fig. 11 are the simulated transfer characteristics using the above mentioned DOS model during stress and recovery. The obtained DOS distribution is shown in Fig. 12, and the values of N_{it} and E_{it} are listed in Table 2. It is to be noted that since off-current region in the transfer curves invariably exists in the negative gate voltage region, donor states have to be kept near conduction band edge (above mid-gap) in order to reproduce the observed behavior. The donor-like states near the mid-gap tend to be a recombination-generation center, helping electrons jump to the conduction band and increasing the leakage current. The acceptor states, on the other hand, extend far below the conduction band and reach up to the mid-gap, which signifies the importance of deep lying defect states in affecting the transfer curves during the stress measurements. Also, important is the role of deep donor traps (1.0 -1.2 eV from the conduction band) at the semiconductor-dielectric interface, which better reproduce the simulated behavior of the off-state leakage currents. On the basis of this model, N_{it} increases by approximately 24 - 30% after stressing the devices for a period of 5000 sec from the virgin state, but is not affected much during the recovery period of 5000 sec.

	Initial		**Stress (5000 sec)**		**Recovery (5000 sec)**	
	N_{it} (cm^{-2})	E_{it} (eV)	N_{it} (cm^{-2})	E_{it} (eV)	N_{it} (cm^{-2})	E_{it} (eV)
20V	$8.4x10^{11}$	1.13	$1.1x10^{12}$	1.16	$1.0x10^{12}$	1.16
50V	$9.3x10^{11}$	1.05	$1.2x10^{12}$	1.03	$1.1x10^{12}$	1.05
$5x10^{-6}$ A	$7.3x10^{11}$	1.09	$9.1x10^{11}$	1.1	$8.9x10^{11}$	1.1
$3x10^{-5}$ A	$8.1x10^{11}$	1.09	$9.3x10^{11}$	1.08	$8.3x10^{11}$	1.08

Table 2. Simulated values of N_{it} and E_{it} of the donor- like traps at semiconductor-dielectric interface for the initial state, after stressing for 5000 sec, and after relaxation for 5000 sec for different gate bias and drain current stress conditions.

The obtained DOS, as in Fig. 12, indicates that acceptor and donor states both vary from virgin to stress state and from stress to recovery state , however, acceptor like defect states are higher in density than the donor like defect states in the region near the conduction band (approximately 0.7 eV from the conduction band). The acceptor like defects also have pronounced effect in this region and affects the transfer curves significantly. Further, it was observed that the variation in N_{TA} and N_{TD} values from virgin to stress state and from stress to recovery state has more dominant effect than the change in slope values (W_{TA} and W_{TD}). An estimate of change in values of N_{TA} and N_{TD} from virgin to stress state and from stress to recovery state revealed that N_{TA} increases approximately 40% more than N_{TD} after stressing the device for a period of 5000 sec from the virgin state, for all the gate bias and current stress levels. This variation in N_{TA} is also significantly more than donor-like states during the recovery period. These results make it clear that acceptor like defects are substantially influential in affecting both the stress and recovery characteristics. This also explains the decrease in S value, positive V_T shift and relatively larger reduction in off currents on stressing the devices, because acceptor like defects strongly affects both the subthreshold and above threshold region.

Based on the simulation results, it is possible to correlate the electrical stress effect to the inherent defect chemistry of ZnO, ambient and to the ZnO-dielectric interface. In ZnO crystals and films, oxygen vacancies and zinc interstitials are identified as the two most common metastable defects (Ashrafi et al, 2007; Özgür et al, 2005). Whereas, positively charged oxygen vacancies can behave as acceptor-like traps, zinc interstitials act as donor defects. The oxygen vacancies tend to trap free electron carriers by a long-range coulomb interaction, which causes a positive shift of the transfer curves. Additionally, oxygen or water may get adsorbed on the surface of films, which predominantly create acceptor-like states in zinc oxide based materials (Chen et al, 2010; Li et al, 2005). Though further detailed studies are needed to distinguish between the operating mechanisms affecting the instability, we can say that the main degradation mechanism is the trapping by acceptor-like defects in upper half of the bandgap of solution processed ZnO, and donor-like trap generation at the semiconductor-dielectric interface.

7. Effect of Li- doping on environmental stability of ZnO TFTs

In solution processed Li-doped ZnO TFTs, Al serves as source and drain electrodes, ITO as gate electrode, and 215nm thick aluminium-tin-oxide (ATO) as insulator. The channel length (L) is 50 µm and width (W) is 1000 µm, respectively. Li-ZnO is coated from a precursor solution following thermal pyrolysis (Nayak et al, 2009). The investigated Li concentrations were 0%, 15% and 25%, and the device characteristics were checked in fresh state and after 7 days of exposure. First, the similar methodology developed in section 6 was adopted that used density of states as exponential distribution of both acceptor and donor –like traps. However, for any set of values of N_{TA}, N_{TD}, W_{TA} and W_{TD}, it was observed that simulated results using this DOS model was only partially successful for ach amount of Li doping. More specifically, the subthreshold region which is highly dependent on donor like traps showed a large amount of deviation in the exposed states. Therefore, another model which Gaussian distribution of both acceptor and donor – like traps is adopted to define the DOS states in these devices. This model too cannot reproduce the experimental device characteristics fully. Based on the above observations, a DOS model that combines exponential distribution of acceptor (A) like defects and Gaussian distribution of donor (D) like defects are employed that follow the expressions in Eq. 4.

Figure 13a and 13b shows the optimized fittings to the experimental transfer characteristics, using the DOS model in Eq. 4, for 0%, 15% and 25% Li-doped ZnO, respectively, in the fresh state and after 7 days of air exposure. The fitting parameters are listed in Table 3 and the obtained DOS distribution is shown in Fig. 14. As can be seen from Fig. 14, the density of acceptor states near the conduction band tail edge is higher, while they are significantly lower as one goes deep down the bandgap, for the devices with 25% Li- doping in comparison to devices without Li-doping. This arises due to the different slope values (W_{TA}) for devices with and without Li-doping. On the other hand, the donor states are significantly lesser in the devices with 25% Li-doping as compared to the devices without doping, in both the fresh and exposed states. Also, in the devices without Li-doping, both the donor and acceptor states increase on exposing the devices to the environment. However, in the case of devices with 25% Li-doping, the donor states showed a slight increase, while acceptor states decrease slightly, on exposing the devices. This might also arise due to some error in fitting parameters. On the whole, however, the devices with 25% Li-doping are not significantly affected by the environmental exposure.

Therefore, these results can partially explain the better performance of Li-doped TFTs in terms of improved subthreshold slope, better on/off ratio and improved air stability than the undoped ones. Also, it can be clearly said that Li- doping is effective in controlling the defect states in ZnO TFTs, which helps in improving its stability when exposed to the air for a prolonged period of time.

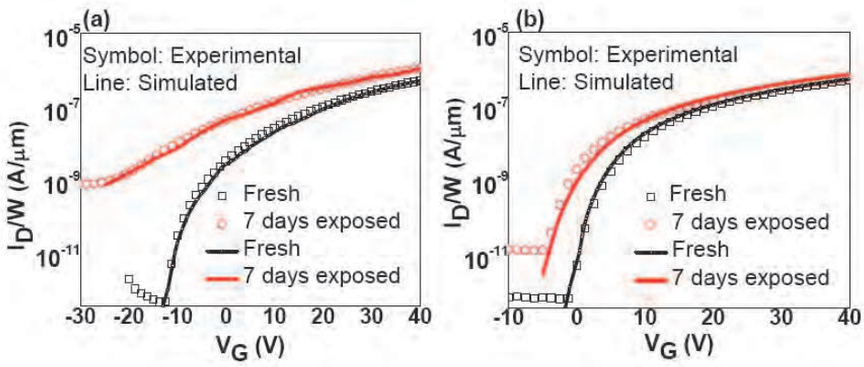


Fig. 13. Comparison of simulated and experimental transfer curves for (a) undoped and (b) 25% Li- doped ZnO TFTs in fresh state and after 7 days of air exposure at drain voltage of 40 V.

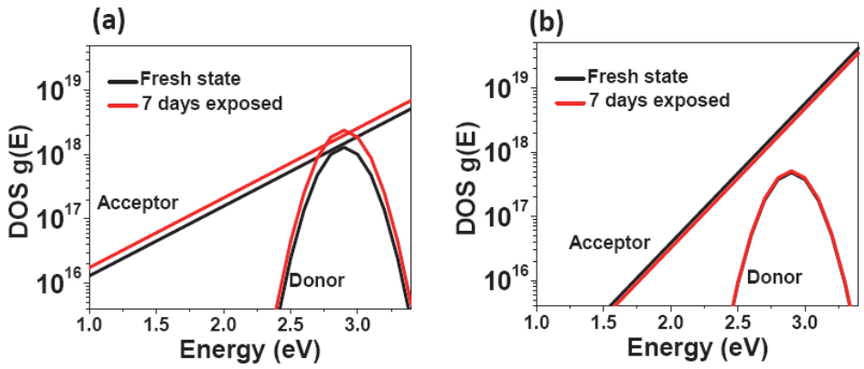


Fig. 14. The obtained density of states (DOS) distribution in the fresh state and after 7 days of air exposure for (a) undoped and (b) 25% Li- doped ZnO TFTs

	0% Li		**25 % Li**	
	Fresh	***Exposed***	***Fresh***	***Exposed***
N_{TA} (cm^{-3})	5.2x10^{18}	7x10^{18}	4.2x10^{19}	3.5x10^{19}
W_{TA} (*eV*)	0.4	0.4	0.2	0.2
N_{GD} (cm^{-3})	1.3x10^{18}	2.4x10^{18}	4.8x10^{17}	5.1x10^{17}
E_{GD} (*eV*)	0.5	0.5	0.5	0.5
W_{GD} (*eV*)	0.2	0.2	0.2	0.2

Table 3. List of fitting parameters for undoped and 25 % Li –doped ZnO TFTs

8. Conclusion

In conclusion, the important role of device simulations in a better understanding of the material properties and device mechanisms is recognized in TFTs based on organic and metal oxide semiconductors. The effect of physical behaviour related to semiconductor film properties in relation to charge injection and charge transport is underlined by providing illustrations from pentacene, TIPS- pentacene and ZnO based TFTs. The device simulations significantly help in explaining the complex device phenomenon that occur at the metal-semiconductor interface, semiconductor-dielectric interface, and in the semiconductor film in the form of defect distribution.

9. References

Alam, M. A., Dodabalapur, A. & Pinto, M. R. (1997), "A two-dimensional simulation of organic transistors." *Ieee Transactions on Electron Devices,* Vol. 44, No. 8, pp. 1332-1337, ISSN 0018-9383

Ashrafi, A. & Jagadish, C. (2007), "Review of zincblende ZnO: Stability of metastable ZnO phases." *Journal of Applied Physics,* Vol. 102, No. 7, pp. 71101-71113, ISSN 0021-8979

Bolognesi, A., Di Carlo, A.&Lugli, P. (2002), "Influence of carrier mobility and contact barrier height on the electrical characteristics of organic transistors." *Applied Physics Letters,* Vol. 81, No. 24, pp. 4646-4648, ISSN 0003-6951

Scott, J. C. & Bozano, L. D. (2007), "Nonvolatile memory elements based on organic materials." *Advanced Materials,* Vol. 19, No. 11, pp. 1452-1463, ISSN 0935-9648

Cherian, S., Donley, C., Mathine, D., LaRussa, L., Xia, W. & Armstrong, N. (2004), "Effects of field dependent mobility and contact barriers on liquid crystalline phthalocyanine organic transistors." *Journal of Applied Physics,* Vol. 96, No. 10, pp. 5638-5643, ISSN 0021-8979

Chen, Y. C., Chang, T. C., Li, H. W., Chen, S. C., Lu, J., Chung, W. F., Tai, Y. H. & Tseng, T. Y. (2010), "Bias-induced oxygen adsorption in zinc tin oxide thin film transistors under dynamic stress." *Applied Physics Letters,* Vol. 96, No. 26, pp. 262104-262107, ISSN 0003-6951

Dinelli, F., Murgia, M., Levy, P., Cavallini, M., Biscarini, F. & de Leeuw, D. M. (2004), "Spatially correlated charge transport in organic thin film transistors." *Physical Review Letters,* Vol. 92, No. 11, pp. 116802 -, ISSN 0031-9007

Dodabalapur, A., Torsi, L. & Katz, H. E. (1995), "Organic Transistors - 2-Dimensional Transport and Improved Electrical Characteristics." *Science,* Vol. 268, No. 5208, pp. 270-271, ISSN 0036-8075

Fortunato, E., Correia, N., Barquinha, P., Pereira, L., Goncalves, G.&Martins, R. (2008), "High-performance flexible hybrid field-effect transistors based on cellulose fiber paper." *Ieee Electron Device Letters,* Vol. 29, No. 9, pp. 988-990, ISSN 0741-3106

Fung, T. C., Chuang, C. S., Chen, C., Abe, K., Cottle, R., Townsend, M., Kumomi, H.&Kanicki, J. (2009), "Two-dimensional numerical simulation of radio frequency sputter amorphous In-Ga-Zn-O thin-film transistors." *Journal of Applied Physics,* Vol. 106, No. 8, pp. 84511-84521, ISSN 0021-8979

Granstrom, E. L. & Frisbie, C. D. (1999), "Field effect conductance measurements on thin crystals of sexithiophene." *Journal of Physical Chemistry B,* Vol. 103, No. 42, pp. 8842-8849, ISSN 1089-5647

Gundlach, D. J., Zhou, L., Nichols, J. A., Jackson, T. N., Necliudov, P. V.&Shur, M. S. (2006), "An experimental study of contact effects in organic thin film transistors." *Journal of Applied Physics,* Vol. 100, No. 2, pp. 024509-024512, ISSN 0021-8979

Gupta, D., Anand, M., Ryu, S. W., Choi, Y. K.&Yoo, S. (2008), "Nonvolatile memory based on sol-gel ZnO thin-film transistors with Ag nanoparticles embedded in the ZnO/gate insulator interface." *Applied Physics Letters,* Vol. 93, No. 22, pp. 224106-224108, ISSN 0003-6951

Gupta, D., Jeon, N.&Yoo, S. (2008), "Modeling the electrical characteristics of TIPS-pentacene thin-film transistors: Effect of contact barrier, field-dependent mobility, and traps." *Organic Electronics,* Vol. 9, No. 6, pp. 1026-1031, ISSN 1566-1199

Gupta, D.&Hong, Y. (2010), "Understanding the effect of semiconductor thickness on device characteristics in organic thin film transistors by way of two-dimensional simulations." *Organic Electronics,* Vol. 11, No. 1, pp. 127-136, ISSN 1566-1199

Gupta, D., Katiyar, M.&Gupta, D. (2009), "An analysis of the difference in behavior of top and bottom contact organic thin film transistors using device simulation." *Organic Electronics,* Vol. 10, No. 5, pp. 775-784, ISSN 1566-1199

Hill, I. G. (2005), "Numerical simulations of contact resistance in organic thin-film transistors." *Applied Physics Letters,* Vol. 87, No. 16, pp. 63514-63516, ISSN 0003-6951

Horowitz, G. (2003), "Tunneling current in polycrystalline organic thin-film transistors." *Advanced Functional Materials,* Vol. 13, No. 1, pp. 53-60, ISSN 1616-301X

Hossain, F. M., Nishii, J., Takagi, S., Ohtomo, A., Fukumura, T., Fujioka, H., Ohno, H., Koinuma, H. & Kawasaki, M. (2003), "Modeling and simulation of polycrystalline ZnO thin-film transistors." *Journal of Applied Physics,* Vol. 94, No. 12, pp. 7768-7777, ISSN 0021-8979

Hossain, F. M., Nishii, J., Takagi, S., Sugihara, T., Ohtomo, A., Fukumura, T., Koinuma, H., Ohno, H.&Kawasaki, M. (2004), "Modeling of grain boundary barrier modulation in ZnO invisible thin film transistors." *Physica E-Low-Dimensional Systems & Nanostructures,* Vol. 21, No. 2-4, pp. 911-915, ISSN 1386-9477

Houili, H., Picon, J. D., Zuppiroli, L.&Bussac, M. N. (2006), "Polarization effects in the channel of an organic field-effect transistor." *Journal of Applied Physics,* Vol. 100, No. 2, pp. 23702-23706, ISSN 0021-8979

Jahinuzzaman, S. M., Sultana, A., Sakariya, K., Servati, P.&Nathan, A. (2005), "Threshold voltage instability of amorphous silicon thin-film transistors under constant current stress." *Applied Physics Letters,* Vol. 87, No. 2, pp. 23502-23505, ISSN 0003-6951

Ishii, H., Sugiyama, K., Ito, E.&Seki, K. (1999), "Energy level alignment and interfacial electronic structures at organic metal and organic organic interfaces." *Advanced Materials,* Vol. 11, No. 8, pp. 605-+, ISSN 0935-9648

Kahn, A., Koch, N.&Gao, W. Y. (2003), "Electronic structure and electrical properties of interfaces between metals and pi-conjugated molecular films." *Journal of Polymer Science Part B-Polymer Physics,* Vol. 41, No. 21, pp. 2529-2548, ISSN 0887-6266

Kang, J. H.&Zhu, X. Y. (2003), "Pi-stacked pentacene thin films grown on Au(111)." *Applied Physics Letters,* Vol. 82, No. 19, pp. 3248-3250, ISSN 0003-6951

Kiguchi, M., Yoshikawa, G., Ikeda, S.&Saiki, K. (2005), "Electronic properties of metal-induced gap states formed at alkali-halide/metal interfaces." *Physical Review B,* Vol. 71, No. 15, pp. 353321-353324, ISSN 1098-0121

Kirova, N.&Bussac, M. N. (2003), "Self-trapping of electrons at the field-effect junction of a molecular crystal." *Physical Review B,* Vol. 68, No. 23, pp. 235312 -235316, ISSN 1098-0121

Koch, N., Ghijsen, J., Johnson, R. L., Schwartz, J., Pireaux, J. J.&Kahn, A. (2002), "Physisorption-like interaction at the interfaces formed by pentacene and samarium." *Journal of Physical Chemistry B,* Vol. 106, No. 16, pp. 4192-4196, ISSN 1520-6106

Knipp, D., Street, R. A., Volkel, A.&Ho, J. (2003), "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport." *Journal of Applied Physics,* Vol. 93, No. 1, pp. 347-355, ISSN 0021-8979

Kymissis, I., Dimitrakopoulos, C. D.&Purushothaman, S. (2001), "High-performance bottom electrode organic thin-film transistors." *Ieee Transactions on Electron Devices,* Vol. 48, No. 6, pp. 1060-1064, ISSN 0018-9383

Lee, K. S., Smith, T. J., Dickey, K. C., Yoo, J. E., Stevenson, K. J.&Loo, Y. L. (2006), "High-resolution characterization of pentacene/polyaniline interfaces in thin-film transistors." *Advanced Functional Materials,* Vol. 16, No. 18, pp. 2409-2414, ISSN 1616-301X

Li, Q. H., Gao, T., Wang, Y. G.&Wang, T. H. (2005), "Adsorption and desorption of oxygen probed from ZnO nanowire films by photocurrent measurements." *Applied Physics Letters,* Vol. 86, No. 12, pp. 123117-123120, ISSN 0003-6951

Masuda, S., Kitamura, K., Okumura, Y., Miyatake, S., Tabata, H.&Kawai, T. (2003), "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties." *Journal of Applied Physics,* Vol. 93, No. 3, pp. 1624-1630, ISSN 0021-8979

Zhou, Y. M., He, Y. G., Lu, A. X.&Wan, Q. (2009), "Simulation of grain boundary effect on characteristics of ZnO thin film transistor by considering the location and orientation of grain boundary." *Chinese Physics B,* Vol. 18, No. 9, pp. 3966-3969, ISSN 1674-1056

McCluskey, M. D.&Jokela, S. J. (2009), "Defects in ZnO." *Journal of Applied Physics,* Vol. 106, No. 7, pp. -, ISSN 0021-8979

Nayak, P. K., Jang, J., Lee, C.&Hong, Y. (2009), "Effects of Li doping on the performance and environmental stability of solution processed ZnO thin film transistors." *Applied Physics Letters,* Vol. 95, No. 19, pp. 71101-71113, ISSN 0003-695

Nelson, S. F., Lin, Y. Y., Gundlach, D. J.&Jackson, T. N. (1998), "Temperature-independent transport in high-mobility pentacene transistors." *Applied Physics Letters,* Vol. 72, No. 15, pp. 1854-1856, ISSN 0003-6951

Ozgur, U., Alivov, Y. I., Liu, C., Teke, A., Reshchikov, M. A., Dogan, S., Avrutin, V., Cho, S. J.&Morkoc, H. (2005), "A comprehensive review of ZnO materials and devices." *Journal of Applied Physics,* Vol. 98, No. 4, pp. 41301-41404, ISSN 0021-8979

Ostroverkhova, O., Cooke, D. G., Hegmann, F. A., Tykwinski, R. R., Parkin, S. R.&Anthony, J. E. (2006), "Anisotropy of transient photoconductivity in functionalized pentacene single crystals." *Applied Physics Letters,* Vol. 89, No. 19, pp. -, ISSN 0003-6951

Park, S. K., Jackson, T. N., Anthony, J. E.&Mourey, D. A. (2007), "High mobility solution processed 6,13-bis(triisopropyl-silylethynyl) pentacene organic thin film transistors." *Applied Physics Letters,* Vol. 91, No. 6, pp. 63514 -63516, ISSN 0003-6951

Pesavento, P. V., Puntambekar, K. P., Frisbie, C. D., McKeen, J. C.&Ruden, P. P. (2006), "Film and contact resistance in pentacene thin-film transistors: Dependence on film thickness, electrode geometry, and correlation with hole mobility." *Journal of Applied Physics,* Vol. 99, No. 9, pp. 94504-94508, ISSN 0021-8979

Pope, M. & Swenberg, C. E. (1999) Electronic Processes in Organic Crystals and Polymers ~Oxford University Press, New York

Puntambekar, K., Dong, J. P., Haugstad, G.&Frisbie, C. D. (2006), "Structural and electrostatic complexity at a pentacene/insulator interface." *Advanced Functional Materials,* Vol. 16, No. 7, pp. 879-884, ISSN 1616-301X

Roichman, Y.&Tessler, N. (2002), "Structures of polymer field-effect transistor: Experimental and numerical analyses." *Applied Physics Letters,* Vol. 80, No. 1, pp. 151-153, ISSN 0003-6951

Ruiz, R., Papadimitratos, A., Mayer, A. C.&Malliaras, G. G. (2005), "Thickness dependence of mobility in pentacene thin-film transistors." *Advanced Materials,* Vol. 17, No. 14, pp. 1795-+, ISSN 0935-9648

Sandberg, H. G. O., Frey, G. L., Shkunov, M. N., Sirringhaus, H., Friend, R. H., Nielsen, M. M.&Kumpf, C. (2002), "Ultrathin regioregular poly(3-hexyl thiophene) field-effect transistors." *Langmuir,* Vol. 18, No. 26, pp. 10176-10182, ISSN 0743-7463

Scheinert, S.&Paasch, G. (2004), "Fabrication and analysis of polymer field-effect transistors." *Physica Status Solidi a-Applied Research,* Vol. 201, No. 6, pp. 1263-1301, ISSN 0031-8965

Schroeder, P. G., France, C. B., Park, J. B.&Parkinson, B. A. (2003), "Orbital alignment and morphology of pentacene deposited on Au(111) and SnS2 studied using photoemission spectroscopy." *Journal of Physical Chemistry B,* Vol. 107, No. 10, pp. 2253-2261, ISSN 1520-6106

Schroeder, R., Majewski, L. A.&Grell, M. (2003), "A study of the threshold voltage in pentacene organic field-effect transistors." *Applied Physics Letters,* Vol. 83, No. 15, pp. 3201-3203, ISSN 0003-6951

Sebastian, L., Weiser, G.&Bassler, H. (1981), "Charge-Transfer Transitions in Solid Tetracene and Pentacene Studied by Electro-Absorption." *Chemical Physics,* Vol. 61, No. 1-2, pp. 125-135, ISSN 0301-0104

Sheraw, C. D., Jackson, T. N., Eaton, D. L.&Anthony, J. E. (2003), "Functionalized pentacene active layer organic thin-film transistors." *Advanced Materials,* Vol. 15, No. 23, pp. 2009-2011, ISSN 0935-9648

Silinsh, E.A. and Čápek, V. (1980) Organic Molecular Crystals. Their Electronic States., New York

Silinsh, E. A., Klimkans, A., Larsson, S.&Capek, V. (1995), "Molecular Polaron States in Polyacene Crystals - Formation and Transfer Processes." *Chemical Physics,* Vol. 198, No. 3, pp. 311-331, ISSN 0301-0104

Stassen, A. F., de Boer, R. W. I., Iosad, N. N.&Morpurgo, A. F. (2004), "Influence of the gate dielectric on the mobility of rubrene single-crystal field-effect transistors." *Applied Physics Letters,* Vol. 85, No. 17, pp. 3899-3901, ISSN 0003-6951

Steudel, S., De Vusser, S., De Jonge, S., Janssen, D., Verlaak, S., Genoe, J.&Heremans, P. (2004), "Influence of the dielectric roughness on the performance of pentacene transistors." *Applied Physics Letters,* Vol. 85, No. 19, pp. 4400-4402, ISSN 0003-6951

Street, R. A.&Salleo, A. (2002), "Contact effects in polymer transistors." *Applied Physics Letters,* Vol. 81, No. 15, pp. 2887-2889, ISSN 0003-6951

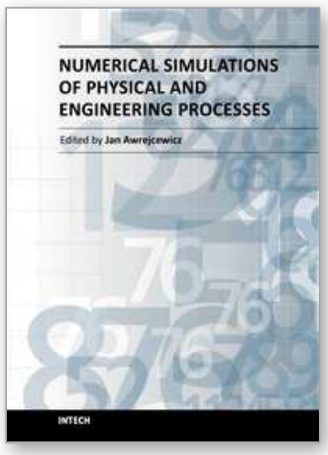
Street, R. A., Knipp, D.&Volkel, A. R. (2002), "Hole transport in polycrystalline pentacene transistors." *Applied Physics Letters,* Vol. 80, No. 9, pp. 1658-1660, ISSN 0003-6951

Tessler, N.&Roichman, Y. (2001), "Two-dimensional simulation of polymer field-effect transistor." *Applied Physics Letters,* Vol. 79, No. 18, pp. 2987-2989, ISSN 0003-6951

Veres, J., Ogier, S. D., Leeming, S. W., Cupertino, D. C.&Khaffaf, S. M. (2003), "Low-k insulators as the choice of dielectrics in organic field-effect transistors." *Advanced Functional Materials,* Vol. 13, No. 3, pp. 199-204, ISSN 1616-301X

Wang, L. A., Fine, D., Basu, D.&Dodabalapur, A. (2007), "Electric-field-dependent charge transport in organic thin-film transistors." *Journal of Applied Physics,* Vol. 101, No. 5, pp. 54515-54519, ISSN 0021-8979

Wehrspohn, R. B., Powell, M. J.&Deane, S. C. (2003), "Kinetics of defect creation in amorphous silicon thin film transistors." *Journal of Applied Physics,* Vol. 93, No. 9, pp. 5780-5788, ISSN 0021-8979



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Numerical Simulations of Physical and Engineering Process is an edited book divided into two parts. Part I devoted to Physical Processes contains 14 chapters, whereas Part II titled Engineering Processes has 13 contributions. The book handles the recent research devoted to numerical simulations of physical and engineering systems. It can be treated as a bridge linking various numerical approaches of two closely inter-related branches of science, i.e. physics and engineering. Since the numerical simulations play a key role in both theoretical and application oriented research, professional reference books are highly needed by pure research scientists, applied mathematicians, engineers as well post-graduate students. In other words, it is expected that the book will serve as an effective tool in training the mentioned groups of researchers and beyond.

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