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## Radiation Hardness of Flash and Nanoparticle Memories

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### 1. Introduction

Recently, the research for new non-volatile memory in the semiconductor industry has become intense, because current flash memory technologies based on the floating-gate (FG) concept are expected to be difficult to scale down for high density, high performance devices (Lankhorst et al., 2005 ; Ouyang et al., 2004 ; Vanheusden et al., 1997). Therefore, a type of non-volatile memory using nanoparticles (NP) as floating gates has attracted much research attention because of its excellent memory performance and high scalability (Tiwari et al., 1996; Park et al., 2002). By utilizing discrete NP as the charge storage element, NP memory is more immune to local oxide defects than flash memory, thus exhibiting longer retention time and allowing more aggressive tunnel oxide scaling than conventional flash memory (Blauwe, 2002; Hanafi et al., 1996). In NP memory, the device performance and reliability depend on many factors, such as the ability to control NP size, size distribution, crystallinity, area density, oxide passivation quality, and the isolation that prevents lateral charge conduction in the NP layer (Ostraat et al., 2001). Thus, NP memory has driven extensive efforts to form NP acting as charging and discharging islands by various methods. Up to now, several techniques have been developed to form uniform NP in gate oxides. For example, Kim (Kim et al., 1999) employed low pressure chemical vapour deposition (LPCVD) to fabricate Si NP with a 4.5 nm average size and  $5 \times 10^{11} \text{cm}^{-2}$  average density. King (King et al., 1998) fabricated Ge NPs by oxidation of a SiGe layer formed by ion implantation, and demonstrated quasi-nonvolatile memory operation with a 0.4 V threshold-voltage shift. Takata (Takata et al., 2003) applied a sputtering method with a special target to fabricate metal nano dots embedded in SiO. Various NP memory devices have been made to realize the fast and low-power operation of such devices, mostly using Si NP devices surrounded by SiO (Gonzalez-Varona et al., 2003). The programming efficiency has been improved with program voltages reduced far below 10 V, owing to the scaling of tunneling SiO<sub>2</sub>. Among the advantages related with the NP approach to FLASH technologies, worth to emphasize that owing to the discrete nature of the storage nodes, NP memories are expected to behave much better than standard FG devices in radiation environments.

This chapter focuses on this particular issue of the radiation hardness of FLASH, and in particular, NP memory technologies. After a review of the main sources of radiation in space and on earth, we will present a detailed review of the effects of radiation on CMOS electronic devices and discuss the state of the art of radiation effects on standard FG FLASH memories

and NP FLASH memories. In the second part of the chapter, we will present and discuss an extensive study conducted on prototype Si nanocrystal (NC) FLASH memories irradiated with protons.

## 2. The main sources of radiation

Radiation environments are encountered in military applications, nuclear power stations, nuclear waste disposal sites, high-altitude avionics, medical and space applications. Radiation type, energy, dose<sup>1</sup> rate and total dose may be very different in each of these application areas and require in many cases radiation-tolerant electronic systems.

The space radiation environment poses a certain radiation risk to all electronic components on the earth-orbiting satellites and planetary mission spacecrafts. The irradiating particles in this environment consist primarily of high-energy electrons, protons, alpha particles, and cosmic rays. The weapon environment such as a nuclear explosion (often referred to as the "gamma dot") is characterized by X-rays, gamma, neutrons, and other reaction debris constituents occurring within a short time span. This can cause latchup and transient upsets in integrated circuits such as memories. Although the natural space environment does not contain the high dose rate pulse characteristics of a nuclear weapon, the electronics systems exposed can accumulate a significant total dose from the electron and protons over a period of several years. The radiation effects of charged particles in the space environment are dominated by ionization, which refers to any type of high energy particle that creates electron-hole (e-h) pairs when passing through a material. It can be either particulate in nature or electromagnetic. In addition to creating e-h pairs, the radiation can cause displacement damage in the crystal lattice by breaking the atomic bonds and creating trapping recombination centers. Both of these damage mechanisms can lead to degradation of the electronic performance. The ionizing electromagnetic radiations of importance are the X-rays and gamma rays. Ionizing particulate radiation can be light uncharged particles such as neutrons, light charged particles such as electrons, protons, alpha, and beta particles, and heavy charged particles (heavy ions) such as iron, bromine, krypton, xenon, etc., which are present in the cosmic ray fluences. Gamma rays (or X-rays) basically produce a similar kind of damage as light charged particles since the dominant mechanism is charge interaction with the material. Neutrons have no charge, and react primarily with the nucleus, causing lattice damage. In Fig. 1 is shown a summary of the possible radiation sources and their effects on electronic, optical and mechanical components.

### 2.1 Space radiation environments

Our planet is surrounded by a radiation rich environment, consisting of mainly energetic charged particles (electrons, protons, heavy ions, see Table 1). They can either be trapped particles, bound to trajectories dictated by the earth's magnetic field, or free, transiting particles originating from the sun or from galactic sources and can be classified in three main categories: the Van Allen belts, the solar cosmic rays (solar flares), the cosmic rays (galactic and not).

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<sup>1</sup>The dose is the energy deposited per unit mass of the target material by the incident radiation and in the S.I. is measured in Gray, Gy. The unit "rad" (radiation absorbed dose) is related to the abandoned "cgs" system and correspond to 0.01Gy. In this study all the doses are transformed into the correspondent doses in SiO<sub>2</sub>.

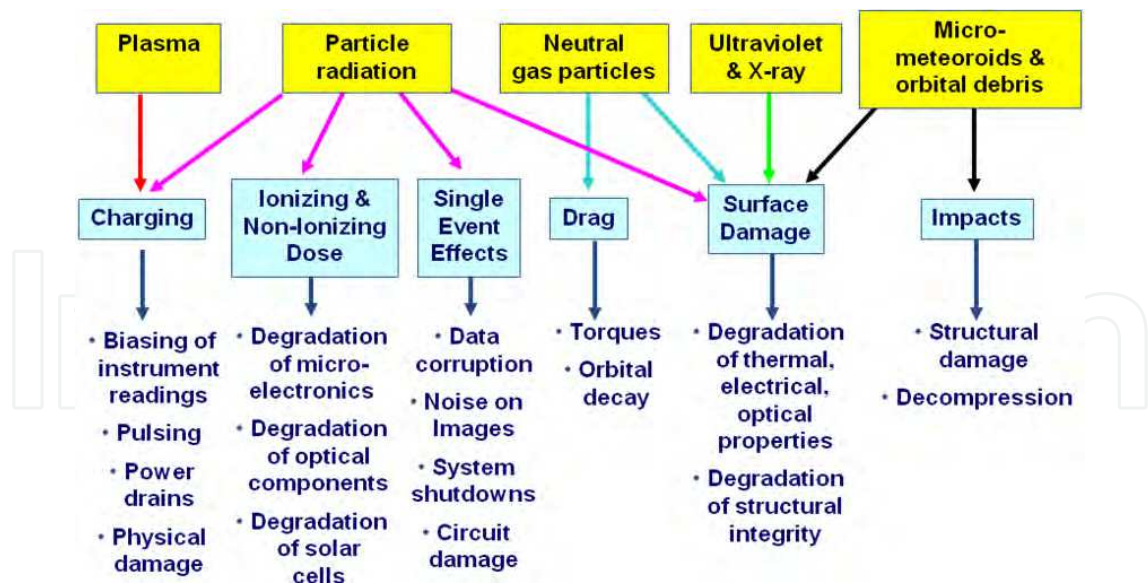


Fig. 1. Radiation sources and their effects on electronic, optical and mechanical components.

Particle type	Maximum Energy
Trapped electrons	10s of MeV
Trapped Protons and Heavy Ions	100s of MeV
Solar Protons	GeV
Solar Heavy Ions	GeV
Galactic cosmic rays	TeV

Table 1. Maximum energies of particles in the space radiation environment (Barth et al., 2002).

2.1.1 The Van-Allen belts

This section discusses natural space environments in which most of the satellites operate, in orbits ranging in altitudes from low earth orbits (150-600 km) to geosynchronous orbits (roughly 35,880 km). Most of the particles in interplanetary space come from the sun in the form of a hot ionized gas called the solar wind; it flows radially from the sun with a speed that in proximity of the Earth varies from about 300 to 1000 km/s, and represents a solar mass loss of about 10<sup>14</sup> kilograms per day.

The radiation environment of greatest interest is the near earth region, about 1-12 earth radii R<sub>e</sub> (where R<sub>e</sub> = 6380 km), which is mainly dominated by electrically charged particles trapped in the earth's magnetosphere, and to a lesser extent by the heavy ions from cosmic rays (solar and galactic). As the earth sweeps through the solar wind, a geomagnetic cavity is formed by the earth's magnetic field (Fig. 2).

The motion of the trapped charge particles is complex, as they gyrate and bounce along the magnetic field lines, and are reflected back and forth between the pairs of conjugate mirror points (regions of maximum magnetic field strength along their trajectories) in the opposite hemispheres. Also, because of the charge, the electrons drift in an easterly direction around earth, whereas protons and heavy ions drift westward. Interplanetary space probes such as the Voyager (and Galileo to Jupiter) encounter ionizing particles trapped in the magnetosphere of other planets, as well as the solar flares and heavy ions from cosmic rays.

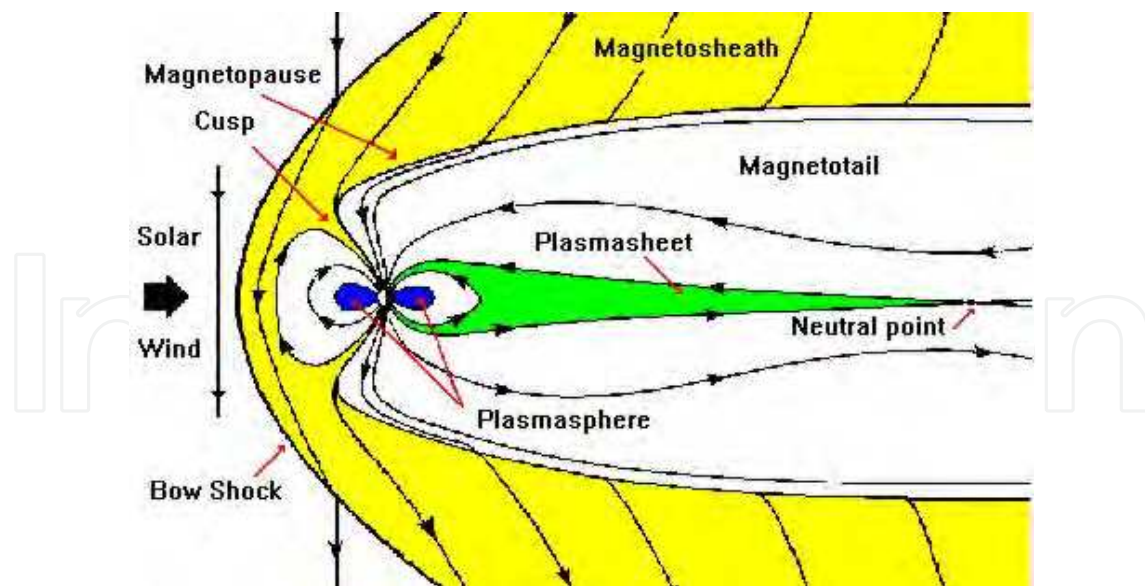


Fig. 2. Interactions between Earth magnetosphere and the solar wind<sup>2</sup>

Electrons in the earth's magnetosphere have energies ranging from low kilo electronvolts to about 7 MeV, and are trapped in the roughly toroidal region which is centered on the geomagnetic equator and extends to about 1-12 earth radii. These trapped electrons are differentiated by "inner zone" (<5 MeV) and "outer zone" (~7 MeV) electron populations. The trapped protons originating mostly from the solar and galactic cosmic rays have energies ranging from a few MeV to about 800 MeV. They occupy generally the same region as the electrons, although the region of highest proton flux for energies  $E_p > 30$  MeV is concentrated in a relatively small area at roughly  $1.5 R_e$ . The actual electron and proton flux encountered by a satellite is strongly dependent upon the orbital parameters, mission launch time, and duration. Electrons and protons from the trapped radiation belts on interacting with spacecraft materials produce secondary radiation (e.g., "bremsstrahlung" or braking radiation from the deceleration of electrons). This secondary radiation can extend the penetration range of primary radiation and lead to an increase in dose deposition. Incident electron and proton fluxes are typically calculated from the trapped radiation environmental models developed by the U.S. National Space Sciences Data Center (NSSDC). The trapped particle fluxes responding to changes in the geomagnetic field induced by the solar activity exhibit dynamic behavior.

### 2.1.2 Solar cosmic rays- solar flares

In addition to the trapped geomagnetic radiation, another contribution to incident particle flux for an orbiting satellite is the transiting radiation from the solar flares. These solar energy particle events (SPE), usually occurring in association with the solar flares, consist mainly of protons (90%), some alpha particles (5-10%), heavy ions, and electrons. This solar flare phenomenon is categorized as an ordinary (OR) event or an anomalously large (AL) event. Particle fluxes from the solar flares can last from a few hours to several days and peak flux during an SPE may be two to five orders of magnitude greater than background, within hours of the event onset. Periods of enhanced flux may last for days, with successive peaks

<sup>2</sup><http://helios.gsfc.nasa.gov/magnet.html>



due to multiple events and enhancements during shock passage. AL events (Fig. 3), although occurring rarely, can cause serious damage to ICs. For ordinary solar events, the relative abundance of helium ions can be between 5-10%, whereas ions heavier than He (e.g., carbon, oxygen, iron, etc.), referred to as the "heavy ions," are very small. However, the solar flare protons which contribute to the total ionizing dose radiation are not that significant a factor compared to the trapped radiation environment.

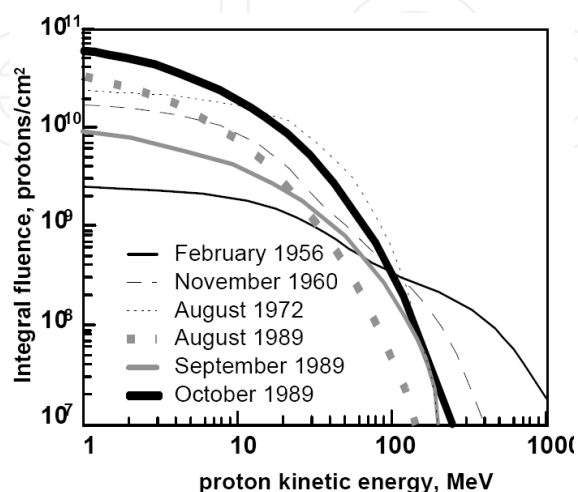


Fig. 3. Distribution in energy of proton fluxes for major past SPEs (free space)

The particles from energetic solar flares (OR events) are heavily attenuated by the geomagnetic field at low altitude and low inclination orbits, such as U.S. Space Shuttle orbits (28.5° inclination). In a 500 km, 57° inclination orbit, some particle fluxes do penetrate. A characteristic of the geomagnetic field which is particularly significant is the South Atlantic Anomaly (SAA), referring to an apparent depression of the magnetic field over the coast of Brazil where the Van Allen radiation belts dip low into the earth's atmosphere. This SAA is responsible for most of the trapped radiation in low earth orbits (LEOs). On the opposite side of the globe, the Southeast-Asian anomaly displays strong particle fluxes at higher altitudes. A polar orbit at any altitude experiences a high degree of exposure, and at geosynchronous orbit, geomagnetic shielding is rather ineffective.

### 2.1.3 Galactic cosmic rays

Another significant contribution to the transiting radiation is from cosmic rays originating from outside the solar system and consisting of 85% protons, 14% alpha particles, and 1% heavier ions. These galactic cosmic rays (GCR) range in energy from a few MeV to over GeV or TeV per nucleon. The total flux of cosmic ray particles (primarily composed of protons) seen outside the magnetosphere at a distance of earth from the sun (1 AU) is approximately 4 particles/cm²s.

Heavy energetic nuclei, HZE, represent ~1% of the GCR and as shown in Fig. 4, where is presented the distribution in energy of several important HZE nuclei, these particles have very high energies, sufficient to penetrate many centimetres of tissue or other materials. In addition, the HZE nuclei are highly charged and, therefore, very densely ionizing. As a consequence, even though the number of HZE particles is relatively small, they have a significant biological impact that is comparable to that of protons.

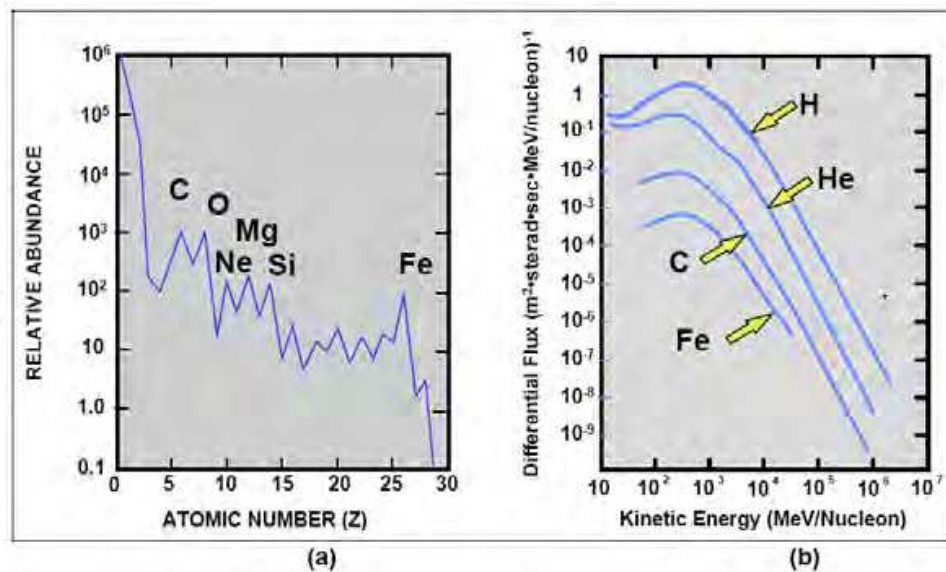


Fig. 4. Abundances (a) and energy spectra (b) of GCR.

### 3. Ionizing radiation effects on MOS devices

Silicon MOS (metal-oxide-semiconductor) devices are by many decades the mainstay of the semiconductor industry. When these devices are exposed to ionizing radiation, significant changes can occur in their characteristics. Ionizing radiation creates mobile electrons and holes in both the insulator and silicon substrate in MOS devices that may lead to a damage of the device. It is interesting to note that these properties have allowed the use of ionizing radiation damage as a tool for scientific study in a number of areas. Indeed, in the past, the basic mechanisms of carrier transport in insulators have been very effectively explored by using various types of ionizing radiation to create mobile carriers and then monitoring their motion by electrical means. These studies have furthered our understanding of polarons, excitons and trap-hopping processes. The generation of interface traps and oxide trapped charge in large numbers by ionizing radiation has allowed the identification of the atomic structures associated with these defects. By providing a means of altering the trapped charge at the  $\text{SiO}_2/\text{Si}$  interface in a given device, the interaction of mobile charge carriers in the channel of an MOS device with that trapped charge can be explored. By creating trapped charge distributions in the oxide layer which provide traps for carriers, tunneling and carrier capture phenomena can be effectively studied. As the semiconductor industry progresses deep into the ULSI era, the technological impact of ionizing radiation effects becomes more and more important. In order to produce the extremely fine geometries required at high levels of integration, the processes used in the manufacture of the integrated circuits themselves may produce ionizing radiation. At the small geometries of current and future integrated circuits, latchup initiated by normal operating conditions has become a major concern. This trend toward small devices has made normal commercial ICs susceptible to single event upsets caused by ionizing particles created by the decay of residual radioactive material in IC packaging material. Thus many of the concerns for radiation hardened circuits have become a concern for standard commercial products. In addition, in order to make circuits for specialized applications requiring operation in an ionizing radiation environment, significant modifications to the technology employed must be made. There are a large number of specialized applications requiring ICs that have a

known, predictable response to ionizing radiation. Satellite systems need electronic components that can operate in the harsh radiation environment around the earth and in space. Without such components satellites would have extremely limited capabilities. Many weapon systems require hardened components to perform their tasks properly through an operational scenario. Nuclear power plants need instrumentation which can withstand the environment near the reactor and continue to provide reliable data. In the nuclear medicine field, it is straightforward the importance of having electronic components with higher performances in radiation environments.

### 3.1 Damaging mechanisms

The way ionizing radiation affects MOS devices is mainly related to build up of oxide trapped charge, increased amount of density of interface states at the oxide boundaries and to the possibility to have single-event-upsets, SEU (Ma & Dressendorfer, 1989). When ionizing radiation passes through the oxide, the energy deposited creates electron/hole pairs with a generation energy of 18 eV/pair. The radiation generated electrons are much more mobile than holes and are swept quickly out of the oxide. Some of them undergo recombination with holes, depending on many different experimental factors. A final positive charge is then observed in the oxide, resulting from the unrecombined holes generated by radiation that remain trapped in the strained areas of the oxide close to the interfaces with Si or the gate material (Fig. 5). The trap sites responsible for this positive charge build up have been identified as E' centers, deep traps in the bulk of SiO<sub>2</sub> originated by a silicon dangling bond in the oxide matrix. Furthermore, an increased amount of interface states is also observed after irradiation at Si/oxide interface. P<sub>b</sub> centers have been found to be responsible for the observed interface states, microscopically related to non bridging silicon atoms between the crystalline silicon substrate and the silicon oxide matrix. This interface bond breaking during irradiation seems to be driven by the excess positive charge and strain present at interface. Finally, in the case of heavy ion irradiation when the incident particle has high enough Linear-Energy-Transfer (LET) transient effects become also important. Indeed the ion along its path inside the device creates a dense cloud of electron-hole pairs generating very intense transient currents that in many cases may result in different kinds of failures of the device itself, even rupture.

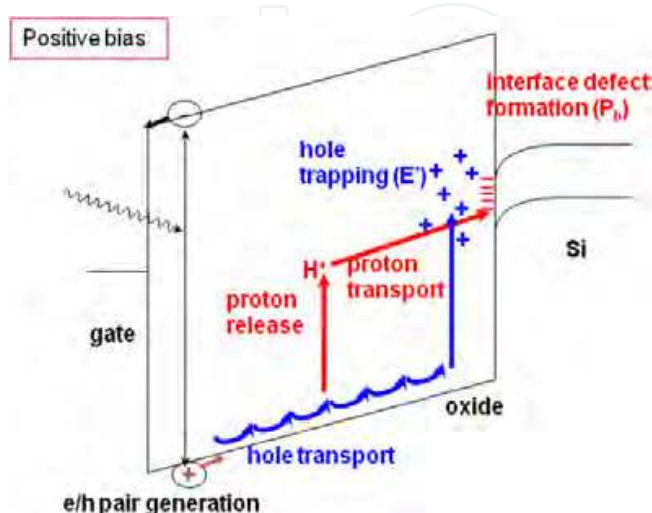


Fig. 5. Detailed representation of the ionizing radiation damage mechanisms into SiO<sub>2</sub>.



Thus, when we are interested into the transient response of an MOS component to single events we perform heavy ion irradiations. When on the other hand we are interested into the effect on devices performance of accumulated damage during long time irradiation exposure we perform total ionizing dose (TID) irradiations, using gamma rays or in special cases electrons or protons.

### 3.2 Performance degradation of FLASH memory devices under irradiation

In MOS microelectronic memory devices, information is stored as quantities of charge. Pulses of ionizing radiation are known to be effective in corrupting the information integrated circuits store. Errors induced by ionizing radiation can be classified in three main classes: soft errors, hard errors and failures. Soft errors are correctable simply by re-entering correct information into the affected elements and can be generated by single ionizing particle or by pulses of ionizing radiation. Hard errors are not recoverable, i.e. are not altered by attempts to rewrite correct information and are caused by single particles like neutrons and heavy ions. Finally, failure events prevent normal device operation and generally are connected to the high transient currents initiated by pulsed ionizing radiation or single events. While RAM can be made insensible to soft errors in many different ways (by design (Liaw, 2003) or by software (Klein, 2005 ; Huang, 2010) ), NVMs are susceptible to all three categories of errors above. The lack of any refresh cycle of the stored information make flash memories vulnerable to data loss at each exposure to ionizing radiation. Considering that Flash memories standards impose a retention time for the data stored of 10 years at least and a minimum  $10^6$  write/erase operations before performance degradation starts, is clear that non-volatile memory cells are in a passive state for most of their lifetime. Until recently, the effects of radiation in Flash memories have mainly been a concern for the space or aircraft applications. The heavy ions and other high energy particles which are abundantly present at altitudes far above the sea-level cause a variety of problems including the soft errors (mainly SEU, Single-Event-Functional-Interrupts (SEFI)), latchup (If the induced parasitic current levels are sufficiently high, they can cause permanent device failures such as a junction burnout) and hard errors pertaining to oxide degradation due to total dose (irreversible bit-flips due for example to high leakage current in the gate oxide). Recent experiments on current generation Flash memories have however shown that significant amount of radiation effects can be observed at the sea level or terrestrial environments. Previously, the most sensitive component of Flash memory used to be the control circuitry for sense amplifiers and charge pumps. The FG cell array on the other hand was considered to be relatively insensitive to radiation strikes at least at terrestrial levels. This is however changing rapidly because with only  $\sim 1000$  or fewer electrons stored in the FG, the cells have now become sensitive to charge deposited by the terrestrial cosmic ray neutrons and alpha particles. But most important, because of the conductive nature of the floating gate, in presence of a weak spot in the tunnel oxide, possibly radiation induced, the whole charge stored could be lost with total loss of information. Even in the case that the damage does not generate device failure, data retention and device performance would be dramatically affected by this defect in the tunnel oxide (Oldham et al., 2006).

## 4. Brief review of radiation effects on FG FLASH memories

In the last decade different teams already investigated the effect of ionizing radiation on FG Flash memories and a summary on the results can be found in the works of Cellere (Cellere et al., 2004a , 2004b, 2004c, 2005) and Oldham (Oldham et al., 2006, 2007).

Cellere investigate the radiation hardness of standard FG memories, under  $^{60}\text{Co}$ , X-ray and 100 MeV protons. The result that worth to mention here is that independently (almost) from the radiation used, information loss starts at doses as low as 100 krad(Si).

Oldham investigates TID and SEE effects on commercial 2Gbit and 4Gbit NAND FG memories. TID effects, in reasonable agreement with Cellere, show that static errors rise abruptly above 75 krad( $\text{SiO}_2$ ) while dynamic errors rise quickly at even lower doses. The errors were found to arise from zeroes that could not be erased into ones due to the failure of the erase function. The SEE were monitored in static and various dynamic modes for LET in the range 0-80 MeV  $\text{cm}^2 \text{mg}^{-1}$ . Error Cross sections seem to saturate to a value of  $\sim 10^{-12} \text{cm}^2/\text{bit}$ .

## 5. Nanocrystal FLASH memory devices under irradiation - A review

NCMs are expected to have better resistance to ionizing radiation: being able to retain information with only a residual fraction of nanocrystals charged, these devices should be quite immune to radiation-induced leakage current, RILC (Larcher et al., 1999; Scarpa et al., 1997; Ceschia et al., 2000; Oldham et al., 2005), and they may in principle exhibit high resistance to both single event (SEE) and total ionizing dose (TID) effects. While some works already investigated the effect of ionizing radiation on FG Flash memories, until now, few works have investigated this issue in NC NVMs and will be briefly reviewed in the next.

Petkov (Petkov et al., 2004) report the first results pertinent to the high total dose (TID) tolerance of Si nanocrystal NVM cells studying prototype NC-Si field effect transistors made by ion implantation. Si ions were implanted at 5 keV to a fluence of  $1.3 \cdot 10^{16} \text{cm}^{-2}$  into a bare 15 nm-thick  $\text{SiO}_2$  layer, grown on top of p-type doped Si wafer. The ion implantation profile shows a peak depth of 10 nm and a stoichiometry at the peak of 1.75:2. The wafers were annealed at  $1050^\circ\text{C}$  for 5 min in dry oxygen, during which time the nanocrystals were formed and the majority of the implantation-induced defects were annealed out. An optically transparent 50 nm poly-Si gate was deposited on top of the wafers. Reference samples without Si NCs were also used. Unfortunately Petkov et al. don't give further details about the final geometry of the device. Radiation experiments were carried out using  $^{60}\text{Co}$  and two different conditions were used: (1)  $V_S = 0 \text{ V}$ ;  $V_{DS}=1.5\text{V}$ ;  $V_G=\pm 6\text{V}$  (write/erase square wave potential), and (2) all contacts grounded. They yielded indistinguishable results for the duration of the experiments, in which the maximum achieved dose was 15 Mrad(Si). The typical hysteresis of a device prior to and after irradiation were recorded on 15 NC-Si FETs with write/erase square wave potential applied to the gate. The electrical characteristics of all transistors were virtually unchanged and it is clear that negligible is the effect of ionizing radiation on position and height of the memory hysteresis. In their work, Petkov et al. consider also another set of 6 NC-Si FETs and three conventional FETs, exposed to ionizing radiation environment with all contacts grounded. The control n-channel FET yielded decreasing gate threshold with dose, notably below 1 Mrad(Si) and according to Petkov, this is considered to be consistent with the accepted models for degradation of metal-oxide-silicon structures under irradiation. The lack of change at 2 Mrad(Si) doses is attributed to saturation of interface defect generation and hole trapping. Both of the NC-Si FET show no significant changes in the entire test range of up to 15 Mrad(Si). This is ascribed to the ion-implantation-induced damage and the subsequent reconstruction of the oxide. Petkov et. al. justify this fact with the argument that oxide properties, especially these related to defect density, charge trapping and mobility, can

differ greatly prior to implantation and after reconstruction. They conclude their work suggesting that for NC-Si technologies that do not utilize implantation, we can expect to observe a shift of the erased state upon radiation exposure, as in conventional FETs.

Oldham (Oldham et al., 2005) reported on the exposition to heavy ion bombardment and total ionizing dose of advanced nanocrystal nonvolatile memories. The test chips were experimental 4Mb Flash EEPROM memories fabricated using 0.13  $\mu\text{m}$  design rules, with NAND architecture (Freescale). Channel hot electron (CHE) injection is used to write (that is, to add electrons to the nanocrystal array), and Fowler-Nordheim tunneling to erase (that is, to remove electrons from the array). The nanocrystals are deposited by a CVD process, where the density and diameter of the particles can be controlled by adjusting the deposition conditions. The tunneling oxide and control gate oxide are  $\text{SiO}_2$  with thicknesses of 4.3 nm and 5.6 nm respectively while the Si NCs have diameter of 4 nm. The heavy ion testing was done using a Single Event Effects Test Facility, which was tuned to 15 MeV/nucleon, using Ar, Kr, Xe and Au ions. Each exposure was to a total fluence of  $10^7$  particles/ $\text{cm}^2$ . Total dose testing was done using a  $^{60}\text{Co}$  source with dose rate of 10 rad/s. Oldham et al. performed their tests in three modes: static mode, in dynamic read mode, and dynamic program and erase modes. In the static testing, a pattern was written, and errors counted after the exposure. In dynamic read testing, a stored pattern was read continuously during the exposure, and the errors counted. The write or program mode was tested by continuously doing a write/read cycle. The erase mode was tested by cycling continuously through erase/write/read steps, and counting errors when the pattern read differed from the pattern expected. Patterns that could be written were all zeroes, all ones, checkerboard, and inverse checkerboard. In heavy ion testing, the errors appear to be all static bit flips, zeroes (electrons storage) turned into ones (holes storage). Oldham estimates that about one ion out of 6 that hits the active gate area changes the state of the cell, even at the highest LET tested so far and the observed cross section is about one sixth times the geometric gate cross-section.

Cester (Cester et al., 2006) performed heavy ion irradiation tests on experimental nanocrystal memory cell arrays provided by ST microelectronics based on CAST architecture. Each nanocrystal MOSFET features  $W/L$  0.2 $\mu\text{m}/0.3\mu\text{m}$ , with a tunnel oxide 5-nm thick and thermally grown on Si. The external control oxide consists of an oxide-nitride-oxide (ONO) stack with an equivalent oxide thickness (EOT) of 12 nm. Silicon nano-islands were realized by low pressure CVD (LPCVD) process in the Si nucleation regime using  $\text{SiH}_4$  as a precursor, followed by a post-deposition crystallization annealing of the islands. A nanocrystal density of  $5 \cdot 10^{11} \text{ cm}^{-2}$  was determined by TEM measurements, with an average nanocrystal diameter of 6 nm. On average each cell contains 300 nanocrystals. Irradiations were performed using a tandem van der graaf accelerator. I (301 MeV,  $\text{LET}=64 \text{ MeV cm}^2 \text{ mg}^{-1}$ ) and Ni (182 MeV,  $\text{LET}=31,3 \text{ MeV cm}^2 \text{ mg}^{-1}$ ) ions were considered at three different fluencies:  $0.83 \cdot 10^8 \text{ cm}^{-2}$ ,  $1.7 \cdot 10^8 \text{ cm}^{-2}$ ,  $3.3 \cdot 10^8 \text{ cm}^{-2}$ . The devices were unbiased during irradiations. Irradiations induce negligible changes in the drain current without affecting the subthreshold slope (swing). On the other hand Cester et al. observe that as the fluence of ions increases, the gate leakage current also increases being higher for ions with higher LET. Wrachien (Wrachien et al., 2008) investigated the performance of nanocrystal memories, similar to those of Cester, and floating gate memories when irradiated with protons of 5 MeV and x-rays of 10 keV. The terminals were kept floating during irradiations and some of the devices were in write or erase state. Wrachien observe that X-rays are much more effective than protons in charge removal from charged devices. What arises in the work of

Wrachien et al. is that the nanocrystal memories seem to behave better than the floating gate memories in these environments since higher doses are needed in the former case respect to the latter to observe a certain charge loss. Also the swing is found to behave better for NCM than FG and the charge retention measurements confirm these results indicating much higher retention for NC memories than FG and thus justifies the interest of the radiation effects community on NC NVMs.

## 6. Fabrication and characterization of Si NC NVMs

The optimized Si NC NVM structures were in the form of capacitors and transistors with Si NCs fabricated according to the ultra-low-energy ion-beam-synthesis (ULE-IBS) technique (Normand et al., 2004). A schematic cross section of the gate area of the devices is shown in Fig. 6. The capacitors had a control-oxide (CO) thickness around 15.5 nm, a tunnelling-oxide (TO) of ~8 nm while the transistors had a CO thickness of 5 nm and TO thickness of 6.5 nm. For both capacitor and transistor structures, the NC layer consisted of Si NCs with mean size of 2-3 nm and density of  $5 \times 10^{11} \text{ cm}^{-2}$ . Reference devices with no Si NCs have been fabricated as well.

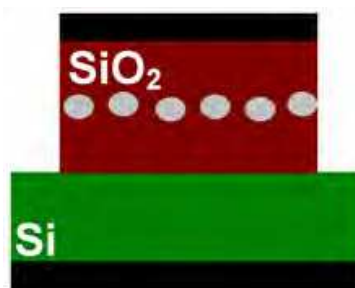


Fig. 6. Schematic of the gate area of the Si NC NVM devices considered in our work.

### 6.1 The Si NC MOS capacitors

The capacitor structures comprise 3 kind of square gates:  $400 \times 400 \mu\text{m}^2$ ,  $200 \times 200 \mu\text{m}^2$  and  $100 \times 100 \mu\text{m}^2$ . The process flow considered in order to fabricate these devices is the following:

1. p-Si substrate with 9 nm thermally grown  $\text{SiO}_2$
2.  $\text{Si}^+$  implantation 1 keV,  $2 \times 10^{16} \text{ cm}^{-2}$
3. annealing at  $950^\circ\text{C}/30 \text{ min}$  in  $\text{N}_2$  (1.5%  $\text{O}_2$ )
4. deposition 10 nm TEOS oxide
5. annealing at  $900^\circ\text{C}/15 \text{ min}$  in  $\text{N}_2$
6. Al evaporation
7. Annealing  $320^\circ\text{C}/30 \text{ min}$  in  $\text{N}_2$

The TEOS oxide has been added in order to increase the CO thickness and thus improve the retention properties of the devices. The total gate oxide thickness of the implanted samples was ~25.5 nm while reference samples (steps 2 and 3 skipped) had a thickness of ~19 nm. The electrical properties of the above devices will be briefly presented in the next paragraphs.

The electrical properties of reference (no Si NCs) capacitors are shown in Fig. 7 where the high and low frequency C-V characteristics are presented together with the density of interface states ( $D_{it}$ ) distribution along the Si band-gap. The oxide thickness extracted from  $C_{ox}$  values is ~18.7 nm. The density of interface states throughout the band-gap is extremely low,  $2 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ , thanks to the very good quality of the  $\text{SiO}_2$  oxide thermally grown on Si substrate.



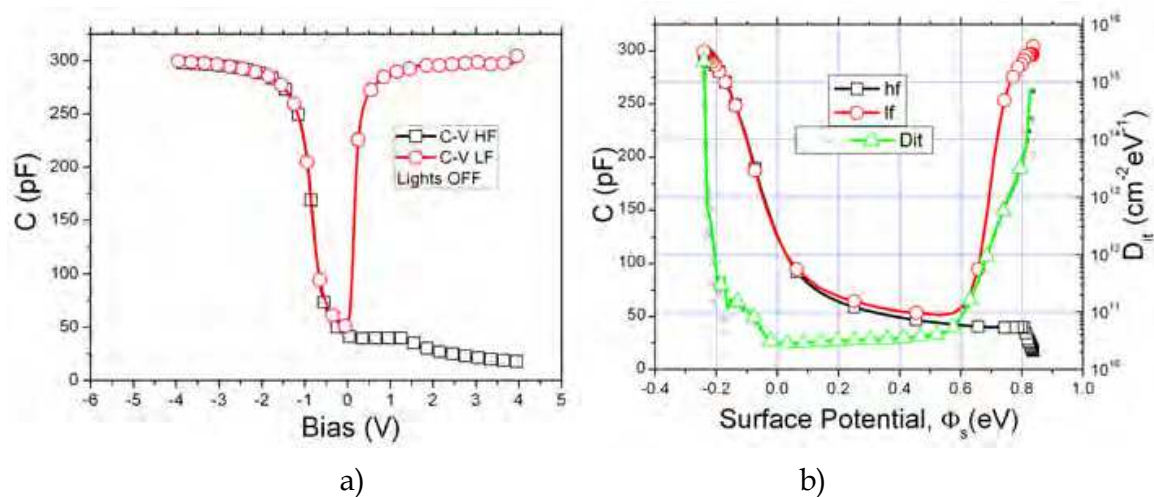


Fig. 7. C-V characteristics and  $D_{it}$  for a reference MOS capacitor with p-Si substrate ( $10^{15} \text{ cm}^{-3}$ ), 18.7 nm  $\text{SiO}_2$  and Al gate of 400 $\mu\text{m}$  side: a) HF - LF characteristics, b) density of states calculated using the high-low frequency method (the HF and LF C-Vs are also shown)

In Fig. 8 is shown the J-V characteristic of the reference MOS capacitor. It is demonstrated there that the conduction mechanism through the oxide is based on Fowler-Nordheim (F-N) tunneling

$$J = A E^2 e^{-B/E} \tag{1}$$

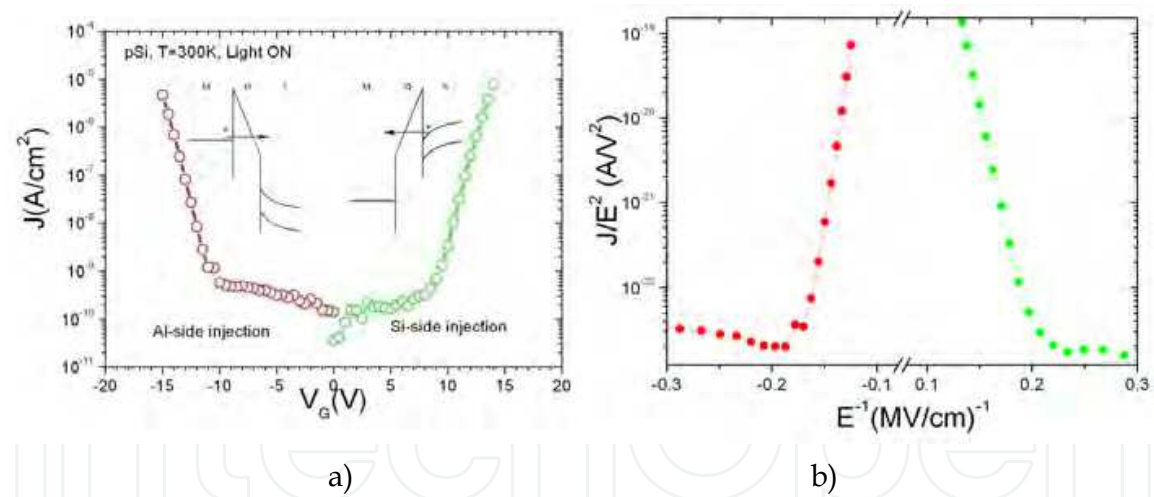


Fig. 8. a) Experimental J-V characteristic for a reference MOS capacitor with p-Si substrate ( $10^{15} \text{ cm}^{-3}$ ), 18.7 nm  $\text{SiO}_2$  and Al gate of 400 $\mu\text{m}$ . Probe light was kept on during the measurement in order to ensure a reasonable amount of minority carriers in inversion (green curve), b) F-N plot of the J-V data in which is clear that for  $E^{-1}$  below 0.2 (MV/cm) $^{-1}$ , i.e. E above 5-6 MV/cm, F-N conduction starts.

and the B parameters extracted from the F-N plot are 194 MV/cm in accumulation (Al-side injection) and 287 MV/cm in inversion (Si-side injection). It should be reminded that the B parameter is related to the effective mass of the tunneling charge carrier and the barrier height. Assuming an electron effective mass in  $\text{SiO}_2$  of  $0.42m_0$ , the extracted barrier heights are 2.7eV and 3.4eV respectively.



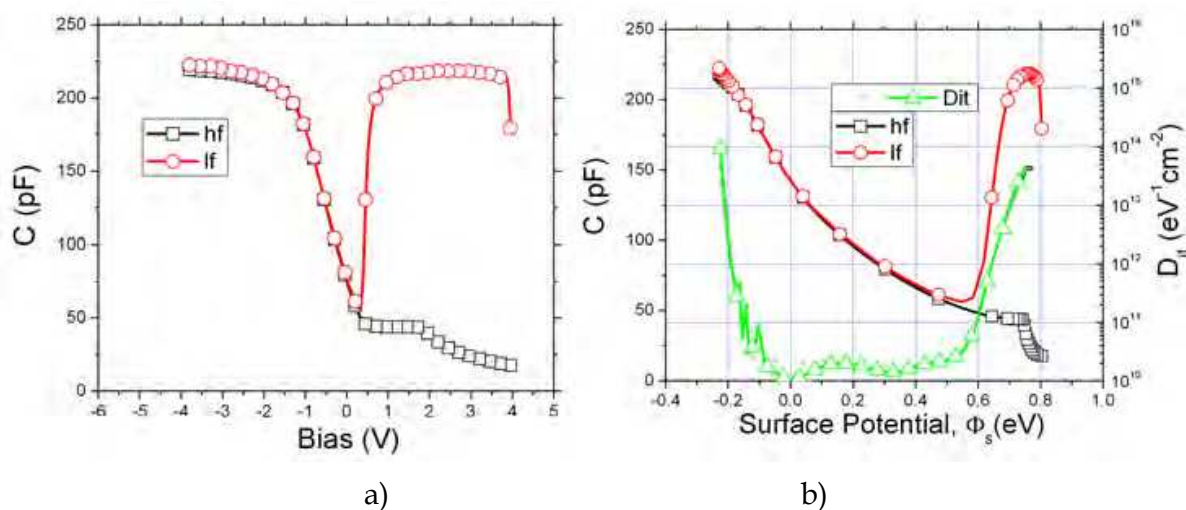


Fig. 9. C-V characteristics and  $D_{it}$  for a Si NC MOS capacitor with p-Si substrate ( $10^{15} \text{ cm}^{-3}$ ), 8 nm  $\text{SiO}_2$  TO, 2-3 nm NCs, 15.5 nm CO and Al gate of 400  $\mu\text{m}$  side: a) HF - LF characteristics, b) density of states calculated using the high-low frequency method (the HF and LF C-Vs are also shown).

The Si NC MOS capacitors present similar electrical properties with the reference capacitors. In Fig. 9, the high and low frequency C-V characteristics are shown together with the  $D_{it}$  distribution along the Si band-gap. The oxide thickness extracted from  $C_{ox}$  values is  $\sim 24.5$  nm. the density of interface states throughout the band-gap is extremely low,  $2 \cdot 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ , thanks to the very good quality of the  $\text{SiO}_2$  oxide thermally grown on Si substrate.

In Fig. 10 is shown the J-V characteristic of the reference MOS capacitor. It is demonstrated there that the conduction mechanism through the oxide is again based on F-N tunneling at least in accumulation (Al-side injection) with a B parameter extracted from the F-N plot of 186 MV/cm reasonably comparable with the one of the reference devices. In inversion (Si-side injection) on the other hand the B parameter extracted is very low in comparison with that of the reference capacitor: 100 MV/cm. Fig. 10c can help us in the explanation of this difference since as it is shown there, comparing the leakage current through the reference and the Si NC MOS becomes clear that for the latter conduction starts at much smaller fields in inversion, around 3.5 MV/cm. Such a field cannot ignite F-N conduction so the above argument demonstrate that there is another conduction mechanism in competition with (maybe dominates) the F-N tunneling from substrate in the Si-NC memory devices in inversion. Of course the fact that F-N plot shows the characteristic linear behavior of every F-N mechanism is telling us that the mechanism dominating over the F-N injection from the Si substrate should be also an F-N mechanism. This last observation drives to the conclusion that the 100 MV/cm B value should arise from the F-N taking place from the electrons trapped in the NC layer that tunnel toward the gate and ignited by the augmented electric field present in the CO when electrons are present into the NCs while, at the same time, the electric field in the TO is reduced. It can be shown that when the overall, through the dielectric structure, electric field is 4 MV/cm and there is a detectable (in terms of flat-band voltage shifts) negative charge into the NCs, the electric field into the CO is around 5 MV/cm and thus able to ignite F-N. Thus the 100 MV/cm of the B value extracted for the Si-side injection case is related not to the barrier  $\text{SiO}_2/\text{Si}$ -conduction band but  $\text{SiO}_2/\text{NC}$ -Si-conduction band (Fig. 10d). The barrier extracted from the 100 MV/cm value is around 1.8 eV.

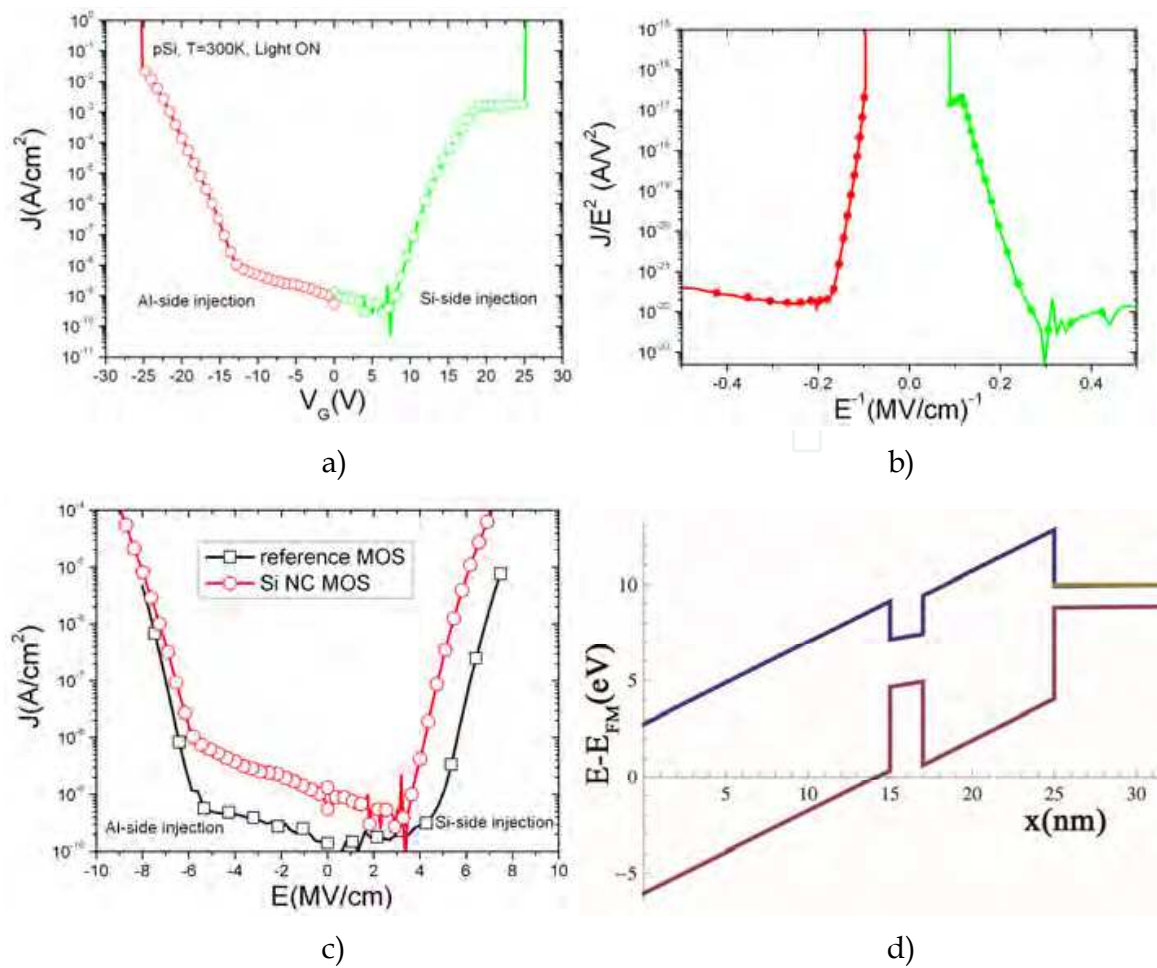


Fig. 10. a) Experimental J-V characteristic for a Si NC MOS capacitor with p-Si substrate ( $10^{15}$  cm<sup>-3</sup>), 8nm SiO<sub>2</sub> TO, 2-3nm NCs, 15.5nm CO and Al gate of 400  $\mu$ m side. Probe light was kept on during the measurement in order to ensure a reasonable amount of minority carriers in inversion (green curve), b) F-N plot of the J-V data in which is clear that in accumulation F-N conduction starts at -6MV/cm while in inversion it seem to start at 3-4 MV/cm, c) comparison between the J-E characteristic of reference and Si NC MOS capacitors, d) Band diagram of the Si NC capacitor under  $V_G=10$  V without charges into the NC layer.

### 6.1.1 Memory window

The memory properties of the devices with Si NCs have been recorded with two equivalent ways: gate sweeps and gate pulses. The latter of course is the one in which we are most interested since the memory in its final application is written/erased by voltage pulses. Gate sweep bias measurements are performed sweeping the the gate voltage circularly i.e. inversion - accumulation - inversion with increasing amplitude of the applied maximum bias. In Fig. 11a are shown the C-V curves obtained with such a measurement; large hysteresis were found for amplitudes above 10V. It should be noted that the hysteresis are counter clock wise, indicating that charging is taking place from the substrate. Upon extraction of the flat-band voltages from the above C-Vs, it is possible to present the data as in Fig. 11b where the memory behaviour of the devices becomes clearer. Electron injection (backward sweeps) seem to start at around 10V, slightly earlier than holes injection (forward sweeps) which start at around 12V while saturation starts at 16V and 18V respectively.

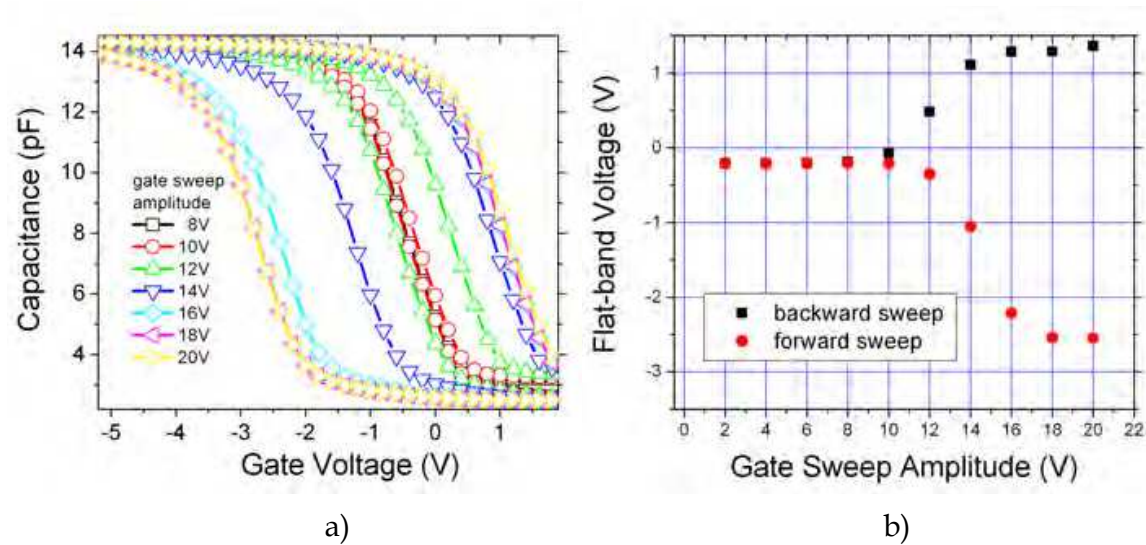


Fig. 11. a) C-V characteristics under gate bias sweeps of several amplitudes; Large hysteresis for amplitudes above 10V are shown, b) memory characteristic as extracted from Fig. 11a.

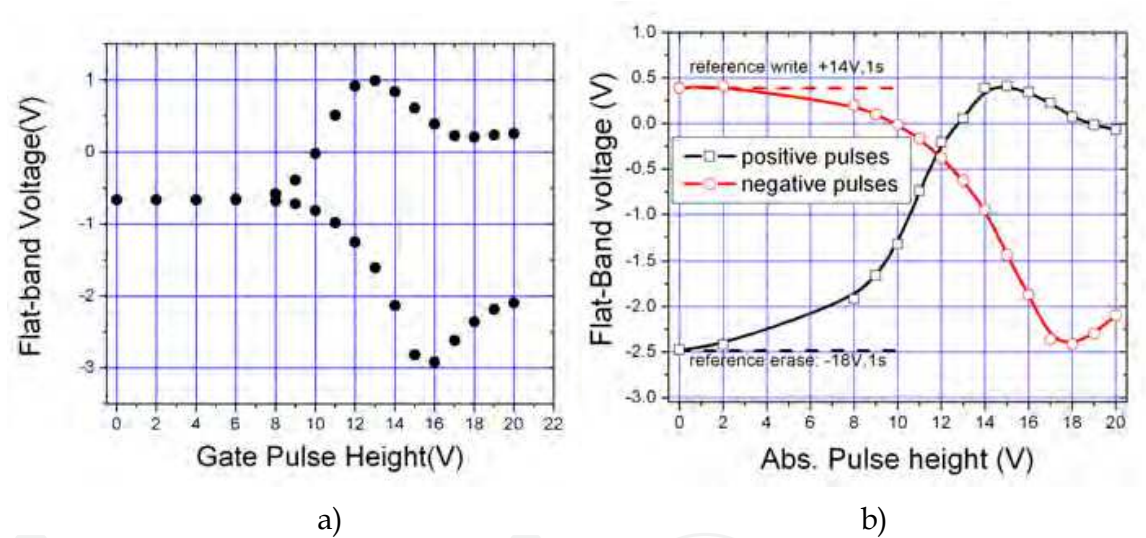


Fig. 12. a) memory characteristic extracted from gate pulse measurements (the upper branch refers to positive pulses), b) Memory behavior under repeated positive and negative pulses. The black curve is obtained keeping the constant the erase (negative) pulse and varying the height of the write (positive) pulse, and the opposite is done for the red one.

Gate pulse measurements are performed applying in sequence pulses of increasing height to the gate and measuring at every pulse a C-V characteristic to monitor the flat-band voltage position. In such a way, with pulses of 1s duration, the results shown in Fig. 12a were obtained (where the upper branch refers to positive pulses and the lower branch to negative pulses). There are similarities between the memory behavior under gate bias sweeps and gate pulses like the maximum width and the saturation behavior at high fields, but, also one difference that is the decreasing (increasing) flat-band voltage in order to approach saturation for positive (negative) pulses. The reason of this phenomenon is that when the fields become high enough charges are not only injected into the NCs but also extracted. Actually there is a dynamic equilibrium between this two components at steady regime that



drives to the smooth behavior observed with gate sweep measurements, on the contrary, this equilibrium is perturbed in presence of pulses favoring charge extraction at high fields and this explains the peculiar shape found for the memory characteristic in Fig. 12a. In its final operation, the memory always switches from write state to erase state and vice versa. Thus, the gate pulse measurement, although gives important informations about the pulsed operation of the memory device, isn't the best one to decide the program and erase condition to be used during its final operation. What should be done is to establish the strength of each positive (negative) pulse starting always from the same erased (programmed) state. This has been done for the Si NC capacitor memories and is shown in Fig. 12b. The most effective programming pulses are +14V and -18V. From now on we will consider as write state or erase state the condition into which is brought the device when programmed with a write pulse +14V,1s or erased with an erase pulse of -18V,1s respectively. The memory window of the device arises then as the difference between the flat-band voltages of the write and erase states. For the Si NC MOS capacitors presented here, the memory window is around 3V.

6.1.2 Charge retention measurements

Charge retention measurements are performed charging a device into one of the two states write or erase and then the evolution with time of the flat-band voltage is recorded for 12 h at least. This is done 1) measuring at regular interval of times the C-V of the device (that was written or erased) in order to obtain a result similar to the example shown in Fig. 13a, and then 2) extracting from the C-Vs the flat-band voltage which is graphed as function of time.

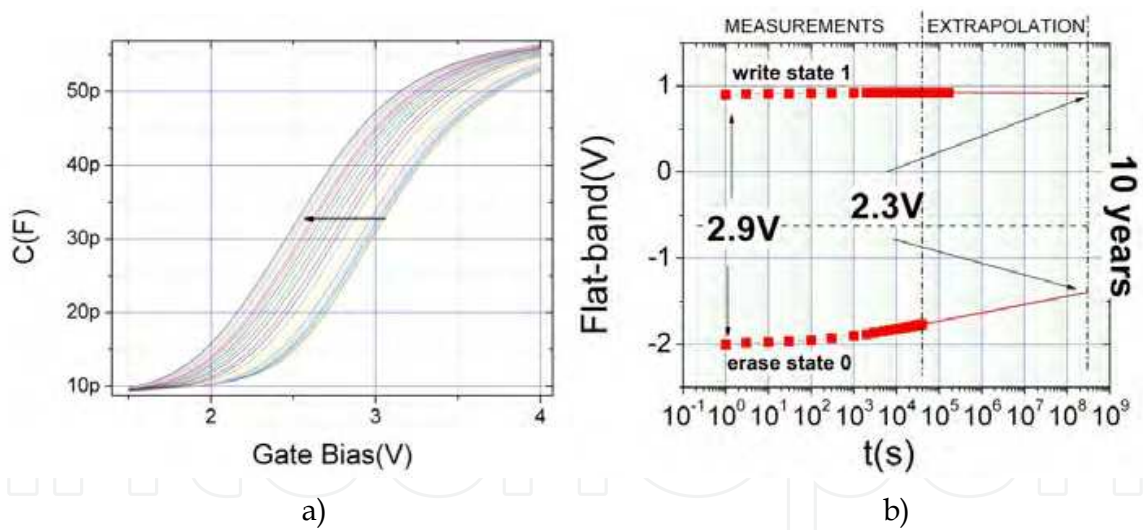


Fig. 13. a) Evolution with time of the C-V characteristic measured at regular interval of times for a Si NC MOS capacitor in the write state. The arrow show increasing time direction. Measurement at room temperature. b) Charge retention measurement in the write and the erase state of the Si NC MOS memory. Measurement performed at room temperature. The electrons loss rate is -4 mV/dec and the holes loss rate is 103 mV/dec.

The above procedure applied to our capacitors drives to the results shown in Fig. 13b where are summarized the measurements for both the write and the erase state. Since the retention curves present in log(t) a linear behavior it is usual to speak in terms of mV/dec loss rate. So, fitting the two curves shown, and assuming that the loss rate will be constant, it is

possible to extrapolate the retention measurements to 10 years. For the erase state the charge loss rate is around 103 mV/dec while for the write state is much smaller, around -4 mV/dec. The charge loss extrapolated at the 10 years retention limit is 20%, thus within the FLASH design standards.

The higher loss rate in erase state (holes retention) than in the write state (electrons retention) has to do with the fact that holes may tunnel back to the substrate by means of imperfections in the TO remained after the implantation and annealing of the Si ions. Electrons on the other hand are not affected by such imperfections and thus the large TO thickness ensures a reliable quantum mechanical barrier against electron loss.

## 6.2 The Si NC MOSFETs

Si NC MOSFETs were provided in structures of two types: depletion (D) and enrichment (E). Furthermore, both types are provided in various W/L configurations: a) constant  $W=100\mu\text{m}$  and  $L=12,10,8,6,4,2\mu\text{m}$ , b)  $L=100\mu\text{m}/W=100\mu\text{m}$  and constant  $L=40\mu\text{m}$  and  $W=40,20,15,10,8\mu\text{m}$ .

Si-NC nMOS transistors were fabricated using a 7 nm thick  $\text{SiO}_2$  layer that was Si implanted and annealed under the same conditions as for NC MOS capacitors. No additional TEOS control oxide was deposited. The final gate dielectric stack includes 6.5 nm thick injection oxide, 2.5 nm thick Si NC layer and 5 nm thick control oxide.

### 6.2.1 Memory window

The memory behavior of the Si NC MOSFETs has been recorded with the gate pulse method mentioned previously. Positive or negative Gate pulses of increasing height are applied in sequence on Fresh devices and after each pulse the  $I_d$ - $V_G$  characteristic is recorded in order to monitor the transistor threshold voltage position. The outcome of such a measurement on

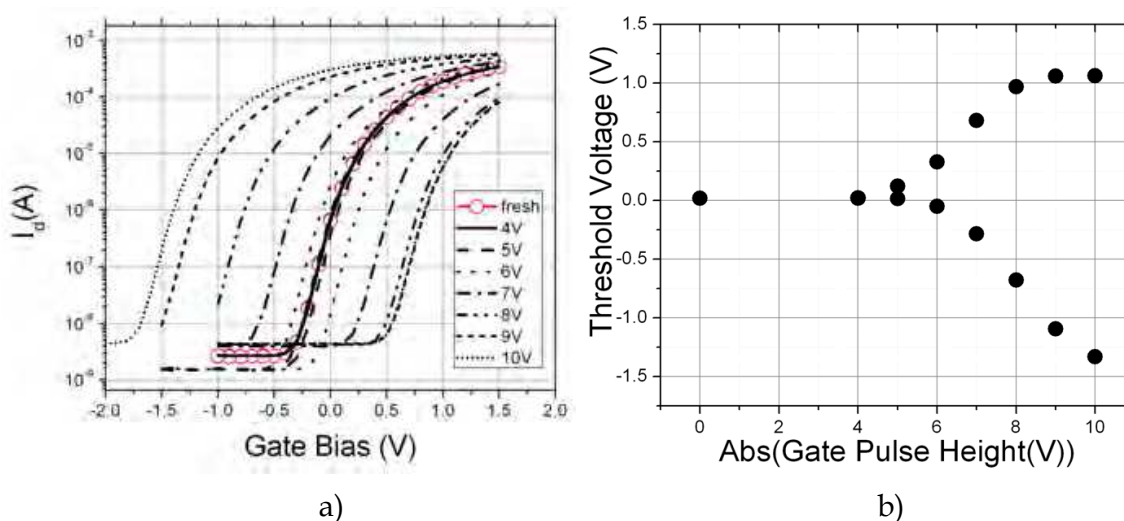


Fig. 14. a)  $I_d$ - $V_G$  characteristics after the application, in sequence, of positive or negative pulses of increasing height (in the legend); the fresh curve refer to the device at the beginning of the measurement i.e. uncharged; on the right of the fresh curve are the characteristics related to positive pulses while on the left are the ones related to negative pulses. b) threshold voltage extracted from a) as function of the gate pulse height; the upper branch is related to positive pulses while the lower branch arises from negative pulses. The pulse duration was constant: 30ms.



our devices, for pulses of 30 ms, is shown in Fig. 14a, while in Fig. 14b the threshold voltages extracted from the  $I_d$ - $V_G$  characteristics are graphed as function of the gate pulse height. Thus, the write or erase states are defined here as the conditions determined by the application of the write pulse +9 V, 30 ms or the erase pulse -9 V, 30 ms respectively. Should be mentioned that the swing of the  $I_d$ - $V_G$  characteristics of such devices is around 127 mV/dec.

### 6.2.2 Charge retention measurements

Charge retention measurements are performed in a similar manner with the measurement on capacitors except the fact that now  $I_d$ - $V_g$  characteristics will be monitored instead of C-Vs. The results are presented in Fig. 15. The overall behavior is very similar to that of NC MOS capacitors but the charge loss rates are much higher because of the thinner TO and CO of the transistor with respect to the capacitor structure. Values of -54mV/dec and 150mV/dec have been extracted for electrons and holes loss rates respectively. The overall charge loss extrapolated to 10 years retention is estimated to be ~57%.

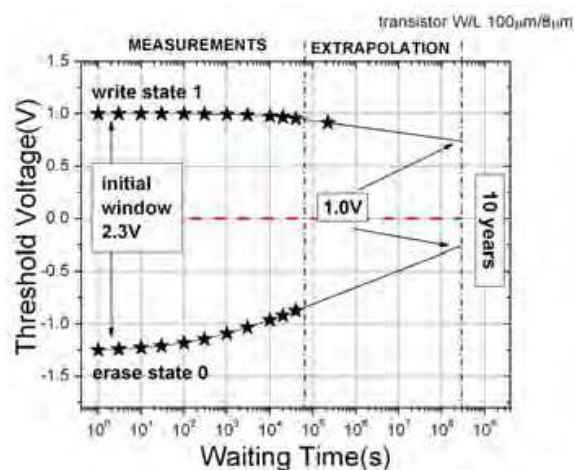


Fig. 15. Charge retention measurement in the write and the erase state of the Si NC MOSFET memory. Measurement performed at room temperature. The electrons loss rate is -54 mV/dec and the holes loss rate is 150 mV/dec.

### 6.2.3 Endurance to write/erase cycles

In order to perform the measurement within few hours, smaller pulse durations have been considered here. The write and erase pulse are always +9 V and -9 V respectively but the duration is now 15 ms so the memory window will be smaller than ~2 V found with 30 ms. The endurance in these transistor memories is outstanding. Results are presented in Fig. 16a where endurance up to  $10^6$  W/E cycles demonstrate the robustness of these devices against stress induced leakage currents (SILC). The endurance measurement is a quite stressful operation for the memory device and for this reason is quite common provide, according to FLASH standards, the retention behavior of a transistor memory cell before and after endurance. In our case the comparison is shown in Fig. 16b. After endurance, the charge loss rates are both increased: electrons loss rate before endurance was -54mV/dec while after was -60mV/dec, holes loss rate before endurance was 150mV/dec while after was 172mV/dec. The extrapolated charge loss after 10 year retention is after endurance ~70% i.e. 13% charge lost because of the stress to which the memory underwent.

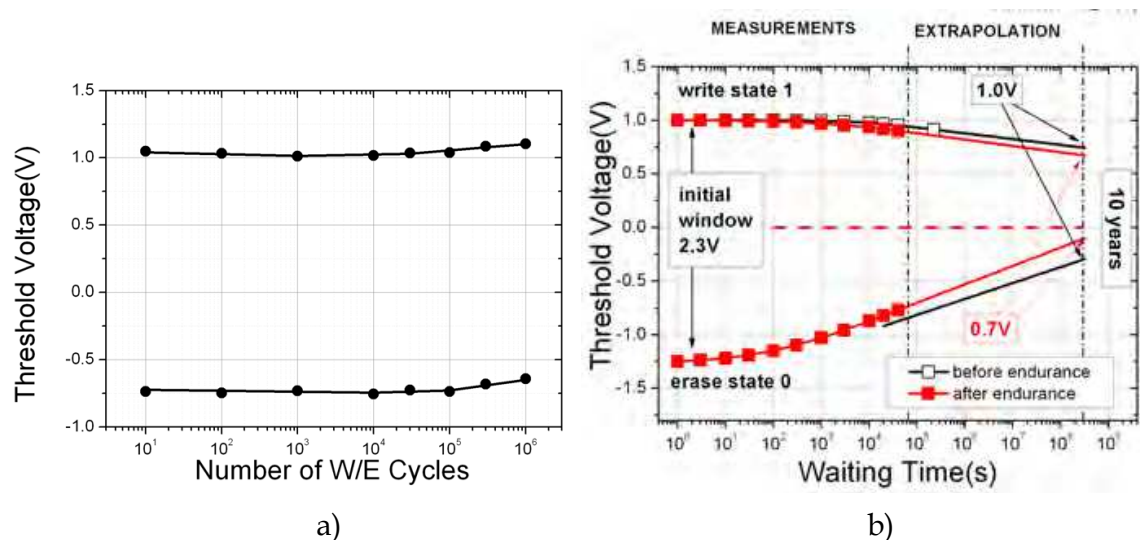


Fig. 16. a) Endurance to w/e cycles performed on Si NC MOSFETs. A reduced pulse duration of 15ms has been considered with write pulses of +9V and erase pulses of -9V. b) charge retention measurement before and after endurance.

## 7. Proton radiation effects on nanocrystal non-volatile memories

The Si NC memory devices, in capacitor and transistor form, presented in section 6, have been irradiated with protons at the Tandem accelerator of the Institute of Nuclear Physics, N.C.S.R. "Demokritos". The energies used ensure that the kind of damage produced is related to TID effects. The ways TID effects alter the operation of NVM cells are essentially two: 1) loss of stored information in the form of bit-flips, and 2) charge retention issues after irradiations (failure to retain the information for 10 years). According to the existing literature on TID effects on standard FG NVMs, briefly reviewed in the previous sections, it is concluded that in FG cells, bit-flips are observed above 100 krad(SiO<sub>2</sub>) while retention issues are observed above ~5 Mrad(SiO<sub>2</sub>). In the next it will be demonstrated that NC NVM cells present a much higher hardness to TID effects than FG cells (Verrelli et al., 2006, 2007).

### 7.1 Irradiations details

The protons considered in our irradiation tests had energies of 1.5MeV and 6.5 MeV. The proton fluences (particles/cm<sup>2</sup>) and the doses (rad(SiO<sub>2</sub>)) considered are shown in Table 2. One important parameter that was constantly monitored during the irradiation was the flux (particles/cm<sup>2</sup>s) of the particles that was kept at ~5 10<sup>9</sup> protons/cm<sup>2</sup>s and this was done keeping constant both the proton current driven by the Tandem (200pA) and the beam spot size. It is very important that the flux remain constant during irradiation cause it is known to be related to changes in the effects produced by radiation (Ma & Dressendorfer, 1989) and thus may complicate the interpretation of the results. The samples irradiated have physical dimension of 1.5x1.5 cm<sup>2</sup> while the proton beam spot has been tuned to be the largest possible i.e. 0.5x0.5 cm<sup>2</sup>. One sample at a time has been irradiated and upon irradiation of all the samples, their electrical characteristics have been studied in our laboratory. The irradiation and all the electrical measurements took place at room temperature and the characterization of the radiation effects ended within one month period time from irradiation. Actually the fastest the samples are characterized after irradiation the better it is,

because the irradiation effects have the property to anneal out with time also at room temperatures (Ma & Dressendorfer, 1989). All the samples have been irradiated with floating terminals except some NC MOS capacitors and transistor which were programmed to “1” or “0”.

Irradiation at 1,5 MeV		Irradiation at 6,5 MeV	
CAPACITORS			
FLUENCE (cm <sup>-2</sup> )	DOSE (Mrad(SiO <sub>2</sub> ))	FLUENCE (cm <sup>-2</sup> )	DOSE (Mrad(SiO <sub>2</sub> ))
5*10 <sup>13</sup>	123	5*10 <sup>13</sup>	119
1*10 <sup>13</sup>	24.6	1*10 <sup>13</sup>	23.7
5*10 <sup>12</sup>	12.3	5*10 <sup>12</sup>	11.9
1*10 <sup>12</sup>	2.46	1*10 <sup>12</sup>	2.37
5*10 <sup>11</sup>	1.23	5*10 <sup>11</sup>	1.19
TRANSISTORS			
3*10 <sup>11</sup>	0.74		
3*10 <sup>12</sup>	7.42		
1*10 <sup>13</sup>	24.6		
3*10 <sup>13</sup>	74.2		

Table 2. Fluencies and doses for the samples involved in this experiment. The capacitors were both NC MOS devices and reference devices i.e. MOS capacitors with no NCs. The transistors were NC MOSFET devices only.

7.2 Electrical characterization of the irradiated devices

At first, we should remark that the capacitor and the transistor samples have a main difference: the former work “vertically” while the latter work “horizontally”. Indeed, in capacitors, the substrate-gate electric field rules everything while in transistors, Id passes from the source to the drain through the channel formed by the inversion layer in the Si substrate and the whole process is confined into few μm from Si-SiO<sub>2</sub> interface. SRIM simulations on our structures show that 1.5 MeV and 6.5 MeV protons end their trajectories into the Si substrate at depths from the Si-SiO<sub>2</sub> interface of 80 and 400μm respectively (for this reason irradiation took place with the devices face to the beam i.e. protons always enter the devices from their gates). This represent an important limitation for capacitor structures which work vertically. The reason is that when a particle like a proton with the energies above mentioned penetrate matter, at the beginning of its track it loses energy in small steps slowing down almost entirely through Coulomb interactions with the atomic electrons of the target material. Because of the large number of these interactions, the slowing down procedure is nearly continuous and along a straight-line path. As the particle slows down, it captures electron(s) to form a neutral atom and thus has an increased probability to have nuclear collisions that may induce displacements and vacancies in the target material lattice. The result is that at the end of range of their tracks, protons destroy the Si crystalline structure transforming it into a porous-like material. Of course the above mentioned effect depends from the fluence of protons. It was found

experimentally that for fluencies above  $10^{14}$  protons/cm<sup>2</sup> the MOS behavior is completely lost due to the isolation achieved between the Si back contact and the gate of the capacitor. The presence of the damage and its amount can be monitored through the value of the series resistance in C-V measurements which increases as the fluence is increased. As it is demonstrated in Fig. 17, this dependence has been found to be approximately linear with the fluence in both the NC MOS capacitors and the reference (no NCs) MOS capacitors.

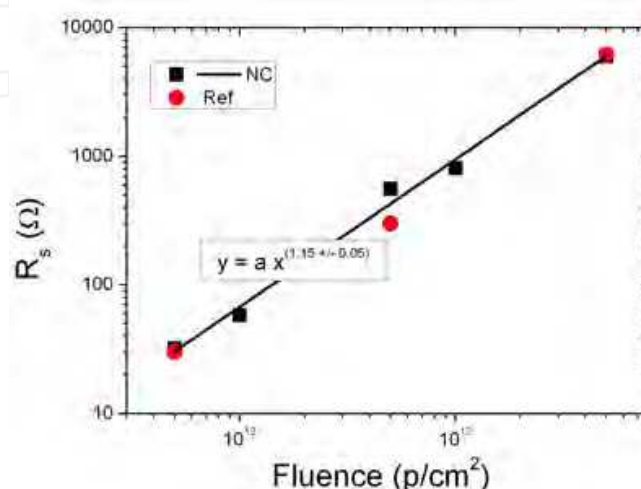


Fig. 17. Dependence upon the fluence of the series resistance measured during C-V measurements on irradiated NC MOS capacitors and reference (no NCs) MOS capacitors.

### 7.2.1 Radiation effects on the D<sub>it</sub>

As mentioned in 3.1, one of the parameter of MOS devices more affected by ionizing radiation is the density of interface states. After irradiation the C-V and G-f characteristics of reference (no NCs) MOS and NC MOS capacitors have been measured in order to estimate the D<sub>it</sub>. Both methods, high-low frequency and conductance, give similar estimations. An example of the effects on the MOS characteristics is shown in Fig. 18a-18c where the C-V frequency dispersion is shown for some of the irradiated NC MOS capacitors.

The extracted values of D<sub>it</sub> at mid-gap have been graphed in function of the dose and are shown in Fig. 18d.

For both reference and NC MOS devices, D<sub>it</sub> increases sub-linearly with dose. Within the measurement errors, our data are in good agreement with the empirical relationship (Ma & Dressendorfer, 1989) that asserts D<sub>it</sub> to be proportional to Dose<sup>2/3</sup>. D<sub>it</sub> distributions were found to be U shaped for the various MOS capacitor samples, with a clear peak in the upper half of the band gap, at around 0.2eV above mid-gap, giving evidence of a sharply distributed electron state in agreement with other observations (Ma & Dressendorfer, 1989).

### 7.2.2 Effects on F-N injection

One important question to answer was to which extent the radiation effects described above affect the MOS characteristics. In order to determine whether the F-N injection mechanism was altered by the ionizing radiation damage to the SiO<sub>2</sub>, the B parameter has been monitored on all the irradiated samples and the result is shown in Fig. 19. This parameter, within experimental errors, does not seem to be affected by the irradiation dose.



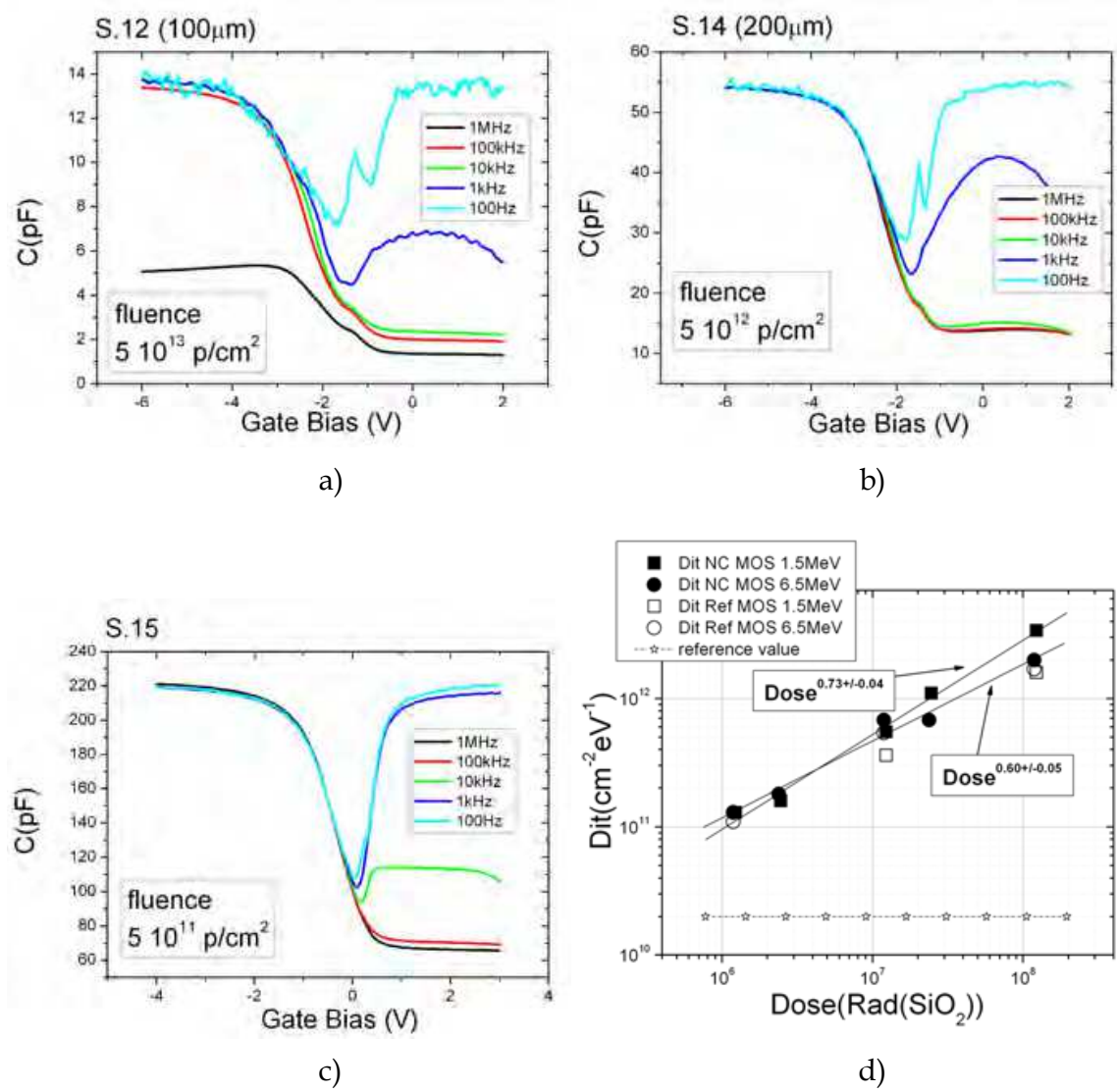


Fig. 18. C-V frequency dispersion for irradiated NC MOS capacitors at different proton fluences: a)  $5 \times 10^{13} \text{ p/cm}^2$ , b)  $5 \times 10^{12} \text{ p/cm}^2$ , c)  $5 \times 10^{11} \text{ p/cm}^2$ . d)  $D_{it}$  versus dose for Reference (without NCs) MOS and NC MOS capacitors irradiated with protons 1.5 MeV and 6.5 MeV.  $D_{it}$  reference value for non irradiated devices is also shown. The lines correspond to linear fits of the NC MOS capacitors experimental data to the relationship  $D_{it} \sim \text{Dose}^b$ .

7.2.3 Radiation induced Flat-band/threshold voltage shift

MOS capacitors irradiated with floating terminals exhibit C-V characteristics shifted to lower voltages compared to the characteristics of non-irradiated samples, in agreement to the well-known observation (Ma & Dressendorfer, 1989) that irradiation creates a net trapped positive charge ( $Q_{ot}$ ) into the SiO<sub>2</sub> layer.

After irradiation of fresh and programmed (+14V/1s write pulse) MOS capacitors, the net positive trapped charge was calculated according to the relation:  $Q_{ot} = -\Delta V_{fb} \cdot C_{ox}$  where  $\Delta V_{fb}$  is the flat-band voltage shift induced by irradiation. The  $Q_{ot}$  vs. radiation-dose data shown in Fig. 20 indicate the following:



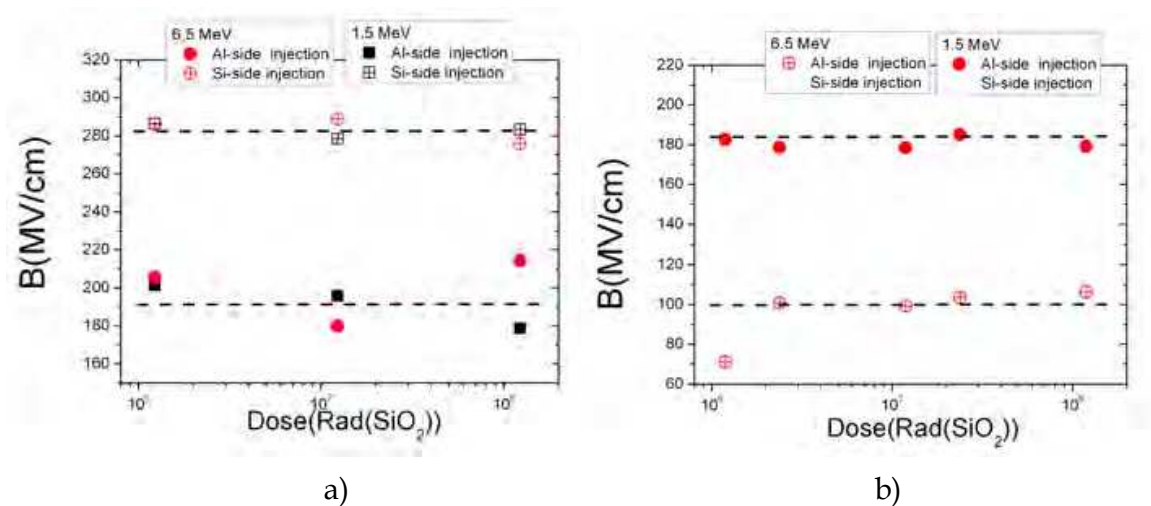


Fig. 19. Values of the B parameter related to F-N conduction in (a) reference MOS and (b) NC MOS capacitors after irradiation. The dashed lines correspond to the values observed before irradiation.

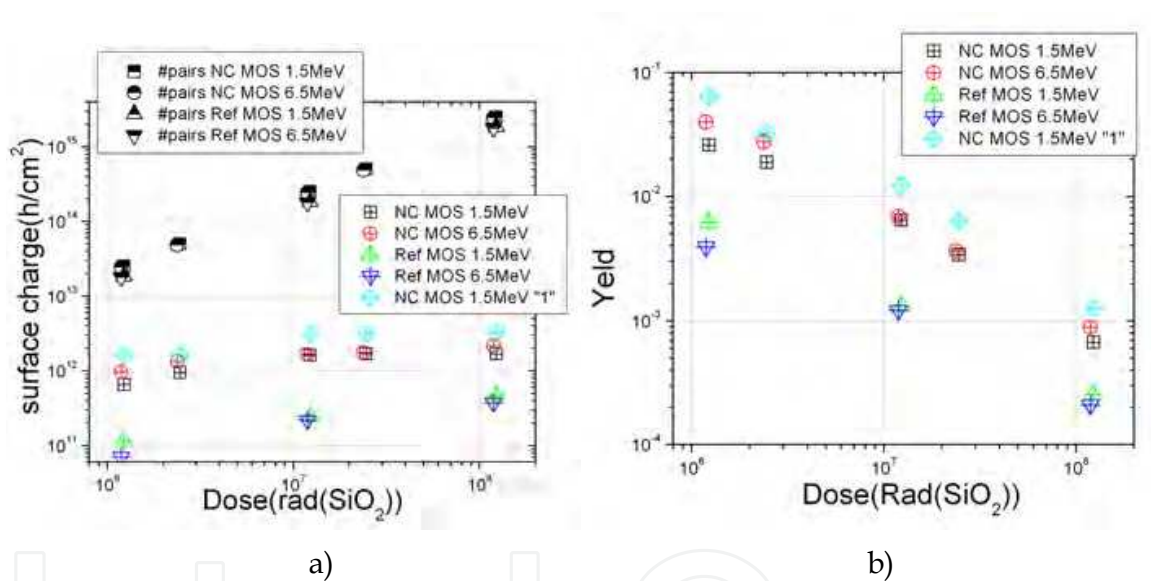


Fig. 20. Values of the B parameter related to F-N conduction in reference MOS (a) and NC MOS capacitors (B) after irradiation. The dashed lines correspond to the values observed before irradiation.

1. In all cases,  $Q_{ot}$  is well below the number of the created electron-hole pairs, thus indicating that only a relatively small number of holes survive the initial fast recombination process i.e. the radiation yield is far smaller than unity (Fig. 20b). The number of electron-hole pairs created by irradiation was evaluated as the ratio of the energy lost by the incident protons into the SiO<sub>2</sub> layer (obtained through TRIM simulations) to the 17eV electron-hole pair generation energy (Ma & Dressendorfer, 1989) in silicon dioxide.
2. Programmed NC-MOS capacitors, exhibit increased ( $\sim 2$  times)  $Q_{ot}$  values compared to capacitors with uncharged NCs. This is attributed to the internal electric field generated by the charged NCs that reduces the hole recombination probability (Ma & Dressendorfer, 1989).

3. The amount of trapped charges in irradiated un-programmed NC MOS capacitors was found to be almost one order of magnitude higher than in the reference MOS samples. This can be related to the extra trapping sites located in the injection and control oxide in the form of excess silicon atoms left behind by the ULE-IBS technique.
4. In all cases  $Q_{ot}$  shows saturation for high irradiation doses (Fig. 20a).
5. All the programmed NC MOS capacitors undergo a bit flip 1→0 following irradiation, (Fig. 21b), in agreement with Petkov (Petkov et al., 2004) where bit flip were observed at 150krad.

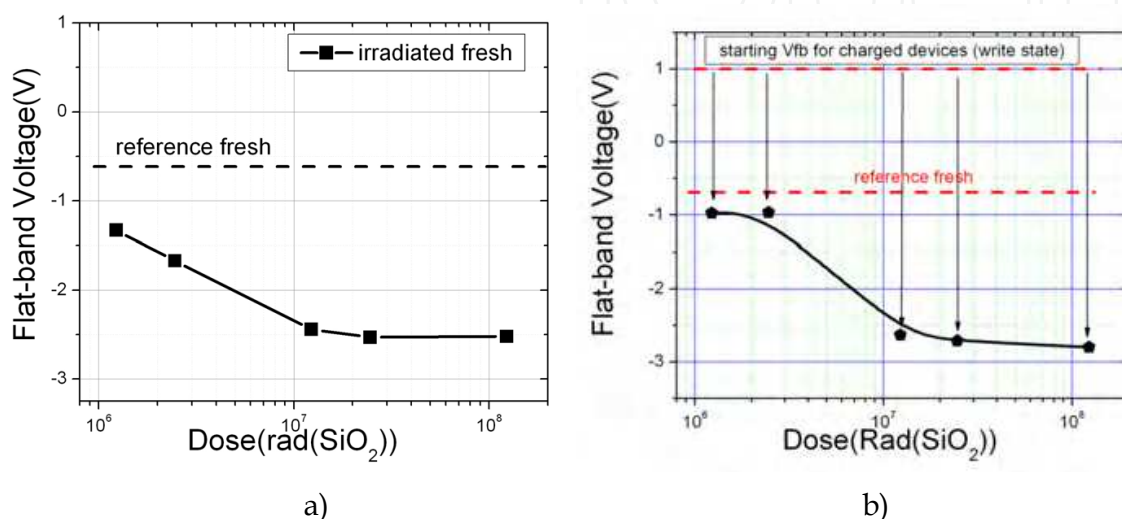


Fig. 21. Flat-band voltage after irradiation for a) fresh NC MOS capacitors and b) programmed “1” NC MOS capacitors.

Fig. 21a indicates that under irradiation the induced positive oxide trapped charge results in a shift of the C-V characteristics by 2V (the overall memory window is about 2.9V). If the oxide trapped charge is not removed from the oxide a permanent shift of the memory window would result, causing serious problems in reading the memory state. It was found that our devices could be restored to their initial memory window by tunnel annealing i.e. by electric field stressing (Ma & Dressendorfer, 1989). The memory behavior of 1.5MeV irradiated NC MOS capacitors was examined by symmetrical sweep C-V measurements of increasing width (2→2→2, 8→8→8, etc.) and under pulse operating conditions (see Fig. 22a). The initial, dose dependent, radiation induced shift disappears gradually by increasing the voltage sweep. Therefore, the memory window of irradiated devices approaches the memory window of the unirradiated devices, as also reported by Petkov (Petkov et al., 2004). In particular it was found that the radiation induced oxide charge can be removed with 1 write or erase pulse as shown in Fig. 22b.

For what concerns the NC MOSFETs similar results with the one presented above holds. As found for the NC MOS capacitors, the radiation induced oxide charge can be easily removed by electric field stressing (for example 1 write or erase pulse). No bit flip has been observed on charged (write state) devices as shown in Fig. 23. Comparing the  $V_{FB}$  shifts observed for the programmed NC MOS capacitors with the  $V_{th}$  shifts for programmed NC nMOS transistors it can be concluded that for the latter devices the effect of radiation induced positive charge trapped into the gate oxide is reduced. It is believed that this effect can be ascribed to the smaller thickness of control and tunneling oxides in the transistor case i.e. to

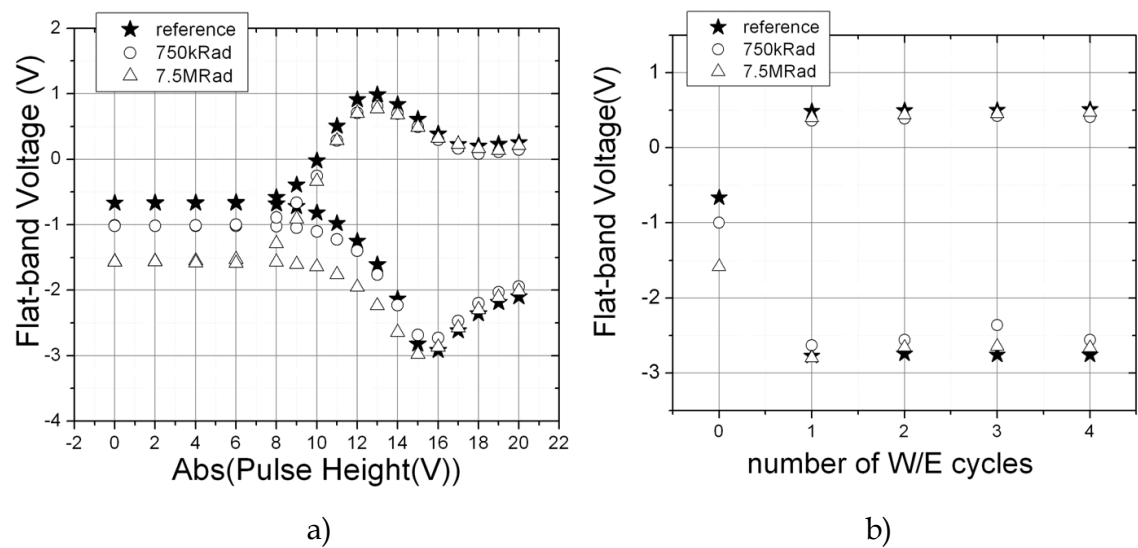


Fig. 22. a) Memory behavior after application of positive and negative pulses (heights from 2V to 20V, 1s duration) on irradiated NC MOS capacitors at 1.5MeV. The initial flat-band voltage differences disappear as higher gate pulses are applied, indicating the removal of the radiation induced positive oxide charge. b) Flat-band voltage evolution during 1s +14V/-16V write/erase cycles on irradiated NC MOS capacitors. The 0 cycle represent the after irradiation flat-band voltage. Differences between the flat-band voltage values of unirradiated and irradiated devices are not observed after the very first write or erase pulse, indicating the immediate removal of the radiation induced positive oxide charge.

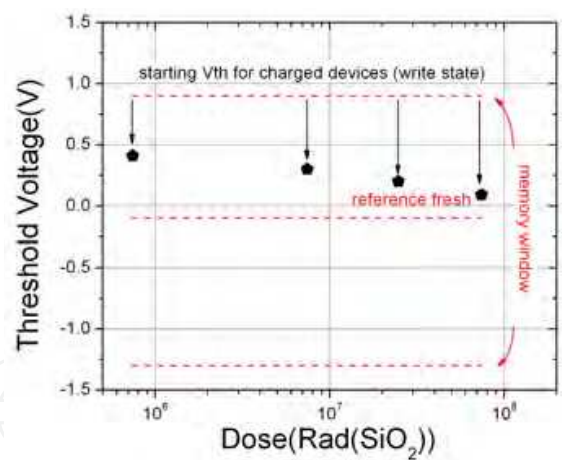


Fig. 23. Threshold voltage measured after irradiation for charged (write) transistors.

the fact that a larger percentage of oxide volume is at tunneling distance from the gate or substrate and thus a smaller volume is left for the radiation induced  $Q_{ot}$  (Ma & Dressendorfer, 1989).

The above result indicate that the read failure of irradiated NC transistor cells may appear only at doses above 1-10 Mrad(SiO<sub>2</sub>), thus more than 10 times higher than in FG cells.

### 7.2.4 Effects on charge retention

The charge retention time of the NC non-volatile memory devices is a characteristic of critical importance. What is required is that the write and erase states remain clearly

distinguished after a 10 yrs retention period. Charge retention was here measured through a waiting time of 12h after placing the devices in full write or erase state conditions. In Fig. 24a is presented the overall evolution of the memory window with time, while in Fig. 24b and Fig. 24d are shown the extracted flat-band voltage decay rates,  $dV_{fb}/d\text{Log}(t)$ . Charge loss rate for the write state is strongly dependent on the irradiation dose while for the erase state no such dependence is observed. It was found that the write state flat-band voltage decay rate depends on irradiation dose as  $\text{Dose}^{2/3}$ , (see Fig. 24b); the same dose

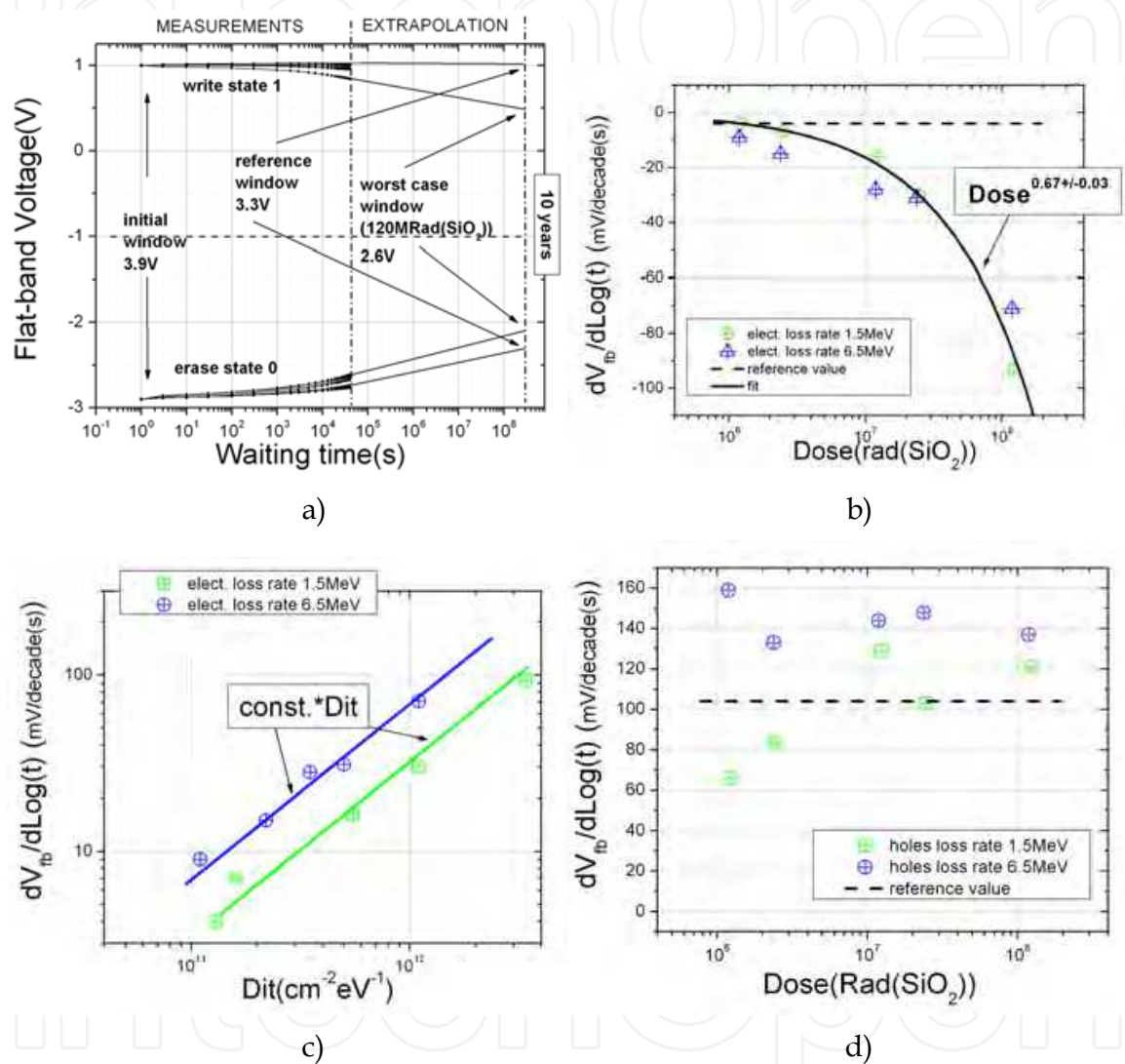


Fig. 24. a) Memory window evolution with time for 1.5MeV protons irradiated NC MOS capacitors. Memory window for unirradiated devices is also indicated. The dashed line is the  $V_{fb}$  of fresh unirradiated devices. These results applies also for 6.5MeV irradiations. b) Flat-band voltage decay rates for write state(1s, +14V) vs dose for irradiated NC MOS capacitors with 1.5MeV and 6.5MeV proton energies. The electron loss rate follows the relationship  $\text{Dose}^{2/3}$ , the same valid for  $D_{it}$ . c) Flat-band voltage decay rates for write state (1s, +14V) are plotted vs  $D_{it}$  and comparison with the relationship  $dV_{fb}/d\text{Log}(t)=\text{const} \cdot D_{it}$  is also shown to demonstrate the linear correlation found between electron loss rate and  $D_{it}$ . d) Flat-band voltage decay rates for erase state (1s, -16V) vs dose for 1.5MeV and 6.5MeV proton energies. A small increase in the loss rate is observed but not clear is the dependence with dose.



dependence that applies for  $D_{it}$ . This strongly suggests that the loss rate of stored electrons is directly related to the damage induced by irradiation at the Si-substrate/SiO<sub>2</sub> interface (Fig. 24c) as it was initially postulated by Shi (Shi et al., 1998). Previous measurements of electron loss at high temperatures revealed that the long-term retention of the present devices is due to the electron storage in NC traps (Dimitrakis & Normand, 2005).

Regarding the erase state (hole storage), the measured flat-band voltage decay rates show a small increase with respect to those of non-irradiated samples and unlike electrons they do not exhibit any clear dependence on dose. These results indicate that the discharging of “0” programmed NC MOS devices is indeed through defects located in the Si-rich injection oxide.

Compared to unirradiated NC devices, the reduction in the extrapolated memory window at 10-yr of irradiated NC devices does not exceed ~20% (worst case of samples irradiated with 120Mrad(SiO<sub>2</sub>)) being ~15% the charge lost by unirradiated devices while for irradiated ones it raises to ~35%.

Concerning the transistors, once again similar results with those presented for the capacitors have been found. Memory window as a function of the waiting time is shown in Fig. 25. It is clear that even in the worst case of NC MOS transistors irradiated with 75Mrad(SiO<sub>2</sub>), long time charge storage behavior is still observed. The 10-yr extrapolated values show that the charge lost is ~74% after irradiation at 75Mrad(SiO<sub>2</sub>) with ~17% more charge lost respect to the unirradiated devices.

It should be remarked that both capacitors and transistor structures irradiated with doses up to ~100 Mrad(SiO<sub>2</sub>) do not show failure of the retention characteristic. This means that retention failure in NC NVM cells may appear only at doses higher than 100 Mrad(SiO<sub>2</sub>), thus more than 10 times higher than in FG cells.

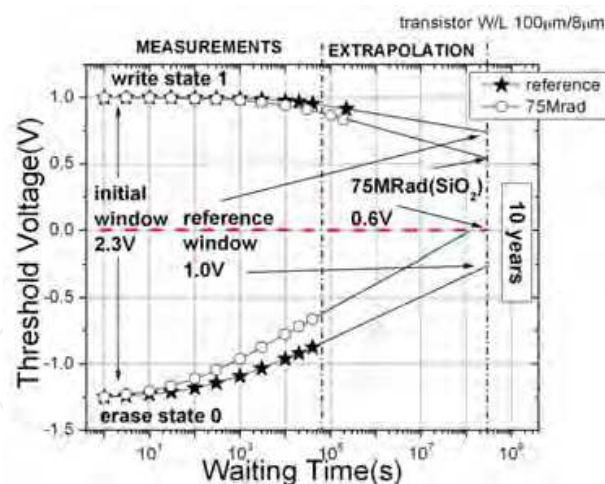


Fig. 25. Memory window evolution for unirradiated and irradiated at the highest dose NC MOS transistors. Extrapolations at 10 years shows that irradiated devices lost 40% of reference window.

### 7.2.5 Effects onto the endurance to write/erase cycles

Another important specification for non-volatile memories relate to the ability to endure repeated write/erase cycles. Endurance measurements, shown in Fig. 26, were carried out through a 15ms +9V/-9V write/erase pulse regime on all irradiated transistors. Neither degradation, nor drift in the memory window has been observed for all irradiated devices.



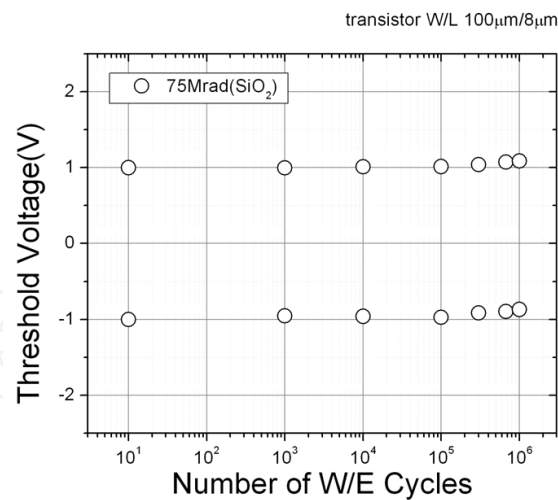


Fig. 26. Memory window evolution for unirradiated and irradiated at the highest dose NC MOS transistors. Extrapolations at 10 years shows that irradiated devices lost 40% of reference window.

## 8. Conclusions

In this chapter Si nanocrystal non-volatile memory devices were presented and characterized electrically. Memory windows as large as 3-4V have been shown with excellent retention and endurance characteristics. The above devices, in capacitor and transistor configuration, have been used in irradiation experiments with high energy protons and high fluencies showing superior radiation hardness, more than 10 times, respect to standard floating gate memories. It was found that transistor memory cells lose their information only above  $10^8$  rad(SiO<sub>2</sub>) which is outstanding. Furthermore, electron retention is affected by radiation and in particular has been identified a clear relationship between electron loss rate and density of interface states, driving to the conclusion that the Si NC NVMs considered in this work loose stored electrons by tunneling through the interface states. Hole's loss rate doesn't seem to be affected by the radiation. Endurance to w/e cycles remains unaltered after irradiation.

## 9. Acknowledgments

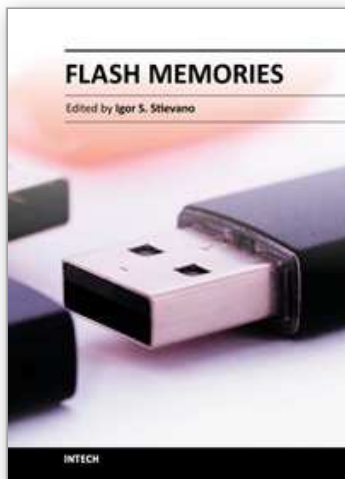
The authors would like to acknowledge the European Space Agency for financial support. We would like also to thank the collaborators who contributed to this research: Dr. P. Normand, Dr. P. Dimitrakis, Prof. M. Kokkoris and Mr. I. Anastasiadis.

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## **Flash Memories**

Edited by Prof. Igor Stievano

ISBN 978-953-307-272-2

Hard cover, 262 pages

**Publisher** InTech

**Published online** 06, September, 2011

**Published in print edition** September, 2011

Flash memories and memory systems are key resources for the development of electronic products implementing converging technologies or exploiting solid-state memory disks. This book illustrates state-of-the-art technologies and research studies on Flash memories. Topics in modeling, design, programming, and materials for memories are covered along with real application examples.

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