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Effect of Native Oxide on the Electric Field-induced Characteristics of Device-Quality Silicon at Room Temperature

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1. Introduction

There is no needing emphasize about the importance of silicon (*Si*) as a material of choice for almost all fields of the new nano- and microelectronics. Due to its unique structural and physical properties, polycrystalline *Si* seems to be of special interest as a base for creating so-called 3D-integrated circuits.

Various studies have established the main processes of carrier transport in the structures based on this material. In particular, it was shown that tunneling and diffusion recombination processes dominate under room temperature and applied low electric fields. Nevertheless, the analysis and numerical simulation of the experimental data do not always take into account the finite dimensions of the investigated structure and the appearance of carrier depletion as an important component of the tunneling current observed experimentally. Besides that, the fabrication of any device based on polycrystalline *Si* requires high-temperature treatment. Therefore, the effect of such a treatment on the electric properties of polycrystalline, amorphous and monocrystalline *Si* is also seemed to be important. Regardless of the huge number of publications describing numerous characteristics of the material and structures based on polycrystalline *Si* of various types of conductivity, the question about room temperature carrier depletion (exclusion from the contact regions) in polycrystalline material is still open.

As is known, native oxides of about 5-10 nm thickness are formed on surfaces after finishing growth of semiconductor bulk materials or deposition (by molecular beam epitaxy, modified liquid phase epitaxy, laser ablation, high-temperature treatment, etc.) of thin films immediately after excluding the samples from the technological chamber. These ultrathin layers form additional potential barriers which can sufficiently affect the performance of active elements.

This chapter reports experimental data resulted from the investigations of room-temperature current-voltage (IVC) and capacitance-voltage (CVC) characteristics performed on amorphous silicon thin films fabricated by the magnetron sputtering technique and bulk crystalline silicon of device quality grown by Czochralsky method. The low-resistive contact pads were placed on front and faceplate surfaces of the samples. Studies of room-temperature electric field-

induced characteristics for these structures are seemed to be important for analyzing operation of multi-element devices (for example, integrated circuits). It was found out that experimental IVC's and CBC's are similar to those of metal-insulator-semiconductor structures. These results are analyzed in framework of semiclassical theory of semiconductor devices.

2. Photosensitivity of amorphous silicon thin films prepared by magnetron sputtering

Amorphous silicon is a unique material for design of a large number of novel optoelectronic and photovoltaic devices. Structures *Me/α-Si* and *α-Si* thin films are the elements of choice not only for fundamental studies but also for practical applications and numerical simulations of their properties.

Examination of photosensitive and external electric field-induced characteristics of these structures is of particular interest. Metal-semiconductor junctions *Al/α-Si* were chosen as an object of the room temperature investigations. Amorphous silicon thin films (thickness up to 300 nm) were manufactured by magnetron sputtering technology in the range of the current density $(10^{-9}\text{-}10^{-7})$ A/cm^2 at T = 300 K.

Current-voltage characteristics nd photosensitivity of the samples was carried out under normal atmospheric conditions before and after the treatment of the structures in molecular hydrogen. The hydrogenation of the samples was provided by the special chamber filled in with molecular H2 during 24 hours at T = 400^{0}C and the gas pressure P_H = 2500 Pa (Khlyap, 2003).
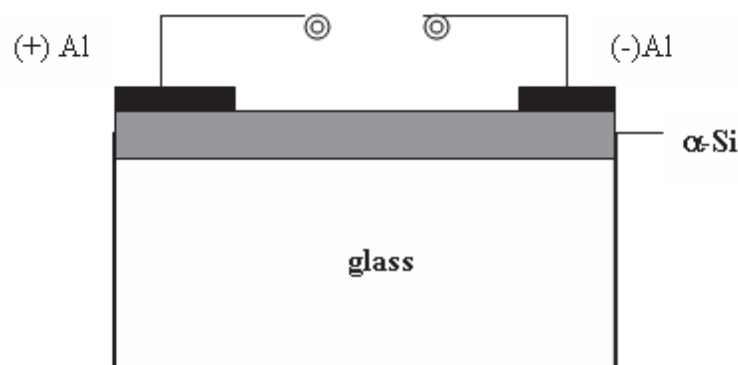

Fig. 1. Sketch of the experimental sample.

The experimental setup is plotted in Fig. 1. *α-Si* layers of 1 μm thickness were deposited on the glass substrate by magnetron sputtering under activation of *SiH$_4$* (silane) plasma dissociation at alternate pulse bias with 55 Hz frequency. Pressure and temperature in the growth chamber were *P* = 70 Pa and 225^{0}C, respectively. Aluminum (*Al*) contacts doped with silicon (1% *Si*) were manufactured through the mask of 1 mm diameter. The investigated structure had been connected to the experimental measurement equipment. Current-voltage characteristics were measured at room temperature under illumination by UV-, near-IR and visual spectral ranges.

The experimental current-voltage characteristics (IVC) of the investigated samples are illustrated by Fig. 2. The experiment was carried out under various illuminations. The IVCs obtained under the background illumination (daylight, curve 1) and under irradiation by the light source with 100 W power (curve 2) are approximated by the following expression:

$$I_{exper} \sim (V_a)^m, \tag{1}$$

where *m < 1*.

IVCs of the structures obtained after irradiation by the light source with wavelengths in the near-IR spectral region (curve 3) and by the UV source (curve 4) can be expressed as

$$I_{exper} \sim I_s \exp(eV_a/k_B T)^m, \tag{2}$$

where I_s is a saturation current defined by the parameters of the film (charge carrier mobility and the dangling bonds density as well as by the tunneling transparency coefficient of the *Al - α-Si* barrier (Terukov, 2000&2001).
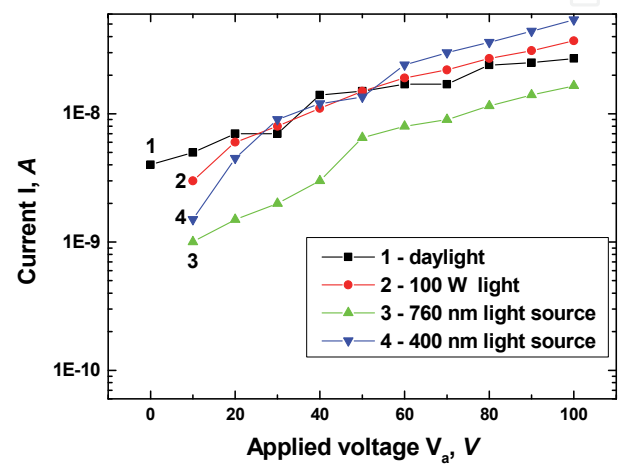

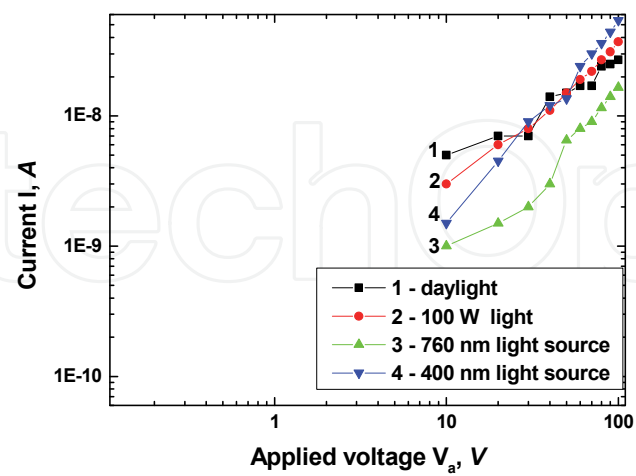Fig. 2. Current-voltage characteristic of the investigated sample (T = 300 K) (Khlyap, 2003).

Fig. 3. Current-voltage characteristics of the investigated structure in double-log scale (Khlyap, 2003).

Re-building the experimental IVC in double-log scale (Fig. 3) allows obtaining more detail information about current mechanisms in the structures investigated.

It is obvious that all the experimental current-voltage dependencies are approximated by straight lines. According to the model (Terukov, 2001; Sze, 2007) one can suggest the following explanation: the investigated samples are high-resistive films with one group of the trap centers localized up the bottom of the conduction band (Fig. 4, Terukov, 2002). Appearance of these centers causes the space charge limited current (SCLC).
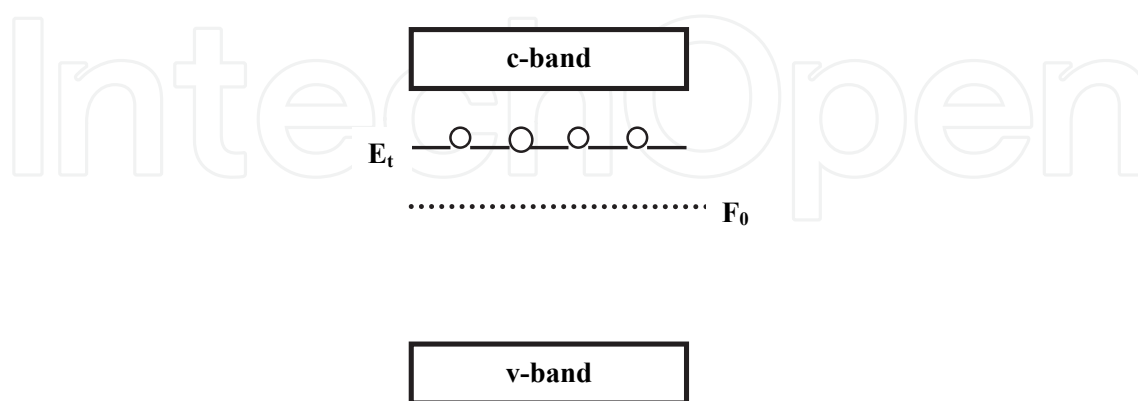

Fig. 4. Schematic drawing of the energy levels in the forbidden gap of amorphous silicon under thermodynamic equilibrium. E_t is the trap level, F_0 is the Fermi level position (Terukov, 2000&2001).

In absence of the external electric field the initial electron concentration in the investigated films is low and determined by the localization of the Fermi level of the material. In turn, the Fermi level localization depends on the concentration and the ionization energy of the trap centers E_t. Under small applied bias the electrons injected from the *Al* contacts are confined by the traps E_t. As the applied voltage increases, the centers E_t receive more and more electrons; at the same time, the concentration of the injected charge carriers is also increasing. This process is experimentally observed in the linear sections of the IVCs with different slopes *m*. UV-radiation accelerates the interaction between the injected charge carriers and the ones accumulated by the trap centers [Terukov, 2000; Khlyap, 2003].

The IR-photosensitivity of the films is of particular importance. The challenge is that the as-grown films are quite not photosensitive. One of the simplest ways to make the layers photosensitive is hydrogenation treatment of the films under certain temperatures. The as-grown layers were placed in the special chamber filled with the molecular hydrogen for 24 hours at 400⁰C (the gas pressure in the chamber was 2500 Pa). Fig. 5 shows the experimental current-voltage dependencies.

The experiment showed a sufficient reduction of the films resistance compared with original values. The slope m has also been changed down to: m ~ 0.6 – 0.7. The photosensitivity in the near-IR spectral region (~1600 nm) is also sufficiently improved at the applied bias 0-50 V (Khlyap, 2003).

3. Charge carriers exclusion in electronic polycrystalline silicon

The simple and reliable technique of current-voltage characteristics measurements was applied for studying processes of carrier transport in the electronic polycrystalline silicon (Reich; Akopian; Khlyap, 2004). The best samples of polycrystalline *Si* grown by the

Czochralsky method were chosen for the investigations. Specimens of columnar and granular crystal structure with dimensions 8mm×2mm×2mm of *n*-type conductivity were polished in the solution *HNO₃:HF:CH₃COOH* = 3:1:1 and rinsed in unionized water in order to maximally avoid the possible influence of surface effects on the results of electrical measurements. The studies were carried out at room temperature under applied electric fields 0 – 104 Vm⁻¹, corresponding to applied biases in the range of 0 – 190 V.
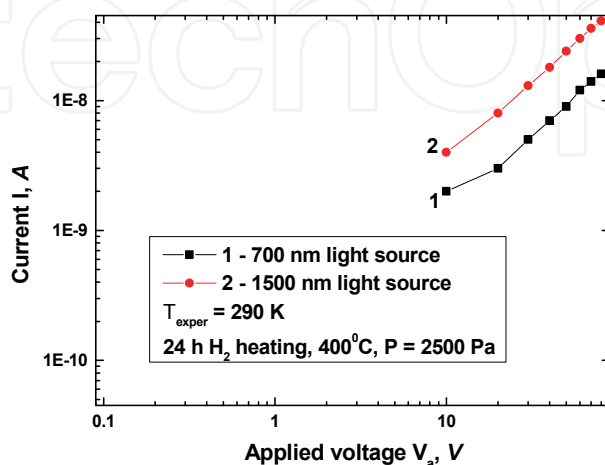

Fig. 5. Experimental current-voltage characteristics of the investigated samples after hydrogenation (Khlyap, 2003).

High-temperature (up to 1200⁰C) heat treatment of the samples was performed under normal atmospheric conditions during 6 h in the furnace of the special construction providing a stationary temperature gradient along the sample. The measurements of current-voltage characteristics (IVC) were performed by means of the traditional bridge method (Sze). Indium contacts were thermally deposited on the lateral facets of the sample. The left and right contacts will be referred further as the first and the second ones, respectively. All experimental dependencies are represented in the coordinates of *ln j ~ (Vₐ)^{1/2}*, where *j* is the current density and *Vₐ* stands for the applied voltage. Fig. 6 shows the IVC of the sample of the columnar polycrystalline-like structure. As one can see, both curves ("forward" and "reverse") have no considerable difference, indicating a good quality of metallic contacts. This IVC demonstrates the domination of at least two-step tunneling with the threshold voltage *V_{TR}* ~ 9 V (Khlyap, 2004).

On the contrary, the IVC of the sample with the granular structure exhibited no asymmetry between the forward and reverse currents (Fig. 7) (Khlyap, 2004).

High-temperature treatment (1100⁰C) of both samples does not change the IVCs qualitatively (Fig. 8). However, the resistance of the samples becomes lower and the threshold voltage of the sample with the columnar structure reduces down to 4 V. Increase of the treatment temperature up to 1100⁰C does not lead to significant changes of the IVCs in neither sample.

As we have noted, the dominant process in carrier transport is the tunneling. Nevertheless, the attempts of numerical simulations of the experimental data according to the theoretical models developed specifically for tunneling currents (Sze) failed to describe the observed results, so that we have been forced to take into consideration the phenomena of carrier
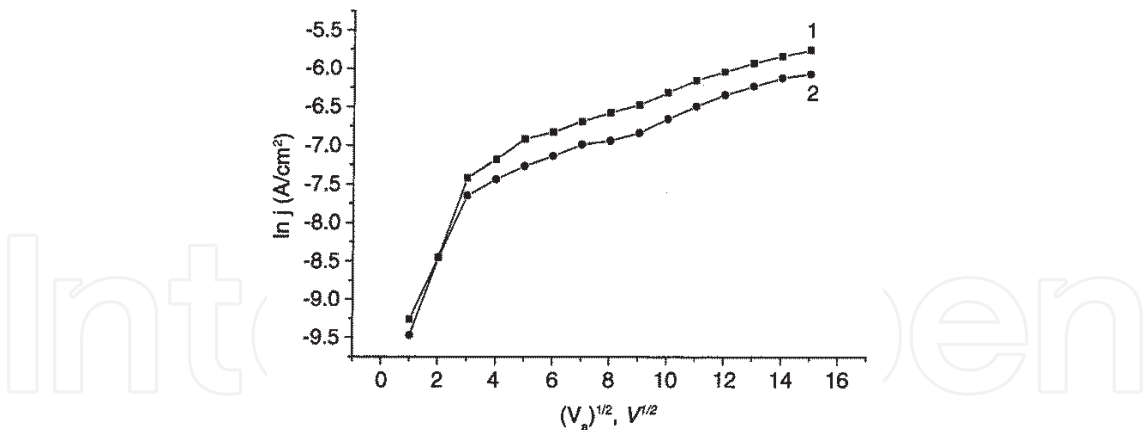
Fig. 6. Forward (curve 1) and reverse (curve 2) currents of the sample with the columnar structure before high temperature treatment (Khlyap, 2004).
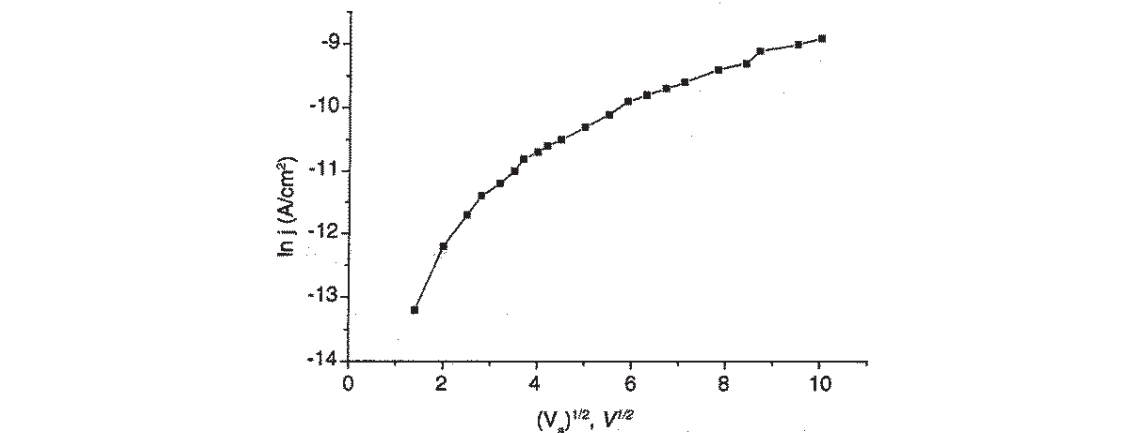

Fig. 7. Current-voltage characteristics of the sample with granular structure before high-temperature treatment (Khlyap, 2004).
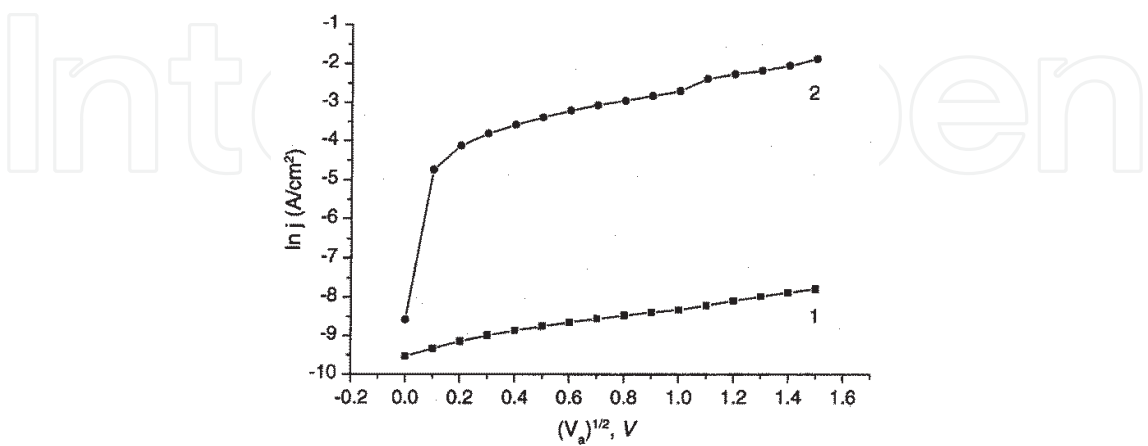

Fig. 8. Current-voltage characteristics of both samples (curve1 corresponds to the sample with granular structure and curve 2 corresponds to the sample with columnar structure) after high-temperature (900^{0}C) treatment (Khlyap, 2004).

depletion and fluctuation of the carrier concentration on the inter-grain boundaries in the bulk of the sample (Reich, Akopian).

The depletion of charge carriers was observed experimentally and analyzed in the Ge-based monocrystalline diodes of finite length (Akopian). The effect strongly depends on the surface recombination velocity, sample length and temperature. The problem is somewhat more complicated for the structures based on polycrystalline materials, because it is necessary to take into account the processes of charge transfer along the sub-grain boundaries. The most important is to estimate the potential distribution in the bulk of the sample in order o determine the regions of carrier depletion. The potential distribution caused by the movement of carriers from the first contact toward the second one is described by the following expression (Akopian):

$$U = (k_B T/e)[lj(D_{ni})-1 - 6l^2(n_0)3/L^2n_i(2n_0 + n_i)], \qquad (3)$$

where l is the length of the sample, j is the charge carriers flow, $L = [(2D_nD_p/(D_n + D_p)\tau]^{1/2}$, $D_{n,p}$ are the diffusion coefficients for electrons and holes and $\tau = 10^{-8}$ s is the lifetime of the carriers (this value is accepted to be the same for both electrons and holes), $n_0 = 10^{10}$ cm^{-3} stands for the intrinsic electron concentration, and $n_i = 10^{18}$ cm^{-3} takes care of the carrier concentration immediately involved in the charge transfer. Numerical estimations were carried out for both the samples. The depletion as an almost completely sweep out of the carriers was observed only for the sample of the columnar structure after the heat treatment at 900^{0}C. The results obtained for this sample are plotted in Fig. 9 for the range of applied biases 0.2-1.8 V, which seems to be of particular interest for device operation. The linear character of the calculated potential distribution shows (Khlyap, 2004) a considerable accumulation of carriers near he second contact region increasing with the increase of the applied bias.
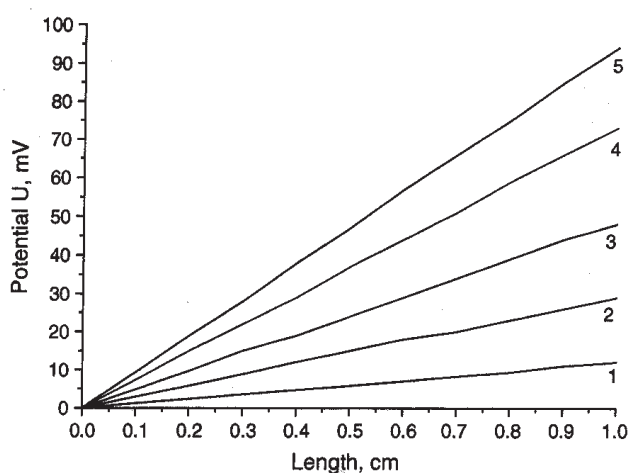

Fig. 9. Potential distribution for the sample with columnar structure after high-temperature (900^{0}C) treatment at the applied voltage V_a, V: (1) 0.2, (2) 0.6, (3) 1.0, (4) 1.4, (5) 1.8 (Khlyap, 2004).

According to the theory developed in (Reich et al.), the tunneling current j reads as follows:

$$\ln(j/j_0) = (-1/5)(2/\pi)^{1/2}(U_0/E_B)^{5/4}[n_i(a_B)^3]^{-1/2}, \qquad (4)$$

where U_0 is the height of the barrier, $E_B = me^4/(h^2/2\pi^2)\varepsilon^2$ and $a_B = (h^2/4\pi^2)^2\varepsilon/me^2$ are the Bohr radius and energy for the electron, m_e is the effective mass, ε is the dielectric constant of *Si*, and j_0 stands for the saturation current. The calculation based on experimental data has demonstrated that the barrier height U_0 before the heat treatment of the samples is 0.48 eV and 0.36 eV for the granular and columnar samples, respectively. After heat treatment under 900⁰C these values are 0.12 and 0.9 eV, respectively (Khlyap, 2004).

In summary, current-voltage characteristics and the effect of the high-temperature heat treatment (900 – 1100⁰C) on carrier transfer in bulk polycrystalline *Si* of granular and columnar structures have been investigated. The temperature 900⁰C has been shown to be optimal for i) reduction of the barrier height in samples of granular structure and ii) a considerable accumulation of carriers in the region of the second contact. The first experimental results reported in (Khlyap, 2004) demonstrated the possibility of additional accumulation of charge carriers in bulk polycrystalline *Si* of *n*-type conductivity after high temperature treatment without sufficient increase of the applied electric field (Khlyap, 2004).

4. Electric characteristics of the structure bulk silicon – native oxide

As we have mentioned above, the native oxide formed immediately after the sample preparation (a bulk specimen or a thin film) is an unavoidable factor of any technological process and the following design of the active element. We have investigated room-temperature electrical (current-voltage, IVC, and capacitance-voltage, CVC) characteristics of the structure bulk silicon-native oxide. The scheme of the contacts (idium pads) deposited on the bulk silicon sample is illustrated in Fig. 10.
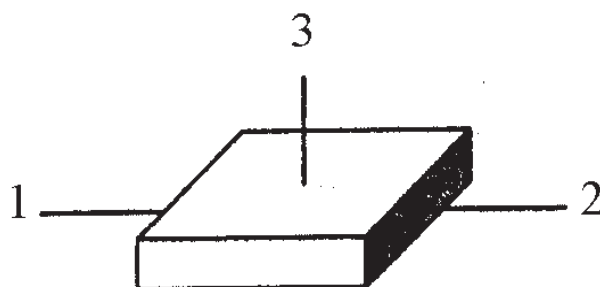

Fig. 10. Schematic image of In-contact pads deposited on the bulk crystalline silicon sample for the room-temperature electric investigations.

We have focused on examining the current-voltage functions registered under the application of external electric field in directions '1-2" and "2-1" as well as in directions "1-3, 2-3" and "3-1, 3-2". The sets of the device-quality crystalline silicon of n-type conductivity were chosen for this experiment. The samples were cut off from the as-grown ingots.

The experimental electric field-induced characteristics are plotted in Fig.11, a-c. Obvious that all the experimental current-voltage functions are described by the power law $I\sim(F_a)^m$, where F_a is an applied electric field, and m is an exponential factor determining the mode of the charge carriers transfer through the sample as a finite volume (directions 1-2 and 2-1) and through the sample volume – sample surface space (direction 1-3). The numerical analysis performed in the frame of the semiclassical model (Sze) demonstrated that the carriers flow through the volume of the sample according to the ballistic – diffusion mode (the forward current, Fig.11, a), and the dominant tunneling current is observed for the

reverse current (Fig.11, b). The tunneling current is also observed for the direction 1-3 (Fig.11, c), but as the applied electric field increases, the tunneling process begins to be suppressed by the diffusion of the curries due to lowering the potential barrier formed by the native oxide.
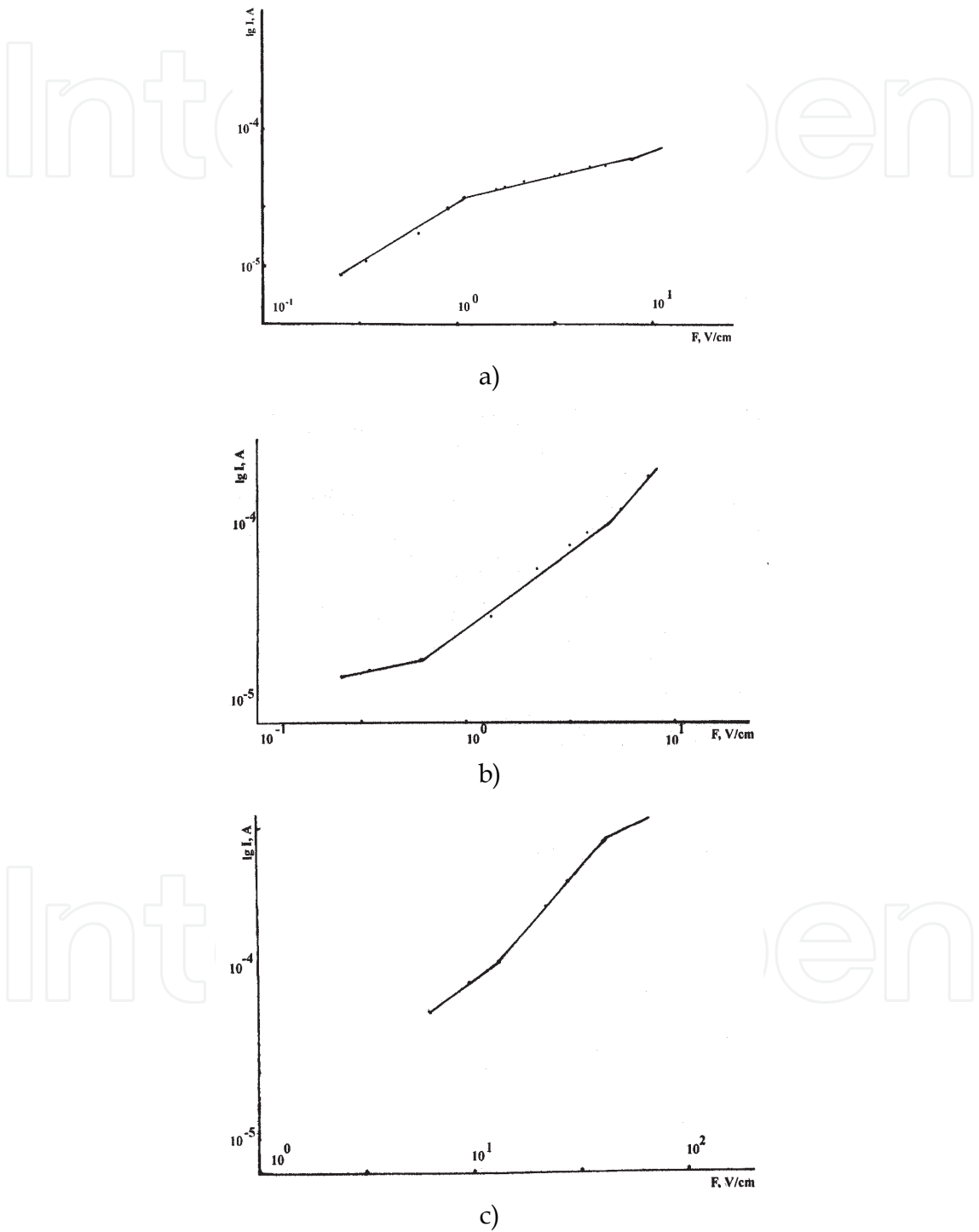

a)

b)

c)

Fig. 11. Room-temperature electric field-induced characteristics of the structure bulk crystalline silicon-native oxide; a) contacts 1-2, b) contacts 2-1, c) contacts 1-3 (see notes in Fig.10).

Thus, these experimental data are of the barrier type which is more typical for as-prepared metal-semiconductor structures. To confirm this conclusion we have made the capacitance-voltage measurements at T = 290 k and the test signal frequency f = 1 kHz. The experimental results are plotted in Fig.12, a-c.
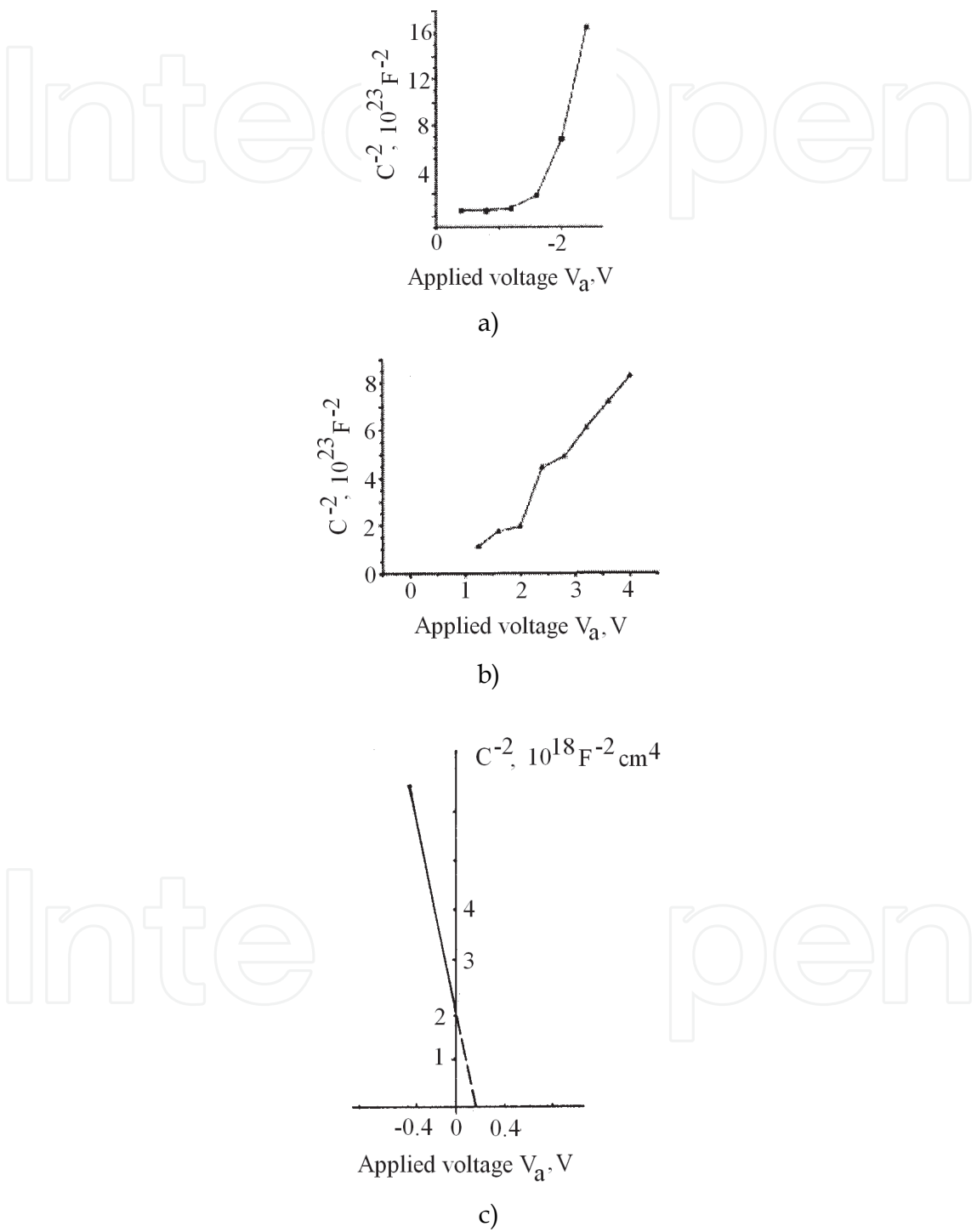

a)

b)

c)

Fig. 12. Room-temperature capacitance-voltage characteristics of the investigated structure under the test signal frequency f = 1 kHz: a) contacts 1-2; b) contacts 1-3 (see notes in Fig.10); c) a control metal-semiconductor structure (In-mono-n-Si).

The experimental data have allowed calculating some main parameters of the structure bulk crystalline silicon-native oxide according to the theory (Sze). The results are listed in Table 1.

Charge centers concentration	Contact	Space charge region width	Diffusion potential
N_{01}=1.26×10^{12} cm^{-2} N_{02}=7.05×10^{12} cm^{-2}	1-2	W_{01}=14.8 μm W_{02}=14.9 μm	V_{d1} = 0.53 V V_{d2} =1.40 V
N_{01}=1.62×10^{13} cm^{-2} N_{02}=1.94×10^{13} cm^{-2}	2-3	W_{01}=15.5 μm W_{02}=15.5 μm	V_{d1} = 3.50 V, V_{d2} = 4.20 V

Table 1. Electric parameters of the investigated structure.

5. Electric parameters of the structure recrystallized nanocrystalline silicon-Cu/Ag-nanocluster contacts

The unique room-temperature electrical characteristics of the porous metallic nanocluster-based structures deposited by the wet chemical technology on conventional silicon-based solar cells were described in (Laptev & Khlyap, 2008). We have analyzed the current-voltage characteristics of Cu-Ag-metallic nanocluster contact stripes and we have registered for the first time dark currents in metallic structures. Morphological investigations (Laptev & Khlyap, Kozar et al., 2010) demonstrated that copper particles are smaller than 0.1 μm and smaller than the pore diameter in silver. The contacts were deposited on nanocrystalline silicon structures obtained by the pulse laser recrystallization of the silicon thin films grown on insulator substrates. The experimental results are illustrated in Fig.13.

The numerical analysis showed the following results: the first section of forward current

$$I = T_{tun}A_{el}(4\varepsilon/9L^2)(2e/m^*)^{1/2}(V_a)^{3/2}$$

(ballistic mode) and the second one as

$$I = T_{tun}A_{el}(2\varepsilon v_s/L^2)V_a,$$

and the reverse current is

$$I = T_{tun}A_{el}(2\varepsilon v_s/L^2)V_a$$

(velocity saturation mode). Here T_{tun} is a tunneling transparency coefficient of the potential barrier formed by the ultrathin native oxide films, A_{el} and L are the electrical area and the length of the investigated structure, respectively, ε is the electrical permittivity of the structure, m^* is the effective mass of the charge carriers in the metallic Cu-Ag-nanoclucter structure, and v_s is the carrier velocity (Kozar et al., 2010). These experimental data lead to the conclusion that the charge carriers can be ejected from the pores of the Cu-Ag-nanocluster wire in the potential barrier and drift under applied electric field (Sze & Ng, 2007; Peleshchak & Yatsyshyn, 1996; Datta, 2006; Ferry & Goodnick, 2005; Rhoderick, 1978).
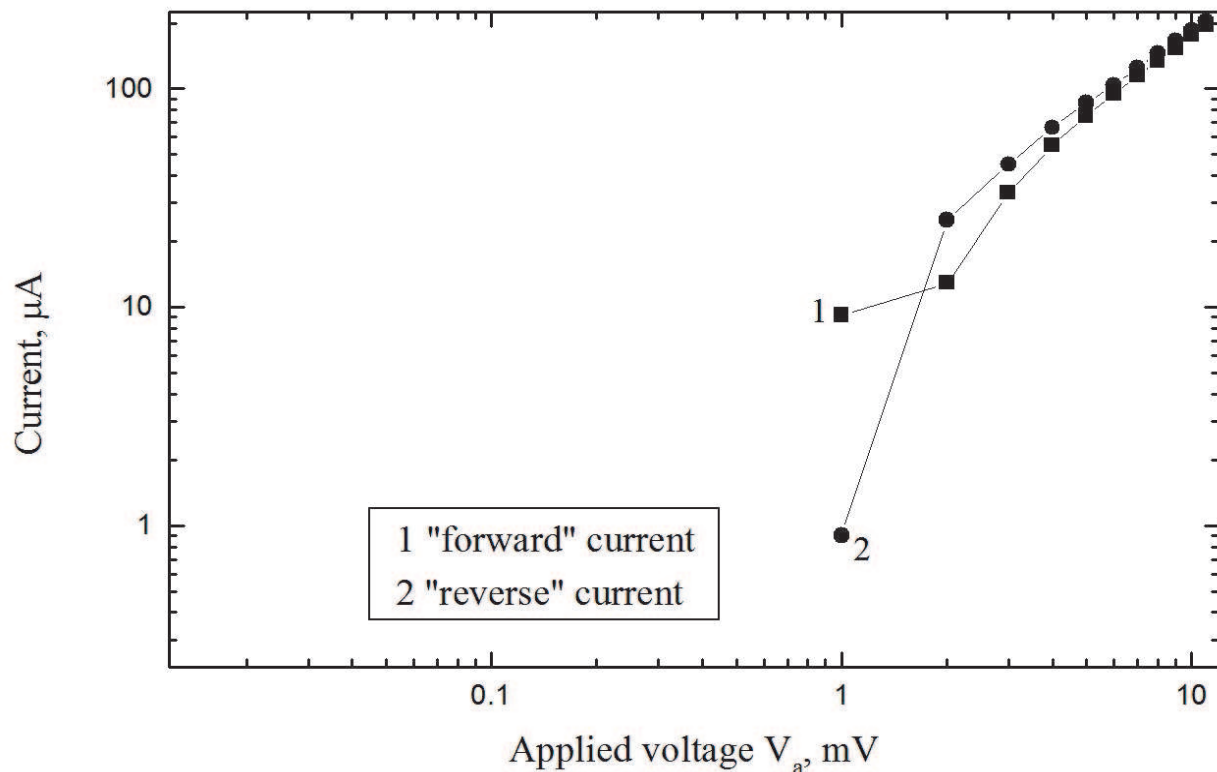
Fig. 13. Room-temperature current-voltage characteristics of the structure recrystallized nanocrystalline silicon-Ag/Cu-nanocluster contacts.

6. Conclusions

The chapter presented here reviews the principal experimental results obtained under simple and reliable room-temperature electric measurements of the structures based on various type of device-quality silicon with taking into account the effect of ultrathin native oxide films unavoidably formed after the preparation of the active element. Amorphous silicon thin films prepared by the magnetron sputtering technology have showed good photosensitive properties. Polycrystalline bulk silicon samples were investigated after the high-temperature treatment in order to clarify this effect on electrical performance of the active elements (in particular, future ICs). The necessity of different placement of contact pads on bulk crystalline silicon samples have forced us to concentrate on the examination of the IVC and CVc of the structures formed by the silicon samples and the native oxide. These investigations demonstrated that the influence of the native oxide ultrathin films forming additional (sharp or graded) potential barriers is to be taken into account under many technological processes using for the device design. And, the attempting to solve the problem of the performance of low-cost high-effective solar cells based on conventional silicon resulted in unique chemical wet deposition technology which has allowed producing Ag/Cu-nanoclustered structures on recrystallized nanocrystalline silicon. Their current-voltage characteristics are similar to those of semiclassical metal-semiconductor structures

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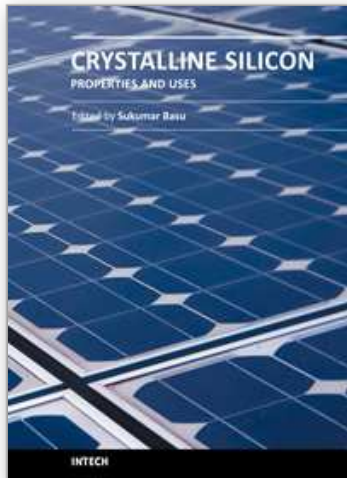
Crystalline Silicon - Properties and Uses

Edited by Prof. Sukumar Basu

The exciting world of crystalline silicon is the source of the spectacular advancement of discrete electronic devices and solar cells. The exploitation of ever changing properties of crystalline silicon with dimensional transformation may indicate more innovative silicon based technologies in near future. For example, the discovery of nanocrystalline silicon has largely overcome the obstacles of using silicon as optoelectronic material. The further research and development is necessary to find out the treasures hidden within this material. The book presents different forms of silicon material, their preparation and properties. The modern techniques to study the surface and interface defect states, dislocations, and so on, in different crystalline forms have been highlighted in this book. This book presents basic and applied aspects of different crystalline forms of silicon in wide range of information from materials to devices.

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Halyna Khlyap, Viktor Laptev, Luydmila Pankiv and Volodymyr Tsmots (2011). Native Oxide as an Unavoidable Factor Affecting Room-Temperature Electric Field-Induced Characteristics of Device-Quality Silicon, Crystalline Silicon - Properties and Uses, Prof. Sukumar Basu (Ed.), ISBN: 978-953-307-587-7, InTech, Available from: http://www.intechopen.com/books/crystalline-silicon-properties-and-uses/native-oxide-as-an-unavoidable-factor-affecting-room-temperature-electric-field-induced-characterist

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