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# Image Artifacts by Charge Pocket in Floating Diffusion Region on CMOS Image Sensors

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## 1. Introduction

Complementary metal-oxide-semiconductor (CMOS) image sensors (CIS) are widely used in applications such as mobile equipment, PC cameras, and portable digital cameras due to their low power consumption and low cost. Today, CIS pixel sizes are being continuously reduced, down to the 1.0  $\mu\text{m}$  level in 90-nm CMOS, as industrial applications require higher pixel density. The industry requests, however, continued good performance even when the pixel dimensions are further reduced. In particular, dark current in CIS is an important parameter that determines the image performance in low light. The dark current component can change the charge capacity in photo diodes (PD) and hence the output signal as a function of location and time (J. P. Albert, 2001 and H.-S. Philip, 1998). An increase in dark current can also affect the dynamic range due to an increase in shot noise (H.Y.Cheng, 2003). By suppressing the dark current, the fixed pattern noise of the imager and the white pixel-defects can be reduced (K. A. Parulski, 1985). Photo diodes and pixel architecture of image sensors have been optimized to reduce image artifacts and hence dark current. (N. V. Loukianova, 2003; H.I.Kwon, 2004).

The key technology feature for high image-quality CMOS image sensor is the formation of a low-leakage buried photodiode with a transfer gate (TG). The buried PD is a promising concept to reduce the dark current. Many researchers reported that the vicinity of the shallow-trench isolation (STI) to the PD is the main source of dark leakage. By designing and characterizing special diode test structures, H. I. Kwon et al. (2004) demonstrated that the dark leakage decreases as the distance between STI and PD increases. Takashi Watanabe et al. (2010) showed that dark current can be improved by avoiding charge diffusion injection from the PD to the substrate using an optimized well structure under the PD. The effects of area, perimeter, and corner on leakage were, however, not separately investigated.

The buried floating diffusion (FD), on the other side of the pass transistor, was also studied by H.I.Kwon et al. (2004) and K. Mabuchi, et al. (2004). H.I.Kwon et al. (2004) explained that

the FD can be the source of increased dark currents in the single frame capture mode, even though dark signal in the normal operation mode is negligible because the signal processing time in the FD is very short compared to the integration time of the transfer gate. K. Mabuchi, et al. (2004) explained that zero lag and zero noise can be achieved when the signal electrons in the buried FD are completely transferred. There was no analysis done, however, on image artifacts, called dark spots, originating from the buried FD in CMOS image sensors.

The following two sections of this chapter deal with technologies to reduce dark leakage in buried photo diodes (Richard Merrill), and to reduce image artifacts in floating diffusions. The discussion begins with the design of new diodes with surface and buried configurations for photo diode and floating diffusion region. In the first section, the mechanism accountable for leakage in diode structures and the dependence of leakage current on electric field are discussed, explaining the importance of introducing a buried floating diffusion to improve dark leakage. In the second section, the mechanism for image artifact in floating diffusions is explained and a new method to avoid artifacts is suggested.

In this paper, leakage current was measured at diode structures with and without boron in Si surface to analyze the difference between surface and buried PD by comparing activation energy. Pinch off voltage and the charge pocket as a function of buried FD types are examined. Simulation and image characterization are done to find out the source of the dark spot. Finally generation mechanism for dark spot in CMOS Active Pixel Sensor (APS) is explained.

## 2. Diode design and fabrication

The design and fabrication of photo diodes and floating diffusion are discussed separately.

### 2.1 Design of surface and buried photo diodes

New test structures are designed to investigate potential sources of leakage at the area, perimeter, and corner of surface and buried photo diodes.

A schematic cross-section of the surface and buried test structures is shown in Figure. 1(a). The buried structure minimizes the surface leakage component as opposed to the surface diode where interface-state generation increases leakage. Fig. 1(b) shows the top view of the test structure with island cell, block, periphery (peri), and island-types. Here, island cell includes the transfer gate and island type does not. The structures are designed to have same area but different perimeter and number of corners to analyze edge and corner leakage components and compare them with standard  $n^+$ /pwell diodes of logic devices (Fig. 2). To analyze the contribution from the area, perimeter, and corners, leakage current is measured using test patterns with large area. Large area block diodes (area  $60000 \mu\text{m}^2$ , peri. :  $910 \mu\text{m}$ , corner : 4 ea) are designed to monitor the leakage current due to bulk and surface of the PD, and perimeter finger type diodes (area :  $60,000 \mu\text{m}^2$ , peri., :  $12,750 \mu\text{m}$ , corner : 300 ea) are designed to measure the leakage current by the sidewall junctions. Corner intensive type diodes (area :  $60,000 \mu\text{m}^2$ , peri.:  $24,000 \mu\text{m}$ , corner : 4,800 ea) also are designed to monitor the corner effect on photo diode. To compare the image quality with and without Si surface effects, CMOS image sensors with  $3.3\mu\text{m} \times 3.3\mu\text{m}$  pixel size are fabricated using the standard  $0.18\mu\text{m}$  CMOS logic process.

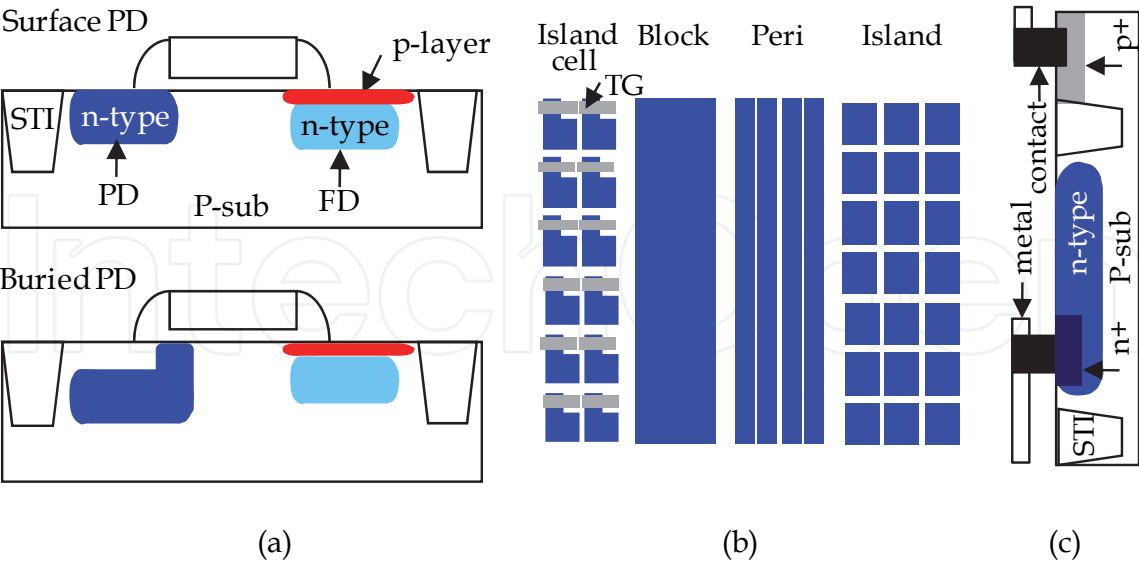


Fig. 1. (a) Schematic cross-section of CMOS image sensor for surface and buried diode. (b) Top view for buried diode structure with island cell, block, peri, and island-types. (c) Concept for test pattern to measure the leakage of diode.

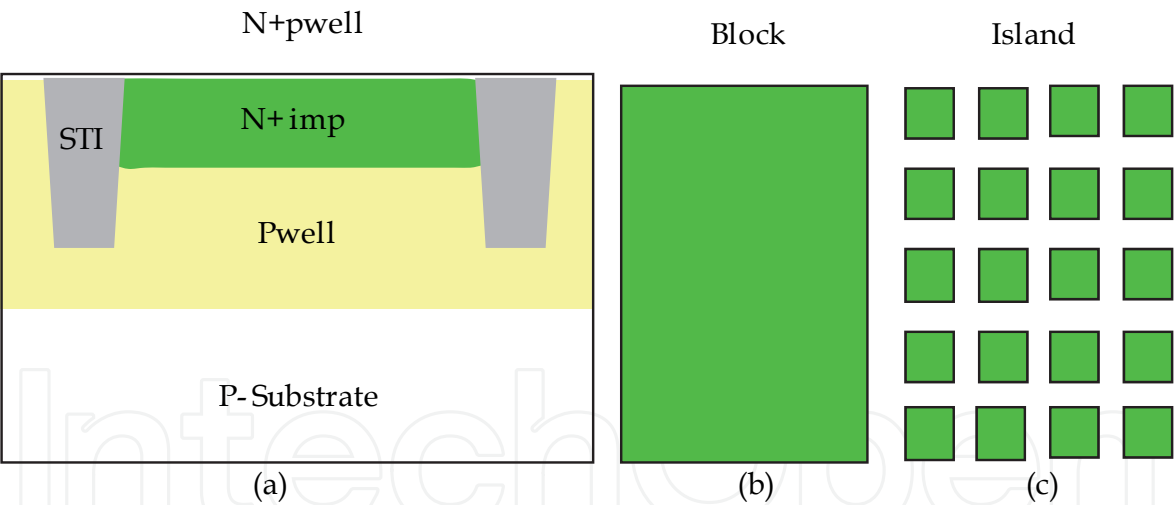


Fig. 2. (a) Shows the cross sectional view for standard n+/pwell diode structure. Fig. 2(b) and 2(c) show top view of standard diode structure for block and island types, respectively. Standard n+/pwell diodes constitute a reference for junction leakage characteristics.

2.2 Diode designs of floating diffusion

To evaluate the leakage characteristics of floating diffusion, two different structures are designed, one with a top p-layer (Fig. 3a), and the other without a top p-layer (Fig. 3b). Both floating diffusions are placed at a safe distance from the STI boundaries. The purpose of adding a top p-layer to one of the buried diffusions is to suppress the surface leakage component by reducing the spread of the junction depletion region into the surface.

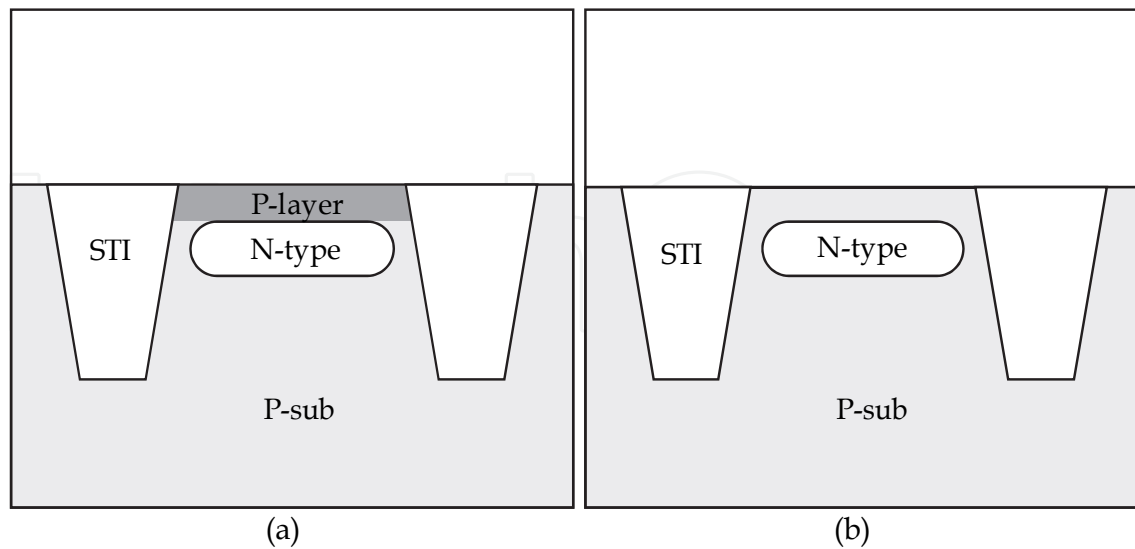


Fig. 3. Schematic cross-section of floating diffusion test structures. (a) with top p-layer. (b) without top p-layer. The p-layer reduces the spread of junction depletion into the surface and hence suppresses the surface leakage component.

### 2.3 Fabrication

The surface and buried photo diodes in Fig. 1 are fabricated in a typical 0.18 $\mu\text{m}$  CMOS logic technology. This includes shallow trench isolation, retrograde channel doping, dual gate oxide (70 $\text{\AA}$ /32 $\text{\AA}$  for 3.3 V/1.8 V) and self-aligned gate and source/drain. The diode is formed by implanting an n-region at a phosphorus dose of  $5.0\text{E}12\text{ cm}^{-2}$  with 75keV while the standard N<sup>+</sup> source/drain is implanted with arsenic at a dose of  $5\text{E}15\text{ cm}^{-2}$  with 50keV. After completion of the process, micro lenses are formed to evaluate the image quality by focusing more light into pixels. Fig.4(a) shows the process sequence for photo diode and floating diffusion region. Photo diode is fabricated after gate patterning. Floating diffusion region as a buried type is applied phosphorus implant after photo diode formation and then processed boron implant before and after sidewall etching. In order to control doping profile under the overlap region of transfer gate, two different kinds of concept are processed as shown in Fig. 4(b). Process-1 means floating diffusion applying phosphorus and boron in FDN and boron in FDP to control capacitance in FD region. This concept is applied a large amount of Ph dose under the overlap region. But, in process-2, phosphorus is applied separately in FDN and FDP step. Ph dose is applied smaller dose in FDN step to control doping profile under the sidewall spacer region as a lower dose than process-1 and is added at FDP step for the remaining dose to make same amount with process-1 which is to control capacitance as the same target with process-1 at the non-overlap region. Thus, boron dose is applied same dose on process-1 and process-2 at FDP step. P-layer dose has to be decided to minimize the leakage and control total capacitance in floating diffusion on both processes. Only difference between process-1 and process-2 is Ph dose under gate overlap in FD side, which is to manage potential profile.

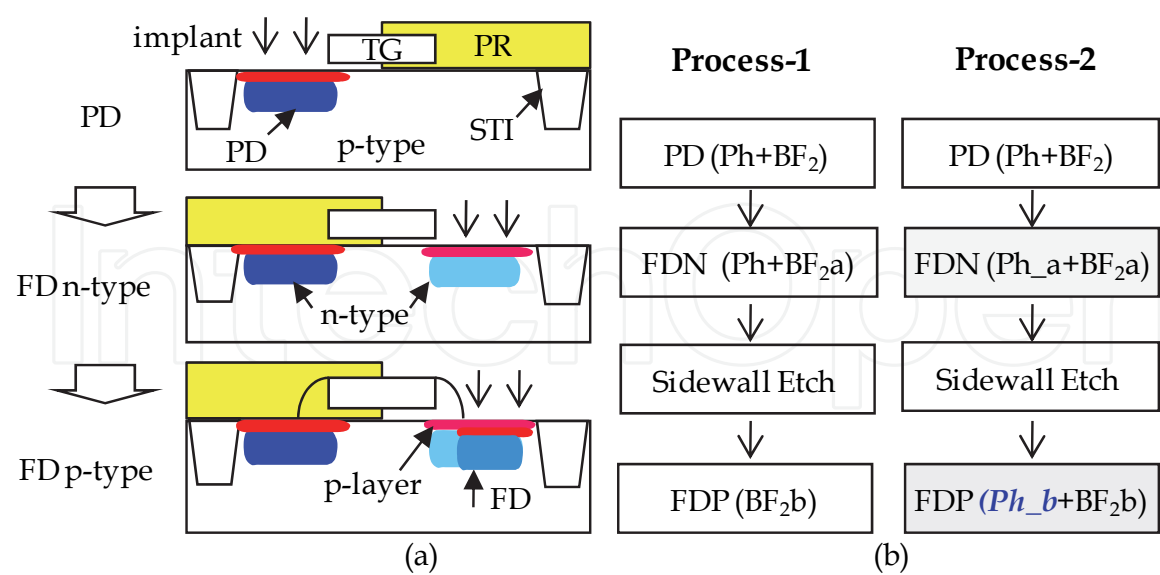


Fig. 4. (a) Process sequence for photo diode and floating diffusion region. Floating diffusion region was fabricated after photo diode process and p-layer region on FD was applied to reduce leakage current. (b) Process condition with process schemes was compared. Total dose for Ph<sub>a</sub> and Ph<sub>b</sub> in process-2 is the same amount with Ph in process-1

3. Measurements and results

This section discusses the electrical characteristics with test pattern types and temperature dependence that have become critical elements affecting image performance with PD and FD structures in scaled CIS technology.

3.1 Photo diode

The new diode structures to monitor silicon surface effects and STI edge effects on PD are evaluated. Characteristics such as dark leakage and activation energy are analyzed. Also, the PD image performance is characterized to confirm the surface effects.

3.1.1 Junction leakage characteristics

The reverse leakage current was measured at room temperature 25°C. The reverse dark current characteristics are shown for different diode configurations in Fig. 5(a). Good leakage characteristic is found for standard n<sup>+</sup>/pwell diodes of block type (Fig. 1). Surface diodes exhibit the highest leakage current. For a given reverse applied bias of 2.0V, the standard n<sup>+</sup>/pwell diode of block type shows around one order of magnitude lower leakage current than the buried diode even though the buried diode was formed at a lower dose than the standard n<sup>+</sup>/pwell junction. Fig. 5(b) shows the reverse dark current characteristics measured in photo diodes of different area, perimeter, and number of contacts. The block type without the STI edge-effect shows the lowest leakage compared to other structures. As shown in Fig. 5(b), current density of PD for perimeter and corner is higher than that of the area type. Diode like pixel array shows highest leakage due to the more corners when it compares with normal diode types.

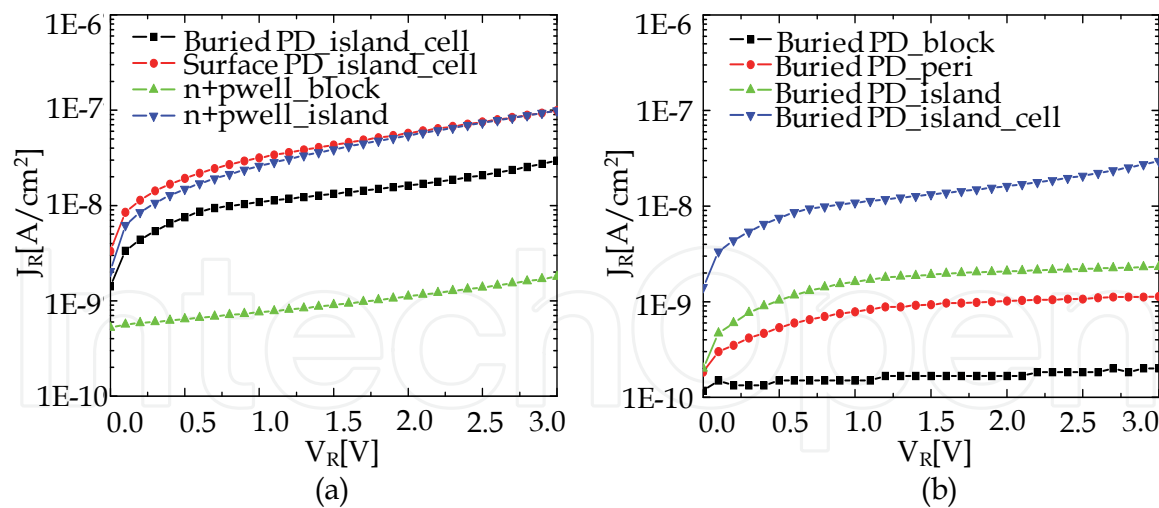


Fig. 5. Measured dark current. (a) Comparison of buried, surface, and standard diode types, (b) Comparison of buried PD of different geometry (or of different area, perimeter and number of corners).

To understand the difference between buried photodiodes and standard n+/pwell diodes, the reverse leakage current was measured as a function of temperature from 25°C to 200°C and analyzed with an Arrhenius plot by plotting  $\log I_R/T^3$  versus  $1/T$ . Arrhenius plots are shown in Fig. 6 for a reverse voltage of 2.0V. Standard n+/pwell diodes with block type show the lowest temperature dependence of reverse current. The total diode area and extracted activation energy ( $E_a$ ) at two temperature ranges are given in Table 1. Activation energies for all diodes are close to half energy gap ( $E_g/2$ ) at low temperature range, which suggests that the reverse current is dominated by generation-recombination current (H.D.Lee, 1998). For standard block-type n+/pwell diodes, at high-temperature range, where the reverse current is dominated by diffusion, the extracted activation energy is 1.13 eV, which is approximately the energy gap,  $E_g$ . However, the high-temperature activation energy of surface diode is 0.80 eV, which is close to that of a standard n+/pwell diode of island type. Also the high-temperature activation energy for a pixel-type buried diode is around 0.83 eV, lower than  $E_g$ . As shown in Fig. 1(c), pixel-type buried diodes have a large number of corners. It is therefore necessary to analyze corner effects in buried diodes.

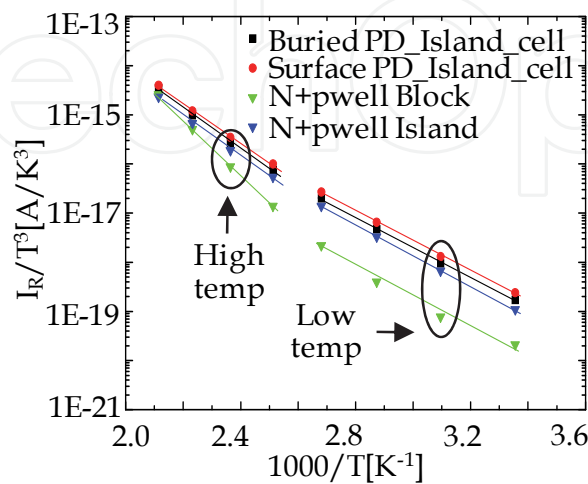


Fig. 6. Arrhenius plot of  $\log I_R/T^3$  versus  $1/T$  for island-type diodes and standard n+/pwell diodes.



Diode type	Area (μm <sup>2</sup> )	Ea [eV] @ 2.0V	
		Low temp	High temp
Buried PD Island_cell	36,000	0.61	0.83
Surface PD Island_cell	18,000	0.60	0.80
N+Pwell block	49,580	0.59	1.13
N+Pwell island	5,560	0.62	0.81

Table 1. Extracted activation energy.

To understand effects for block, perimeter, and corner with buried PD types, the reverse leakage current is also measured as a function of temperature from 25°C to 200°C and analyzed with an Arrhenius plot by plotting  $\log I_R/T^3$  versus  $1/T$ . Fig.7 shows an Arrhenius plots ( $\log I_R/T^3$  versus  $1/T$ ) for the leakage current at 2.0V reverse bias with buried PD types. As shown in Table 2,  $E_a$  at high temperature range shows a strong dependence of diode structures. That is,  $E_a$  decreases as a length of perimeter and a number of corners increase. Buried PD of island-type and buried PD island-cell types show similar activation energies. This means that the increase in leakage could be attributed to an increase in perimeter and number of corners since surface and STI components is suppressed.

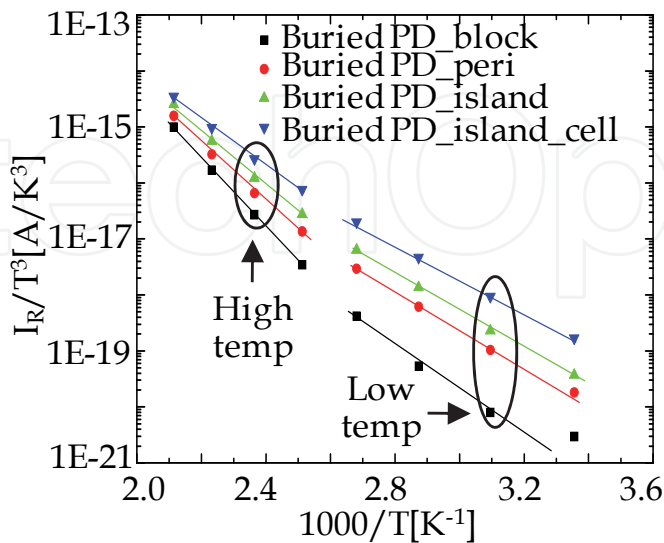


Fig. 7. Arrhenius plot ( $\log I_R/T^3$  versus  $1/T$ ) as a function of pattern types of buried PDs.



Buried PD Type	Area ( $\mu\text{m}^2$ )	Peri ( $\mu\text{m}$ )	Corner (ea)	Ea [eV] (L/H-temp)
Block	60,000	910	4	0.82 / 1.12
Peri	60,000	12,750	300	0.65 / 1.02
Island	60,000	24,000	4,800	0.66 / 0.97
Island _cell	36,000	14,400	2,880	0.61 / 0.83

Table 2. Activation energy as a function of pattern types of buried PDs

Components of area, perimeter, and corners from each test pattern are defined in Table 2. Three simultaneous equations are used to separately extract the contributions of area, perimeter, and corners to the total leakage current. Fig. 8 shows the results of three components which are extracted from leakage current data for the test pattern with block, perimeter and corner structure.

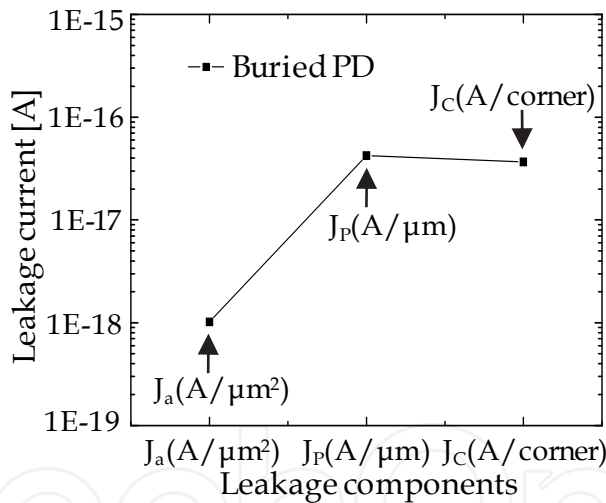


Fig. 8. Extracted leakage components for area ( $J_a$ ), perimeter ( $J_p$ ), and corner ( $J_c$ ) from measurements on buried diodes of different geometry.

The contribution for perimeter current ( $J_p$ ) and corner current ( $J_c$ ) are higher than that of the area current ( $J_a$ ).

3.1.2 Image performance

The impact of dark leakage on image quality is an important part of this experiment. Image quality is evaluated for the different diode configurations. Figure 9 shows images captured in the normal mode for the surface photodiode and the buried photodiode. The image quality of buried photodiode in Fig. 9(b) is superior to that of the surface photodiode shown in Fig. 9(a). This shows that image quality can be drastically affected by surface induced noise.

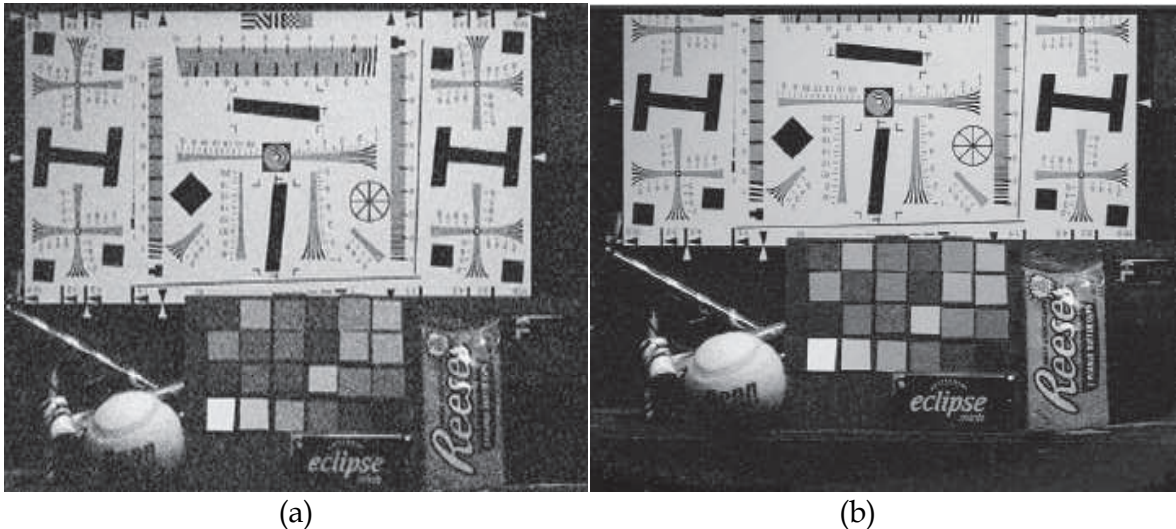


Fig. 9. (a) Image quality for surface PD. (b) Image quality for buried PD. The buried PD results in a superior image quality than the surface PD.

3.2 Floating diffusion

New diode structures to monitor the silicon surface effect and STI edge effect on floating region are evaluated. The characteristics such as dark leakage and activation energy in these diode structures are analyzed. Finally image performance is characterized to understand the mechanism of dark spots.

3.2.1 Floating diffusion leakage characteristics

To determine the leakage caused by surface effects, the activation energy is extracted from measurements of leakage current on floating diffusion of different configuration as a function of reverse bias in the temperature range 25°C to 200°C. Fig. 10 shows the Arrhenius plot used to extract activation energy under constant reverse bias  $V_r$  of 2.0V.  $E_a$  is extracted from the slopes in the high and low temperature ranges

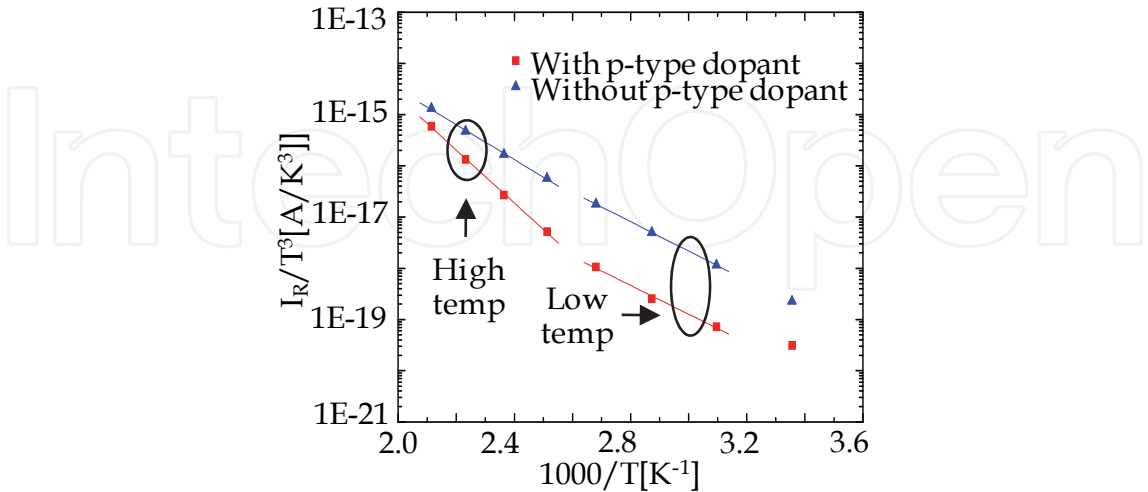


Fig. 10. Arrhenius plot ( $\log I_R/T^3$  versus  $1/T$ ) as a function of pattern types with and without boron is extracted from the measurements of large area test patterns as a function of temperatures. The diode structure without a p-layer shows higher leakage components than that with a top p-layer.

Type	Area (um <sup>2</sup> )		Peri (um)		Corner (ea)		Ea [eV]	
	A <sub>b</sub>	%	P <sub>b</sub>	%	C <sub>b</sub>	%	Low temp	High temp
With p-layer	30000	51	24000	41	4800	8.2	0.56	1.02
Without p-layer	30000	51	24000	41	4800	8.2	0.57	0.68

Table 3. Extracted activation energy from measurements on floating diffusions of identical dimensions with and without a top p-layer

Table 3 compares the activation energy extracted from measurements on floating diffusions of identical geometries with and without a top p-layer. The activation energy for both floating diffusions is close to half of the energy gap at the low temperature, which suggests that the reverse current is dominated by generation-recombination current. For the floating diffusion with top p-layer, the extracted high-temperature activation energy is about 1.02 eV, which is close to the energy gap. In this temperature range, the reverse current is dominated by diffusion current. The activation energy of the buried diffusion without top p-layer is, however, about 0.68 eV. Thus, it can be assumed that without a top p-layer the surface generation component becomes dominant, exhibiting an activation energy below  $E_g$ . The top p-layer was introduced to suppress the surface leakage component in photo diodes (I. Inoue at al., 2003). The above results demonstrate that the top p-layer can also be implemented for floating diffusions to suppress surface leakage.

3.2.2 Pinch off voltage

The gate-drain overlap region of the pass transistor must be optimized to fully transfer the integrated charge from the photodiode to the floating diffusion. To confirm the charge transportation in this overlap region, floating diffusion designed 2-different concepts by changing of doping profile Figure 11(a) shows the top view for photo diode with transfer gate Tr. and floating diffusion. Floating diffusion separates two diode regions with and without gate overlap. Diode with gate overlap is the type with overlap under sidewall spacer in floating diffusion, and diode without gate overlap is the type with STI effect. In order to evaluate both effects, it is necessary to design new JFET (Junction Field Effect Transistor) structure to monitor pinch off voltage in floating diffusion. Test patterns have been designed to see effect for the overlap under sidewall spacer and the STI edge as shown in Fig. 11(b) and Fig. 11(c). Fig.11(d) shows the concept for test pattern to measure pinch off voltage. Ph under sidewall spacer in Fig. 11(b) was applied to the lower dose than that of center diode region. Pinch off voltage between Fig. 11(b) and Fig. 11(c) will be different due to JFET structure schemes.

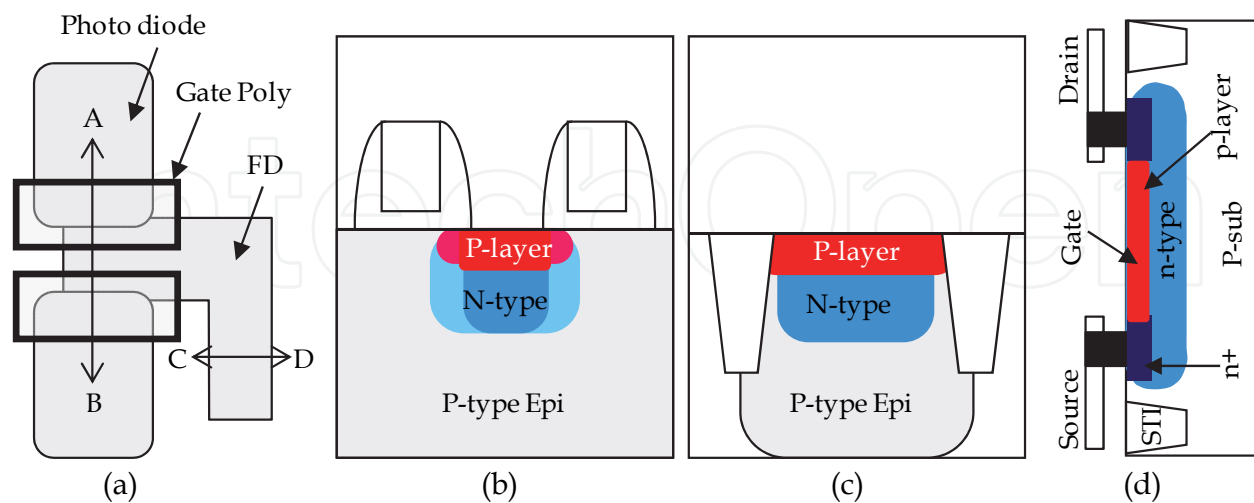


Fig. 11. The region of photo diode, pass transistor, and floating diffusion for four-transistor type active pixel. (a) Layout. (b) Tape-A : Cross sectional view for diode on line AB region (c) Type-B : Cross sectional view for diode on line CD region. (d) Concept for test pattern to measure the pinch off voltage. Source direct frontside and drain direct backside on (b) and (c). Also gate connected with p-sub.

In order to confirm the changing of the doping profile, pinch off voltage is measured in JFET (junction field effect transistor) structure as shown in Fig. 12(a). Pinch off is defined as a voltage when junction is fully depleted by applying reverse voltage at the p-layer and p-sub region. Here pinch off voltage can be defined the ratio of n- and p-type doping concentration. Doping profile with FD regions can be easily analyzed by using the JFET structure. Dependences of process and test pattern are analyzed to understand doping profile by measuring pinch off voltage. Fig. 12(b) shows the pinch off voltage for gate poly-bounded FD (type-A) and STI-bounded FD (type-B) as a function of test patterns for process-1 and -2. Gate poly-bounded FD (Type-A) shows the different pinch off voltage with process-1 and process-2. Clearly, the increase of pinch off voltage in process-2 leads to the changing of doping profile under sidewall spacer in gate poly-bounded FD (type-A), which could explain the electric field improved in the sidewall spacer overlap region. But STI-bounded FD (type-B) shows similar pinch off voltage without processes, which means pn diode controlled to the same dose. For the test pattern types, gate poly-bounded FD (type-A) with sidewall spacer overlap has higher pinch off voltage than that of STI-bounded FD (type-B). This means that pattern geometric can be effected the difference of pinch off voltage during biasing. From these results, it is observed that process-2 has lower n-type doping concentration than process-1 on gate poly-bounded FD (type-A) as expected. This is interpreted as a concept to reduce pinch off voltage by controlling doping profile under sidewall overlap region. Therefore, it is concluded that the controlling of dopant ratio to have same electric field both sidewall overlap and center region is possible to transfer integrated charges without loss in sidewall overlap.



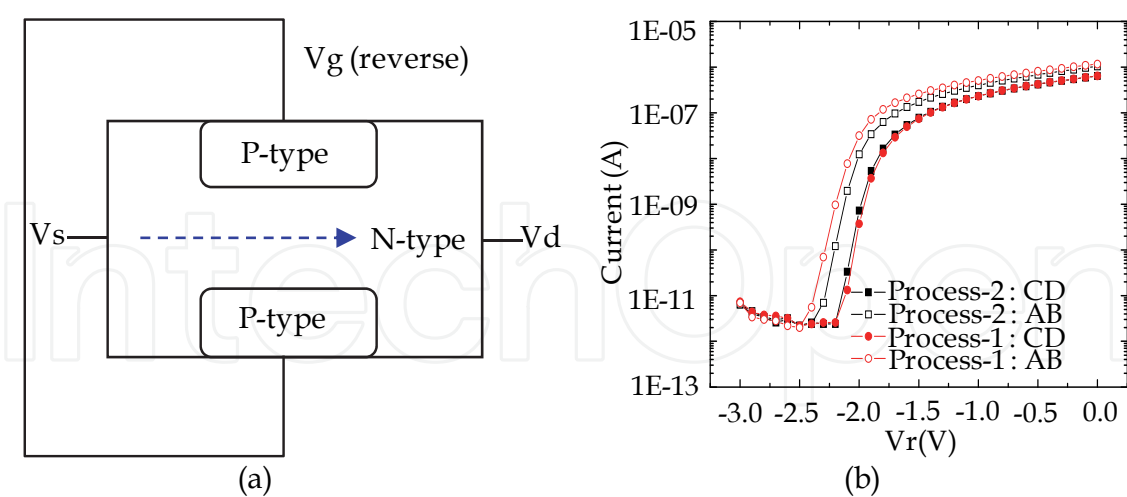


Fig. 12. (a) Concept for JFET to measure pinchoff voltage. (b) Comparison pinch off voltage with process schemes and regions for floating diffusion.

3.2.3 Image performance

From these experiments, we can suspect that a charge pocket in the floating diffusion regions can change the output voltage. To confirm this, image quality has been analyzed by using the camera system. Fig. 13a shows artifact in the pixel area randomly distributed, which means that due to the confined signal charge under sidewall spacer in process-1 described in Fig. 4, the output voltage is low in dark spot regions compared to defect free pixels. Fig. 13b shows good image, without dark spots for process-2.

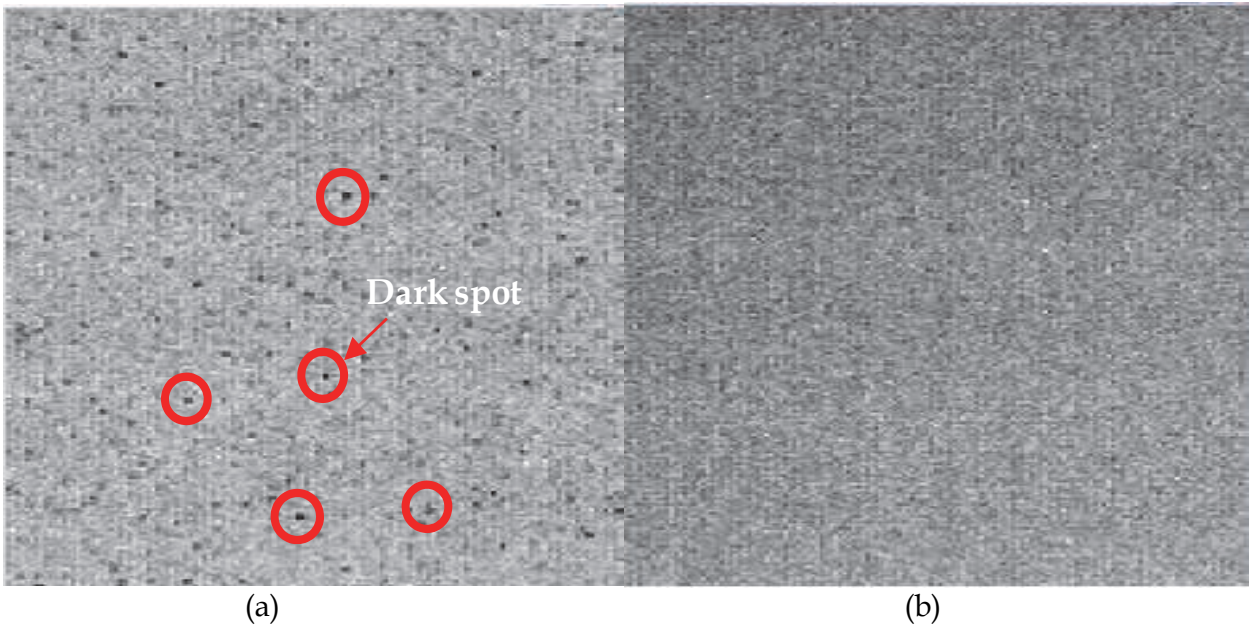


Fig. 13. Image performance analyzed by the camera system. (a) Image for process-1. Dark spot means pixel with low output voltage. (b) Image for process-2. Dark spots were removed.

4. Simulations

Simulations are done to relate electrical test results to photodiode and floating diffusion types. The electric field distribution is compared for photodiodes of different types, and charge pockets in floating diffusions are identified by comparing the potential profiles for different floating diffusion types.

4.1 Photo diode

Electric field both surface and buried PD is compared to find weak point for leakage characteristics. Also doping profile is analyzed at the surface PD to confirm the STI edge effect.

4.1.1 Electric field

Junction leakage current is the highest in the surface diode test structure, even if area is smaller than buried diode. Electric field and doping profile are compared between diode structures by simulation to see the difference. Electric field for surface diode is concentrated at the edge region of junction near the Si surface as shown in Fig. 14(a). Moreover, the junction is located near the Si surface region where the largest electric field is. Fig. 14(b) shows buried diode profile and electric field. As shown in Fig. 14(b), buried diode has two junctions, bottom and top, and has an additional junction at the plug region. Electric field is highest at the corner region of diode and plug. Also buried diode junction has a lower electric field than surface diode. From the simulation result, electric field shows pattern dependence independent of surface effects. It is suspected, from comparison of electric fields, that the higher leakage current at surface diode is induced from edge and surface.

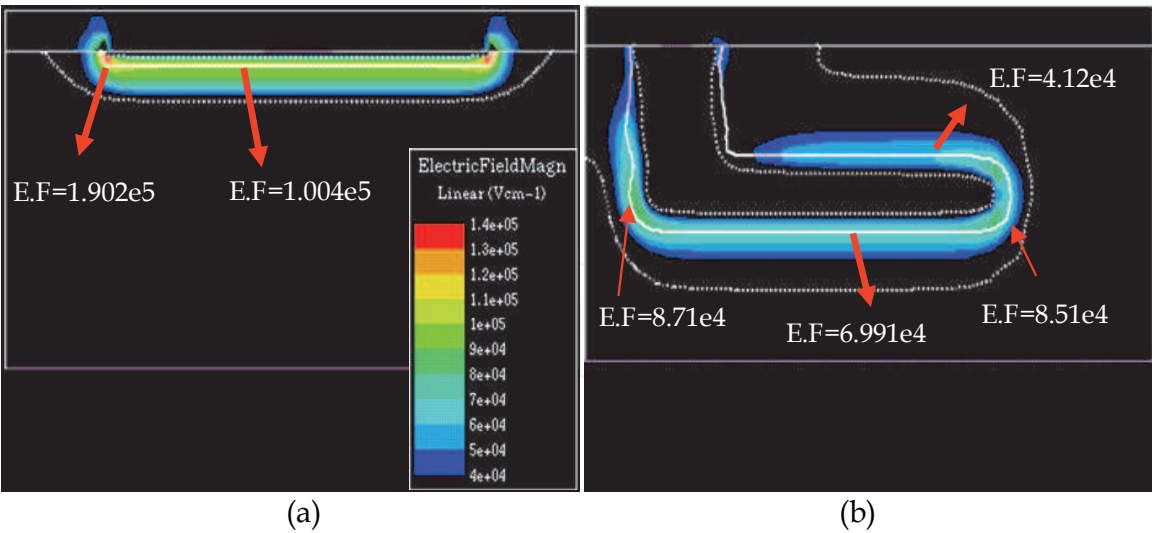


Fig. 14. (a) Electric field contour at  $V_R = 2.0$  V for blue PD. (b) Electric field contour at  $V_R = 2.0$  V for buried PD.

4.1.2 Doping profile for surface PD

In order to evaluate the defective sidewall effect of STI and the interface traps of surface on CIS, an image sensor with 3 Mega pixels is fabricated where edge of surface diode is

controlled to isolate it from the STI using boron implantation. Two-dimensional boron profile simulations with SUPREM-4 are run on an image sensor where boron is implanted to separate the photo diode from the STI edge. The results in Fig. 15 confirm that a p-region of adequate concentration and width is formed, electrically separating the photodiode from the STI boundary

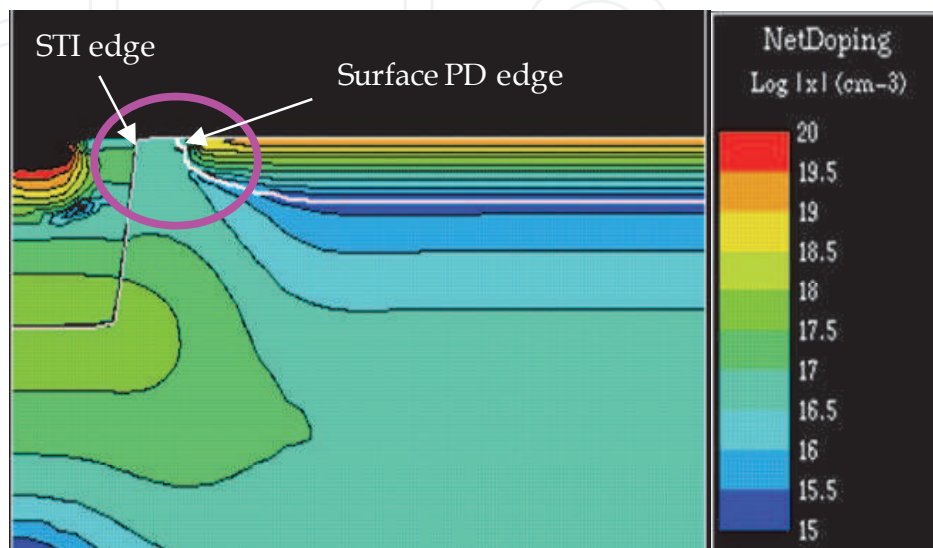


Fig. 15. 2D doping profile for surface PD at STI edge. Boron is applied between edge of STI and Surface PD.

## 4.2 Floating diffusion

Potential profile and pinch off voltage with FD types are compared to find the location for charge pocket. Also pinch off voltage is analyzed with FD types to confirm the potential profile.

### 4.2.1 Potential profile

Figures 16a and 16b show the simulated potential profiles for the gate poly-bounded and STI-bounded FD shown, respectively, in Fig. 11b as type-A, and in Fig. 11c as type-B. The structures are fabricated in process-1 (Fig. 4). Simulation is done for an applied reverse bias of 3.3V. The potential profile at gate poly-bounded FD shows the higher than that of STI-bounded FD. Higher potential under the sidewall spacer indicate charge pocket because higher voltage is needed to do pinch off. Thus, the integrated charge can't be fully transported in without loss under sidewall spacer overlap region.

Figures 17a and 17b show the simulated potential profiles for the gate poly-bounded and STI-bounded FD shown, respectively, in Fig. 11b as type-A, and in Fig. 11c as type-B. The structures are fabricated in process-2 (Fig. 4). Simulation is done for an applied reverse bias of 3.3V. The potential profile under the sidewall spacer does not create a charge pocket. Also, the potential profiles are similar for type A and type B FD, suggesting that the impurity profiles are also similar. Thus, the integrated charge can be transported in both types without loss under sidewall overlap region.



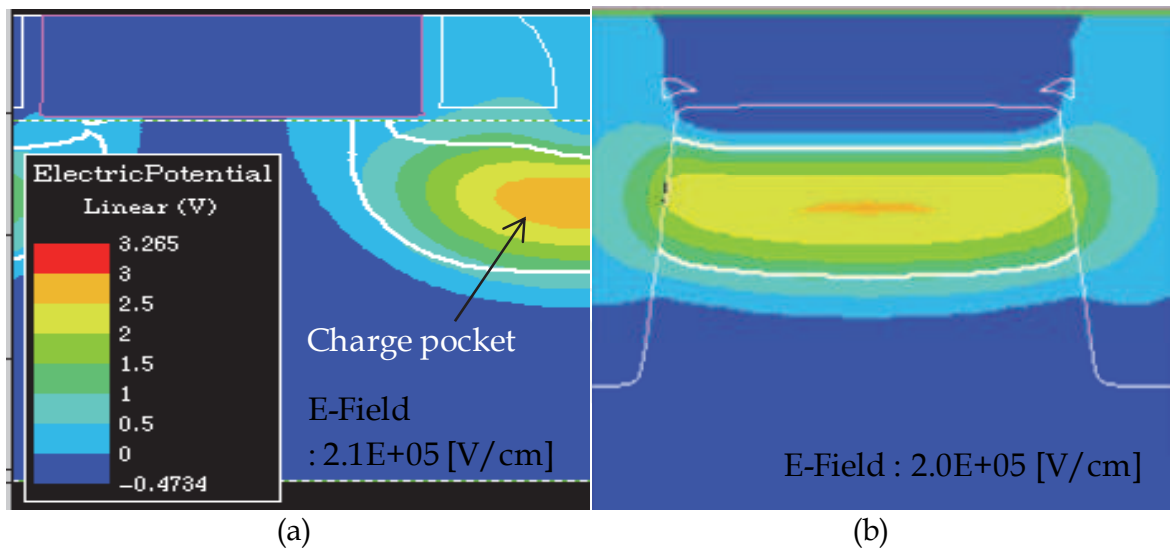


Fig. 16. Simulated potential profile for process-1. (a) Profile for gate poly-bounded FD. (b) Profile for STI-bounded FD. Gate poly-bounded FD shows the highest potential than STI-bounded FD.

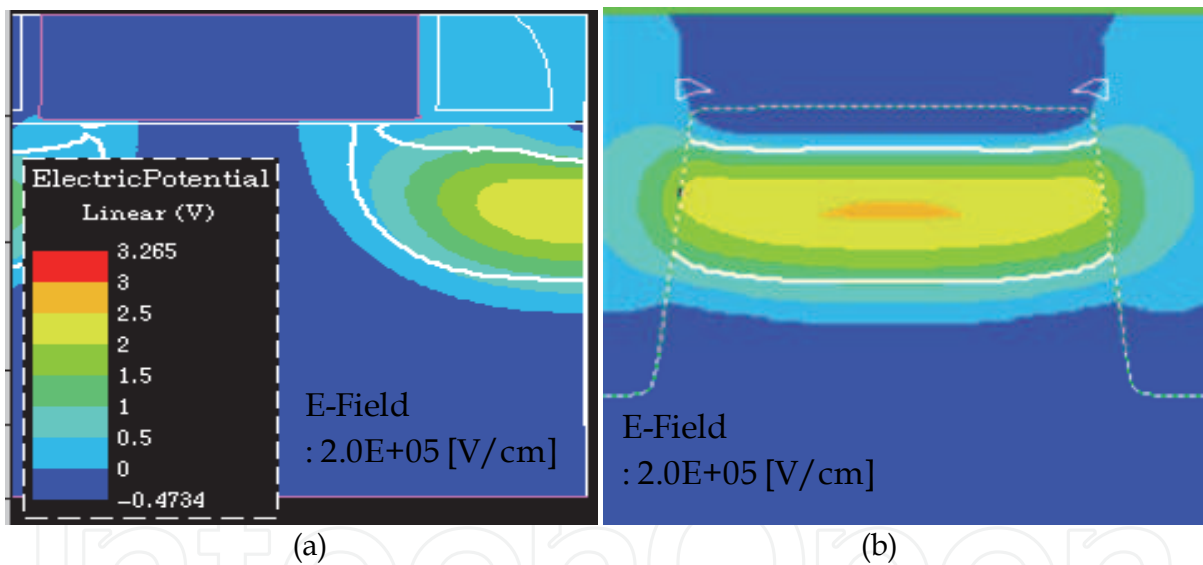


Fig. 17. Simulated potential profile for process-2. (a) Profile for gate poly-bounded FD. Here area for the highest electrical potential decreases than that of process-1. (b) Profile for STI-bounded FD. Here high potential region shows very small area and similar profile with process-1.

4.2.2 Charge pocket and delta vout

I. Inoue et al (2003) explained charge pocket model on local region under sidewall within photo diode and focused image lag in terms of potential barrier and potential pocket in the buried photo diode. Fig. 18(a) shows the current path from photo diode to floating diffusion during signal processing. In the present experiment, the FD is constructed as a buried diode covered with a p-top layer. When a potential pocket is generated in the FD in a local region under sidewall, it can become a source for output voltage variation on the APS. Fig. 18(b)

shows a schematic of the potential distribution causing a charge pocket between the photo diode and the gate of the source follower (SF). To completely transfer the signal electrons from photo diode to the gate of the SF, the potential under sidewall overlap region (AB line) has to be higher than or equal to that in FD center (CD line). Otherwise, a fraction of the signal charge would be confined in the sidewall overlap region and the integrated signal would not be completely transferred through the gate of the SF. The output signal would then be smaller than expected.

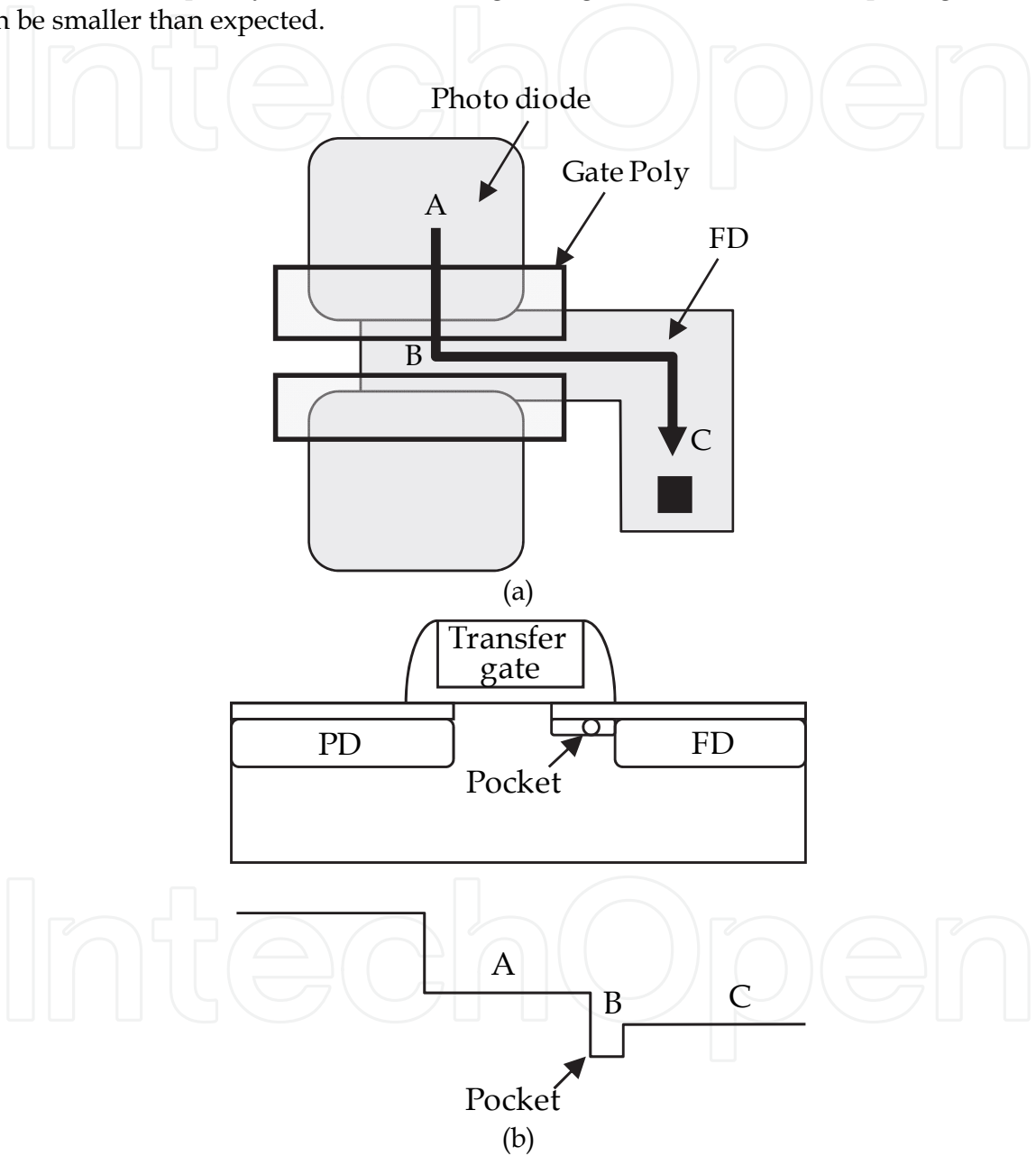


Fig. 18. (a) The potential pocket for the schematic cross section. (b) The diagram for potential distribution.

To establish the relationship between charge pocket and output voltage in the APS, transient simulation is done on the APS circuit as shown in Fig. 19a. Output voltage is calculated from simulation as a function of charge pockets in FD region, whereby the charge pockets is changed intentionally to see the difference in the output voltage. Delta Vout means the

voltage difference between  $V_{out1}$  and  $V_{out2}$  during the readout interval in the timing diagram for an APS pixel as shown in Fig. 19b.  $V_{out}$  is measured before and after charging electrons transfer from PD to FD region. In the presence of a local charge pocket on the path through FD during pixel operation, delta  $V_{out}$  would be reduced from the expected value. As shown in Fig. 19c, delta  $V_{out}$  decreases as the amount of pocket charge in FD increases. Pocket-free FD structure can be achieved by controlling the dopant ratio between n- and p-type to the same value throughout the FD regions.

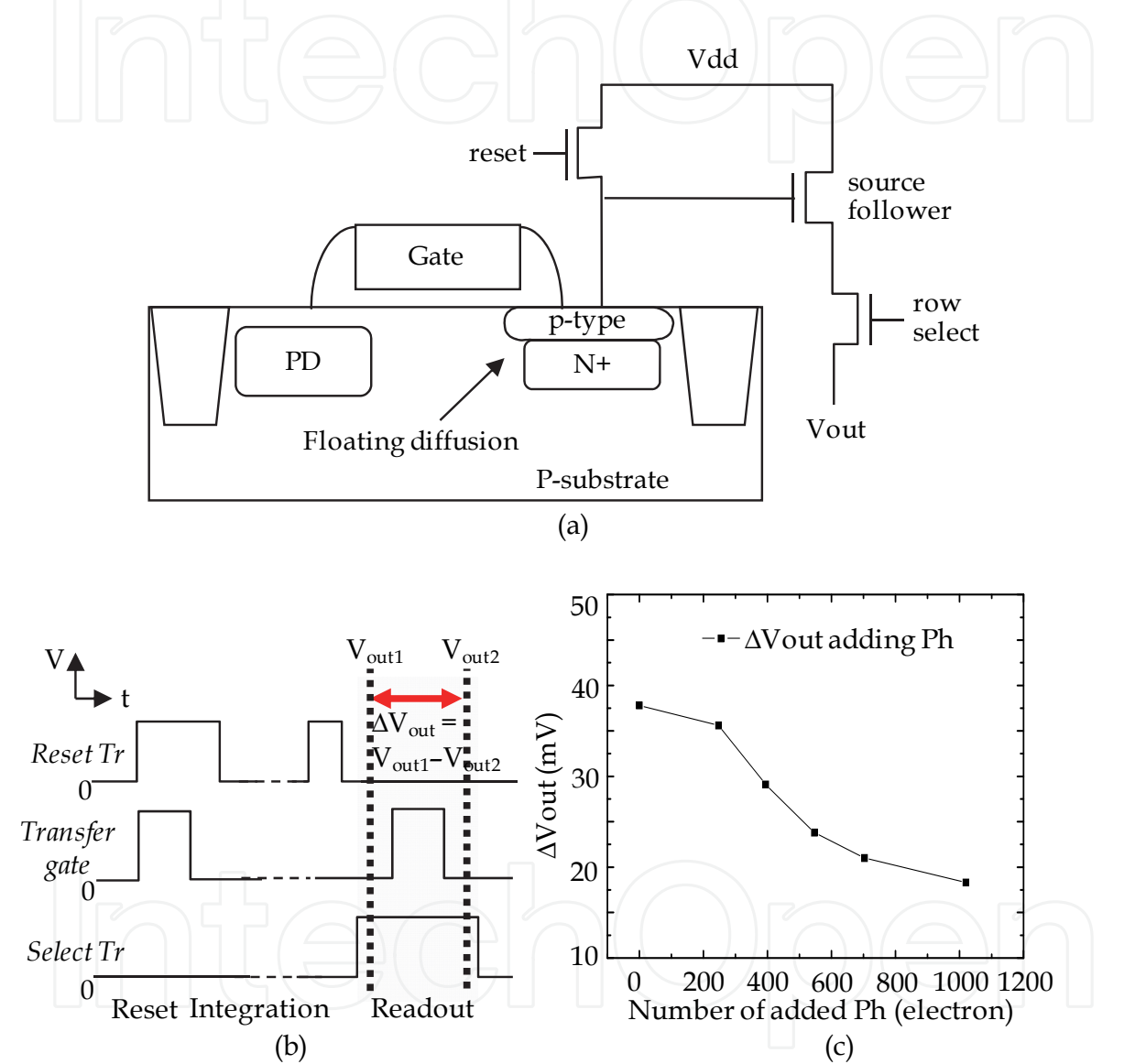


Fig. 19. (a) Circuit for four-transistor type active pixel. (b) Timing diagram for APS circuit. (c)  $\Delta V_{out}$  as a function of charge pockets.

5. Discussion

The floating diffusion is designed to transfer the integrated charge from the photo diode to the source follower without time delay in the active pixel sensor (APS). The floating diffusion is shared with the drain of the transfer transistor and reset transistor, and the gate of the source follower in APS which consists of photodiode, reset transistor, transfer gate,

source-follower transistor, and select transistor. Photodiode and floating diffusion are depleted during the reset period by turning on reset the transistor and transfer gate. During integration time, electron charge generated by an incident optical signal is integrated in the photodiode. After integration, the floating diffusion is reset at a reference voltage ( $V_{out1}$ ) by turning on the reset transistor only. The reference voltage is sampled in the readout period between turning on the select transistor and turning on the transfer gate. Charge in photodiode is transferred into floating diffusion by turning on the transfer gate and converting into voltage signal. A voltage  $V_{out2}$  is sensed on the floating diffusion after turning off the transfer gate. The optical signal is interpreted as the voltage difference between the reference voltage  $V_{out1}$  and the sensing voltage  $V_{out2}$ . Conversion gain of charge to voltage depends on the capacitance of photodiode and that of floating drain node. Dark current in the read-out process influences image parameters such as dark signal, conversion gain, noise, and signal to noise ratio (SNR). On the other hand, fill factor, i.e., the ratio of light-sensitive (photodiode) area to pixel total size, decreases as the shrink of pixel pitch shrinks. This reduces the sensitivity and SNR due to the reduction in photodiode size. To improve the fill factor, 2 or 4 shared pixel architectures, sharing both the floating diffusion and the source follower transistor are needed (J. Bogaerts, 2006 and Young Chan Kim, 2009). Therefore, a larger floating diffusion area is needed, however, at the cost of increasing the floating diffusion capacitance and hence decreasing the conversion gain. To reduce the capacitance of the floating diffusion, a buried floating diffusion should be implemented. The control of capacitance and potential profile in a buried floating diffusion is therefore very important.

## 6. Summary and conclusions

The leakage current and activation energy are compared for diodes of different configurations, using a standard n+/pwell diode as a reference. The temperature dependence of leakage yields an activation energy which depends on area, perimeter and number of corners for the buried photodiode (PD) with a top p-layer. For the first time, leakage characteristics are analyzed for a buried PD, taking into account area, perimeter, and corner effects.

In addition, leakage current and activation energy are analyzed for a buried floating diffusion (FD) with and without a top p-layer using a new diode structure. It is confirmed that the dark current can be reduced by implementing a buried floating diffusion rather than a surface FD. A charge pocket under the sidewall spacer can change the output voltage and cause a dark spot on the image. This is predicted by TSUPREM 4 simulation.

It is shown that the charge pocket can be generated by a higher doping concentration under the sidewall at the drain-side of the transfer gate, including FD region. This charge pocket is an image artifact that causes the output voltage to drop.

In summary, the mechanism for dark spots has explained by investigating pinch off voltage and potential profile on buried FD. Dark spot can be controlled by removing charge pocket under the sidewall spacer in the buried FD. The buried FD is a good candidate to control the capacitance and reduce dark leakage in future designs.

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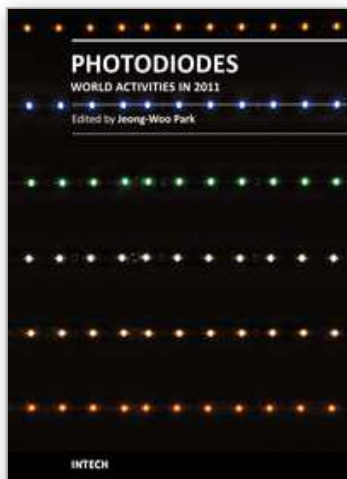
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Photodiodes or photodetectors are in one boat with our human race. Efforts of people in related fields are contained in this book. This book would be valuable to those who want to obtain knowledge and inspiration in the related area.

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