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Silicon-Based Nanowire MOSFETs: From Process and Device Physics to Simulation and Modeling

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1. Introduction

Over the past few years tremendous progress has been made on the process, application, device physics and compact modeling of nanowire MOSFETs. We would like to review the above aspects of silicon-based nanowire, focusing on its crucial compact models and the circuit performance demonstration based on our group research work and understanding on nanowire MOSFET progress.

Nanowire MOSFETs are recognized as one of the most promising candidates to extend Moore's law into nanoelectronics era. Both the top-down (Singh et al., 2008) and bottom-up (Lu & Lieber, 2006) approaches are widely studied to prepare ultra small nanowire. With bottom-up method, nanowires are generally synthesized by using metal nanoclusters as catalysts via a vapor-liquid-solid process (Lu & Lieber, 2006). After growth nanowires are transferred to silicon substrate to form FET structure. With top-down technique there are various fabrication approaches, such as hard mask trimming, etching in H_2 ambient and stress limited oxidation (Singh et al., 2008). 5-nm gate length device has been demonstrated (Liow et al., 2008). Nanowire MOSFETs prepared with both methods find application in logic circuits (Singh et al., 2008), memory (Singh et al., 2008) and sensors (Stern et al., 2008).

Due to the quantum confinement in cross section of nanowire MOSFETs, especially of nanowires with diameter smaller than 15nm, electron mobility behaves differently from its bulk counterpart. Phonon-limited electron mobility decreases with reducing the wire size (Kotlyar et al., 2004) while total electron mobility is enhanced due to volume inversion at high transverse field (Jin et al., 2007). Although whether or not ballistic transport can occur in the silicon nanowire MOSFETs with ultrasmall channel length is disputable (Ferry et al., 2008), it deserves our attention. In the ballistic transport regime, carrier scattering in the device channel is totally suppressed. The study of ballistic transport in nanowire MOSFETs provides the upper limit to their performances. Under extreme scaling of nanowire MOSFETs, the atoms in nanowire cross section are countable. It is believed that the change in bandstructure of one dimensional nanowire influences the device performances (Neophytou et al., 2008). The above mentioned phenomenon are studied and simulated with various numerical approaches and also need to be accounted for in the advanced compact models.

Compact models for silicon nanowire MOSFETs have been developed for design and simulation of nanowire-based circuits. They also provide guides for optimal device design. Natural length theory of nanowire MOSFETs sets the criterion of optimizing device parameters, e.g. the radius, oxide thickness to maintain electrical performance. Superior to Plummer's work, Taur's scaling theory (Yu et al., 2008) takes into account the lateral distribution of gate oxide field and allows consideration of relatively thicker high-k dielectric. Core models of undoped nanowire MOSFETs where quantum effect is not significant are well established (Iñíguez et al., 2005; Bian et al., 2007; He J. et al., 2007). By rigorously solving Poisson's equation in polar coordinate, the electrostatic potential distribution in cross section of nanowire is obtained. Combined with Pao-Sah's drift-diffusion formula, current characteristics of long channel ideal nanowire MOSFETs are derived. Following Ward's channel charge partition scheme, terminal capacitance models are obtained. Various forms of this core model exist, such as charge-based (Iñíguez et al., 2005), potential-based (Bian et al., 2007) and carrier-based (He J. et al., 2007) model. Each has its own advantages. Potential-based model is further used to explain the dynamic depletion effect in nanowire (Zhang L. et al., 2009a), while charge-based model has been extended to cover the doped nanowire MOSFETs (Yang et al., 2008). In order to accurately reproduce the electric performances of nanowire MOSFETs, advanced effect models are integrated into the core model frame, e.g. short channel effects , quantum confinement effects , velocity saturation effect (Zhang L. et al., 2009b), etc. A preliminary compact model for silicon nanowire MOSFETs is presented in (Yang et al., 2008) where several advanced effect models are included as optional modules. Another capacitance based analytic model of ballistic silicon nanowire is also given in (Wang, 2005).

Working out an analytic model covering ballistic and diffusive transport and also realizing transition between both (Michetti et al.,2009) is another challenging task. With the above mentioned preliminary compact model for silicon nanowire MOSFET implemented into circuit simulations by Verilog-A, several representative logic circuits are simulated (Yang et al., 2008). Current status process, device physics, simulation and modeling of silicon-based namowire MOSFETs is reviewed, and the circuit performance is also analyzed. Moreover, the future possible trend of nanowire MOSET is finally outlined in this chapter.

2. Nanowire fabrication process

Silicon nanowire (SiNW) transistors have shown promising potential to revolutionize the applications of electronic, optical, chemical and biological devices (Black, 2005 ; Barrelet et al.,2004; Ramanathan et al., 2005; Hood et al., 2004). The conventional approach for the fabrication of silicon nanowires is a bottom-up approach from one of many pathways ranging from chemistry, laser-assisted or e-beam directed patterning (Cui et al., 2001a) in a controllable fashion down to sub 10nm diameter in width. One of the many established methods is by nanocluster assisted vapor-liquid-solid (VLS) growth mechanism in which metal nanoclusters mediate the nanowire growth. A more subtle approach of the bottom-up method for the patterning of silicon nanowires is by laser-assisted catalytic growth (Zhang, Y. F. et al., 1998). A bottom-up formation approach is advantageous for creating small silicon nanowires. However, the orientation growth of the wires is a major issue and the repeatability for device use is highly challenging. The formation of silicon nanowires from the top-patterning takes a completely different philosophy from the chemical or laser-assisted method. It relies on the grid formation on standard mask and transformation onto

the silicon wafer surface. Due to the limitations of photo-lithography, mostly top-down controlled patterning methods have been developed by successive stress-limited oxidation. One possible method is by thermal oxidation of silicon pre-cursor under refinement (Liu et al., 1993). The starting Si columns are first patterned by Reactive-Ion-Based techniques to refine very small dimensions of silicon pattern, allowing for a series of thermal oxidation with controlled temperature and time. Due to the accumulated stress, the oxidation rate becomes extremely slow and results in the formation of silicon nanowires. Silicon pillars down to 2nm in diameter have been successfully fabricated by stress-limited oxidation (Liu et al., 1994; Kedzierski et al., 1997).

2.1 Single nanowire fabrication
2.1.1 Top-down method
The formation of Silicon Nanowire from the top-patterning takes a completely different philosophy than the chemical or laser assisted method (Kedzierski et al., 1997). It relies on the grid formation on standard mask and transformation onto the silicon wafer surface. Unfortunately, the common challenge of photo-lithography is the definition limit due to the physical obstruction of visible light. Numerous methods are proposed to stretch the top-down patterning limit since silicon nanowires are widely studied. One possible method is by thermal oxidation of silicon pre-cursor under refinement as shown in Figure 1. A small silicon is firstly patterned by Reactive-Ion-Based techniques to refine very small dimensions of silicon pattern allowing for a series of thermal oxidation with controlled temperature and exposure time. Due to the surrounding stress developed at the silicon outer wall, the inside of silicon gradually decreases and results in trends of silicon nanowires.
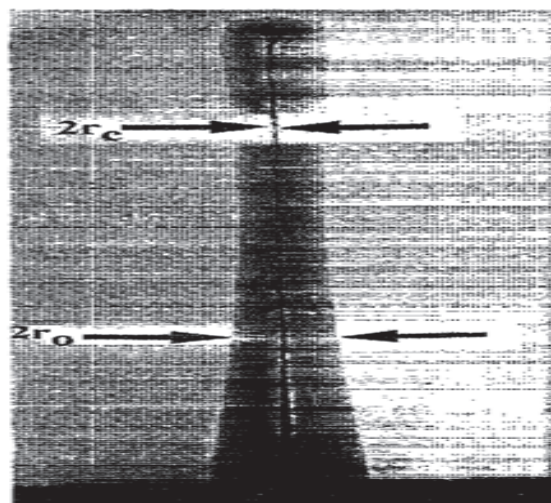

Fig. 1. Stress limited oxidation Silicon Nanowire (From Liu H. et al. Appl. Phys. Lett., Vol. 64, No.11, (Mar 1994))

This method is also applied onto Silicon-On-Insulator based materials (Black, 2005) to promote better stress limiting effect such that more rounded silicon cores are formed as shown in Figure 2. The extra buried oxide layer under the device silicon acts as a relieve site for oxidation flow promotion. In other words, the oxidation rate around the silicon is isotropic and hence the stress is evenly distributed along the surface. As a result, better control rates on the silicon cross-section can be achieved.
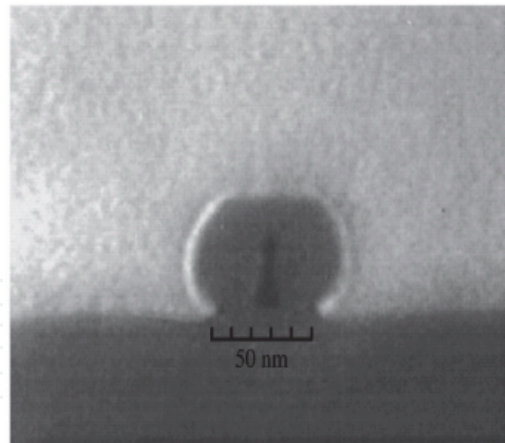
Fig. 2. Silicon-On-Insulator based Silicon Nanowire (From Kedzierski J., J. Vac. Sci. Technol. B, Vol. 15, No. 6, (July 1997))

2.1.2 Bottom-up method

The fabrication of silcon nanowire comes from many pathways ranging from chemistry, laser assisted or e-beam directed patterning (Cui et al., 2001a) in a controllable fashion down to sub 10nm diameter in width. One out of the many established method is by nanocluster assisted vapor-liquid-solid (VLS) growth mechanism in which metal nanoclusters mediate the Nanowire growth. The size of the metal catalysts determines the diameter of the Nos implying that with a narrow size distribution could be obtained by exploiting well-defined catalysts. High single-crystallinity configuration is reached by the chemical controlled method; however, the drawback is an uncontrolled growth orientation which deters its motivation for transistor application use.
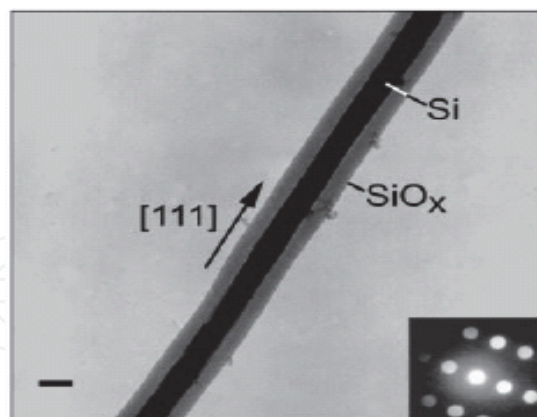

Fig. 3. Silicon Nanowire prepared by laser ablation method (From Alfredo M. Morales, *Science* 279, 208 (1998))

A more subtle approach of the bottom-up method as shown in Figure 3 for Silicon Nanowire patterning is by laser assisted catalytic growth (Zhang, Y. F. et al., 1998). The energy and pulsed controlled laser beam with sub-UV wavelength range is capable of cutting tiny target Silicon element site followed by a high temperature vapor condensation with the addition of metallic nano chemical cluster. The ablated silicon-metallic served as a growing site for silicon reaction growth in the liquid state under extremely high temperature. After cooling,

the grown silicon solidities and results in strands of nanowires with better crystallinity and straightness. The above mentioned bottom-up formation approach is advantageous in creating small dimensions silicon nanowires (Figure 4). However, the orientation growth of the wires is a major issue and the repeatability for device use is highly challenging.
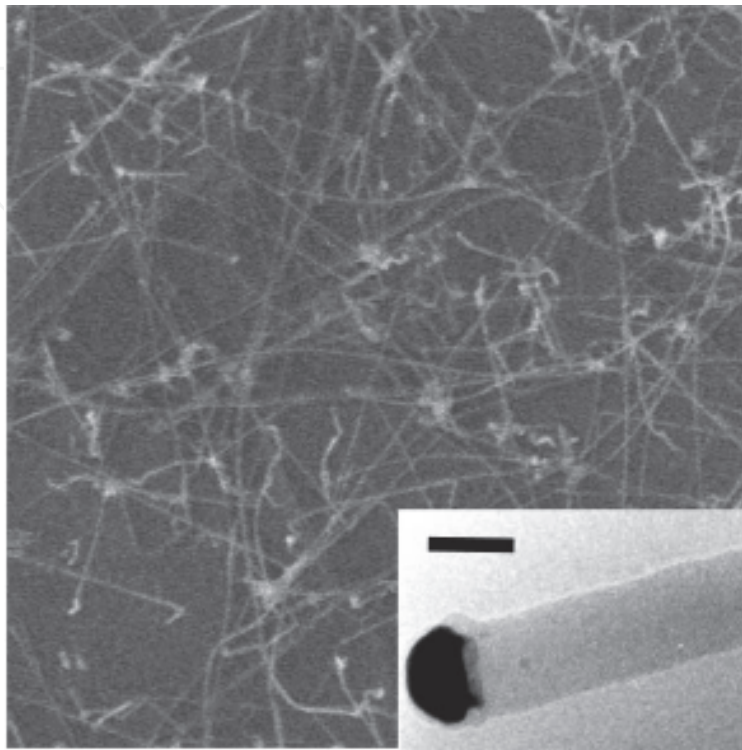

Fig. 4. Diameter controlled synthesis by single metallic crystal. The scale bar is 20 nm. (From Cui Y., Applied Physics Letters Volume 78, Number 15)

2.2 Multiple nanowire

The nanowires discussed above are single wires with localized shrinkage at a direct point of location (Black, 2005). As mentioned above, the excitement of multiple wires is the capability to increase the current throughput due to the carrier transport limitation for each single wire. The fabrication process for multiple wires is much complicated due to the replicating challenge for multiple patterns, or the ability to define grids in the multiple directions. A horizontal pitched silicon nanowire is shown by applying self-alignment of diblock copolymer films on an already lithographically defined mask (Figure 5). The interaction between the photo resist and co-reacting polymer aids to sub-divide the nano patterns into more and refined line structures (Bera et al., 2008). The promotion of multiple wires in the vertically direction is also proposed but with much greater challenge. One difficulty of vertical wires is the ability to control the vertical pitches. This problem can be resolved by utilizing the crystallinity orientation of silicon lattice structure along different direction. The existence of KOH etch is known for highly crystallinity oriented disruption. By splitting the crystal orientation, different etch planes are exposed and therefore oxidation of the structure will separate the silicon into different regions as shown in Figure 6. It is seen the above method has limitation to double silicon nanowires. To extend the number of small wires, another approach is proposed by utilizing the Si/SiGe technology (Namatsu et al., 1997). A

stacked heterogeneous layer of mega structure is used to generate different silicon sites. The pattern precursor is then subjected to conventional oxidation process which than leaving multiple wires behind. This is currently the most reliable repeating process with virtually no limit on the number of stacked cores to be formed (Figure 7).
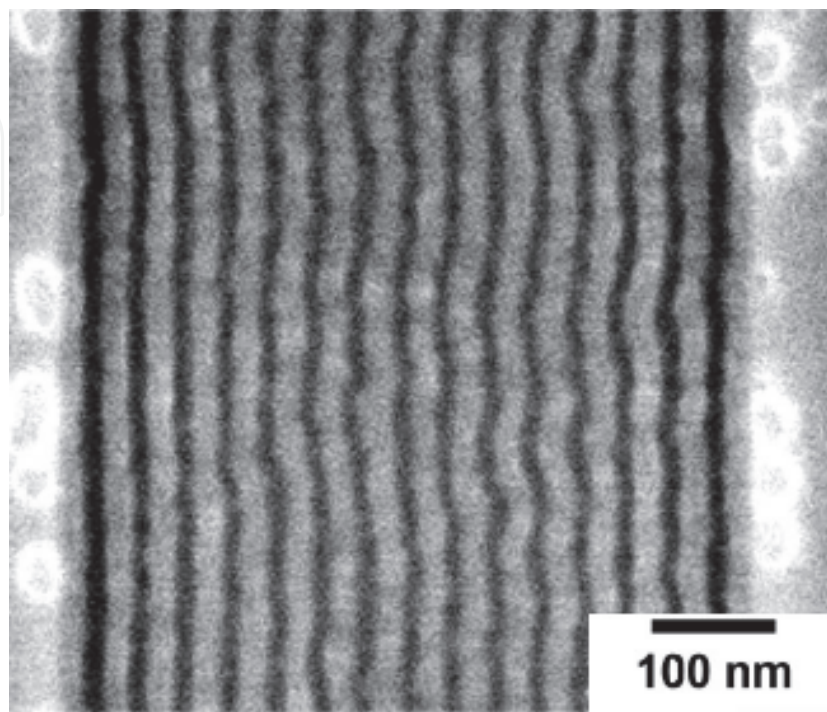

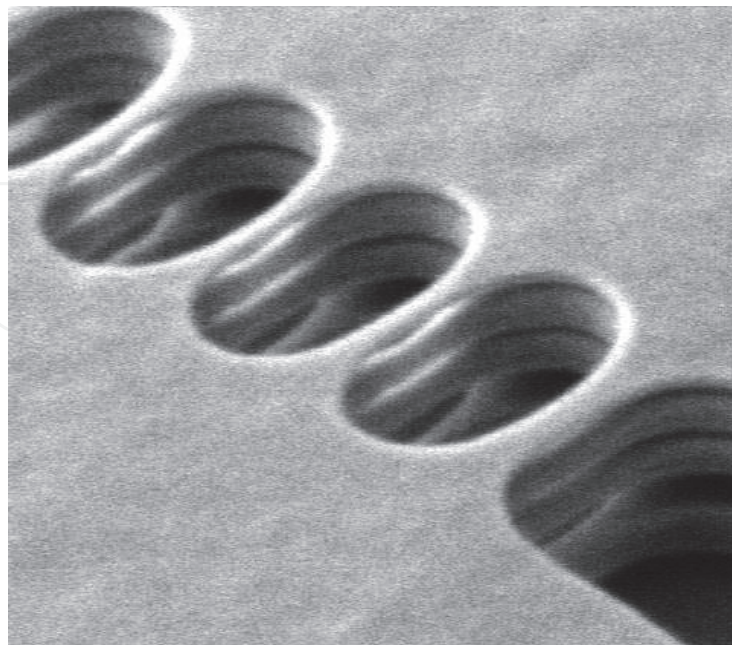Fig. 5. Horizontal Multiple Silicon Nanowires. (From, C. T. Black, Applied Physics Letters 87, 163116 2005)

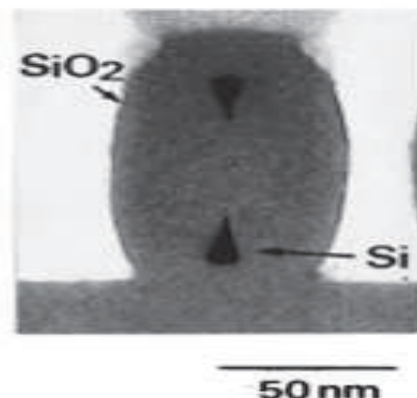Fig. 6. SiGe based vertical multiple Silicon Nanowire (From L. K. Bera, IEEE IEDM '06, pp. 551-554)

Fig. 7. Twin KOH based Multiple Silicon Nanowire (From Hideo Namatsu, J. Vac. Sci. Technol. B, Vol.15, No.5)

2.3 Vertically stacked nanowire process

The advantage of multiple wires is the capability to increase the current throughput with an increasing number of conducting channels. However, horizontal stacking increases the integration density and vertical pillars are hard to integrate into a traditional planar technology. A vertically stacked silicon nanowire concept has been introduced resulting in an increase in the drive current without impacting the density of integration (Fang et al., 2007).

Fabricating horizontal SiNWs using self-limiting oxidation has also been proposed (Liu et al., 2007). Silicon lines are defined on silicon-on-insulator with an electron beam lithography followed by metal liftoff process and silicon plasma etching. Low temperature oxidation is then used to shrink these lines to a sub-10 nm diameter. But the resulting geometry and shape of the nanowire are difficult to control and need sophisticated equipments and process control. A more controllable method has been demonstrated to fabricate horizontal nanowires using a multi-material system such as Si/SiGe/Ge/SiGe stacks (Bera et al., 2006; Dupre et al., 2008) but the process requires careful handling of the hetero-material interface. Among the methods to form vertical nanowires, the Bosch process plus stress-limited oxidation is the simplest in terms of the equipment needed.

2.3.1 Bosch process plus stress-limited oxidation approach and advantage

Figure 8 shows the key steps of the process to form vertically stacked nanowires. First, the Bosch Process is repeated by ICP to form a scallop pattern along the sidewall of a tall silicon ridge. Then stress-limited oxidation trims down the narrow region at the silicon ridge to form stacked nanowires (Ng.et al.,2007, 2009).

The active area is defined by a high resolution photo lithography on an oxide hardmask. The Bosch cycle technique (Chang et al., 2005) was employed to create a periodic sidewall profile by balancing the ICP etch and passivation step in each cycle. After the first etching phase, the patterned bulk-Si is first masked by a C_4F_8-based resistant polymer before the subsequent SF_6 plasma etches in the unprotected region. ICP etch is proceeded for 7 seconds under C_4F_8 (15sccm), SF_6 (45sccm), O_2 (5sccm) at 600W. The passivation cycle continues for 5.2 seconds under C_4F_8 (75sccm) at 200W. The scallop pattern that results from this process is shown in Figure 9(a). The widths of the ridges and troughs are controlled by the initial lithography and the etch time versus the passivation time in each cycle. After forming the
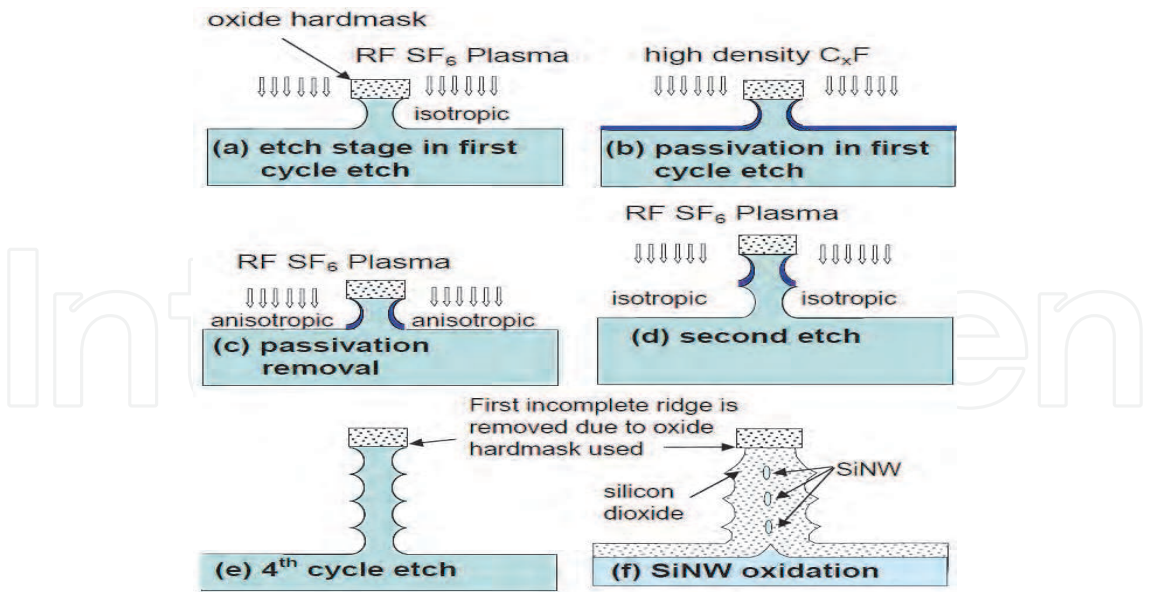
Fig. 8. Nanowire formation by Bosch etching and stress-limited oxidation (From R. M. Y. Ng, IEEE Elect. Dev. Lett , Vol. 30, No. 5, 2009)

scallop pattern, dry oxidation at 1000oC is performed to consume the narrow region of the silicon ridge and isolate the nanowires. The evolution of the process with time is shown in the SEM images in Figure 9(b)-(d). The oxidation is self-limiting due to the stress resulting from the volume expansion during the formation of the silicon dioxide as shown in Figure 9. It is noted that for an initial mask width of 100nm, the entire silicon ridge is consumed. For an initial mask width of 200nm and 300nm, the oxidation is self-limiting as shown in Figure 10. A reduction of oxide thickness (negative oxidation rate) is observed after prolonged oxidation due to the oxide densification effect. It should be noted that the oxide hardmask facilitates the removal of the incomplete ridge at the top of the silicon nanowire stack as illustrated in Figure 8(e) and (f) so that the dimensions of the stacked nanowires become more uniform.
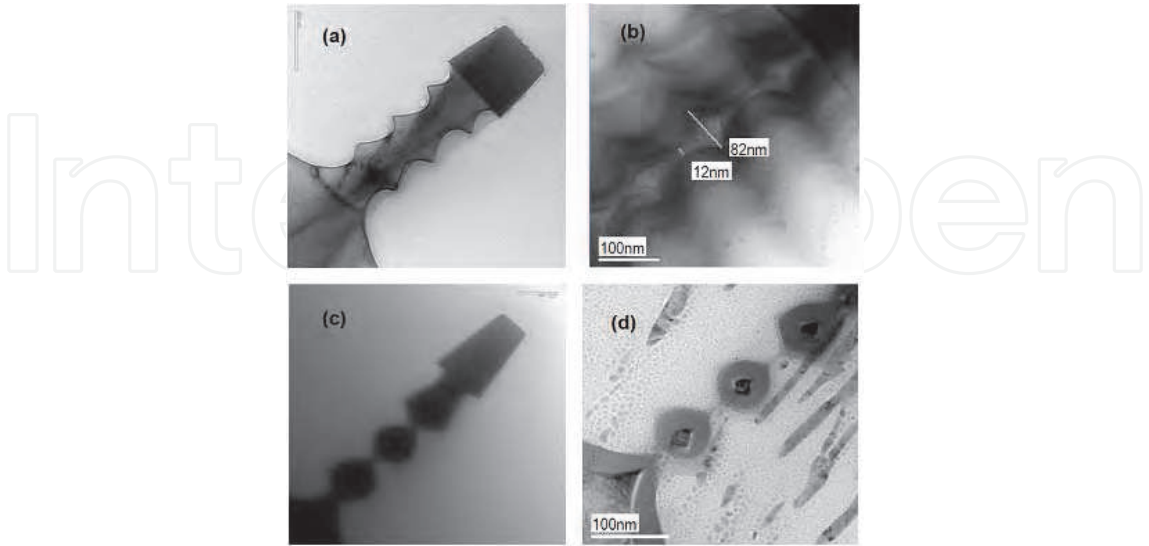

Fig. 9. TEM images showing the time evolution of the nanowire geometry (a) right after the Bosch etching and after (b) 30mins (c) 60mins and (d) 120mins of oxidation (From R. M. Y. Ng, IEEE Elect. Dev. Lett , Vol. 30, No. 5)
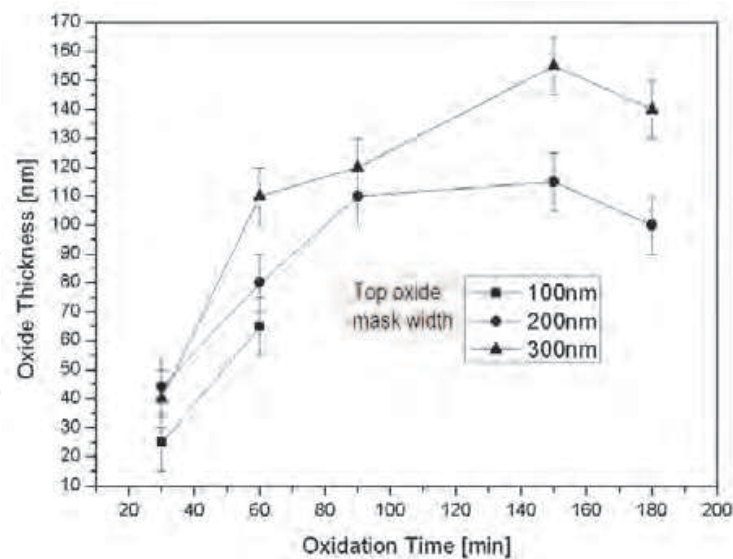
Fig. 10. Sidewall oxidation rate at 1000oC in oxygen ambient with different top oxide hardmask widths (From R. M. Y. Ng, IEEE Elect. Dev. Lett , Vol. 30, No. 5)

By controlling the initial width of the wide and narrow regions of the silicon ridges the vertical separation between the wider regions, elliptical and even triangular nanowires can be formed. To ensure the nanowires can be separated, the width of the narrow regions of the ridge should be less than 200nm. Due to the curvature effect, oxidation is in general slower at the narrow regions. As a result, wide regions should be at least 100nm wider than the narrow regions to form the residual nanowires after prolonged oxidation. Despite the different crystal orientation, the oxidation rate after the nanowire separation is quite uniform in all directions regardless of initial shape and dimension. This observation is due to the nature of the stress-limited process rather than the reaction rate limited process.

Therefore, vertically stacked SiNWs have been successfully fabricated using Inductive Coupled Plasma etching followed by stress-limited oxidation through a careful design process and optimization. Since the SiNW is trimmed from the Si wafers, the single crystal property of the SiNW is maintained when observed from the atomic plane, showing the existence of the crystallographic alignment. The shape and size of the nanowires can be controlled by varying the process conditions.

3. Silicon-based nanowire MOSFETs modeling and simulation

3.1 Core model for undoped nanowire

As a result of the interest in implementing SRG MOSFET to extend the scaling of CMOS technology, physics-based models are important in electrical circuit simulators to predict the performance of circuits when these devices are in use. It is well known that a complete surrounding-gate MOSFET model should not only be used to predict the SRG MOSFET current-voltage characteristics, but also be used in the calculation of terminal charges and various capacitances in the large signal and small signal simulations.

Here, an analytic carrier-based terminal charge and capacitance-voltage compact model for the long channel undoped surrounding-gate MOSFETs is also developed directly from both the current continuity principle and channel charge partition scheme based on our previous theoretical results (He, J. et al.,2004, 2006a). The analytic model is based on the exact device

physics and covers all regions of SRG MOSFET operation, from the sub-threshold to the strong inversion and from the linear to the saturation. Terminal charges and trans-capacitances of SRG MOSFETs are calculated with the newly developed model and further compared with the three-dimensional (3-D) numerical simulation.

The coordinate system and energy band used in this work is shown in Figure 11 with r representing the radial distance from the centre of the silicon film and $r = R$ giving the silicon film radius. It is also assumed that the quasi-Fermi level is constant in the radial direction, so that the current flows only along the channel (y direction). The energy levels are referenced to the electron quasi-Fermi level of the source end since there is no body contact in the undoped SRG MOSFETs.

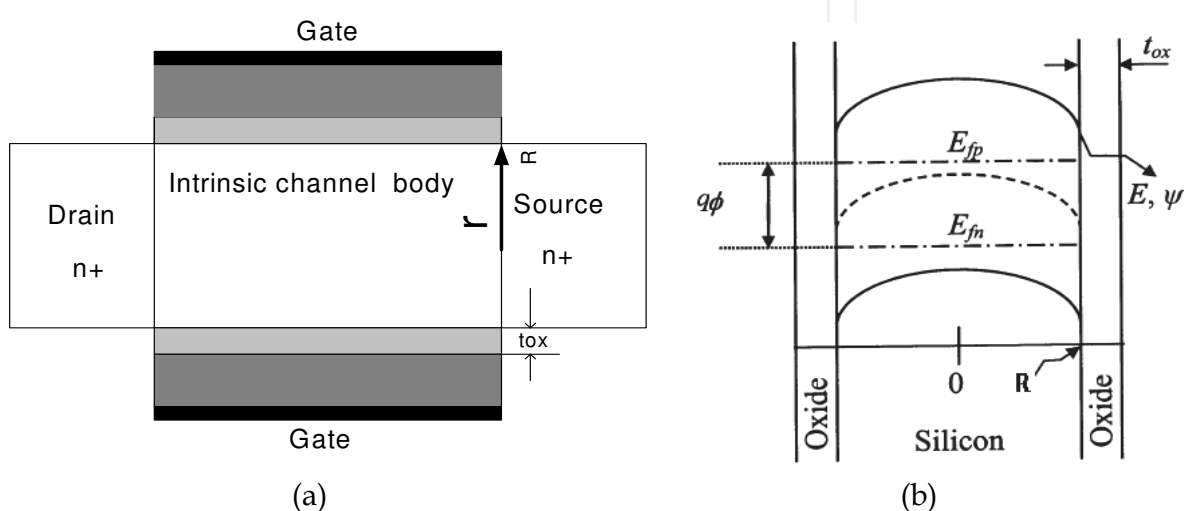(a)   (b)

Fig. 11. The coordinate system(a) and energy band(b) used in this work. (From He J. IEEE TED, Vol. 54, No. 6, June 2007)

Following the basic device physics of SRG MOSFET (Jiménez et al., 2004; Iñíguez et al., 2005; Moldovan et al., 2007; He, J. et al.,2004, 2006a) under the Gradual-Channel–Approximation (GCA), the solution to the1-D Poisson–Boltzmann equation is valid in terms of the carrier concentration:

$$V_{gs} - \Delta\phi_i - V_{ch} = \frac{1}{\beta}\ln\left(\frac{n_0}{n_i}\right) - \frac{2}{\beta}\ln\left[1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right] + \frac{R^2\varepsilon_{si}\ln\left[1 + \frac{t_{ox}}{R}\right]}{2\beta L_i^2\varepsilon_{ox}}\frac{\frac{n_0}{n_i}}{\left[1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]} \tag{1}$$

where all symbols have their common physics meanings:

$1/\beta = kT/q$ is the thermal voltage.

n_i is the silicon intrinsic carrier concentration ($1.14\times10^{10}cm^{-3}$ at room temperature).

n_0 is the induced carrier concentration at the reference coordinate point (at the centre of the silicon film in this study).

$\Delta\phi_i$ is the work function difference between the gate and the channel silicon body.

V_{ch} is the quasi-Fermi-potential with $V_{ch} = 0$ at the source end and $V_{ch} = V_{ds}$ at the drain end.

L_i^{-2} =q²ni/kTε$_{si}$ is the reciprocal of the square of the intrinsic silicon Debye length.

Based on Poisson's equation solution, the total inversion charge density is expressed as:

$$Q_i = \frac{R\varepsilon_{si}}{2\beta L_i^2} \frac{\dfrac{n_0}{n_i}}{\left[1 - \dfrac{R^2}{8L_i^2}\dfrac{n_0}{n_i}\right]} \qquad (2)$$

Following Pao-Sah current formulation (Pao & Sah, 1966), the drain current can be written as

$$I_{DS} = \mu_0 \frac{W}{L} \int_0^{V_{DS}} Q_i(V)dV = \mu_0 \frac{W}{L} \int_{n_{0S}}^{n_{0D}} Q_i(n_0)\frac{dV}{dn_0}dn_0 \qquad (3)$$

where n_{0s} and n_{0d} are the solutions of Eq.(1) corresponding to $V_{ch} = V_s = 0$ and $V_{ch} = V_{ds}$, respectively. μ_0 is the effective mobility, assumed constant here. W and L are the SRG MOSFET channel width and length, respectively.

Substituting n_0 with dV_{ch}/dy and the inversion charge expression in Eq. (2) into (3) and performing analytical integration, the carrier-based drain current is obtained:

$$I_{ds} = \mu_0 \frac{2\pi\varepsilon_{si}}{L}\left(\frac{2}{\beta}\right)^2 F[n_0]\bigg|_{n_{0d}}^{n_{0s}} \qquad (4)$$

where

$$F[n_0] = \left[\ln\left[1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right] + 2\left(1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right)^{-1} + \theta\left(\left(1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right)^{-2} - 2\left(1 - \frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right)^{-1}\right)\right] \qquad (5)$$

with $\theta = \dfrac{2\varepsilon_{si}}{\varepsilon_{ox}}\ln\left[1 + \dfrac{t_{ox}}{R}\right]$

In order to simplify the derivation, we define a normalized carrier concentration $\rho = 1 - \dfrac{R^2}{8L_i^2}\dfrac{n_0}{n_i}$. As a result, (5) is simplified to $F(\rho) = \ln\rho + 2\rho^{-1} + \theta(\rho^{-2} - 2\rho^{-1})$.

Based on a similar procedure, the analytic source and drain terminal charges are obtained and the final results are given as follows

$$Q_s = -\frac{8\varepsilon_{si}\pi L}{\beta}\frac{F(\rho_d)G(\rho)\bigg|_{\rho_d}^{\rho_s} + M(\rho)\bigg|_{\rho_d}^{\rho_s}}{\left[F(\rho)\bigg|_{\rho_d}^{\rho_s}\right]^2} \qquad (6a)$$

$$Q_d = -\frac{8\varepsilon_{si}\pi L}{\beta}\frac{F(\rho_s)G(\rho)\bigg|_{\rho_s}^{\rho_d} + M(\rho)\bigg|_{\rho_s}^{\rho_d}}{\left[F(\rho)\bigg|_{\rho_s}^{\rho_d}\right]^2} \qquad (6b)$$

with

$$M(\rho) = \left(\frac{4}{3}\rho^{-3} - \frac{5}{2}\rho^{-2} - \rho^{-1} + \frac{1-3\rho}{\rho^2}\ln\rho - \frac{1}{2}(\ln\rho)^2\right)$$
$$+ \theta\left(\frac{3}{2}\rho^{-4} - \frac{43}{9}\rho^{-3} + \frac{9}{2}\rho^{-2} + \frac{2-6\rho+6\rho^2}{3\rho^3}\ln\rho\right) \qquad (6c)$$
$$+ 2\theta^2\left(\frac{1}{5}\rho^{-5} - \rho^{-4} + \frac{5}{3}\rho^{-3} - \rho^{-2}\right)$$

and

$$G(\rho) = \rho^{-2} - 3\rho^{-1} - \ln\rho + 2\theta\left(\frac{1}{3}\rho^{-3} - \rho^{-2} + \rho^{-1}\right) \qquad (6d)$$

From Eqs.6 (a-d), all three terminal charges of SRG MOSFETs can be analytically calculated from the normalized electron concentration ρ_s and ρ_d from the solutions of (1) corresponding to $V_{ch} = 0$ and $V_{ch} = V_{ds}$, respectively.

The SRG MOSFET is essentially a three terminal device, a nine-capacitance matrix is written as

$$C_{ij} = \begin{cases} \dfrac{\partial Q_i}{\partial V_j} & i = j \\ -\dfrac{\partial Q_i}{\partial V_j} & i \neq j \end{cases} = \begin{bmatrix} C_{ss} & C_{sd} & C_{sg} \\ C_{ds} & C_{dd} & C_{dg} \\ C_{gs} & C_{gd} & C_{gg} \end{bmatrix} \qquad (7)$$

With the analytical expressions of the three terminal charges formulated, all capacitances are derived as a function of the carrier concentration in the silicon centre n_{0s} and n_{0d} by means of the series law of calculus. The analytical expressions of all nine trans-capacitances can be simplified by using the dependency of the trans-capacitance matrix:

$$C_{gg} = C_{sg} + C_{dg} = C_{gs} + C_{gd} \qquad (8a)$$

$$C_{ss} = C_{sd} + C_{sg} = C_{gs} + C_{ds} \qquad (8b)$$

$$C_{dd} = C_{sd} + C_{gd} = C_{ds} + C_{dg} \qquad (8c)$$

The details of these independent trans-capacitances are displayed in (He J. et al., 2007). Using the derived analytic expressions of the carrier concentrations, terminal charges, and the trans-capacitances, all current-voltage and capacitance-voltage characteristics of a long channel surrounding-gate MOSFET device can be predicted and analyzed with respect to different geometrical parameters and bias operation conditions in Figure 12-18. The detailed discussion is included in (He J. et al., 2007). The validity of the analytical solutions is confirmed by comparing model predictions with simulation data obtained using the 3-D numerical solvers. Through the results and discussion, we get that the explicit expressions to the terminal charges and trans-capacitance not only lead to a more clear understanding of surrounding-gate MOSFET device physics, but also provide a better infrastructure to develop a complete carrier-based model for the surrounding-gate MOSFET based circuit simulation.
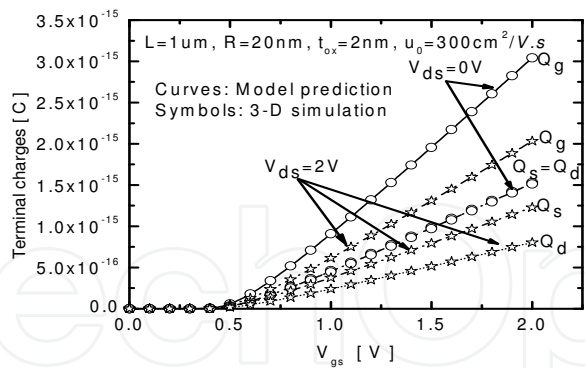
Fig. 12. Terminal charge versus gate voltage for different V_{ds}, compared with the numerical 3-D simulation (symbols) for a long channel undoped surrounding-gate MOSFET with L=1um, tox=2nm, R=20nm, $u_0 = 300 cm^2 / Vs$, and W= $2\pi R$. (From He J. IEEE TED, Vol. 54, No. 6, June 2007)
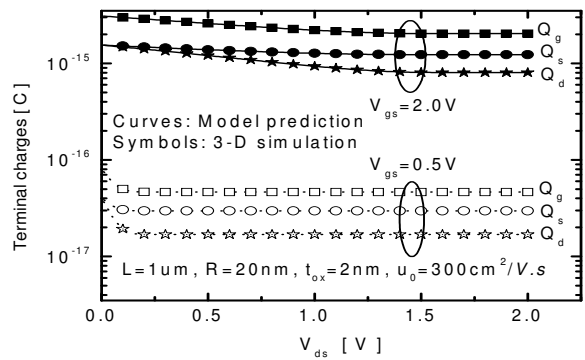

Fig. 13. Terminal charge versus V_{ds} for different V_{gs} (From He J. IEEE TED, Vol. 54, No. 6, June 2007)
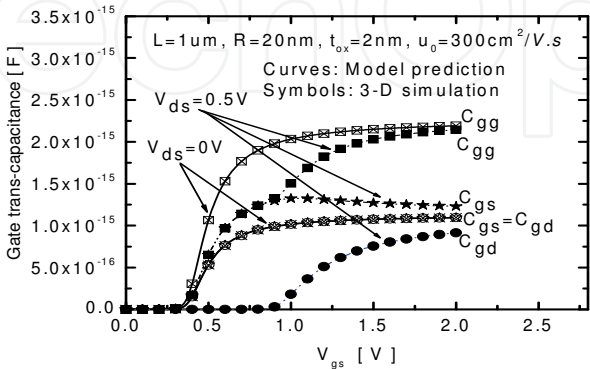

Fig. 14. Gate trans-capacitance versus gate voltage for different V_{ds} (He J. From He J., IEEE TED, Vol. 54, No. 6, June 2007)
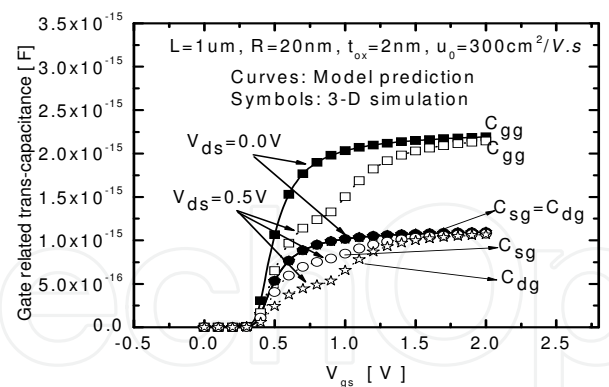
Fig. 15. Gate voltage related trans-capacitances versus V_{ds} (From He J. IEEE TED, Vol. 54, No. 6, June 2007)
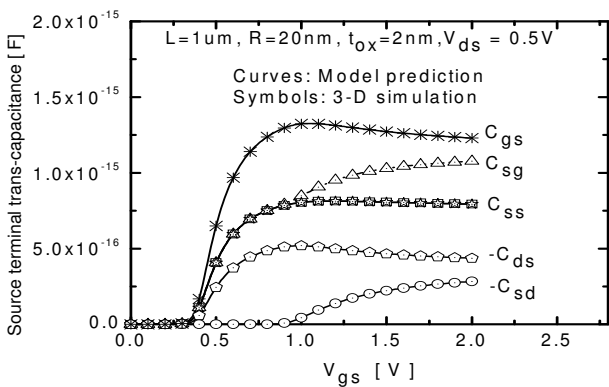

Fig. 16. Source terminal trans-capacitances versus V_{gs} (From He J. IEEE TED, Vol. 54, No. 6, June 2007)
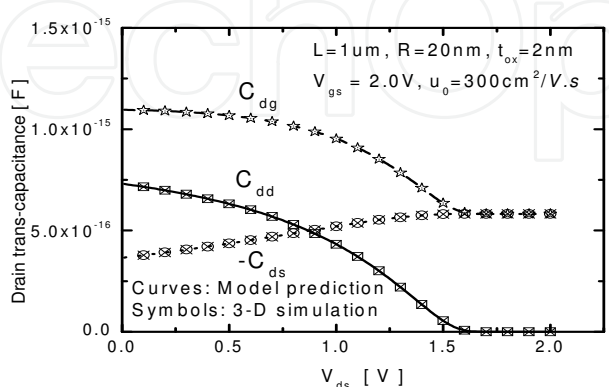

Fig. 17. Drain terminal trans-capacitances versus V_{ds} (From He J. IEEE TED, Vol. 54, No. 6, June 2007)
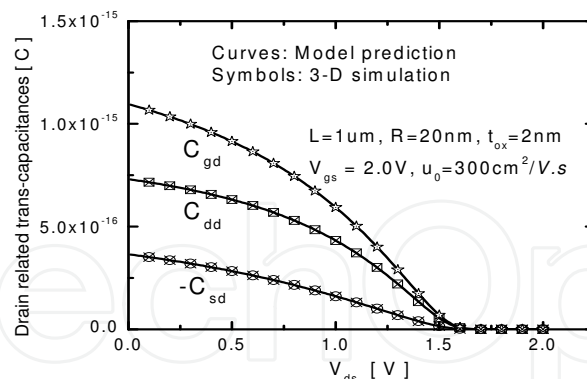
Fig. 18. Drain related trans-capacitances versus V_{ds} (From He J. IEEE TED, Vol. 54, No. 6, June 2007)

A basic feature of the above modeling works is to use an undoped (or lightly doped) body assumption to sustain the theory results. The idea of an undoped body, sometimes referred to as "intrinsic channel", is expected to have special advantages such as the low leakage current, free-statistic dopant fluctuation, and improved short-channel effects. However, the practical SRG MOSFET is always a doped body structure due to a small order unintentional doping ($10^{12} cm^{-3} \sim 10^{15} cm^{-3}$) during the real fabrication process. Thus, the undoped body is only an ideal approximation for light and low-doped case in all non-classical CMOS device. The practical SRG device may be designed as a fully depleted MOSFET in order to take the advantages of the undoped body via the low body concentration process and materials. Since the dopant concentration does not only change the surface potential magnitude, but also strongly changes the device sub-threshold slope, an analytic doped SRG MOSFET model is highly desirable for the circuit design and performance test. So a compact model for doping nanowire is showed next.

3.2 Unified core model for dopings in nanowire

Following the carrier-based approach (He, J. et al., 2006a, 2006b) and using a superposition principle, an approximate carrier-based compact model for the fully depleted SRG MOSFETs with a finite doping body is approximately developed directly from both the Poisson equation solution and the Pao-Sah current formulation. The standard cylindrical coordinate formulation of the Poisson-Boltzmann equation in a doped SRG MOSFET is written as:

$$\frac{d^2\phi}{dr^2} + \frac{1}{r}\frac{d\phi}{dr} = \frac{qN_a}{\varepsilon_{si}}\left[1 + \left(\frac{n_i}{N_a}\right)^2 \exp\left(\beta(\phi - V)\right)\right] \tag{9}$$

Where n_i and N_a are the intrinsic silicon concentration and the body doping concentration in the silicon film with the unit of cm^{-3}, respectively ε_{si} and ϕ are the silicon dielectric constant and the electrostatic potential in *Volt* respectively. r is the cylindrical coordinate in *cm* along the radius direction of the silicon film. $1/\beta$ And V are the thermal voltage and the quasi-Fermi-potential in Volt.

The Boltzmann statistics can be expressed as:

$$n = \frac{n_i^2}{N_a} \exp\left(\beta(\phi - V)\right) \tag{10a}$$

and

$$n_0 = \frac{n_i^2}{N_a} \exp\left(\beta(\phi_0 - V)\right) \tag{10b}$$

Where n_0 and ϕ_0 are the induced electron concentration in cm^{-3} and the electrostatic potential in V at $r = 0$. In a SRG MOSFET, the silicon radius center where the electric field is always zero is chosen as coordinate reference point.

The Poisson equation solution in terms of the carrier concentration can be written as (He, J. et al., 2006a, 2006b)

$$\phi_{sI} - \phi_{0I} = \frac{2}{\beta} \ln\left[1 - \frac{R^2}{8L_D^2} \frac{n_0}{N_a} \right] \tag{11}$$

Where ϕ_{SI} and ϕ_{0I} are the silicon surface and centric potentials in $Volt$ contributed by the induced electron charge. $L_D = \sqrt{\varepsilon_{si} kT / q^2 N_a}$ is the Debye length in cm of silicon film with doping concentration of N_a.

Similarly, we obtain the inversion density from the carrier-based Poisson equation solution in (He, J. et al., 2006a, 2006b)

$$Q_I = \frac{\varepsilon_{si} R}{2\beta L_D^2} \frac{n_0 / N_a}{1 - \frac{R^2}{8L_D^2} \frac{n_0}{N_a}} \tag{12}$$

If only the dopant is considered in (9) and the fully depletion approximation is used, the Poisson equation solution in the SRG can be written as

$$Q_b = \sqrt{q \varepsilon_{si} N_a (\phi_s - \phi_0)} \tag{13}$$

$$\phi_{sB} - \phi_{0B} = \frac{q_b R}{4\varepsilon_{si}} \tag{14}$$

where Q_b is the depleted charge density in $C \cdot cm^{-2}$ in the silicon film contributed by the doping atom. ϕ_{sB} and ϕ_{0B} are the silicon surface and centric potentials in V contributed by the depletion charge density, respectively.

thus $\phi_s = \phi_{sI} + \phi_{sB}$

$$\phi_s = \phi_0 + \sqrt{\frac{q N_a R^2}{16\varepsilon_{si}} (\phi_s - \phi_0)} - \frac{2}{\beta} \ln\left[1 - \frac{R^2}{8L_D^2} \frac{n_0}{N_a} \right] \tag{15}$$

and (4) plus (5):

$$Q_{tot} = Q_b + Q_I = \sqrt{q\varepsilon_{si}N_a(\phi_s - \phi_0)} + \frac{\varepsilon_{si}R}{2\beta L_D^2}\frac{n_0/N_a}{1-\frac{R^2}{8L_D^2}\frac{n_0}{N_a}} \tag{16}$$

where ϕ_s and Q_{tot} are the total silicon surface potential in V and the total charge in $C \cdot cm^{-2}$ contributed by the induced mobile electron charges and the depleted charges, respectively. Through (15), we can get the surface potential in terms of the carrier concentration.

$$\phi_s = \phi_0 + \left[\sqrt{\alpha^2/4 - \frac{2}{\beta}\ln\left[1-\frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]} + \alpha/2\right]^2 \tag{17}$$

where $\alpha^2 = \frac{qN_aR^2}{16\varepsilon_{si}}$, and the complete analytic solution of the Poisson equation is obtained in terms of the carrier concentration:

$$\begin{aligned}V_{gs} - \Delta\varphi - V - 2\phi_F &= \frac{1}{\beta}\ln\left(\frac{n_0}{N_a}\right) + \left[\sqrt{\alpha^2/4 - \frac{2}{\beta}\ln\left[1-\frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]} + \frac{\alpha}{2}\right]^2 \\ &+ \gamma\left[\sqrt{\alpha^2/4 - \frac{2}{\beta}\ln\left[1-\frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]} + \frac{\alpha}{2}\right] + \frac{\varepsilon_{si}R}{2\beta C_{OX}L_D^2}\frac{n_0/N_a}{1-\frac{R^2}{8L_D^2}\frac{n_0}{N_a}}\end{aligned} \tag{18}$$

where $\gamma = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}}$ is the bulk bias factor.

(18) gives the closed form expression of electron concentration at the silicon film center as a function of bias conditions, dopant concentration, and geometry sizes.

The drain current is written as:

$$I_{DS} = \mu\frac{W}{L}\int_0^{V_{DS}} q_{Ii}dV = \mu\frac{W}{L}\int_{n_{0s}}^{n_{0D}} q_I(n_0)\frac{dV}{dn_0}dn_0 \tag{19}$$

Where n_{0S} and n_{0D} are solutions of (18) corresponding to $V = 0$ being the source end voltage and $V = V_{ds}$ being the drain end voltage, respectively. μ is the effective channel mobility of the SRG MOSFET in $cm^2/V.s$. L and $W = 2\pi R$ are the effective channel length and width of the SRG MOSFET in cm, respectively. Note that the dV/dy can also be expressed as a function of n_0 by differentiating (18). Substituting these factors into (19), integrating can be performed approximately yet analytically to yield:

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{DS}} q_I dV = \frac{4\pi\mu\varepsilon_{si}}{L}\left(\frac{2}{\beta}\right)^2 f(n_0)\Big|_{n_{0d}}^{n_{0s}} \tag{20}$$

where

$$f\left(n_0\right) = \frac{1}{2}\ln\left[1 - \frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right] + \frac{\left[\varepsilon_{ox} - 2\varepsilon_{si}\ln\left(1 + \frac{t_{ox}}{R}\right)\right]}{\varepsilon_{ox}\left[1 - \frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]} + \frac{\varepsilon_{si}\ln\left(1 + \frac{t_{ox}}{R}\right)}{\varepsilon_{ox}\left[1 - \frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]^2}$$

$$+ \frac{\beta}{2}(\alpha + \gamma)\sqrt{\alpha^2/4 - \frac{2}{\beta}\ln\left[1 - \frac{R^2}{8L_D^2}\frac{n_0}{N_a}\right]} \qquad (21)$$

The fully depleted SRG MOSFET characteristics for all operation regions can be predicted from this compact yet continuous, analytic model. The characteristics of surface potential and centric potential for different doped concentrations from the intrinsic undoped assumption are showed in Figure 19 and 20, and their relative error is also predicted by the analytic model compared with the 3-D numerical simulation. It is found that the relative error increases with the increase of the body concentration for the given geometry parameters, when the body doping concentration is $1e16cm^{-3}$ the relative error is within the order of 1e-3, but the relative error increases to the order of 1e-2 for the doping concentration up to $1e17cm^{-3}$. Figure 21 and 22 show the comparison of I_{ds} versus V_{GS} and V_{DS} between the analytic solution (curves) and the 3-D simulation (symbols) for the different doping concentration. The SRG MOSFET current predicted by the analytic model shows a good match with the 3-D numerical simulation from the sub-threshold region to the strong inversion region for most doping concentrations.

We should point out that some second-order physics effects of the nanoscale SRG MOSFETs such as short-channel effects, the drain induced barrier lowering effect, and the more important inversion layer quantum effect (QME) are important for the analysis of nanoscale SRG MOSFET although they are ignored in above study to give a clear presentation of the SRG MOSFET charge and capacitance model. For example, the QME drives the peaks of electron concentration away from the interface between the gate oxide and the silicon film,

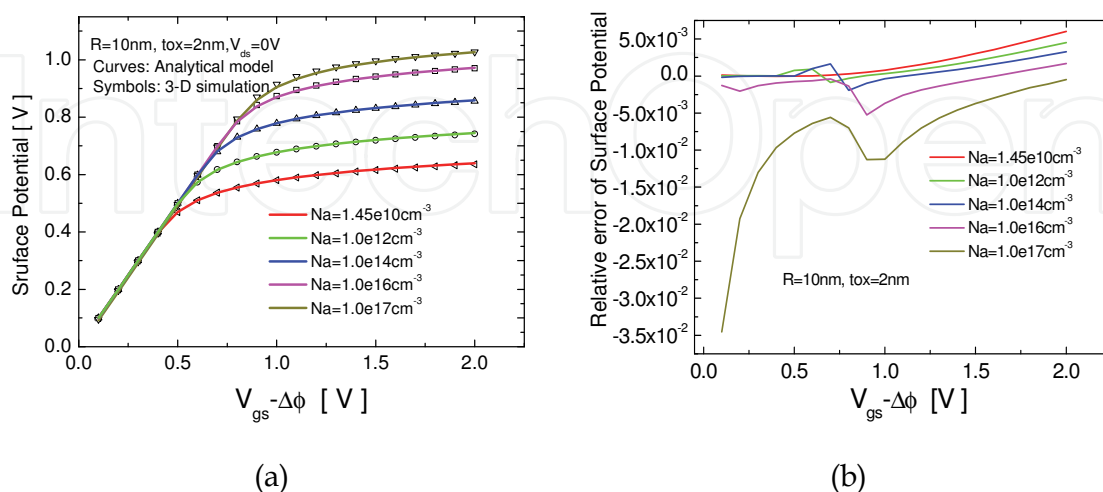(a)   (b)

Fig. 19. (a) the comparison of the surface potential versus gate voltage curves for five different doped concentrations and (b) the relative error of the surface potential. (From He J. Semicond. Sci. Technol. 22 (2007) 671–677)
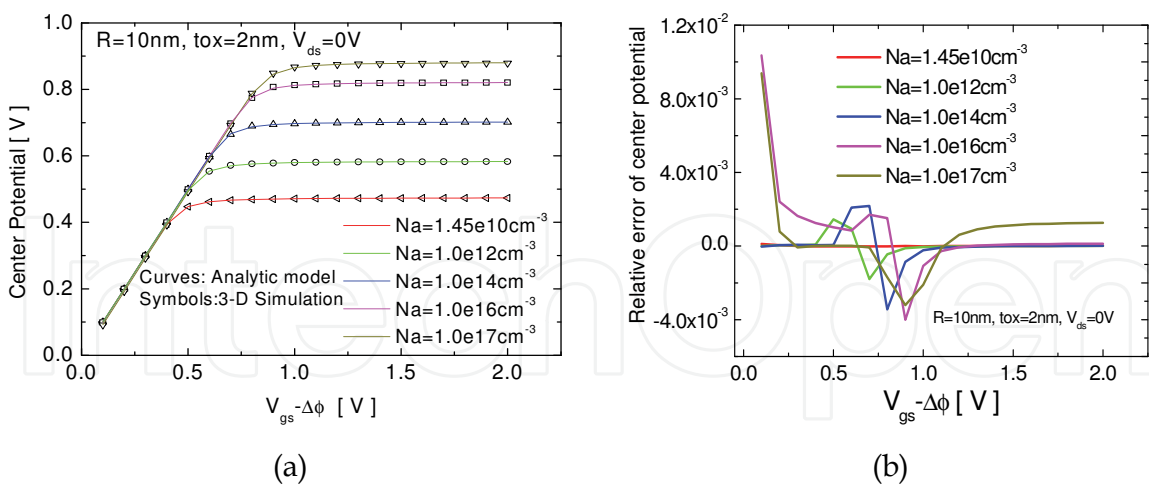
Fig. 20. (a) the comparison of the centric potential versus gate voltage curves and (b) the resultant relative error(from He J. Semicond. Sci. Technol. 22 (2007) 671–677)
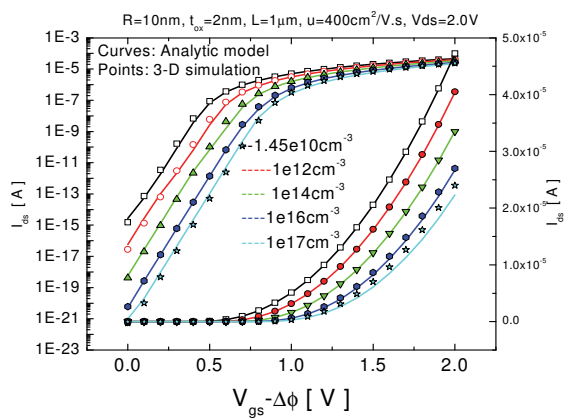

Fig. 21. I_{ds} versus V_{GS} and compared with the 3-D numerical simulation (from He J. Semicond. Sci. Technol. 22 (2007) 671–677)
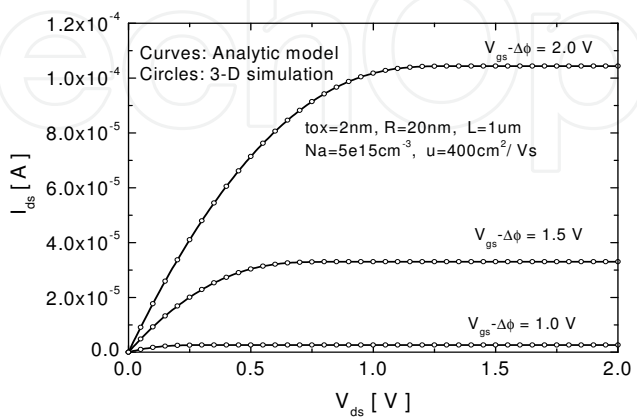

Fig. 22. I_{ds} versus V_{DS} and compared with the 3-D numerical simulation (from He J. Semicond. Sci. Technol. 22 (2007) 671–677)

and pushes the peaks toward the centre of the silicon channel. As a result, the QME causes an increase in the threshold voltage and degradation in the sub-threshold slope, especially with the reduction of the silicon film radius. In addition, the short-channel effects also lead to the threshold voltage reduction and sub-threshold slope degradation with the reduction of the SRG MOSFET channel length. Next, we will introduce second-order physics effects in the compact model of the nanoscale SRG MOSFETs.

3.3 Unified model for nanowire with advanced effects
Starting from Poisson's equation solution, an accurate inversion charge (Qin) equation is obtained for the long channel SNWTs with arbitrary doped bodies. Moreover, some advanced physical effects such as short channel effects (SCEs), quantum mechanical effects (QMEs), high field mobility degradation and velocity saturation have all been incorporated into the model.

3.3.1 Modeling short channel effects
For the transistor with short channel length, the voltage at the drain terminal has significant impact on the channel potential, known as SCEs. In generally, SCEs induce threshold voltage roll-off, subthreshold slope degradation, drain induced barrier lowering. In addition, channel length modulation and carrier velocity saturation and overshoot become important at short channel length as well. Here, SCEs are modeled following the BSIM5 approach. Assume the surface potential in a short channel device can be expressed as:

$$\phi_s(y) = \phi_{s0} + \phi_{s,3D}(y) \tag{22}$$

where ϕ_{s0} is the solution of the 2D Poisson's equation. After substituting (22) into (9) and considering boundary condition, we got

$$\phi_S(y) = \phi_{S0} + \frac{(v_{ds} + v_{bi} - \phi_{s0})\sinh[y/\lambda] + (v_{bi} - \phi_{s0})\sinh[(L - y)/\lambda]}{\sin[L/\lambda]} \tag{23}$$

Its minimum value, which determines the threshold voltage at a low v_{ds}, is given by:

$$\phi_{s,\min} = \phi_{s0} + \frac{(v_{ds} + 2v_{bi} - 2\phi_{s0})\sinh[L/2\lambda]}{\sin[L/\lambda]} \tag{24}$$

where $\lambda = \sqrt{t_{oxeff} \cdot \frac{R}{2} \cdot \frac{\varepsilon_{si}}{\varepsilon_{ox}} + \frac{1}{4}R^2}$ is the natural length of SNWT by assuming the highest leakage path lies at the center of the channel. Combining ϕ_{s0} with equation of boundary condition, we get a new surface potential solution in terms of inversion charge:

$$q_{dep} + q_{in} = v_{gs} - \Delta\phi - \alpha \cdot \phi_s + f_{SCE} \cdot (v_{ds} + 2v_{bi}) \tag{25a}$$

and a inversion charge solution can be obtained:

$$\frac{v_{gs} - v_{th}}{\alpha} - v_{ch} = \frac{q_{in}}{\alpha} + \ln q_{in} + \ln(1 + H \cdot q_{in}) \tag{25b}$$

where $\alpha = 1 + 2 \cdot f_{SCE}$ is the subthreshold slope (SS);

$f_{SCE} = 1 / \left[2 \cosh \left(L/2/\lambda \right) - 2 \right]$ is the SCEs factor;

$v_{th} = v_{th0} + \Delta v_{th,VOL} + \Delta v_{th,SCE}$ is the new threshold voltage;

$\Delta v_{th,SCE} = f_{SCE} \cdot \left[2 \cdot \left(v_{th,Long} - q_{dep} - v_{bi} \right) - v_{ds} \right]$ is the threshold voltage roll-off induced by the SCEs. A drain current expression can further be derived using (25b):

$$I_{ds} = \frac{2\pi R \mu_{eff} C_{oxeff}}{\beta^2 L_{eff}} \left[f(q_d) - f(q_s) \right] \tag{26a}$$

with

$$f(q_{in}) = -\frac{q_{in}^{2}}{2\alpha} - 2q_{in} + \frac{1}{H} \ln \left(1 + H \cdot q_{in} \right) \tag{26b}$$

Comparison with numerical simulation results shown in Figure 23(a) shows the correctness of the threshold voltage roll-off and DIBL described by the proposed SCEs model. Figure 23(b) shows that the transfer characteristics with subthreshold slope degradation as predicted in the proposed the short channel model. The strong inversion drain current is not affected by the SCEs, which is expected.
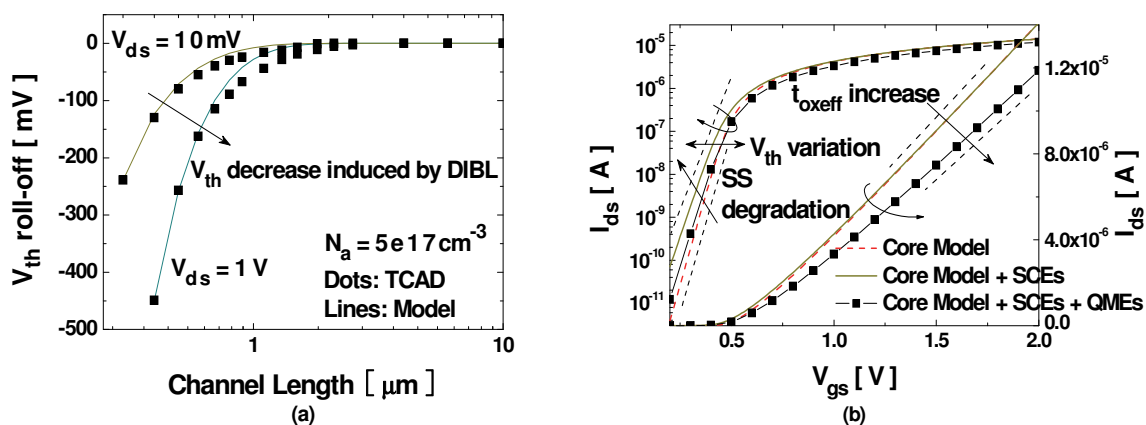

Fig. 23. (a) the threshold voltage roll-off versus channel length and (b) transfer characteristics in the short channel model (From Yang J. IEEE TED, Vol. 55, No. 11, November 2008)

3.3.2 Modeling quantum-mechanical (QM) effects and other advanced physical effects

In highly scaled device, the QM confinement of the carrier in the thin silicon channel is significant. As in bulk MOSFETs, the large vertical electric field leads to a strong band bending and carrier confinement at the surface, known as EC as shown in Figure 24. The deviation of the location of peak carrier concentration from the surface decreases the channel carrier concentration and leads a decrease in the gate capacitance (Francis et al., 1992):

$$\Delta t_{ox} = \Delta = a \cdot \left(\frac{\hbar^2}{2qm_e E_{avg}} \right)^{1/3} \tag{27a}$$

$$C_{oxeff} = \varepsilon_{ox} \left[(R - \Delta/3) \cdot \ln \left((R + t_{ox})/(R - \Delta/3) \right) \right]^{-1} \tag{27b}$$

where m_e is the effective mass of the electron corresponding to the lowest electric sub-band, and $E_{avg} = C_{ox}\left(q_{dep} + \overline{q}_{in}/3\right)\big/\beta\varepsilon_{si}$ is the average surface field. Besides the EC, there is a strong carrier confinement in nanoscale SNWTs even at low electric fields in the channel. It is because the carriers are confined in a rectangular well formed by the gate insulator around, known as SC. In SC and EC, the conduction band split into several subbands as shown in Figure 24. Since the carriers stays at the subband with the lower energy first, the reduction of the amount of carriers can be modeled by the widening the effective band-gap (Arora, 1993) and replace v_{ch} in (25b) by

$$v_{ch} \rightarrow v_{ch} + \frac{E_0}{q} = v_{ch} + \lambda_q \frac{1}{q}\left(\frac{\hbar^2\pi^2}{4m_e R^2}\right) \tag{28}$$

The simulation results shown in Figure 23(b) illustrates the model can predicted the threshold voltage roll off and gate capacitance degradation induced by QME correctly.
The modeling of other advanced physical effects such as poly-depletion effects and mobility degradation of this work are imported from the BSIM5 approach. Velocity saturation, velocity overshoot and ballistic transport (source-end velocity limit) is handled in a unified way using the saturation charge concept:

$$q_{insat} = \frac{q_{in}}{1 + 2\beta n v_{sat} L_{eff}\big/\mu_{eff}\left(2n + k_{sativ}q_{in}\right)} \tag{29a}$$

$$q_{ineff} = \sqrt[m]{q_{insat}^{\ m} + q_{in}^{\ m}} \tag{29b}$$

where n and m are the only parameters. The effective inversion charge q_{ineff} at the source and drain ends are substituted into the final current expression (26) to calculate the device output current. A complete ballistic transport model is not considered in this work, as ballistic transport will not be significant until the channel length is scaled to less than 10nm (Duan et al., 2001). The dc characteristics for a small size SNWT predicted by the complete compact model is demonstrated in Figure 25.
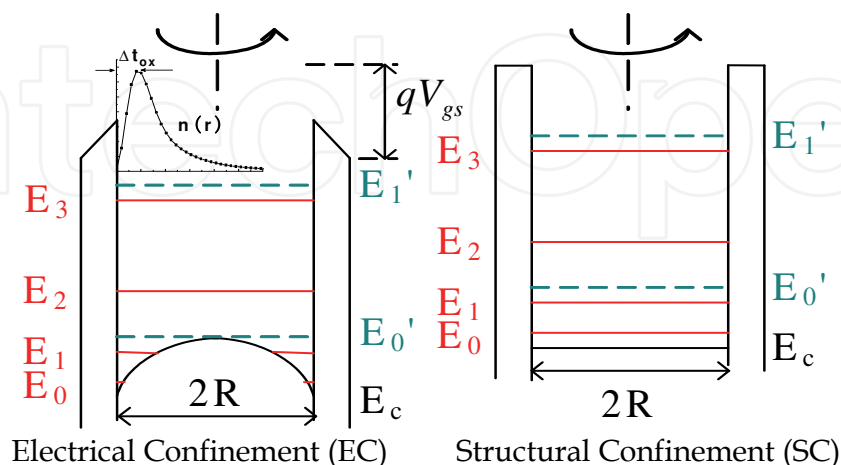

Fig. 24. Energy-band diagrams showing the carrier confinement and the quantization of electronic energy levels in the small size channel due to electrical confinement and structural confinement (From IEEE TED, Vol. 55, No. 11, November 2008)
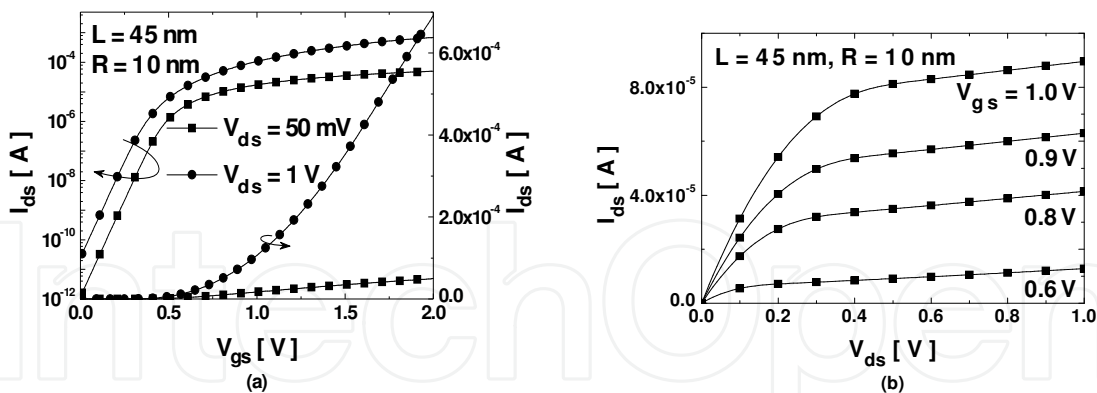
Fig. 25. (a) Ids-Vgs and (b) Ids-Vds characteristics predicted by the complete compact model for a small size SNWT (From IEEE TED, Vol. 55, No. 11, November 2008)

3.4 Ge/Si core/shell nanowire MOSFETs modeling

As one promising molecular device, Ge/Si core/shell nanowire MOSFET has been intensively studied experimentally and theoretically (Xiang et al., 2006; Lu et al., 2005; Fan et al., 2008; Musin & Wang, 2005; Liang et al., 2007; He, Y. et al., 2008) in recent years. Such a device utilizes the bandstructure engineering (Xiang et al., 2006), strain effect (He, Y. et al., 2008) and ballistic transport of 1-dimensional (1D) hole gas (Liang et al., 2007), resulting in very high carrier mobility and excellent performance. At the same time, an analytic compact model is also highly desirable for both physical insight into and performance evaluation of the core/shell based NWFET devices. However, it has not been available so far due to the complexity in analytically modeling the corresponding heterostructure, strain effect and ballistic transport. Nevertheless, some theoretical progresses on non-classical MOSFETs have provided the base for us to develop a primary analytical electrostatic potential model.

Here, starting from Poisson-Boltzmann equation in the Ge/Si core/shell NWFETs, the classical analytic expressions of electrostatic potential and charges in the semiconductor layers are derived out under the gradual channel approximation.

The schematic diagram and corresponding coordinate of a long channel Ge/Si core/shell NWFET are shown in Figure 26, where z is the channel direction, r is the radial direction, t_{ox} is the thickness of gate dielectric, r_0 and R are the radii of germanium core and silicon shell, respectively.
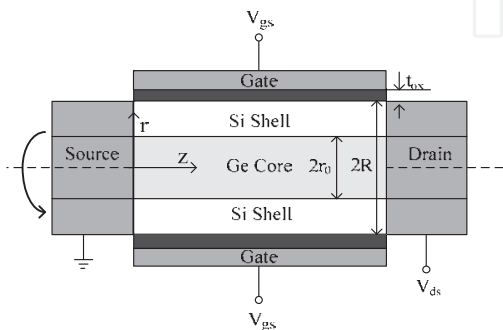

Fig. 26. Shematic diagrame of a Ge/Si core/shell NWFET

The assumed condition in the model derivation include: an abrupt heterojunction between germanium and silicon, an intrinsic or lightly doped body and a long device channel. Quantum confinement and strain effect are neglected for simplicity. Under gradual channel approximation (GCA), the Poisson-Boltzmann equations in Ge/Si core/shell NWFETs are written as the following forms with only hole term considered:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right) = -\frac{qn_{iGe}}{\varepsilon_{Ge}}\exp\left(\frac{V_{bi} - \phi + V_{ch}}{V_t}\right), 0 \le r \le r_0 \tag{30}$$

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right) = -\frac{qn_{isi}}{\varepsilon_{si}}\exp\left(\frac{V_{ch} - \phi}{V_t}\right), r_0 < r \le R \tag{31}$$

where ϕ is the electrostatic potential, V_{bi} is the self-built voltage of intrinsic Ge/Si heterojunction, V_{ch} is hole quasi-Fermi potential, q is the electronic charge, V_t is the thermal potential, $n_{iGe}(n_{isi})$ and $\varepsilon_{Ge}(\varepsilon_{si})$ are the intrinsic carrier concentration and permittivity of germanium (silicon), respectively. The Ge/Si core/shell NWFET behaves like a depletion p-channel device due to the band offset between intrinsic germanium and silicon. Hole accumulation in both germanium core and silicon shell are handled while electron is neglected. Also notice that V_{ch} is assumed to be constant along the radius according to quasi-equilibrium approximation, being a negative value for p type device.

For simplicity, a normalized formulation of (31) is used to find its solution in the shell region, the detailed process is showed in (Zhang L. et al., 2008). (31) in the silicon shell layer is solved concisely as:

$$\phi_{si}(r) = V_{ch} - V_t\ln(2A^2L_{si}^2/r^2) - V_t\ln\left[\beta_{si}(r/r_0)^A\right] + 2V_t\ln\left[1 - \beta_{si}(r/r_0)^A\right] \tag{32}$$

where β_{si} and A are two intermediary parameters to be decided by the boundary condition, L_{si} is the Debye length of intrinsic silicon $L_{si} = \sqrt{\varepsilon_{si}V_t/(qn_{isi})}$.

And then the radial electric field in the silicon shell layer is obtained:

$$E_{si}(r) = -\frac{d\phi_{si}}{dr} = \frac{V_t}{r}\left[A - 2 + 2A\frac{\beta_{si}(r/r_0)^A}{1 - \beta_{si}(r/r_0)^A}\right] \tag{33}$$

Similarly, electrostatic potential and electric field in the germanium core layer are given at A=2:

$$\phi_{Ge}(r) = V_{bi} + V_{ch} - V_t\ln(8L_{Ge}^2/r_0^2) - V_t\ln(\beta_{Ge}) + 2V_t\ln[1 - \beta_{Ge}(r/r_0)^2] \tag{34}$$

and

$$E_{Ge}(r) = -\frac{d\phi_{Ge}}{dr} = \frac{4V_t}{r_0}\frac{\beta_{Ge}(r/r_0)}{1 - \beta_{Ge}(r/r_0)^2} \tag{35}$$

where L_{Ge} is the Debye length of intrinsic germanium $L_{Ge} = \sqrt{\varepsilon_{Ge}V_t/(qn_{iGe})}$. Also the intermediary parameter β_{Ge} is evaluated from the boundary condition.

At the interface between silicon and gate oxide layer, surface potential and electric filed are obtained according to the above equation:

$$\phi_s = V_{ch} + V_t \ln(2A^2 \frac{L_{si}^2}{R^2}) + V_t \ln\left[\beta_{si}(\frac{R}{r_0})^A \right] - 2V_t \ln\left[1 - \beta_{si}(\frac{R}{r_0})^A \right] \tag{36}$$

$$E_s = \frac{V_t}{R}\left[(A-2) + 2A \frac{\beta_{si}(R/r_0)^A}{1 - \beta_{si}(R/r_0)^A} \right] \tag{37}$$

Following Gauss's Law and electric flux continuity condition, we get the final input voltage equation:

$$\frac{V_{ch} - (V_{gs} - \Delta\phi)}{V_t} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} \ln(1 + \frac{t_{ox}}{R})\left[(A-2) + 2A \frac{\beta_{si}(R/r_0)^A}{1 - \beta_{si}(R/r_0)^A} \right] +$$
$$+ \ln(\frac{2A^2 L_{si}^2}{R^2}) + \ln\left[\beta_{si}(\frac{R}{r_0})^A \right] - 2\ln\left[1 - \beta_{si}(\frac{R}{r_0})^A \right] \tag{38}$$

Similar to the existing compact models for bulk and other non-planar MOSFET, the input voltage equation and its solution is the base for further developing drain current models and advanced effect models. The detailed solving procedure for (38) is described as follows.

At the interface between germanium core layer and silicon shell layer both the potential and electric flux need to be continuous. So the parameters A, β_{si} and β_{Ge} are arrived.

For the studied Ge/Si core/shell structure, it is verified that A is always larger than 2 with gate voltage increasing for the Ge/Si core/shell structure. On the other hand, A has an upper limit set which is independent of the bias condition (Figure 27). And the three intermediary parameters are obtained simultaneously by the shooting secant method. After that, interface potential ϕ_{r_0} and centric potential ϕ_0 are obtained directly by substituting $r = r_0$ and $r = 0$ into (34), respectively:

$$\phi_{r_0} = V_{bi} + V_{ch} - V_t \ln(8L_{Ge}^2/r_0^2) - V_t \ln(\beta_{Ge}) + 2V_t \ln[1 - \beta_{Ge}] \tag{39}$$

$$\phi_0 = V_{bi} + V_{ch} - V_t \ln(8L_{Ge}^2/r_0^2) - V_t \ln(\beta_{Ge}) \tag{40}$$

Hole charge density in germanium core and silicon shell layers are directly obtained through Gauss's law:

$$Q_{mGe} = 4\varepsilon_{Ge} \frac{V_t}{r_0} \frac{\beta_{Ge}}{1 - \beta_{Ge}} \tag{41a}$$

$$Q_{msi} = 2A\varepsilon_{si} \frac{V_t}{R}\left[\frac{1}{1 - \beta_{si}(R/r_0)^A} - \frac{1}{1 - \beta_{si}} \right] \tag{41b}$$

respectively.

The total hole charge density in the channel is also obtained as:

$$-Q_g = \frac{\varepsilon_{si} V_t}{R}\left[(A-2) + 2A\frac{\beta_{si}(R/r_0)^A}{1-\beta_{si}(R/r_0)^A}\right] \tag{41c}$$

Note that Q_{msi} represents the charge density per unit area at the interface between the silicon shell and oxide layer while Q_{mGe} denotes that at the interface between the germanium core layer and silicon shell layer. As a result, gate capacitance of the core/shell structure is obtained by differentiating gate charge Q_g with respect to the gate voltage as follows:

$$C_g = \frac{dQ_g}{dV_{gs}} = C_{ox}\left[1 - \frac{d\phi_s}{dV_{gs}}\right] = C_{ox}\left[1 - \frac{d\phi_s}{dA}\bigg/\frac{dV_{gs}}{dA}\right] \tag{42}$$

where $d\phi_s/dA$ and dV_{gs}/dA are obtained from (36) and (38), respectively.
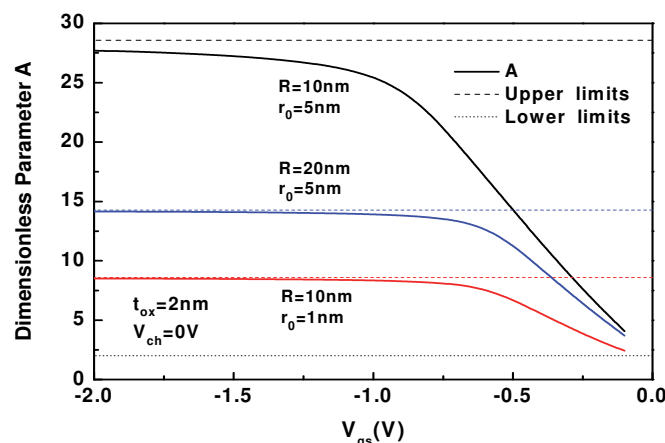
Fig. 27. The parameter A versus V_{gs} for different Ge/Si core/shell structures (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)

In summary, the analytical electrostatic potential equation and its solution are presented above. In this section the analytic potential model is verified through numerical simulation. The physical parameters of silicon and germanium in both the analytical model and numerical simulator are taken from (Sze, 1981). The spatial potential, electric field and hole charge density are obtained under classical device physics through intermediary parameter A, β_{si} and β_{Ge} for the given gate voltage, quasi-Fermi potential and structure parameters. So once the three intermediary parameters are solved for the given bias and device geometry, the characteristics of the Ge/Si core/shell structure are directly obtained form the analytic model prediction. The potential, electric field and charge density solution are illustrated in Figure 28-32 for one geometry configuration: $R=10nm$, $r_0=5nm$, and $t_{ox}=2nm$ in comparison with numerical simulation results. The results show that excellent agreements are observed between the analytic model and the numerical simulation in all these figures and the Ge/Si core/shell heterostucture NWFET exhibits its unique characteristics, much different from a common SRG MOSFET. A more detailed discussion is displayed in (Zhang L. et al., 2008).
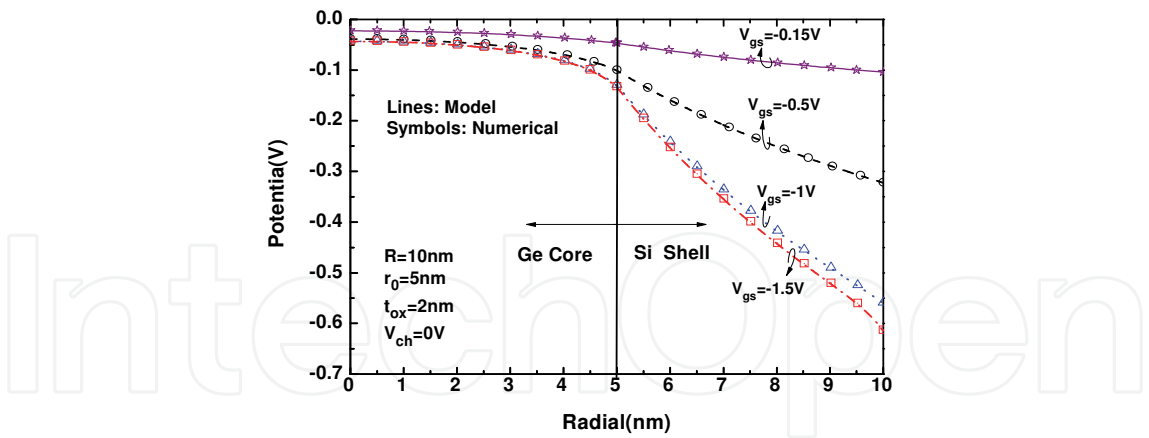
Fig. 28. Potential distribution along the radial of a Ge/Si core/shell structure. The lines denote results obtained from the analytic model and the symbols are results from numerical simulation (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)
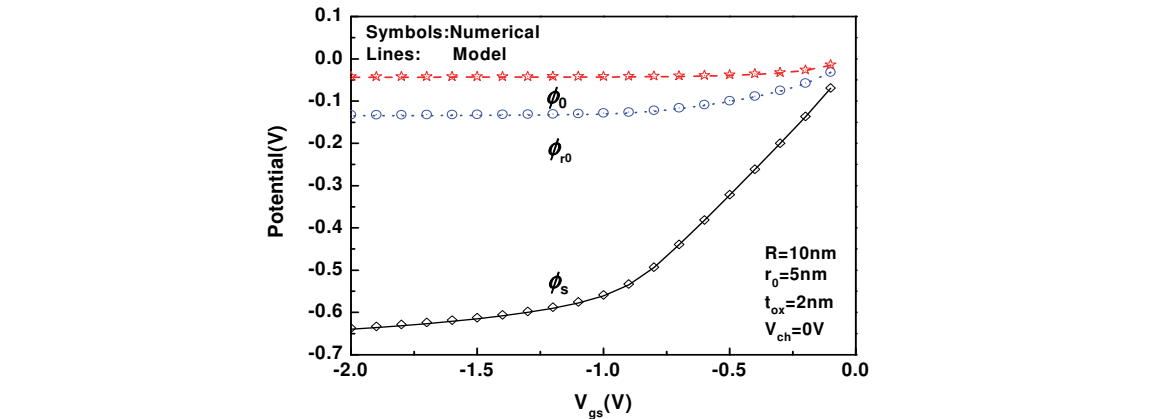

Fig. 29. ϕ_s, ϕ_{r_0} and ϕ_0 of a Ge/Si core/shell structure as functions of V_{gs} obtained form the analytic model (curves) in comparison with numerical simulation (symbols) (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)
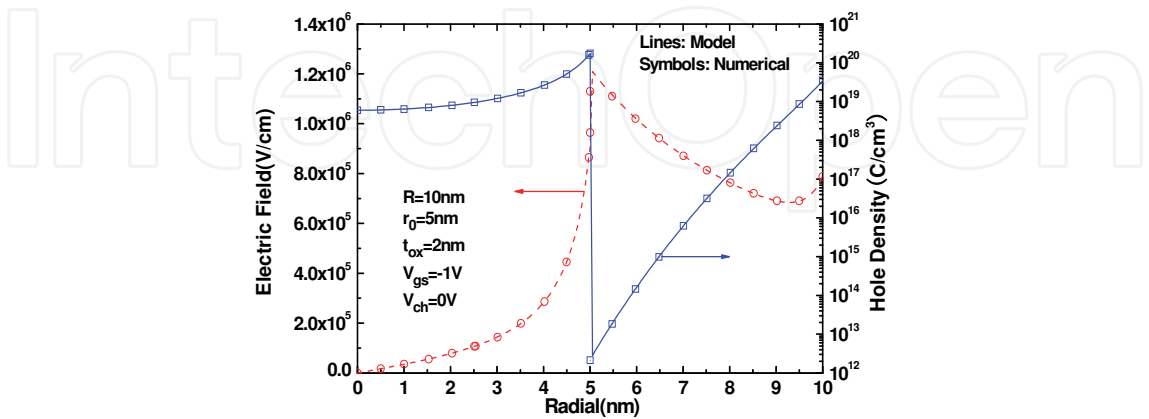

Fig. 30. Electric field and hole density distributions along the radial of a Ge/Si core/shell structure at $V_{gs} = -1V$, obtained from the analytic model (lines) in comparison with numerical simulation (symbols) (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)
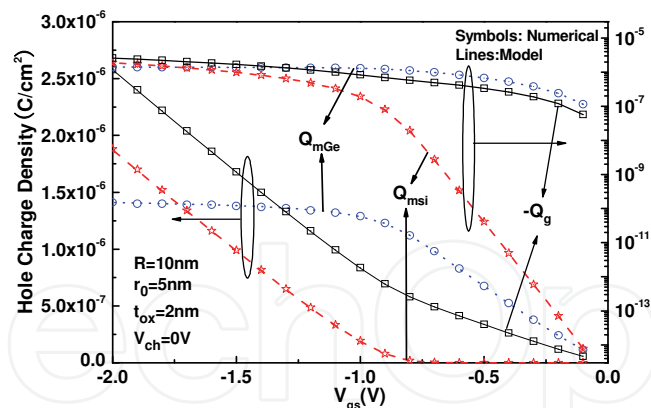
Fig. 31. Charge density Q_{mGe}, Q_{msi} and $-Q_g$ of a Ge/Si core/shell structure as functions of V_{gs} both in linear and logarithm coordinates, obtained from the analytic model (lines) in comparison with numerical simulation (symbols). (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)
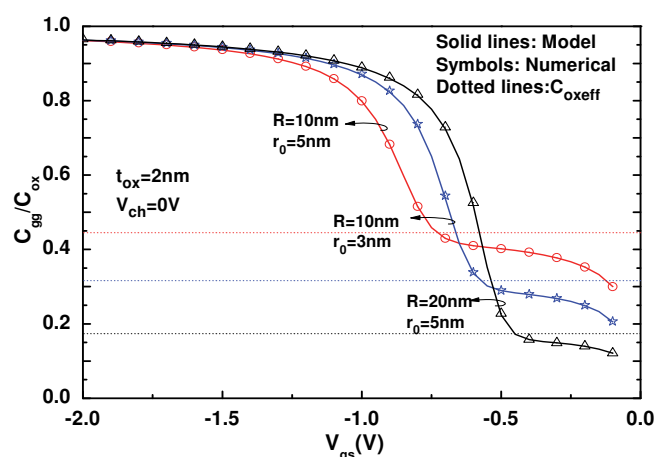

Fig. 32. Normalized gate capacitance C_{gg}/C_{ox} curves as a function of V_{gs} from the analytic model (solid lines) in comparison with numerical simulation (symbols). Dotted lines denote three corresponding C_{oxeff} (Zhang L. IEEE TED, Vol. 55, No. 11, Nov. 2008)

4. Nanowire–based circuit simulation

Paralleling the advance of process technology to fabricate SNWT (Cui et al., 2001c; Duan et al., 2001), compact models for the SNWTs have also been developed for circuit simulations in recent years. A general model for doped SNWTs may be very useful for device scientists to optimize the device structure and for circuit designers to evaluate the performance of the SNWT circuits. Here, a design oriented compact model for SNWTs, applicable for a wide range of doping concentrations (i.e. from 10^{10} to 10^{19}cm-3) and geometrical dimensions is presented. Starting from Poisson's equation solution, an accurate inversion charge (Qin) equation is obtained for the long channel SNWTs with arbitrary doped bodies. Then a charge based drain current (Ids) expressions is derived. Transconductance (gm), output conductance (gds), terminal charges (Q) and capacitance (Cij) are all derived analytically

and verified by TCAD simulation (Synopsys, 2005). And then this model is also implemented in the circuit simulator by the Verilog-A language and its application in circuit simulations is also demonstrated.
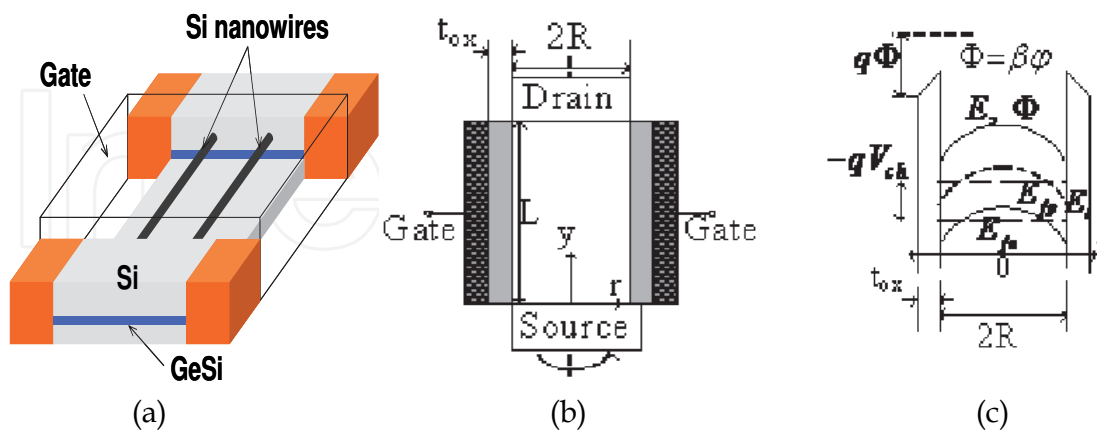

Fig. 33. (a) Stereoscopic schematic, (b) cross-section schematic, and (c) energy band diagram of an N-type SNWT (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)

The device structure, coordinate system, and corresponding energy band diagram of a doped SNWT studied in this work are shown in Figure 33 (a), (b) and (c), respectively. For an n-type device, the hole Fermi level Efp remains constant along the channel if the current of majority carriers is neglected. Consequently, Efp can be defined as the energy reference level in this work. The 3D Poisson-Boltzmann equation in the SNWT structure is written as

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right)+\frac{d^2\phi}{dy^2}=\frac{1}{L_D{}^2}\left[1+e^{\phi-v_{ch}-2\phi_f}\right] \tag{43}$$

where $\phi_f = \ln(N_a/n_i)$ is the Fermi-potential, v_{ch} is the quasi-Fermi potential, ϕ is the channel potential, and $L_D{}^2 = kT\varepsilon_{si}/q^2 N_a$ is the Debye's length of the silicon body with doping N_a. All other variables have there usual meanings. All the potentials in this work are normalized by thermal voltage β, and the charges by β/C_{ox}, unless otherwise specified. $C_{ox} = \dfrac{\varepsilon_{ox}}{R\ln(1+t_{ox}/R)}$ is the effective oxide capacitance.

This 3D problem is simplified into two separate parts along the vertical and current flow directions. And we get the relationship:

$$v_{gs} - v_{th0} - \Delta v_{th,VOL} - v_{ch} = q_{in} + \ln q_{in} + \ln(1 + H \cdot q_{in}) \tag{44}$$

where $v_{th0} = \Delta\phi + 2\phi_f + q_{dep} - \ln\dfrac{4\varepsilon_{si}}{RC_{ox}}q_{dep}$ is the transistor threshold voltage similarly to bulk MOSFET; $\Delta v_{th,VOL} = -\ln\dfrac{1}{2q_{dep}}\left[1 - \exp\left(-\dfrac{C_{ox}R}{2\varepsilon_{si}}q_{dep}\right)\right]$ is the extra part of threshold voltage induced by the special geometric structure of SNWT and $q_{in} = q^2 n_0 R/2kTC_{ox}$ is given as the total mobile charge sheet density in the channel.
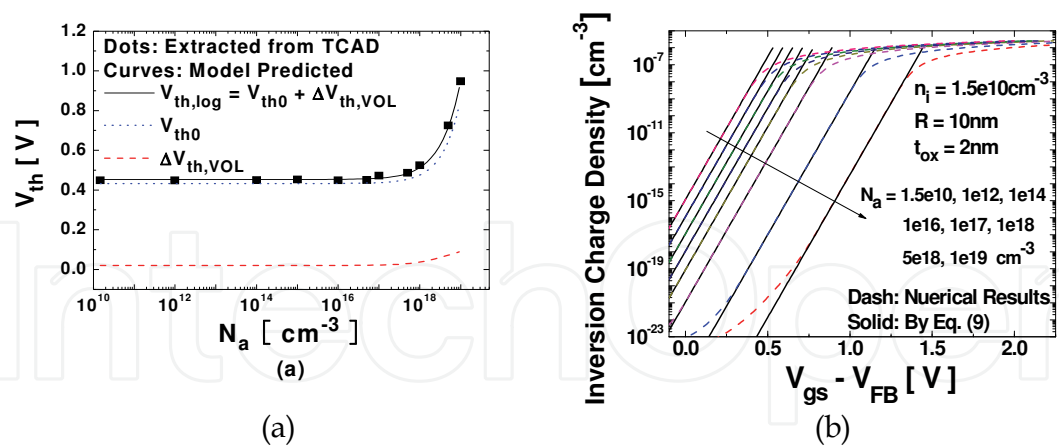
(a)   (b)

Fig. 34. (a) Vth model is compared with TCAD extracted by second derivative method in a long channel SNWT (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)

Through the above equation, the validity of the threshold voltage modeling is verified, see Figure 34，and the characteristics of inversion charge with different condition are got and shown in Figure 35.
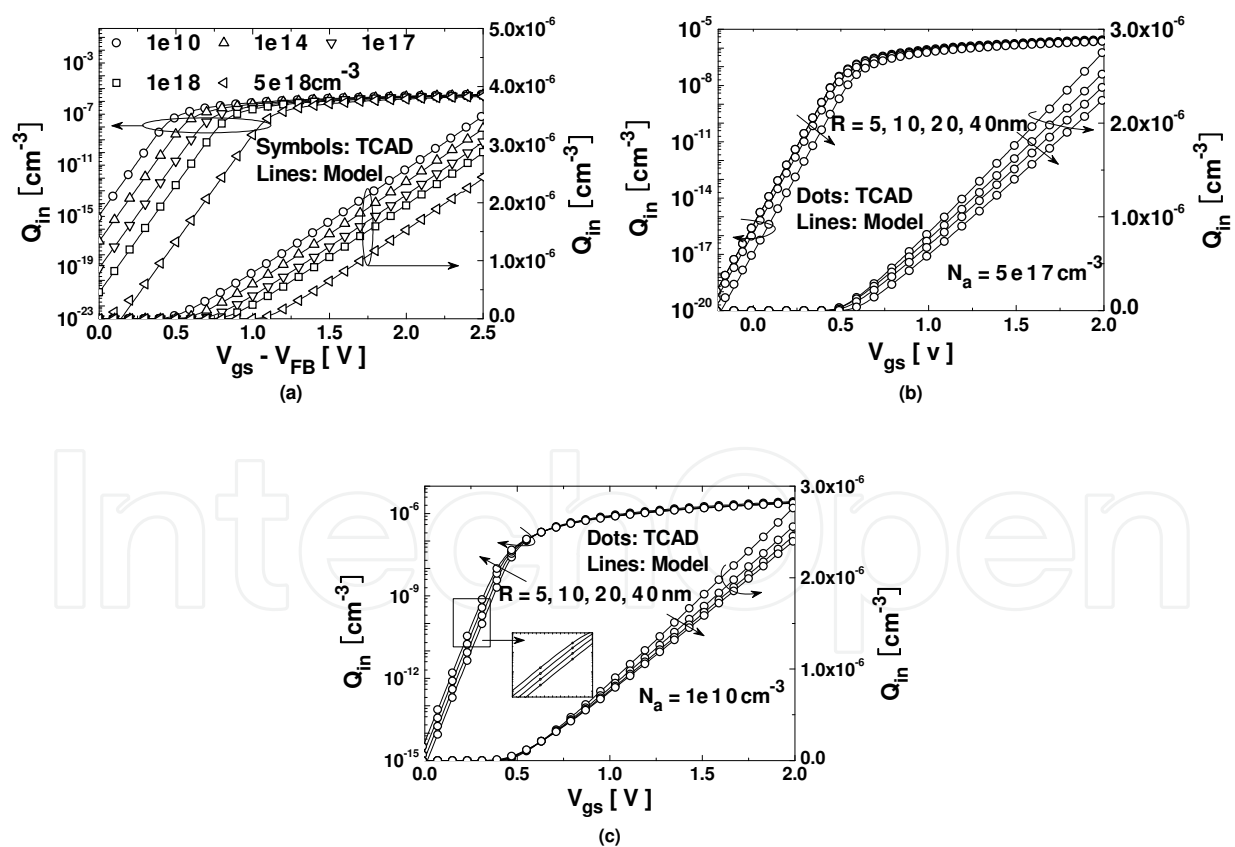

Fig. 35. Inversion charge equation verification for long channel SNWTs (a) with doping variation, (b) with geometric size variation in doped case and (c) with geometric size variation in undoped case (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)

The analytical drain current expression is obtained as:

$$I_{ds} = \frac{2\pi R \mu_{eff} C_{ox}}{\beta^2 L_{eff}} \left[f(q_d) - f(q_s) \right] \tag{45}$$

where μ_{eff} is the effective mobility in the channel; V_{ds} is the quasi-Fermi potential in the drain terminals; q_d and q_s are normalized inversion charge per unit gate area at the source and drain terminals with $f(q_{in}) = -\frac{1}{2}q_{in}^2 - 2q_{in} + \frac{1}{H}\ln(1 + H \cdot q_{in})$

Transconductance and output conductance can be derived analytically from the expressions of drain current:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{V_{ds}} = \frac{2\pi R \mu_{eff} C_{ox}}{\beta L_{eff}}(q_s - q_d) \tag{46a}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}\bigg|_{V_{gs}} = \frac{2\pi R \mu_{eff} C_{ox}}{\beta L_{eff}} q_d \tag{46b}$$

Analytical expressions for inversion charges at each terminal are desired for efficient transient circuit simulation. For a SNWT, there are three terminal charges, associating with gate, source, and drain, respectively: the gate charge Qg can be computed by integrating the channel charge density along the channel; The drain and source charges, denoted as Qd and Qs, can be derived analytically by using the Ward-Dutton linear-charge-partition method:

$$Q_g = \frac{2\pi R C_{ox}}{\beta^2} \int_0^{V_{ds}} q_{in} dy \tag{47a}$$

$$Q_d = -\frac{2\pi R C_{ox}}{\beta^2} \int_0^{V_{ds}} \frac{y}{L} q_{in} dy \tag{47b}$$

$$Q_s = -Q_g - Q_d \tag{47c}$$

where y/L are obtained from the current continuity condition

$$\frac{y}{L} = \frac{f(q_{in}) - f(q_s)}{f(q_d) - f(q_s)} \tag{48}$$

The model predicted I-V characteristics are verified by comparing with TCAD simulation under various biasing voltages, a wide range of doping concentrations and geometric dimensions as shown in Figure 36. The error between the proposed model and the 3-D numerical simulation is less than 5% with devices with intrinsic to heavily doped body with a doping of 10^{19} cm-3. The numerical simulation results demonstrate the accuracy of the proposed model from the linear to saturation and from the sub-threshold to strong inversion regions.

In contrast to digital circuits, analog design focus on the first derivatives such as gm/Ids and Cij, which are shown in Figure 37. At Vds=0, Cgs=Cgd and Csg=Cdg in the figures indicate that the developed model has inherent the source/drain symmetry characteristic, which is important for analog and RF applications. Note that the verifications of the core I-V and C-V models are done without any fitting parameters.

The compact SNWT model has been implemented in a commercial circuit simulator ADS2006A by the Verilog-A language to demonstrate practicality of the model. This implementation includes a procedure to produce an initial guess and convergent correction methods to help the nonlinear equation (25b) to calculate the inversion charge. DC, ac, and transient simulations of many sample circuits are performed. Figure 38 shows the transient analysis of a 21-stage SNWT ring oscillator by this model. The waveforms of three successive stages are plotted in the figure. Compared with a ring oscillator constructed by DG MOSFETs (Taur et al., 2004), the oscillator frequency in this work is much higher, illustrating a smaller transistor input capacitances relative to the higher current drive in SNWT device. In the case of high parasitic capacitance, parallel connection of several SNWTs can be used.
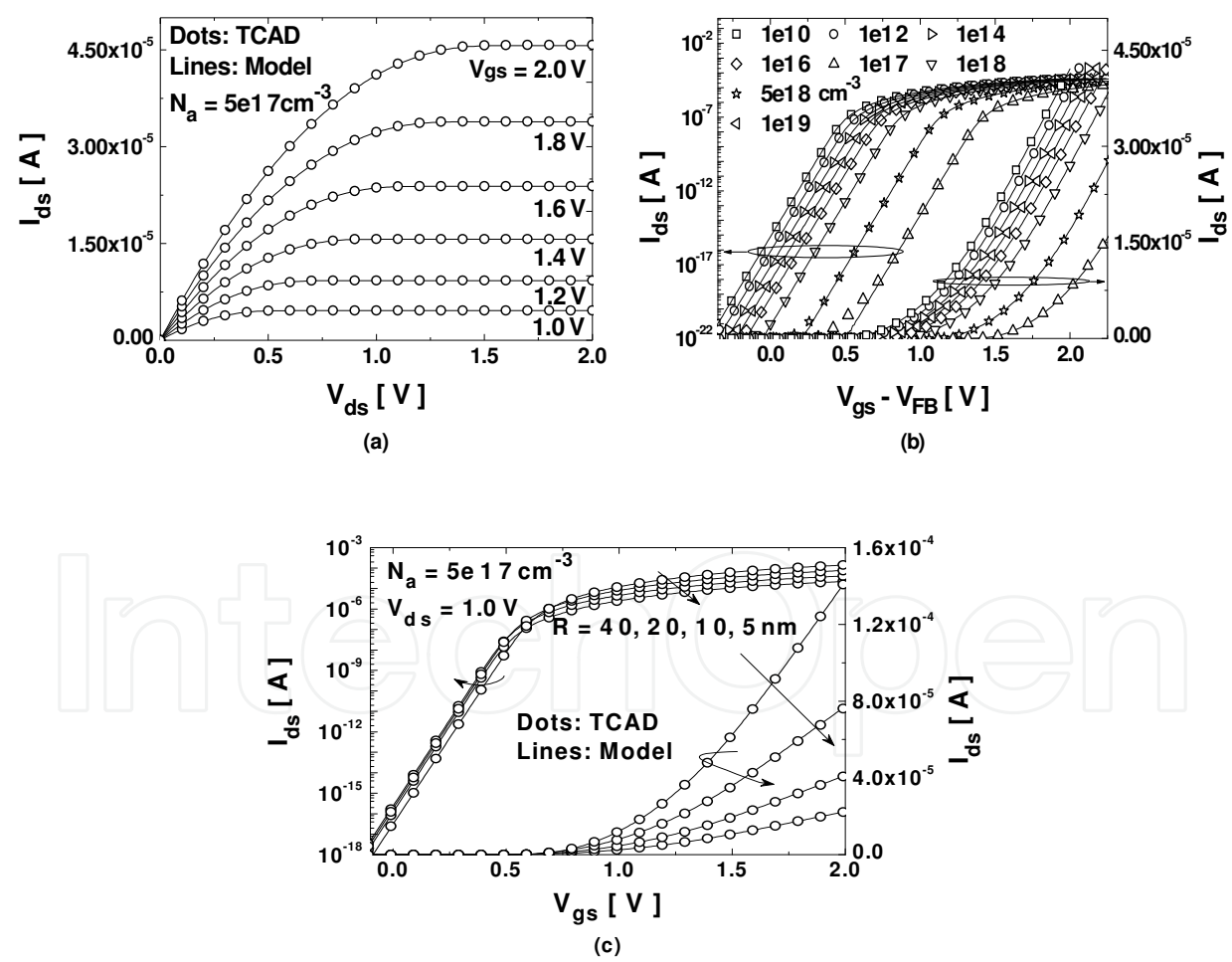

Fig. 36. dc I-V characteristics verification for long channel SNWTs (a) Ids-Vds (b) Ids-Vgs with doping variation (Symbols: TCAD, Lines: Model) and (c) Ids-Vgs with geometric size variation. (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)
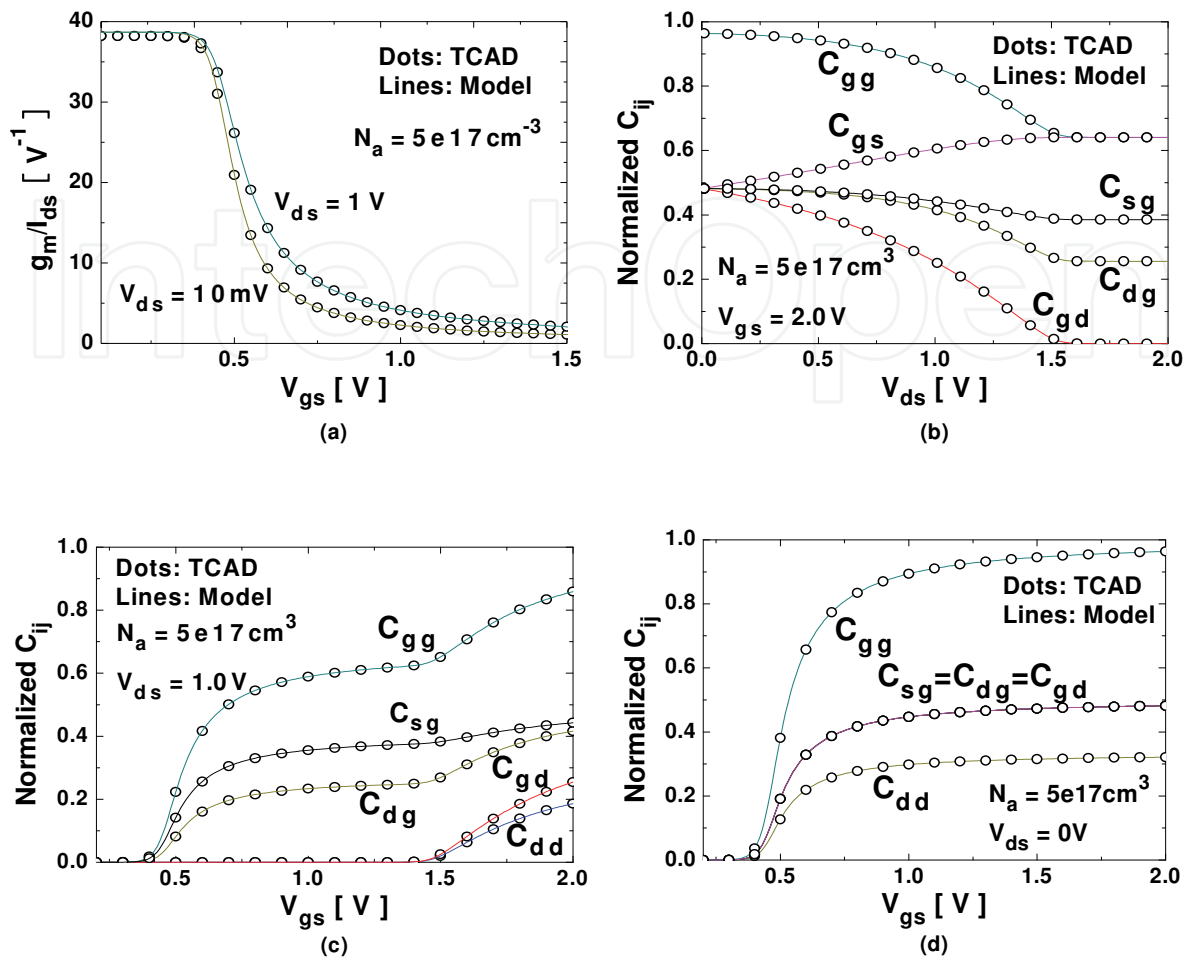
Fig. 37. ac characteristics verification of the model for a long channel SNWT (a) gm-efficiency, (b) C-Vds, (c) C-Vgs (at Vds≠0) and (d) C-Vgs (at Vds=0) (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)

5. Conclusion

In this chapter, after a brief outline of the silicon-based nanowire fabrication technology, we discussed simulation and compact model of nanowire MOSFET following the device physics understanding and exploring. In the developed compact model, the short channel effect, quantum mechanic effect and other are analyzed and the predicted results are also compared with the 3-D numerical simulation. Based on such a verified physics based SPICE model, the nanowire based circuit performance is simulated and demonstrated.
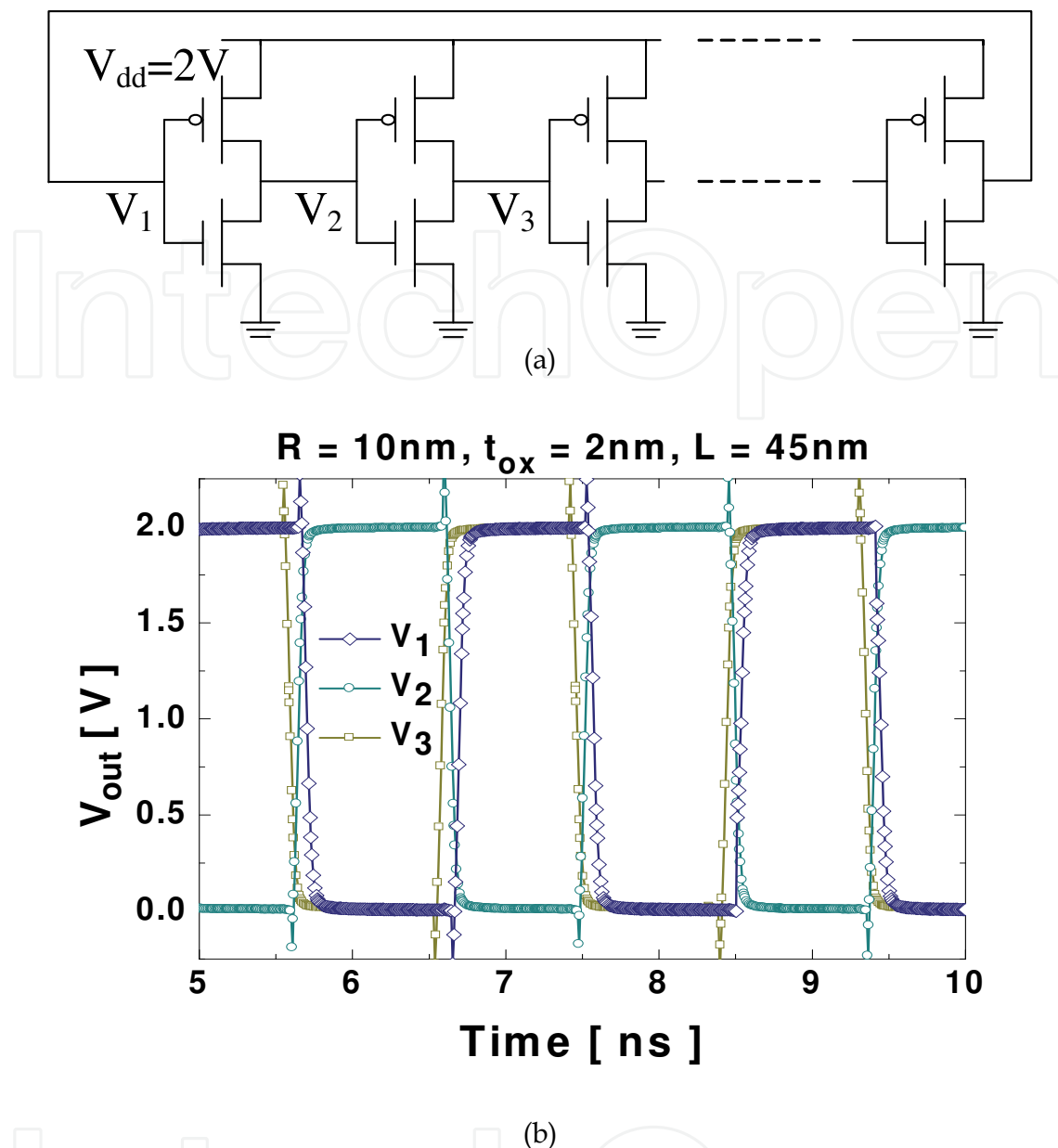
6. Acknowledgment

(a)

(b)

Fig. 38. (a) Circuit schematic of a 21-stage SNWT ring oscillator, and (b) the waveforms of three successive outputs in a transient analysis by ADS2006A (From Yang J., IEEE TED, Vol. 55, No. 11, Nov. 2008)

7. References

Arora, N., MOSFET models for VLSI circuit simulation: theory and practice, *Springer-Verlag New York Inc.*, ISBN 0387823956, Secaucus, NJ, USA

Barrelet, C. J., Greytak, A. N., & Lieber, C. M., (2004). Nanowire Photonic Circuits Elements, *Nano Letters*, vol. 4, no. 10, (September, 2004), pp.1981-1985, ISSN 10.1021

Bera, L. K., Nguyen, H. S., Singh, N., Liow, T. Y., Huang, D. X., Hoe, K. M., Tung, C. H., Fang, W. W., Rustagi, S. C., Jiang, Y., Lo, G. Q., Balasubramanian, N., & Kwong, D. L., Three Dimensionally Stacked SiGe Nanowire Array and Gate-All-Around p-

MOSFETs, *IEEE International Electron Devices Meeting, 2006*, pp. 551-554, ISBN 1-4244-0438-X, San Francisco, CA, USA, Dec 11-13, 2006

Black, C. T., (2005). Self-aligned self assembly of multi-nanowire silicon field effect transistors, *Appl. Phys. Lett.* Vol. 87, No.16, (October 2005), pp.163116-163118, ISSN 0003-6951

Bian, W., He, J., Tao, Y., Fang, M., & Feng, J., (2007). An analytic potential-based model for undoped nanoscale surrounding-gate MOSFETs, *IEEE Transactions on Electron Devices*, Vol. 54, No.9, (Sept. 2007), pp. 2293-2303, ISSN 0018-9383

Chang, C., Wang, Y. F., Kanamori, Y., Shih, J. J., Kawai, Y., Lee, C. K., Wu, K. C., & Esashi, M., (2005). Etching submicrometer trenches by using the Bosch process and its application to the fabrication of antireflection structures, *J. Micromech. Microeng.*, Vol. 15, No. 3, (March 2005), pp.580-585, ISSN 0960-1317

Cui, Y. & Lieber, C. M., (2001). Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks, *Science*, Vol.291, No.5505, (February 2001), pp.851-853, ISSN 1095-9203

Cui, Y., Lauhon, L., Gudiksen, M., Wang, J., & Lieber, C., (2001). Diameter-controlled synthesis of single-crystal silicon nanowires, *Applied Physics Letters*, Vol. 78, No.15, (APRIL 2001), pp. 2214-2216, ISSN 1077-3118

Cui, Y., Wei, Q., Park, H., & Lieber, C. M., (2001). Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species, *Science*, Vol. 293, No. 5533, (August 2001), pp. 1289–1292, ISSN 1095-9203

Duan, X., Huang, Y., Cui, Y., Wang, J., & Lieber, C. M., (2001). Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices, *Nature*, Vol. 409, (January 2001), pp. 66–69, ISSN 0028-0836

Dupre, C., et. al. 15nm-diameter 3D Stacked Nanowires with Independent Gates Operation: ΦFET, *IEEE International Electron Devices Meeting, 2008*, pp. 749-752, ISBN 978-1-4244-2377-4, San Francisco, CA, USA, Dec15-17, 2008

Fang, W. W., Singh, N., Bera, L. K., Nguyen, H. S., Rustagi, S. C., Lo, G. Q., Balasubramanian, N., & Kwong, D. L., (2007). "Vertically stacked SiGe nanowire array channel CMOS transistors", *IEEE Electron Device Letters*, Vol. 28, No. 3, (March 2007), pp. 211-213, ISSN 0741-3106

Fan, Z., Ho, J. C.. Jacobson, Z. A., Razavi, H.. & Javey, A., (2008). Large-scale, heterogeneous integration of nanowire arrays for image sensor circuitry, *Proc. Nat. Acad. Sci.*, Vol.105, No.32, (Aug., 2008), pp.11066 -11070, ISSN 11066-11070

Ferry, D., Gilbert, M., & Akis, R., (2008), Some considerations on nanowires in nanoelectronics, *IEEE Transactions on Electron Devices*, Vol. 55, No.11, (Nov. 2008), pp. 2820-2826, ISSN 0018-9383

Francis, P., Terao, A., Flandre, D., & Van de Wiele, F., (1992). Characteristics of nMOS/GAA (Gate-All-Around) transistors near threshold, *Microelectronic Engineering*, Vol. 19, No. 1-4, (August 2002), pp. 815-818, ISSN 0167-9317(92)90551-2

He, J., & Chan, M., physics based analytical solution to undoped cylindrical surrounding-gate (SRG) MOSFETs. *15th IEEE Int. Conf. on Devices, Circuits and Systems*, pp. 26-28, ISBN 0-7803-8777-5, Dominican Republic, Nov.3-5, 2004

He, J, Zhang, X., Zhang, G., Chan, M., & Wang, Y., (2006). A carrier-based DCIV model for long channel undoped cylindrical surrounding-gate MOSFETs, *Solid-State Electronics*, Vol. 50, No. 3, (March, 2006), pp. 416-421, ISSN 0038-1101

He, J., Zhang, X., Zhang, G., Chan, M., & Wang, Y., A complete carrier-based non-charge-sheet analytic theory for nano-scale undoped surrounding-gate MOSFETs. *Proceedings of ISQED'2006*, pp.115-120, ISBN 0-7695-2523-7, San Jose, Costa Rica, Mar. 28, 2006

He, J., Bian, W., Tao, Y., Yang, S., & Tang, X., (2007). Analytic carrier-based charge and capacitance model for long-channel undoped surrounding-gate MOSFETs, *IEEE Transactions on Electron Devices*, Vol. 54, No.6, (June 2007), pp. 1478-1485, ISSN 0018-9383

He, Y., Fan, C., Zhao, Y., Du, G., Liu, X., & Han, R., Impact of inhomogeneous strain on the valence band structure of Ge-Si core-shell nanowires, *Proc. Int. Conf. on Simulation of Semiconductor Process and Devices*, pp. 121-124, ISBN 978-1-4244-1753-7 Hakone, Sept. 9-11, 2008

Hood, L., Heath, J. R., Phelps, M. E., & Lin, B., (2004). Systems Biology and New Technologies Enable Predictive and Preventative Medicine, *Science*, Vol. 306, No.5696, (October 2004), pp.640-643, ISSN 1095-9203

Iñíguez, B., Jiménez, D., Riog, J., Hamid, H.A., Marsal, L. F., & Pallarès, J., (2005). Explicit continuous model for long channel undoped surrounding-gate MOSFETs, *IEEE Trans on Electron Devices*, Vol.52, No.8, (Aug. 2005), pp. 1868-1873, ISSN 0018-9383

Jiménez, D., Sáenz, J. J., Iñíguez, B., Suñé, J., Marsal, L. F., & Pallarès, J., (2004). Continuous analytical current-voltage model for surrounding-gate MOSFETs, *IEEE Electron Device Letters*, Vol. 25, No.8, (Aug. 2004), pp. 571-573, ISSN 0741-3106

Jin, S., Fischetti, M., & Tang, T., (2007). Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity, *Journal of Applied Physics*, Vol. 102, No.8, (October 2007), pp. 083715-083728, ISSN 0021-8979

Kedzierski, J., Bokor, J., & Kisielowski, C., (1997). Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation, *J. Vac. Sci. Technol. B*, Vol. 15, No. 6, (July 1997), pp.2825-2828, ISSN 0734-211X

Kotlyar, R., Obradovic, B., Matagne, P., Stettler, M., & Giles, M., (2004), Assessment of room-temperature phonon-limited mobility in gated silicon nanowires, *Applied Physics Letters*, Vol. 84, No.25, (June 2004), pp. 5270-5272, ISSN 0003-6951

Liang, G., Xiang, J., Kharche, N., Klimeck, G., Lieber, C. M., & Lundstrom, M., (2007). Performance Analysis of a Ge/Si Core/Shell Nanowire Field-Effect Transistor, *Nano Letter*, Vol. 7, No.3, (January, 2007), pp. 642-646

Liow, T., Tan, K., Lee, R., Zhu, M., Tan, B., Samudra, G., Balasubramanian, N., & Yeo, Y., (2008), "5 nm gate length Nanowire-FETs and planar UTB-FETs with pure germanium source/drain stressors and laser-free Melt-Enhanced Dopant (MeltED) diffusion and activation technique," *Symposium on VLSI Technology*, pp. 36-37, ISBN 978-1-4244-1802-2, Honolulu, HI, June 17-19, 2008

Liu, H., Biegelsen, D. K., Johnson, N. M., Ponce, F. A., & Peace, R. F. W., (1993). Self-limiting oxidation of Si nanowires, *J. Vac. Sci. Technol. B*, Vol. 11, No. 6, (Nov 1993), pp.2532-2537, ISSN 1071-1023

Liu, H., Biegelsen, D. K., Ponce, F. A., Johnson, N. M., & Peace, R. F. W., (1994). Self-limiting oxidation for fabricating sub-5nm silicon nanowires, *Applied Physics Letters*, Vol. 64, No.11, (Mar 1994), pp.1383-1385, ISSN 0003-6951

Lu, W., Xiang, J., Timko, B. P., Wu, Y., & Lieber, C. M., (2005), One-dimensional hole gas in germanium/silicon nanowire heterostructures, *Proc. Nat. Acad. Sci.*, Vol.102, No.29, (July, 2005), pp.10046 -10051, ISSN 10046-10051

Lu, W. & Lieber, C., (2006), Semiconductor nanowires, *Journal of Physics D: Applied Physics*, vol. 39, NO. 21, (June, 2006), pp. R387, ISSN 0022-3727

Michetti, P., Mugnaini, G., & Iannaccone, G., (2009). Analytical model of nanowire FETs in a partially ballistic or dissipative transport regime, *IEEE Transactions on Electron Devices*, Vol. 56, No.7, (July 2009), pp. 1402-1410, ISSN 0018-9383

Moldovan, O., Iñíguez, B., Jiménez, D., & Riog, J., (2007). Analytical Charge and Capacitance Models of Undoped Cylindrical Surrounding-Gate MOSFETs, *IEEE Trans on Electron Devices*, Vol.54, No.1, (January, 2007), pp.162-165, ISSN 0018-9383

Musin, R. N. & Wang X. Q., (2005). Structural and electronic properties of epitaxial core-shell nanowire heterostructures, *Physics Review B*, Vol.71, No.15, (April 2005), pp. 15538-15541, ISSN 1098-0121

Morales, A. & Lieber, C., A laser ablation method for the synthesis of crystalline semiconductor nanowires, (1998). *Science*, Vol. 279, No.208, (JANUARY 1998), pp. 208-211, ISSN 1095-9203

Namatsu, H., Horiguchi, S., Nagase, M., & Kurihara, K., (1997). "Fabrication of one-dimensional nanowires structures utilizing crystallographic orientation in silicon and their conductance characteristics", *J. Vac. Sci. Technol. B*, Vol.15, No.5, (July 1997), pp.1688-1696, ISSN 0734-211X

Neophytou, N., Paul, A., Lundstrom, M., & Klimeck G., (2008), Bandstructure effects in silicon nanowire electron transport, *IEEE Transactions on Electron Devices*, Vol. 55, No.6, (June 2008), pp. 1286-1297, ISSN 0018-9383

Ng, R. M. Y., Wang, T., Liu, F., Zuo, X., He, J. & Chan, M., (2009). Vertically Stacked Silicon Nanowire Transistors Fabricated by Inductive Plasma Etching and Stress Limited Oxidation, *IEEE Electron Device Letters*, Vol. 30, No. 5, (May 2009), pp. 520-522, ISSN 0741-3106

Ng, R. M. Y., Wang, T., & Chan, M., A New Approach to Fabricate Vertically Stacked Single-Crystalline Silicon Nanowires, *Proceedings of 2007 IEEE EDSSC*, pp. 133-136, ISBN 978-1-4244-0637-1, Tainan, Taiwan, China, December 20-22, 2007

Pao, H. C. & Sah, C. T., (1966). Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors, *Solid-State Electronics*, Vol. 9, No.10, (September 2002), pp. 927-937, ISSN 0038-1101(66)90068-2

Ramanathan, K., Bangar, M. A., Yun, M., Chen, W., Myung, N. V., & Mulchandani, A., (2005). Bioaffinity Sensing Using Biologically Functionalized Conducting Polymer Nanowire, *J. AM. CHEM. SOC.*, Vol. 127, No.2, (December, 2004), pp.496-497, ISSN 10.1021

Singh, N., Buddharaju, K. D., Manhas, S. K., Agarwal, A., Rustagi, S. C., Lo, G. Q., Balasubramanian, N., & Kwong, D. L., (2008), Si, SiGe Nanowire Devices by Top–Down Technology and Their Applications, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 55, NO. 11, (July, 2008), pp. 3107- 3118, ISSN 0018-9383

Stern, E., Vacic, A., & Reed, M., (2008), Semiconducting nanowire field-effect transistor biomolecular sensors, *IEEE Transactions on Electron Devices*, Vol. 55, No.11, (Nov. 2008), pp. 3119-3130, ISSN 0018-9383

Synopsys, TCAD Sentaurus Device User's Manual , Mountain View, CA, 2005

Sze, S.M., Physics of Semiconductor Devices, 2nd ed. *Wiley*, ISBN 978-0-471-14323-9, New York, USA

Taur, Y., Liang, X., Wang, W., & Lu, H., (2004). A continuous, analytic drain–current model for DG MOSFETs, *IEEE Electron Device Letter*, Vol. 25, No. 2, (Feb. 2004), pp. 107–109, ISSN 0741-3106

Xiang, J., Lu, W., Hu, Y., Yan, H., & Lieber, C. M., (2006). Ge/Si nanowire heterostructures as high performance field-effect transistors, *Nature*, Vol.441, No.25, (May 2006), pp.489-493, ISSN 0028-0836

Yang, J., He, J., Liu, F., Zhang, L., Zhang, X., & Chan M., (2008). A compact model of silicon-based nanowire MOSFETs for circuit simulation and design, *IEEE Transactions on Electron Devices*, Vol. 55, No.11, (Nov. 2008), pp. 2898-2906, ISSN 0018-9383

Yu, B., Wang, L., Yuan, Y., Asbeck, P., & Taur, Y., (2008). Scaling of nanowire transistors, *IEEE Transactions on Electron Devices*, Vol. 55, No.11, (Nov. 2008), pp. 2846-2858, ISSN 0018-9383

Zhang L., He J., Zhang J., Liu F., Fu Y., Song Y., & Zhang X., (2008). An Analytic Model for Nanowire MOSFETs With Ge/Si Core/Shell Structure," IEEE Transactions on Electron Devices , Vol. 55, No.11, (Nov. 2008), pp. 2907-2917, ISSN 0018-9383

Zhang. L., Zhang. J., Liu. F., Chen. L., Xu. Y., Zhou. W., He, F., An analytic channel potential based model for dynamic depletion surrounding-gate mosfets with arbitrary doping level, 1st Asia Symposium on Quality Electronic Design, ASQED 2009, pp. 131-135, ISBN 978-1-4244-4952-1, Kuala Lumpur, Malaysia, 15-16 July 2009

Zhang, L., Guan, Y., Zhou, W., Chen, L., Xu, Y., & He, J., (2009). A carrier-based analytic drain current model incorporating velocity saturation for undoped surrounding-gate MOSFETs, *Semiconductor Science and Technology*, Vol. 24, No. 11, (Oct. 2009), pp. 115003-115010, ISSN 0268-1242

Zhang, Y. F., Tang, Y. H., Wang, N., Yu, D. P., Lee, C. S., Bello, I., & Lee, S. T., (1998). Silicon nanowires prepared by laser ablation at high temperature, *Applied Physics Letters*, Vol.72, No.15, (Apr 1998), pp.1835-1837, ISSN 0003-6951

Wang, J., "Device Physics and Simulation of Silicon Nanowire Transistors", PhD thesis, Purdue University, 2005
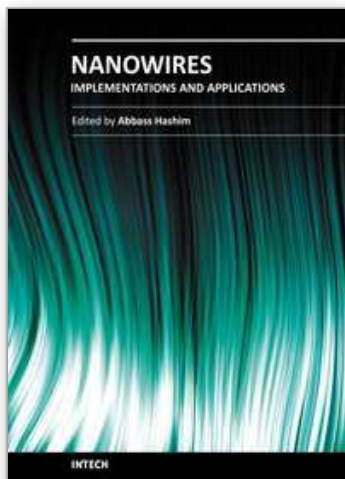
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