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## RF CMOS Background

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### 1. Introduction

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) (or just MOS) is widely used and presents many advantages over the bipolar transistors (BJT) in many applications. It requires less silicon area and its fabrication process is relatively simpler. It is possible to implement most analog and digital circuits using almost exclusively MOS transistors. All these properties allow packing a large number of devices in a single integrated circuit. Additionally, and most important, its operation requires less power, making it extremely suitable to RFID circuits.

This chapter aims to provide background on MOS transistors, from its physical operation to modeling, including RF modeling. The basic knowledge is essential to analyze and to design RFID circuits implemented using CMOS transistors. The chapter also presents noise analysis which is essential to low voltage signal, as it is the case of RFID circuits.

### 2. Physical CMOS operation

Fig. 1 shows the physical structure of the  $n$ -channel MOS transistor, or just  $n$ MOS transistor. The transistor is fabricated in a  $p$ -type silicon substrate. Two heavily doped  $n$ -type regions, indicated as  $n^+$ , are created in the substrate and will act as the source and drain (in terms of structure, source and drain can be interchanged). A thin layer of silicon oxide ( $\text{SiO}_2$ ), of thickness  $t_{\text{ox}}$  (typically between 2 and 50 nm), is formed on the surface of the substrate, between the drain and the source regions. The silicon oxide is an excellent electrical isolator. Metal (or polysilicon, which is conductor) is deposited on top of the oxide layer to form the gate electrode. Metal contacts are also made in the source and drain regions, in addition to contact to the bulk, also known as the substrate or body. Therefore, the four contacts were formed: D-drain, S-source, G-gate and B-bulk.

The gate region has a length  $L$  and a width  $W$ , which are two important design parameters of the MOS transistor. Usually  $L$  is in the range of  $0.1\mu\text{m}$  to  $3\mu\text{m}$  while  $W$  is in the range of  $0.2\mu\text{m}$  to  $100\mu\text{m}$ .

There is also the  $p$ -channel MOS transistor, or just  $p$ MOS transistor, in which the dopings are reversed to the  $n$ MOS transistor.

#### 2.1 Forming the channel

As can be observed from the Fig. 1, the substrate forms  $pn$  junctions with the drain and the source. In normal operation both junctions must be kept reverse-biased, or at least out of the

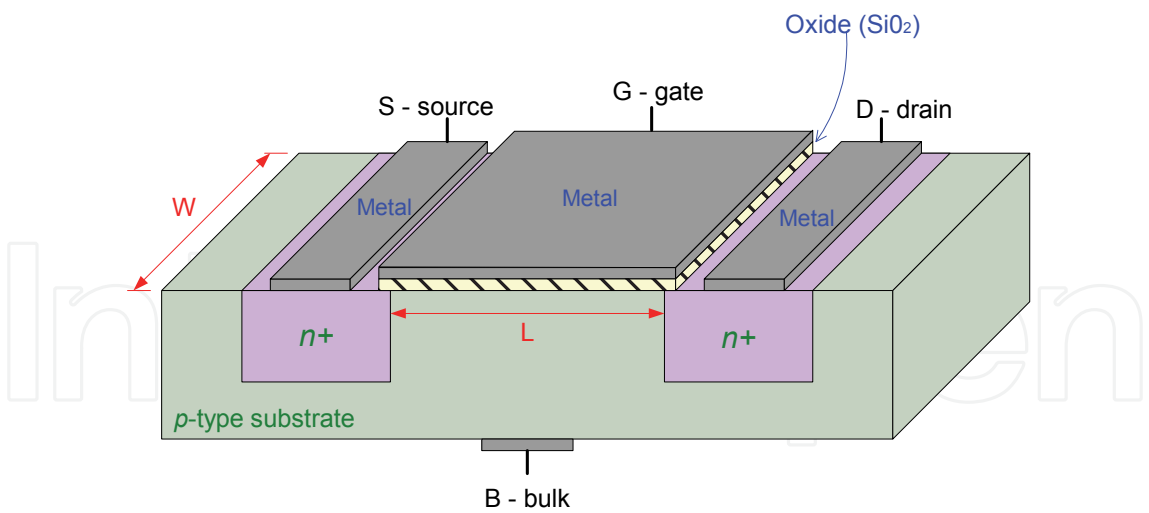


Fig. 1. Physical structure of an *n*MOS transistor.

forward condition all the time. Since the drain is biased at a positive voltage, it is only necessary to connect the bulk to the ground in order to keep both junctions cut off. With no bias applied to the gate, there are two back-to-back diodes between drain and source, and consequently, there is no current. This is true since each *pn* junction forms a diode. In fact, the resistance between drain and source under this circumstance is in the range of  $10^{12}\Omega$ .

When a positive voltage is applied between gate and source -  $v_{GS}$ , holes (which are positively charged) are repelled from the surface of the substrate. As the voltage increases, the surface becomes completely depleted of charge. The voltage at which this occurs is known as threshold voltage -  $V_t$ .

If  $v_{GS}$  is further increased, electrons (which are negative charges) accumulate near the surface, under the gate, and an *n* region is created, thus forming a channel between drain and source, as indicated in Fig. 2. The channel was formed by inverting the substrate surface from *p* type to *n* type. Fig. 2 also shows the depletion region that forms around the channel and the two junctions.

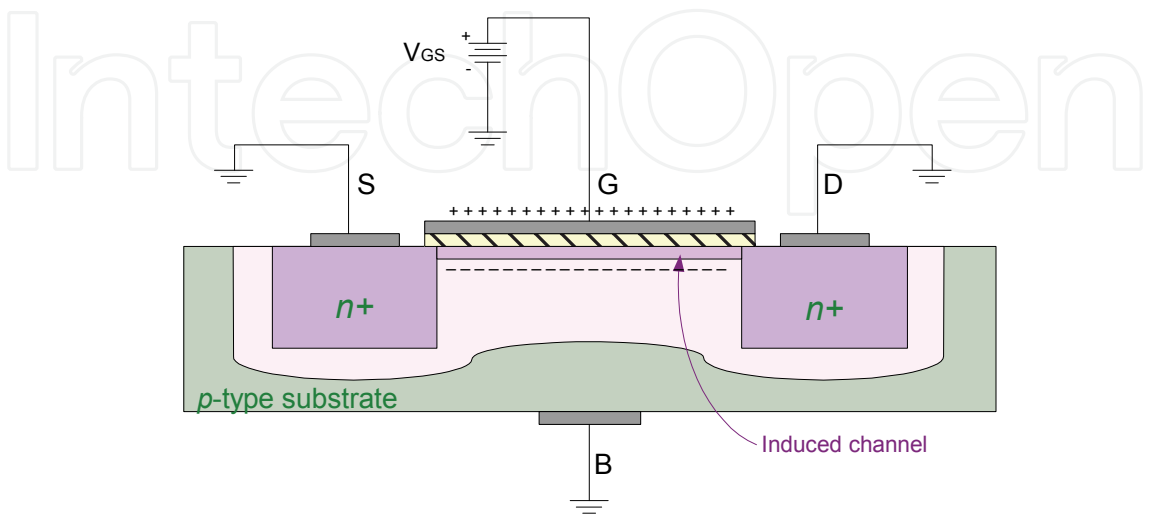


Fig. 2. *n*MOS with an induced channel.

The symbols for the  $n$ MOS transistor are given in Fig. 3, although other symbols may be found in the literature. The symbol in Fig. 3.a corresponds to the four terminal connection, and the symbol in Fig. 3.b corresponds to the three terminal connection, where source and substrate are shorted.

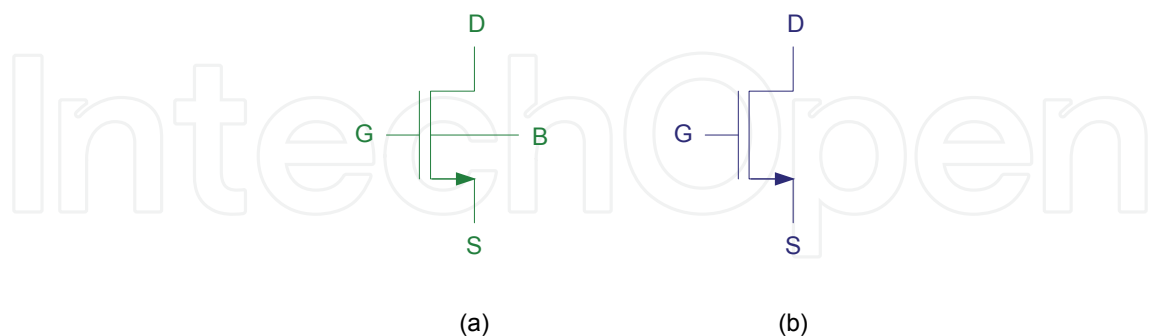


Fig. 3. Symbols for  $n$ MOS transistor; (a) four terminals and (b) three terminals.

## 2.2 Triode condition

Now, if a very small voltage  $v_{DS}$  is applied between drain and source, as indicated in Fig. 4, there will be a current flow through the channel. The current through the channel, named drain current -  $i_D$  is directly dependent on the voltage  $v_{GS}$  and the voltage  $v_{DS}$ . If  $v_{GS}$  increases, the channel becomes deeper and more current can flow. If  $v_{DS}$  is increased, based on Ohm's Law, there will be more current, since the channel behaves as a resistance. It follows that the transistor is operating as a linear resistance whose value is controlled by  $v_{GS}$ . The resistance is very high for  $v_{GS} \leq V_t$  and it decreases as  $v_{GS}$  increases. This condition of operation is known as ohmic, linear or triode.

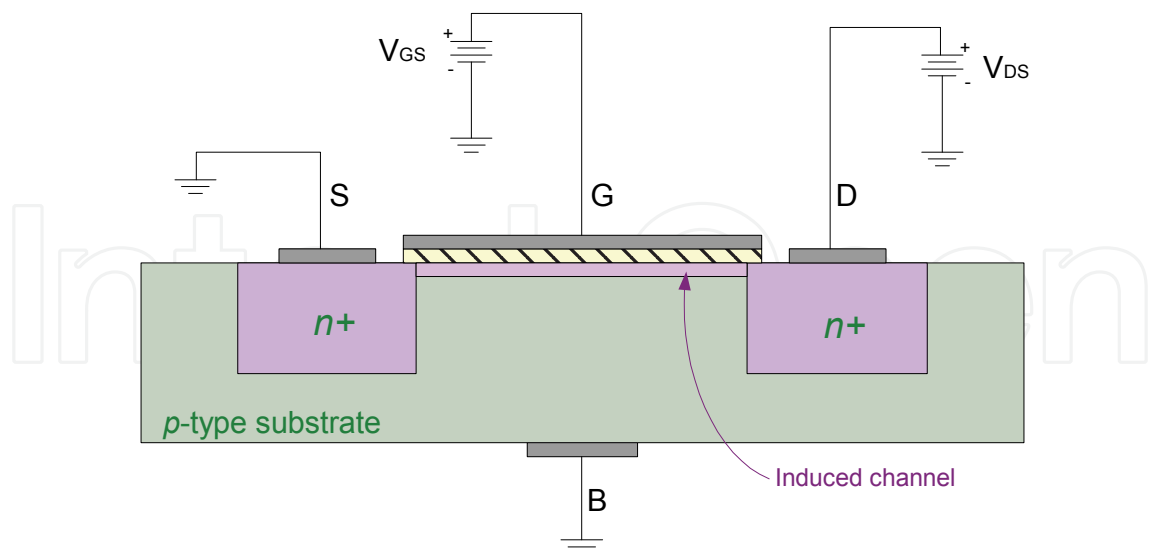


Fig. 4. Conduction under very small  $v_{DS}$ .

## 2.3 Saturation condition

As  $v_{DS}$  increases, the difference  $v_{DS} - v_{DS}$  becomes smaller at the edge between the gate and the drain diffusion, and therefore the channel becomes shallow. Therefore, the channel

assumes a tapered shape, as indicated in Fig. 5. Since the channel becomes smaller at the drain end, its resistance increases, and therefore, the transistor does not operate ideally as a linearly controlled resistor.

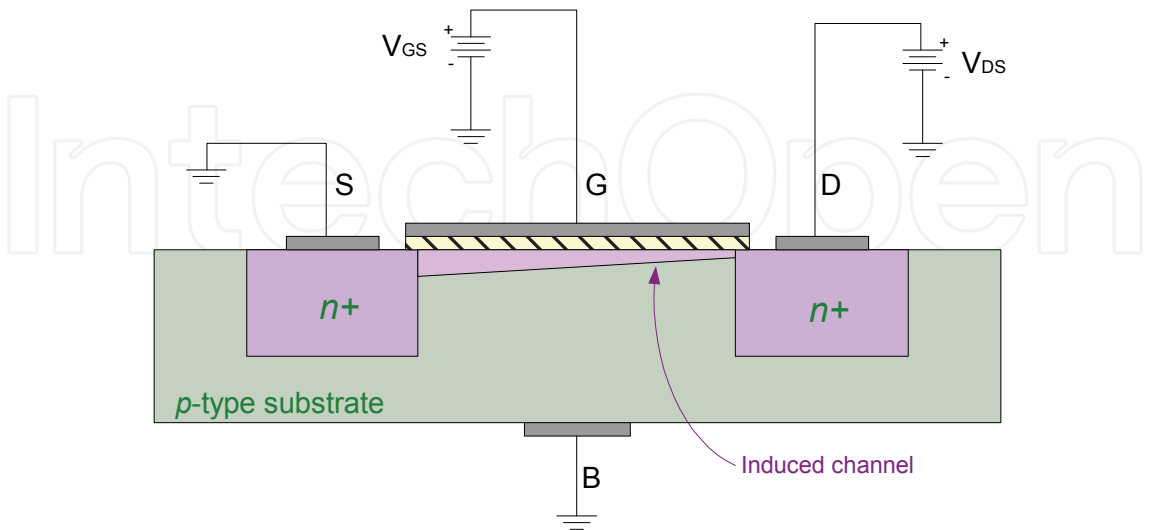


Fig. 5. Conduction under  $0 < v_{DS} < v_{GS} - V_t$ .

At the condition  $v_{DS} = v_{GS} - V_t$ , the channel ceases to exist at the drain side, as shown in Fig. 6. This situation is known as pinch off. At this point, further increases in  $v_{DS}$  moves the end of the channel further away from the drain, as presented in Fig. 7. This condition of operation is referred as saturation, therefore  $v_{DS}$  is referred as  $v_{DSSAT} = v_{GS} - V_t$ .

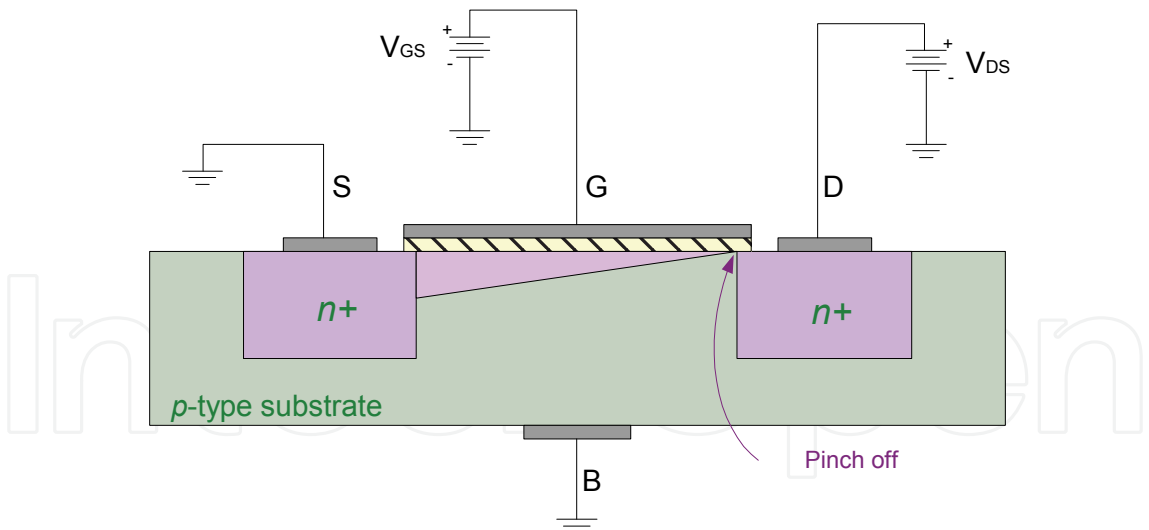


Fig. 6. Conduction under  $v_{DS} = v_{GS} - V_t$ .

Once the transistor enters the saturation region of operation, the drain current  $i_D$  becomes independent of the  $v_{DS}$ . Fig. 8 summarizes the conditions of operation of an  $n$ MOS transistor. Close to  $v_{DS} = 0$ , current  $i_D$  is directly proportional to  $v_{DS}$ , with slope proportional to  $v_{GS} - V_t$ . As  $v_{DS}$  approaches  $v_{DS} = v_{GS} - V_t$ , the curve of bends because the channel resistance increases. After the  $v_{DS} = v_{GS} - V_t$ , the current becomes independent of  $v_{DS}$ .

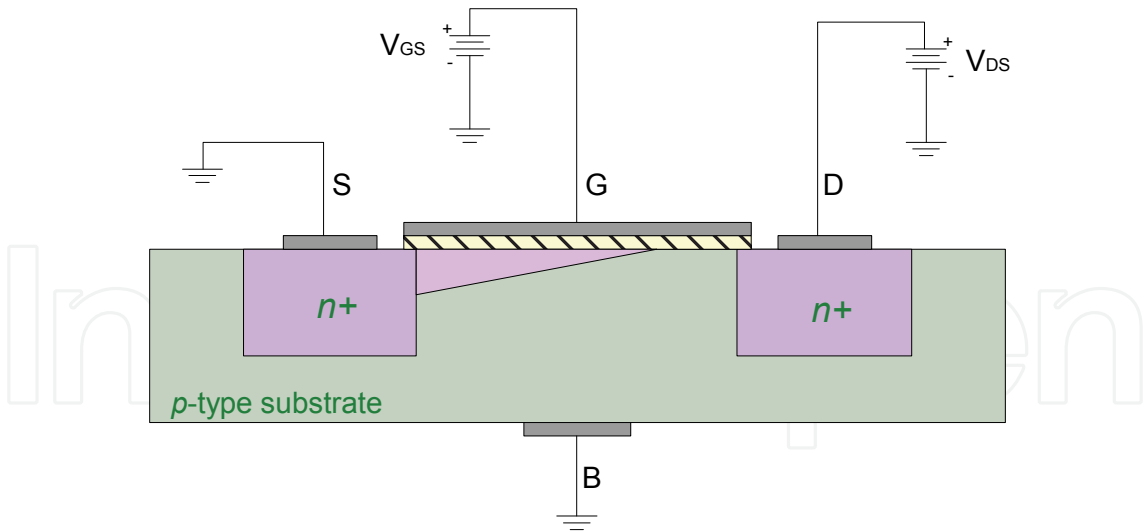


Fig. 7. Conduction under  $v_{DS} > v_{GS} - V_t$ .

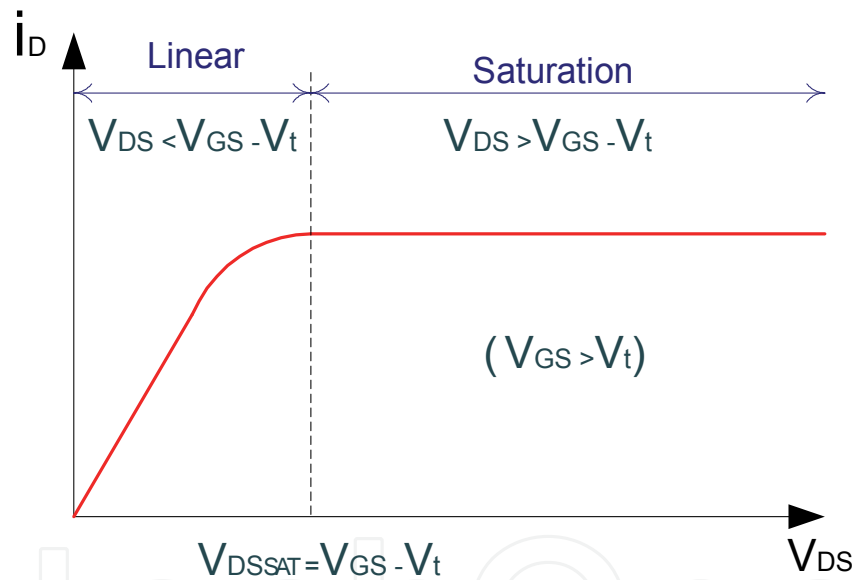


Fig. 8. Operation condition of an *n*MOS transistor.

2.4 Deriving the  $i_D - v_{DS}$  relationship

Consider the biasing depicted in Fig. 9. Since the channel potential varies from zero at the source to  $v_{DS}$  at the drain, the local voltage difference between gate and the channel varies from  $v_{GS}$  to  $v_{GS} - v_{DS}$ . Therefore, the channel density, or charge per unit length, is given as:

$$Q_d(x) = WC_{ox}[\mathcal{V}_{GS} - \mathcal{V}(x) - V_t] \tag{1}$$

where  $v(x)$  is the potential at  $x$  and  $C_{ox}$  is the capacitance, per unity area, formed by the gate and the channel.

Since, by definition, current is proportional to charge times velocity, and considering the current is the same along the channel, then:

$$i_D = -WC_{ox}[\mathcal{V}_{GS} - \mathcal{V}(x) - V_t]v \quad (2)$$

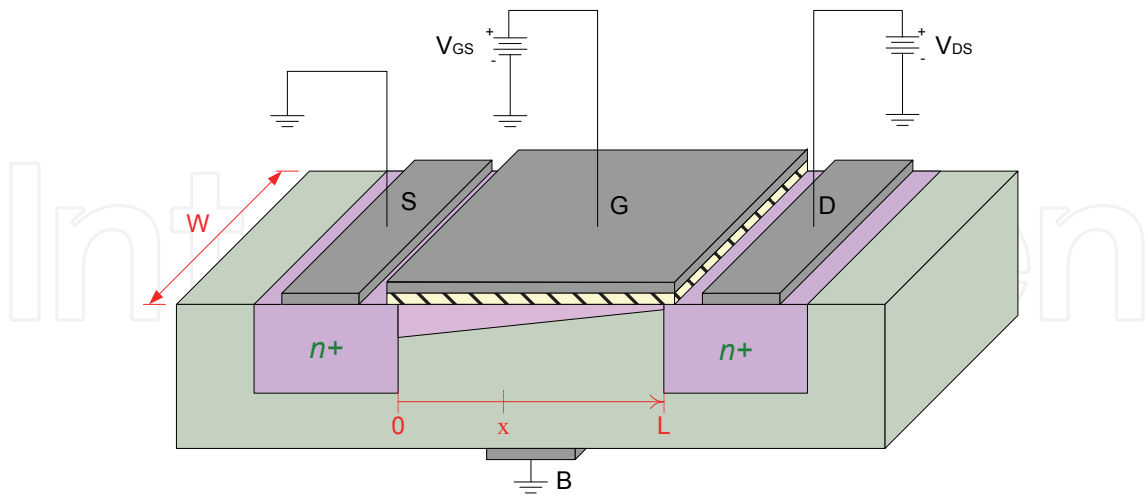


Fig. 9. Biasing of an *n*MOS.

The minus signal is due to the negative charge of electrons. The velocity of carriers at low fields is the product of mobility ( $\mu$ ) and the electric field ( $E$ ). Noting that  $E(x) = -dV / dx$  and representing the electrons mobility by  $\mu_n$ , then expression (2) can be rewritten as:

$$i_D = WC_{ox}[\mathcal{V}_{GS} - \mathcal{V}(x) - V_t]\mu_n \frac{dV(x)}{dx} \quad (3)$$

Now integrating along the channel, one obtains:

$$\int_0^L i_D dx = \int_0^{V_{DS}} WC_{ox}[\mathcal{V}_{GS} - \mathcal{V}(x) - V_t]\mu_n dV(x) \quad (4)$$

Thus, the expression for the drain current in the triode region is:

$$i_D = \mu_n C_{ox} \frac{W}{L} [(\mathcal{V}_{GS} - V_t)\mathcal{V}_{DS} - \frac{\mathcal{V}_{DS}^2}{2}] \quad (5)$$

The value of the current for the saturation operation can be obtained by replacing  $v_{DS} = v_{GS} - V_t$  into expression (5), as:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\mathcal{V}_{GS} - V_t)^2 \quad (6)$$

As described earlier, the current does not depend on  $v_{DS}$ . It can be observed from expressions (5) and (6) that the current is proportional to the ratio  $W / L$ , which is known as the aspect ratio. The designer can alter the aspect ratio to obtain the desired  $i$ - $v$  characteristic.

Observe that expression (6) was obtained using the value of  $L$ , as given in Fig. 9. Nevertheless, when the transistor is saturated, the channel becomes shorter, as shown in Fig. 7. A reduction in the length of the channel, known as channel length modulation, means a variation in the resistance, and therefore a variation in the current  $i_D$ .

Expression (6) can be modified in order to include the variation in the channel length, represented as  $L-\Delta L$ , as:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - \Delta L} (\mathcal{V}_{GS} - V_t)^2 \quad (7)$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{1}{1 - (\Delta L / L)} (\mathcal{V}_{GS} - V_t)^2$$

which can be approximated to:

$$i_D \cong \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( 1 + \frac{\Delta L}{L} \right) (\mathcal{V}_{GS} - V_t)^2 \quad (8)$$

Since  $\Delta L/L$  is proportional to  $v_{DS}$  (the larger  $v_{DS}$  the larger will be  $\Delta L$ ), then:

$$i_D \cong \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\mathcal{V}_{GS} - V_t)^2 (1 + \lambda \mathcal{V}_{DS}) \quad (9)$$

where  $\lambda$  is the parameter of proportionality.

The effect of channel length modulation can be seen in the  $i_D - v_{DS}$  characteristic of a MOS transistor shown in Fig. 10. The dependence of  $v_{DS}$  on  $i_D$  in the saturation region can be seen is represent by  $(1 + \lambda \mathcal{V}_{DS})$  in expression (9) and can be observed in Fig. 10.

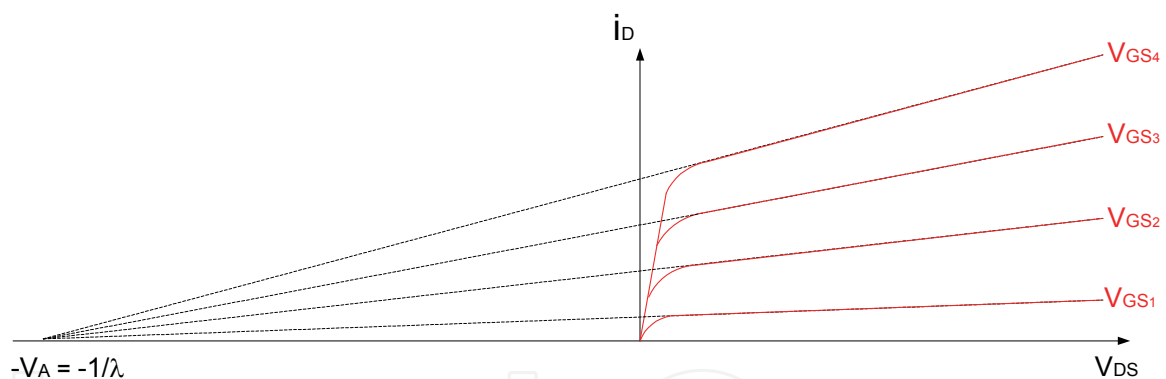


Fig. 10. Effect of channel modulation on saturation current.

An extrapolation of  $i_D - v_{DS}$  intercepts the  $v_{DS}$  axis at  $v_{DS} = -V_A$ , known as Early voltage. For a given process,  $V_A$  is proportional to  $L$ , selected by the designer. Typically,  $V_A$  is in the range of 5 V/ $\mu\text{m}$  to 50 V/ $\mu\text{m}$ .

## 2.5 Output resistance

Fig. 10 and expression (9) show that an increase in  $v_{DS}$  causes an increase in  $i_D$ , meaning a resistive behavior. The value of the resistance is given as:

$$r_o = \left[ \frac{\partial i_D}{\partial \mathcal{V}_{DS}} \right]^{-1} = \left[ \lambda \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\mathcal{V}_{GS} - V_t)^2 \right]^{-1} \quad (10)$$

which can be simplified to:



$$r_o = \frac{1}{\lambda i_D} = \frac{V_A}{i_D} \quad (11)$$

Therefore, a MOS transistor in the saturation region is not totally independent of  $v_{DS}$  and presents an output impedance given by (11)

Considering the transistor operating in the triode region, as given by expression (5), if the value of  $v_{DS}$  is sufficiently small,  $v_{DS}^2$  can be neglected, and therefore:

$$i_D \cong \mu_n C_{ox} \frac{W}{L} [(v_{GS} - V_t) v_{DS}] \quad (12)$$

This relationship represents the behavior of the MOS transistor as a linear resistance whose value is controlled by  $v_{GS}$ , as given by:

$$r_{ds} = \frac{v_{DS}}{i_D} = [\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)]^{-1} \quad (13)$$

## 2.6 Transconductance

The large signal behavior of a MOS transistor in the saturation region is given by expression (6). Nevertheless, for a given biasing, the designer may be interested in the small signal behavior of the transistor. For a given small variation in the  $v_{GS}$ , around the biasing, there will be a variation in the  $i_D$  current, given by the transconductance, as:

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}} \quad (14)$$

which results in:

$$g_m = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) \quad (15)$$

Observe the transconductance depends on the ratio  $W/L$  and on the value of  $v_{GS}$ , and they can be controlled by the designer. By using expression (6), then expression can be written as:

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} i_D} \quad (16)$$

In this case, the transconductance depends on the ratio  $W/L$  and the  $i_D$  current. That expression can be written also as:

$$g_m = 2 \frac{i_D}{(v_{GS} - V_t)} \quad (17)$$

It clearly does not depend on ratio  $W/L$  but it depends on both  $v_{GS}$  and  $i_D$ .

## 2.7 Body effect

In many circuits, the substrate and the source are not at the same potential, as it is possible to stack transistors. In that case, the substrate it is at lower potential than the source, and

therefore the source-substrate junction becomes reversed biased. This reverse biasing widens the depletion layer, which in turn reduces the channel depth.

The effect of the bulk-source voltage  $V_{SB}$  can be easily represented by a change in the threshold voltage -  $V_t$ , as given by:

$$V_t = V_{t0} + \gamma [\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}] \quad (18)$$

where  $V_{t0}$  is the threshold voltage for  $V_{SB} = 0$ ,  $\phi_f$  is a physical parameter (usually  $2\phi_f = 0.6V$ ) and  $\gamma$  is a fabrication-process parameter given by:

$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \quad (19)$$

where  $q$  is the electron charge ( $1.6 \times 10^{19} C$ ),  $N_A$  is the doping concentration of the substrate and  $\epsilon_s$  is the permittivity of silicon ( $1.17\epsilon_0 = 1.17 \times 8.854 \times 10^{-14} = 1.04 \times 10^{-12} F/cm$ ).

Any signal between substrate and source promotes a drain current component. The substrate acts as a second gate, and in turn will present a corresponding transconductance, named body transconductance, given as:

$$g_{mb} = \left. \frac{\partial i_D}{\partial V_{DS}} \right|_{\substack{V_{GS}=V_{GS} \\ V_{BS}=V_{BS}}} \quad (20)$$

From expressions (6), (17) and (18), then it is possible to state that:

$$g_{mb} = \chi g_m \quad (21)$$

where  $\chi$  is given by:

$$\chi = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} \quad (22)$$

And it is in the range of 0.1 to 0.

## 2.8 Small signal model

Considering the output impedance, the transconductance and the body effect, the small signal model of a  $n$ MOS transistor is given by Fig. 11, known as hybrid- $\pi$  model.

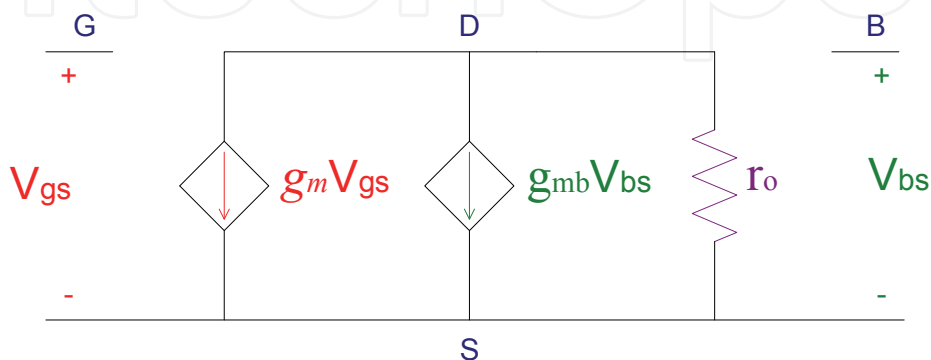


Fig. 11. Hybrid- $\pi$  model.

If the source and the substrate are at the same potential, then the model can be simplified, as the term  $g_{mb}v_{bs}$  goes to zero. The simplified hybrid- $\pi$  model is shown in Fig. 12.

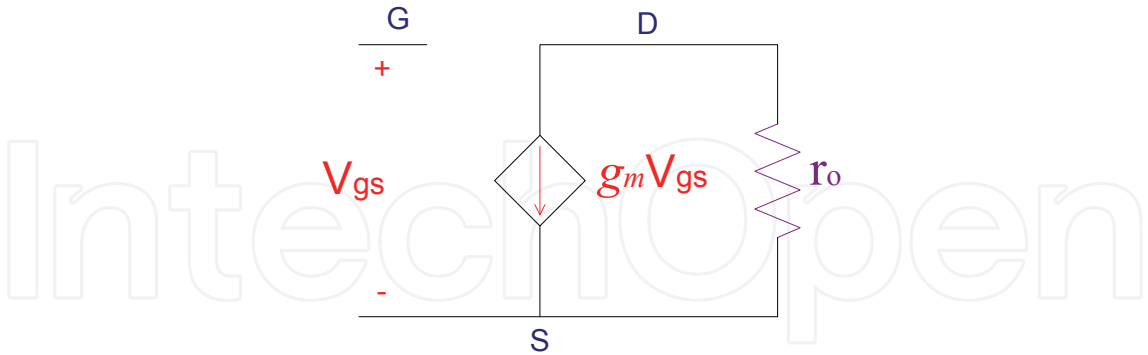


Fig. 12. Simplified hybrid- $\pi$  model.

2.9 Summary

Table 1 summarizes the main  $n$ MOS equations.

Saturation	Condition	$v_{DS} \geq v_{GS} - V_t$
	$i$ - $v$ characteristic	$i_D \cong \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2$
	Output resistance	$r_o = \frac{1}{\lambda i_D} = \frac{V_A}{i_D}$
	Transconductance	$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} i_D}$ $g_m = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)$ $g_m = 2 \frac{i_D}{(v_{GS} - V_t)}$
	Body transconductance	$g_{mb} = \chi g_m = \frac{\gamma}{2 \sqrt{2 \phi_f + V_{SB}}} g_m$
Triode	Condition	$v_{DS} < v_{GS} - V_t$
	$i$ - $v$ characteristic	$i_D = \mu_n C_{ox} \frac{W}{L} [(v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2}]$
	Output resistance	$r_{linear} = \frac{v_{DS}}{i_D} = [\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)]^{-1}$
	Threshold voltage	$V_t = V_{t0} + \gamma [\sqrt{2 \phi_f + V_{SB}} - \sqrt{2 \phi_f}]$

Table 1. Summary of  $n$ MOS equations.

2.10  $p$ MOS transistor

In a  $p$ MOS transistor, a  $p$  channel is formed on an  $n$  substrate. Therefore, its operation is virtually the same as the  $n$ MOS transistor, except that all voltages and currents are opposite

as in the  $n$ MOS transistor. Fig. 13 shows the symbols for the  $p$ MOS transistor, although other symbols may be found in the literature. The symbol in Fig. 13.a corresponds to the four terminal connection, and the symbol in Fig. 13.b corresponds to the three terminal connection, where source and substrate are shorted.

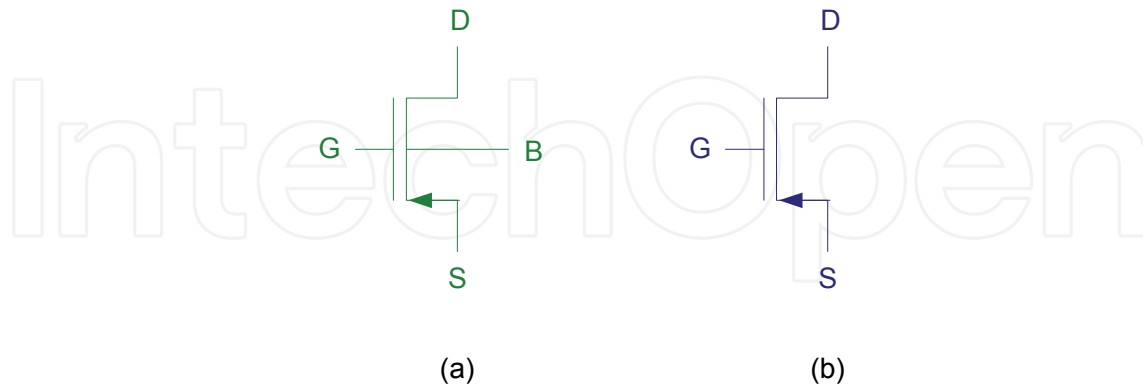


Fig. 13. Symbols for  $p$ MOS transistor; (a) four terminals and (b) three terminals.

### 3. RF CMOS model

Unfortunately, the structure and the operation of a MOS transistor present parasitic capacitances that limit its frequency of operation. The parasitic capacitances may result from the capacitor formed between the gate and the channel, between gate and source/drain, and between drain/source and substrate.

#### 3.1 Gate capacitances

The gate, the dielectric and the channel form a capacitor. When the transistor is working in the triode region with a small voltage  $v_{DS}$ , the channel will be of uniform depth, as shown in Fig. 4. Therefore, the gate-channel capacitance can be considered equally divided between the source and the drain, and their values are:

$$C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox} \text{ (triode region)} \quad (23)$$

When the transistor is working in the saturation region, the channel presents a tapered shape and it is pinched off at the drain end, as presented in Fig. 7. It can be seen that the gate to channel capacitance is almost entirely modeled at the source, since the drain does not present a channel. It can be shown that the capacitances are:

$$\begin{aligned} C_{gs} &= \frac{2}{3} WLC_{ox} \text{ (saturation region)} \\ C_{gd} &\approx 0 \end{aligned} \quad (24)$$

If the transistor is cut off, there is no capacitance between gate and channel, since there is no channel for cut off. The entire capacitance is then between the gate and the substrate, therefore:

$$\begin{aligned} C_{gs} &= C_{gd} = 0 \text{ (cut off)} \\ C_{gb} &= WLC_{ox} \end{aligned} \quad (25)$$

As can be observed from Fig. 1, the gate extends over the drain and the source areas. Therefore, there is an overlapping capacitance between the gate and the drain/source. Denoting the overlapping length by  $L_{ov}$ , then the overlap capacitance can be seen to be:

$$C_{gs_{ov}} = C_{gd_{ov}} = WL_{ov}C_{ox} \quad (26)$$

For modern processes,  $L_{ov}$  is usually in the range of 5% to 10% of  $L$ .

### 3.2 Junction capacitances

As shown by Fig. 2 there are two reversed biased junctions formed between the substrate and source/drain. Each junction consists of two semiconductors (drain/source and the substrate) and the depletion layer, thus forming a capacitor. The source-substrate capacitance can be found to be:

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \quad (27)$$

where  $V_0$  is the junction built-in voltage (0.6 V to 0.8 V),  $V_{SB}$  is the magnitude of the reversed bias voltage and  $C_{sb0}$  is the capacitance at zero reverse bias voltage.

By the same way, the drain-substrate capacitance is given by:

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} \quad (28)$$

### 3.3 The high frequency model

The small signal model of the MOS transistor given in Fig. 11 can be update to include the gate and the junction capacitances, as presented in Fig. 14. Although this model represents the transistor for high frequencies, it is very complex for manual analysis.

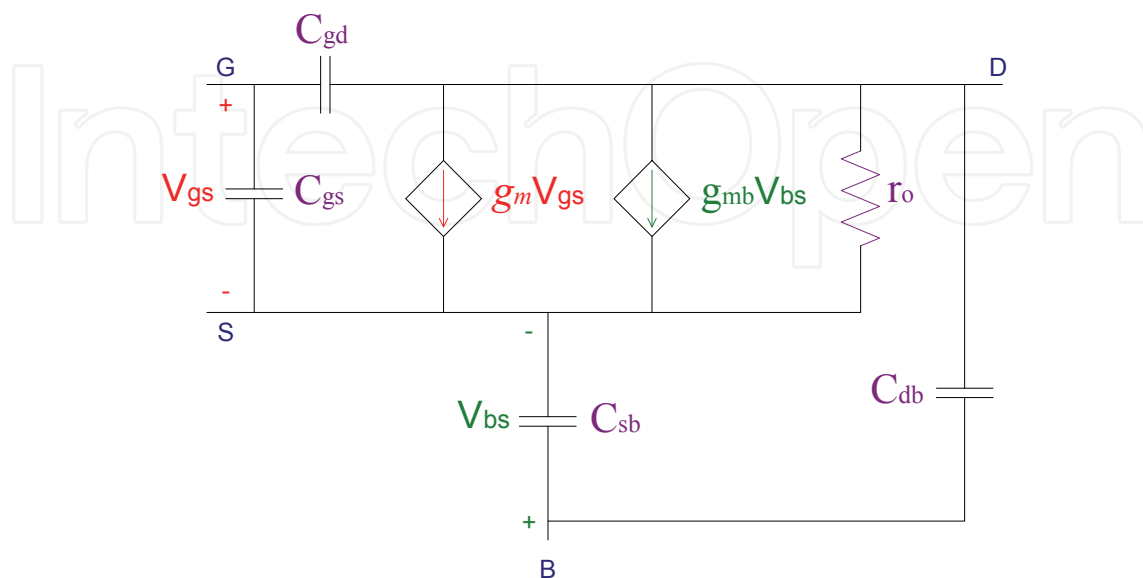


Fig. 14. Hybrid-π model including the parasitic capacitances.

If the source and the substrate are shorted, the model can be greatly simplified, as shown in Fig. 15.

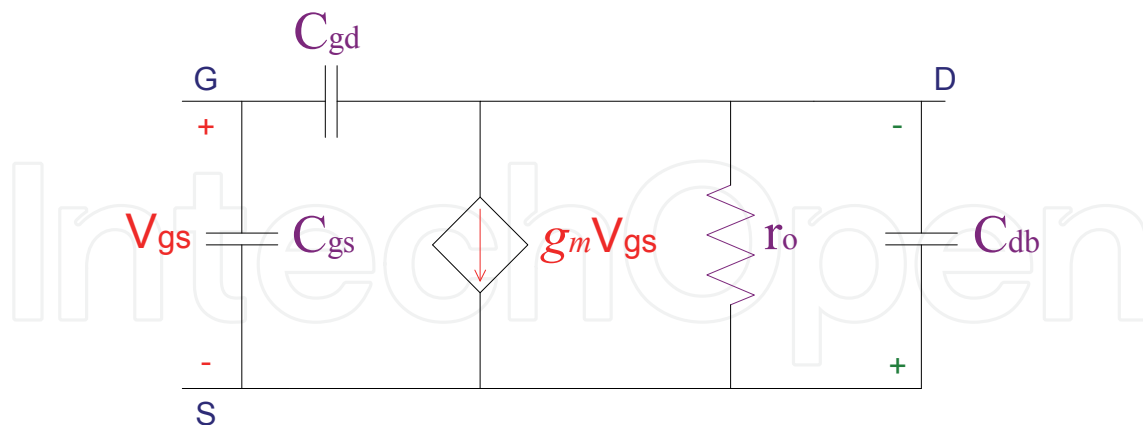


Fig. 15. Simplified high frequency model for source and substrate shorted.

#### 4. Unity gain frequency

An important Fig. of merit for the MOS transistor is the unit gain frequency that is defined as the frequency in which the short circuit current gain becomes unit. This definition is based in the common source configuration, as shown in Fig. 16.

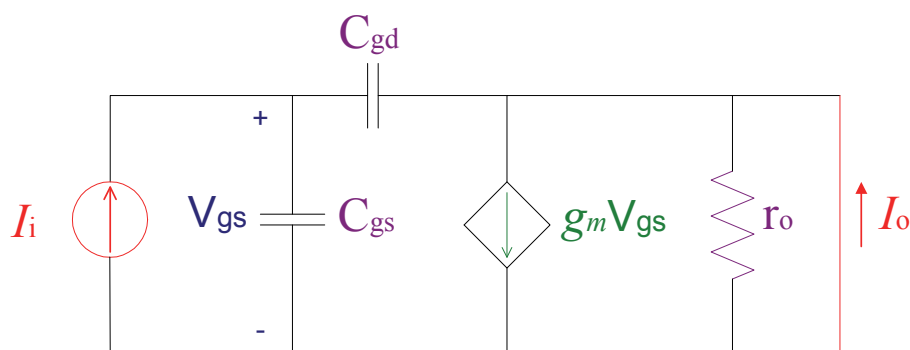


Fig. 16. Circuit model used to obtain the unit gain frequency.

The current  $I_o$  in the short circuit is given by:

$$I_o = g_m V_{gs} - sC_{gd} V_{gs} \cong g_m V_{gs} \quad (29)$$

The approximation is due to the fact that  $C_{gd}$  is very small and can be neglected. Also, from the circuit,  $V_{gs}$  can be expressed as:

$$V_{gs} = \frac{I_i}{s(C_{gs} + C_{gd})} \quad (30)$$

Therefore, from expressions (29) and (30):

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})} \quad (31)$$

Since the magnitude of  $I_o/I_i$  should be 1, as per definition, and considering physical frequencies ( $s=j\omega$ ), then:

$$\omega_T = \frac{g_m}{(C_{gs} + C_{gd})} \quad (32)$$

Therefore, the unit gain frequency is:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (33)$$

As can be observed, the unit gain frequency is directly proportional to  $g_m$  and inversely proportional to the internal capacitances. Therefore, in terms of frequency response the transistor should have large  $g_m$  and small capacitances.

#### 4. RF CMOS noise model

The two most important types of noise in MOS devices are the  $1/f$  noise and the thermal noise.

##### 4.1 Thermal noise

The main source of thermal noise in a MOS transistor is due to the resistive channel in the active region, and has a value of:

$$i_d^2 = 4kT\gamma g_m \quad (34)$$

where  $k$  is the Boltzmann's constant (about  $1.38 \times 10^{-23}$  J/K),  $T$  is the absolute temperature in kelvins and  $\gamma$  is a constant that is approximately  $2/3$  for long channel transistors and increase to the range  $1-2$  for short channel devices.

The other source of thermal noise is the gate. Fluctuation in the channel potential couples capacitively into the gate terminal, which in turn translates into a noise gate current. Noise gate current can also be produced by the resistive material of the gate. This total noise gate can be ignored at low frequencies but becomes significant at high frequencies as it is the case of RF circuits. It has been shown the gate noise may be expressed as:

$$i_g^2 = 4kT\delta g_g \quad (35)$$

where  $\delta$  is approximately  $4/3$  for long channel transistors and increase to the range  $2-4$  for short channel devices, and  $g_g$  is given by:

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_m} \quad (36)$$

Mostly of the time, instead of using a current source at the gate, it is more convenient to consider an equivalent voltage source. The equivalent voltage source of expressions (31) and (32) is given by:

$$v_g^2 = 4kT \delta r_g \quad (37)$$

where  $r_g$  is given by:

$$r_g = \frac{1}{5g_m} \quad (38)$$

#### 4.2 1/f noise

The  $1/f$  noise, also known as flicker noise or pink noise, arises mainly due to the surface imperfections that can trap and release charges. Since MOS devices are naturally surface devices, they produce much more  $1/f$  than bipolar devices (which are bulk devices). This noise is also generated by defects and impurities that randomly trap and release charges. The trapping times are statistically distributed in such a way that lead to a  $1/f$  noise spectrum.

The  $1/f$  noise can be modeled by a voltage source in series with the gate, of value:

$$v_f^2 = \frac{\beta}{WLC_{ox}f} \quad (39)$$

For  $p$ MOS devices,  $\beta$  is typically about  $10^{-28}C^2/m^2$ , but it can be up to 50 times larger for  $n$ MOS devices.

As can be observed from expression (53), the  $1/f$  noise is smaller for larger devices. This occurs because the large capacitance smoothes the fluctuation in the channel charge. Therefore, in order to achieve good  $1/f$  performance, larger devices should be used.

The  $1/f$  can also be modeled as a current source at the drain whose value is:

$$i_f^2 = \frac{\beta g_m^2}{WLC_{ox}^2 f} \cong \frac{\beta}{f} \omega_T^2 A \Delta f \quad (40)$$

where  $A$  is the area of the gate.

#### 4.3 Noise model

The noise model of an  $n$ MOS transistor is presented in Fig. 17, where the transistor is considered noiseless. The decision of placing the noise sources as a voltage source at the gate, or as a current source at the drain is just a matter of convenience according to the circuit under analysis. As an example, the values of Fig. 17 could be:

$$\begin{aligned} v^2 &= v_g^2 = 4kT \delta r_g \\ i^2 &= i_d^2 + i_f^2 = 4kT \gamma g_m + \frac{\beta g_m^2}{WLC_{ox}^2 f} \end{aligned} \quad (41)$$

### 5. Conclusions

The proper understanding of physical operation to modeling of CMOS transistors is essential to the analysis and design of RFID circuits. Among its advantages, the CMOS transistors demands lower power consumption than other transistors.

Noise analysis of CMOS transistors is also fundamental to analysis and design of any circuit, including RFID.



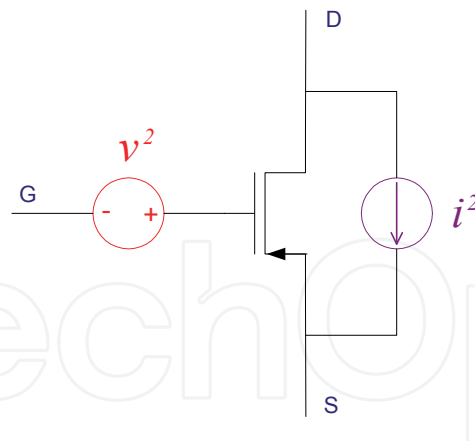


Fig. 17. Noise model of an  $n$ MOS transistor.

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With the increased adoption of RFID (Radio Frequency Identification) across multiple industries, new research opportunities have arisen among many academic and engineering communities who are currently interested in maximizing the practice potential of this technology and in minimizing all its potential risks. Aiming at providing an outstanding survey of recent advances in RFID technology, this book brings together interesting research results and innovative ideas from scholars and researchers worldwide. Current Trends and Challenges in RFID offers important insights into: RF/RFID Background, RFID Tag/Antennas, RFID Readers, RFID Protocols and Algorithms, RFID Applications and Solutions. Comprehensive enough, the present book is invaluable to engineers, scholars, graduate students, industrial and technology insiders, as well as engineering and technology aficionados.

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