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Solitary Electromagnetic Waves Generated by the Switching Mode Circuit

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1. Introduction

The switching mode circuit (SMC) performs by the switching transistor or the other switching devices. Usually, unlike the distorted continuous signal voltage on the linear circuit, the signal voltage of the SMC has two stationary states. The SMC has been applied widely to the power circuit and the signal circuit including the digital circuit now. The performance of the SMC has been supported by the improvement of the semiconductors. For example, the International Technology Roadmap for Semiconductors (ITRS) is showing the details of the technology trend of the worldwide semiconductors [1]. According to the ITRS, the technology about the high performance system on a chip (SoC) or the VLSI has been improved to 45*nm* from 78*nm* in the last five years. However the gate delay of the PMOS FET stays between 1.65*ps* and 1.73*ps*, and is increasing slightly. In addition, the improvement of the on-chip clock frequency is staying in 5-6*GHz* approximately. Many results of the research about the on-chip interconnect were presented [2, 3]. The themes of these studies are the influence of the resistance, the parasitic capacitances, the power noise, the substrate noise, and others to the performance of the SoC [4, 5]. Meanwhile, the on-chip transmission line interconnect [6, 7] and the optical interconnect [8] were proposed for improving the performance of the SoC. Many results of the study of the power distribution network (PDN) about the EMI also were presented [9-14]. The relevant papers which include above ones and the conventional theories were discussed from the point of view of the stagnation of the performance of the SoC and the suppression of the EMI of the SMC. Concurrently, the development of the theory and the technologies suitable to the SMC was started. As a result, the solitary electromagnetic wave (SEMW) theory and the technologies of the low impedance lossy line (LILL) and the matched impedance lossy line (MILL) were successfully developed. These are presented below together with the result of the analysis, experiments, and the review of the conventional theory and engineering.

2. Review of the conventional theories and engineering

2.1 EMW theory

The EMW theory is the most trusted fundamental theory for the AC circuit including the SMC. It was presented by James Clerk Maxwell in 1873 and the existence of the EMW was first confirmed experimentally by H. R. Hertz in 1888. This theory was based on the vector EMW equation. The vector EMW equation has been developed by fusing the Maxwell's

theory and the undulation equation. The undulation equation handles the continuous wave and it was presented by Jean Le Rond d'Alembert in 1750. In 1881, Oliver Heaviside replaced the electromagnetic potential field by the force field and simplified the complexity of Maxwell's theory to four differential equations which are known now as Maxwell's laws or Maxwell's equations.
Maxwell's vector EMW equations in vacuum are

$$\nabla^2 \dot{E} - \mu_0 \varepsilon_0 \frac{\partial^2 \dot{E}}{\partial t^2} = 0 \,,\ \nabla^2 \dot{H} - \mu_0 \varepsilon_0 \frac{\partial^2 \dot{H}}{\partial t^2} = 0 \tag{1}$$

The traveling speed of the EMW is

$$c = 1/\sqrt{\mu_0 \varepsilon_0} \tag{2}$$

In (2), c corresponds to the velocity of the light in vacuum.
When the EMW is vibrating at a constant angular velocity, the modified (1) is

$$\dot{E} = i\sqrt{2}E_o \cos\left\{\omega\left(t \mp z\sqrt{\mu_o \varepsilon_o}\right) + \theta\right\},\ \dot{H} = \pm j\sqrt{2}H_0 \sqrt{\frac{\varepsilon_o}{\mu_o}} \cos\left\{\omega\left(t \mp z\sqrt{\mu_o \varepsilon_o}\right) + \theta\right\} \tag{3}$$

where i is the unit vector of the standard transverse direction against the traveling direction, j is the unit vector of the perpendicular direction to the standard transverse direction.
According to (3), the EMW consists of the electric field wave and the magnetic field wave. These waves are at right angles to each other and both wave shapes are same except its magnitude.
The alternate current (AC) circuit is defined by the electromagnetism as the circuit of the EMW because the electric field and the magnetic field are vibrating on it. According to the Ampère's circuital law, the AC is the integrated magnetic field around a closed loop to the conductor. The vibrating magnetic field forms the magnetic wave which constitutes the EMW. The EMW can travel at near speed to the light through the insulator of the transmission line. The EMW cannot travel through the conductor. The skin depth causes the attenuation when the EMW travels on the transmission line. It shows the sinking degree of the electric field or the magnetic field into the conductor.
The quasi-stationary state is one of the definitions in the electromagnetism. The EMI is negligible when the length of all wires in the circuit is quite shorter than the wave length. Such AC circuit can be handled as the quasi-stationary closed circuit (QSCC).
The EMW theory handles the continuous wave as shown in (3). Therefore, the Fourier transform is necessary to analyze the distorted EMW. It is believed that the signal voltage wave of the SMC consists of many harmonic waves by the idea of the Fourier transform. It's very convincing mathematically. However, the following serious problems will be caused when it is applied to the SMC. That is, though the wave shape of the signal voltage of the SMC has two stationary states obviously, the stationary state got from the Fourier transform is only one. Furthermore, the timing information of the intermittent signal wave on the SMC is lost.

2.2 AC circuit theory

The Kirchhoff's circuit law is one of the most important laws in the AC circuit theory. It was presented in 1845. The principle of superposition which is based on this law is quite convenient for analyzing the complex AC circuit. The AC circuit theory is the basic theory of

the simulation program with integrated circuit emphasis (SPICE) which is used for the design and analysis of the AC circuit all over the world. It includes HSPICE, PSPICE, and XSPICE. The SPICE has been used also for the design and the analysis of the SMC for a long time.
The lumped element model is used in this theory. The lumped element model consists of 4 kinds of elements which are the inductance (*L*), capacitance (*C*), resistance (*R*), and conductance (*G*). Each element is formed as the component usually and functions independently from the electromagnetic phenomenon in the circuit.
Fig. 1 shows the transmission coefficient (S_{21}) when the capacitor and the short circuit are connected to the transmission line. They were measured by the network analyzer.

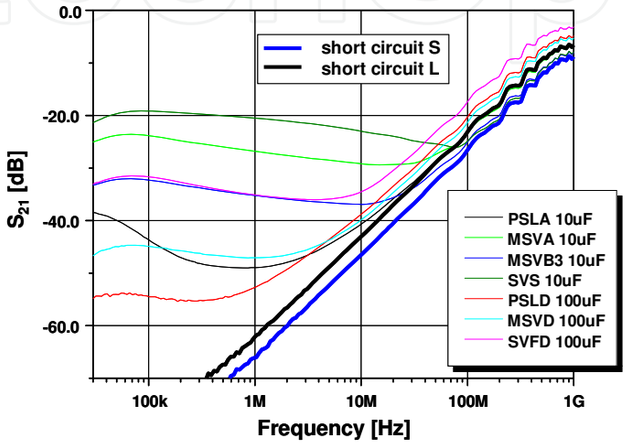


Fig. 1. Measured S_{21} of the transmission line

The small tantalum capacitors of 10μF and the large tantalum capacitors of 100μF were mounted on the coplanar line S and the coplanar line L each, the characteristic impedance of each coplanar line was 50Ω, each short circuit S and short circuit L were formed by shorting the pads for the capacitor on the coplanar line S and the coplanar line L.
In Fig. 1, each S_{21} of the small tantalum capacitor and large tantalum capacitor are approaching to S_{21} of the short circuits S and short circuits L at the frequency which is more than 10 *MHz*.
The transmission coefficient of the transmission line when the capacitor connected in parallel with it is

$$S_{21} = \frac{2Z_C}{2Z_C + Z_0} \tag{4}$$

where $Z_C=(2\pi fC)^{-1}$, C is the capacitance of the capacitor, Z_0 is the characteristic impedance of the transmission cable equipped to the network analyzer.
The idea that the impedance of the capacitor can be got from (4) approximately has been believed by almost all circuit engineers as well as the capacitor manufacturers. However, this idea is not correct because the impedance of the capacitor is got from $(2\pi fC)^{-1}$ theoretically and the capacitor is used also in series to the transmission line.
S_{21} depends on the materials and the form of the transmission line. However the capacitor has not the structure of the transmission line. Therefore the capacitor which is connected to the transmission line in parallel disturbs slightly the traveling of the EMW as the short circuit in Fig. 1. The curves of S_{21} in Fig. 1 will move to the low frequency side when the capacitors are connected by the through holes to the power plane and the ground plate as

conventional instead of the coplanar. From above, it can be said that Fig. 1 and (4) show the application limitation of the Kirchhoff's circuit law as well as the principle of superposition.
According to the AC circuit theory, the current in the circuit is defined as the average speed of the electron (dq/dt) in the wire which is called the electron current hereinafter. According to the physics, dq/dt is quite small. For example, it becomes $3.68\times10^{-4}m/s$ in the case of the copper wire which has the cross-sectional area of $1mm^2$. Therefore, the electron current is valid only on the direct current (DC) circuit or the stationary circuit. The idea that one of the functions of the capacitor is charging the electron does not conform to the electromagnetism which defines it as the electrostatic energy consisting of the electric field. Nevertheless, above definition and idea will be permitted for the actual design and analysis when the AC circuit is the QSCC.
From above, it should be understood that the AC circuit theory is the theory for the QSCC. Therefore, the design and analysis by the SPICE will be available for the QSCC part of the AC circuit including the SMC without troubles. However, it has been the difficult problem how to be formed to the QSCC because the power lines and the signal lines are included in them.

2.3 Telecommunication engineering (TELE)

The TELE has been used for design of the transmission line of the SMC as well as the high–frequency AC circuit. The idea of the characteristic impedance is useful for designing of the transmission line of the SMC. The theory of the TELE is based on the telegrapher's equation and it was presented by Oliver Heaviside in 1880. The telegrapher's equation was developed by fusing the undulation equation and the AC circuit theory instead of the Maxwell's equation, because the AC circuit theory was the only theory for the electric engineers at this times. Therefore, the line current in the telegrapher's equation is the electron current. In addition, some breaches in the TELE to the EMW theory are found at the boundary of the conductor and the insulator.
Nonetheless the existence value for the design and analysis of the transmission line is not spoiled. The concept of the characteristic impedance is effective to only the useful signal wave travelling on the transmission line.

3. SEMW theory

We imagined that the SMC generates the SEMW instead of the distorted EMW. This idea will be effective for finding way out of the above mentioned stagnation of the semiconductor technologies because it will solve above mentioned serious problems caused by the application of the Fourier transform. The SEMW theory was developed by fusing the EMW theory and the NLU theory. It is also the fruits of the discussion with the co-author who graduated from the department of the physics of the university.

3.1 NLU theory

The solitary wave was found out as the great wave by John Scott Russell who was making an experiment for smoothing the run of the boat in a canal in 1834. However this discovery was not recognized by the scientist at this times. D. J. Korteweg and G. de Vries (KdV) presented the equation about the wave traveling one direction on the shallow water in 1895. The KdV equation is

$$\frac{\partial \eta}{\partial t}+\frac{3c_0}{2h}\eta\frac{\partial \eta}{\partial \xi}+\frac{c_0h^2}{6}\frac{\partial^3 \eta}{\partial \xi^3}=0 \tag{5}$$

where η is the altitude from the average surface of the water, ξ is the coordinate which is moving at the velocity of $c_0 = (gh)^{1/2}$ and, $\xi = x - c_0 t$, g is the constant of gravitation, and h is the average depth of the water.
The special solution of (5) by KdV is

$$\eta = \eta_0 \sec h^2 \left(\frac{1}{2} \sqrt{\frac{3\eta_0}{h^3}} (x - ct) \right) \tag{6}$$

$$c = c_0 \left(1 + \frac{\eta_0}{2h} \right) = \sqrt{gh} \left(1 + \frac{\eta_0}{2h} \right) \tag{7}$$

where η_0 is the magnitude of the wave.
N. J. Zabusky and M. D. Kruskal confirmed the existence of the solitary wave at the computer simulation based on the KdV equation about the heat conducting system in 1965. They discovered the following characteristics similar to the particle to the solitary wave and named it soliton.

a. Soliton travels without changing its speed and wave shape.
b. The magnitude and the speed of the soliton are not influenced by crossing.
c. When the magnitude becomes larger, the wave length becomes smaller and the traveling speed becomes faster.

3.2 Generation mechanism of the SEMW

The SoC consists of the on-chip inverters which are formed by the NMOS FET and the PMOSFET. The PMOS FET leads the switching motion of the CMOS circuit when it turns on. On the other hand, the NMOS FET leads the switching motion of the on-chip inverter when it turns off.
According to the semiconductor physics [15] and the ITRS, the saturation drain current of the MOS FET at the voltage higher than V_T is

$$I_{dsat} = A \cdot I_{dsat,p} \cdot (V_g - V_{T,sat}) \Big/ z \left(V_{dd} - V_{T,sat} \right) \tag{8}$$

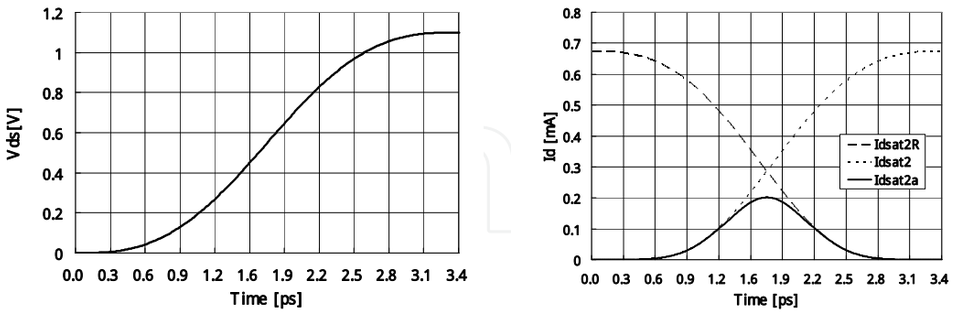
where, A is the conversion coefficient, V_{dd} is the supply voltage, $I_{dsat,p}$ is the peak saturation drain current of the MOS FET, $V_{T,sat}$ is the saturation threshold voltage, z is the gate width, V_T is the threshold voltage, and V_g is the gate voltage.
The drain current of the MOS FET at up to the saturation threshold voltage is

$$I_d = \left(I_{sd \cdot leak} / z \right) \cdot V_g / V_{dd} \tag{9}$$

where $I_{sd\ leak}$ is the subthreshold leakage current.
The drain current increases in response to the half of VDD ($1.1V$) from zero according to the curve line got from (8) and (9). The drain current decreases in response to zero from $0.55V$ according to the inverse curve line formed by (8) and (9).
The 2009 technology node of the ITRS 2008update is used at the following calculation. The calculation condition in (8) and (9) about the PMOS FET is as follows; V_{dd} is $1.1V$, $I_{dsat,p}$ is $1.317mA/\mu m$ at V_{dd}, $V_{T,sat}$ is $196mV$, $I_{sd\ leak}$ is $0.17\mu A/\mu m$ at V_{dd}, and z is $108nm$.
According to the ITRS, the voltage between drain and source (V_{ds}) is

$$V_{ds} = \frac{1}{C_{ox}} \int_0^{2T_1} I_{dsat1a} dt \tag{10}$$

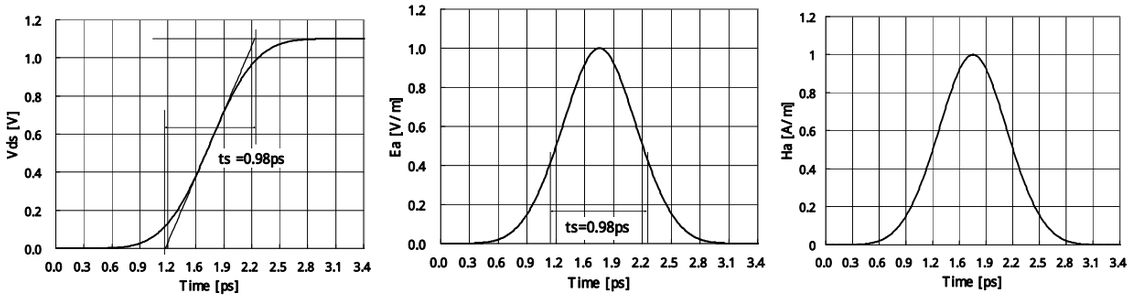
T_1 is 1.7*ps* which is got from (10) when V_{ds} is 0.55V, C_{ox} is 0.875*fF*.
Fig. 2 shows the calculated waveform of the PMOS FET. Fig. 2. a shows V_{ds1} and Fig. 2. b shows I_{dsat2a}.



a) V_{ds1} b) I_{dsat2a}

Fig. 2. Calculated waveform of the PMOS FET

In Fig. 2. a, V_{ds1} was got from (10). In Fig. 2. b, each I_{dsat2} and I_{dsat2R} was got from (8) and (9) by using the wave shape of V_{ds1} in Fig. 2. a as Vg, and the drain current I_{dsat2a} was got from merging I_{dsat2R} and I_{dsat2}. At all calculations for getting the wave shape, the vector is ignored.
Fig. 3 shows the calculated waveform of the PMOS FET on the second stage of the on-chip inverter. Fig. 3. a shows the drain-source voltage V_{ds}. Fig. 3. b shows the electric field of between the drain and the source. Fig. 3. c shows the magnetic field.



a) V_{ds} b) E_a c) H_a

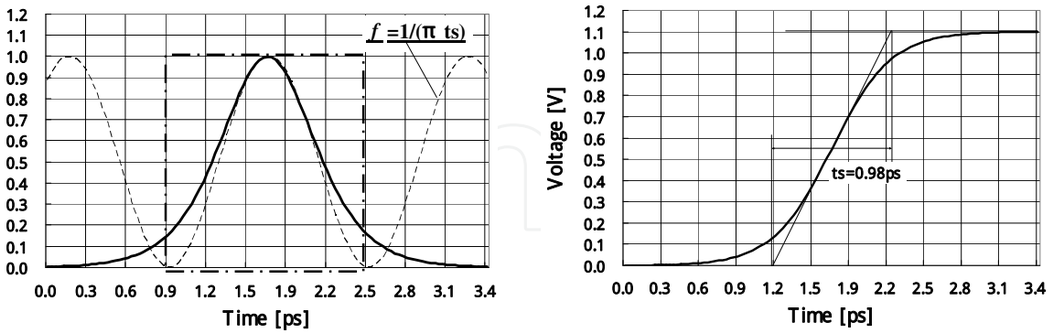
Fig. 3. Calculated waveform of the PMOS FET on the second stage of the on-chip inverter

In Fig. 3. b, E_a is the differential value of the drain-source voltage V_{ds} according to the definition of the voltage potential in the electromagnetism. In Fig. 3. c, and H_a is got from the drain current I_{dsat2a} by applying the Ampère's law. Each peak value of E_a and H_a was set to 1 and the actual peak values of them depend on the parameters of the formation and the materials of the PMOS FET.
According to (1), the changing electric field and the magnetic field form the EMW and traveling. Therefore both E_a and H_a should be form to a kind of the EMW.
The EMW is the field free from the mass. When the EMW is applied to (6), the equation of the soliton is

$$u(t) = A \cdot \sec h^2\left(B\left(t - T_1\right)\right) \tag{11}$$

where A is the magnitude of the wave, B is the constant of the wave shape.

Fig. 4. shows the calculated result about the soliton. Fig. 4. a shows the wave shape of the soliton calculated by (11) when T_1 = 1.7*ps*, A = 1, and B = 20.55. Fig. 4. b shows the integral wave shape of the soliton in Fig. 4. a.



a) Wave shape of the Soliton b) Integral wave shape of the soliton

Fig. 4. Calculated result about the soliton

In Fig. 4. a, the calculated soliton wave is similar to E_a and H_a in Fig. 3. In the calculation, t was set to 3.4*ps* from 3.7*fs*. In Fig. 4. b, the maximum magnitude was set to 1.1*V* and the calculated soliton wave is similar to the wave shape in Fig. 3. a. The wave shapes in Fig. 4. a and Fig. 4. b are formed by one switching action by the PMOS FET. Therefore, unlike the Gaussian wave, no harmonic waves can be included in these wave shapes. Therefore, we named them the SEMW. The generation mechanism of the SEMW is similar to the great wave which was observed by John Scott Russell. In addition, it is also similar to the generation mechanism of the tsunami which was recognized as a kind of the soliton.
According to (3), the vector wave equations of the SEMW on the transmission line is

$$\dot{E} = i\sqrt{2}E_o \sec h^2\left(B\left(\ t \mp z\sqrt{\mu\varepsilon}\right) + T_1\right),\ \dot{H} = \pm j\sqrt{2}\sqrt{\frac{\varepsilon}{\mu}} \sec h^2\left(B\left(\ t \mp z\sqrt{\mu\varepsilon}\right) + T_1\right) \tag{12}$$

where i is the unit vector of the standard transverse direction against the traveling direction, j is the unit vector of the perpendicular direction to the standard transverse direction, μ is the dielectric constant, ε is the permeability, z is the travelling distance, and T_1 is the initial value of time.
According to (12), the SEMW consists of the solitary electric field wave (SEW) and the solitary magnetic field wave (SMW) and these waves are at right angles to each other and both wave shapes are same except its magnitude.
The definition of the wave length (λ_S) of the SEMW in the SEMW theory is

$$\lambda_S = \sqrt{\mu\varepsilon}/t_S \tag{13}$$

where t_S is the specified rise time of the V_{DS} of the PMOS FET in Fig. 3. a and Fig. 3. b.
Hundreds of millions of transistors are formed in the semiconductor layer, the on-chip interconnect layers are placed on the semiconductor layer, the power supply wiring layer (PSWL) which consist of the power mesh and the ground mesh are placed on the on-chip interconnect layer in the typical SoC.
The distributed element model is not necessary for the design and the analysis of the SMC when the rise time (t_r) of the signal voltage is larger than 2.5 times of the traveling time (t_f)

on the transmission line [16]. t_r is defined the time between 10 percent and 90 percent of the final voltage. This means the SMC can be handled as the QSCC when $t_r > 2.5t_f$. λ_S on the on-chip interconnect is 179μm at the 2009 technology node of the ITRS 2008update because t_S is 0.98ps and the relative dielectric constant (ε_r) is 2.7. When all of the on-chip interconnect including the power supply wiring are shorter than 72μm, the closed SMC at this technology can be handled as the QSCC.

In Fig. 4, the sine-wave having the frequency of $(\pi t_S)^{-1}$ is shown. The idea about the significant frequency (SF) was presented [17]. This idea cannot be directly applied to the SEMW theory because it has been discussed about the harmonic waves.

The properties of the modified significant frequency (MSF) which is defined according to the SEMW theory are as follows;

a. The correlation of the time domain wave shape of the SEMW and half wave shape of the sine-wave having the frequency of $(\pi t_S)^{-1}$ is about 85%.
b. No spectra exist except the MSF.

As the result, both frequency analysis and time analysis of the SMC become easy by the idea of the MSF.

The calculation time to get the wave shapes of Fig. 3 was about ten hours by using the desktop computer. The calculation to get the wave shapes of the next stage of the inverter was not finished during one week. On the other hand, the calculation to get the wave shapes of Fig. 4 was finished at once. Therefore, the design and analysis will quicken when the SEMW theory is applied to the SMC.

By the way, conventionally, I_{dsat2a} corresponding to H_a in Fig. 3. c has been recognized as the penetrating current. This current has been hated conventionally because this induces a brief spike in power consumption and becomes a serious issue at high-frequencies. However, according to the SEMW theory, this current or magnetic field is necessary to form the signal and its magnitude should be designed suitably.

3.3 Behaviours of the SEMW on the transmission line

Fig. 5 shows the equivalent circuit of the SMC including the on-chip inverter.

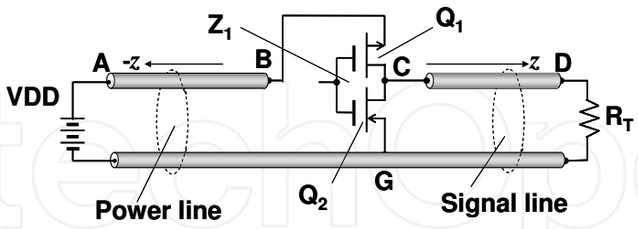
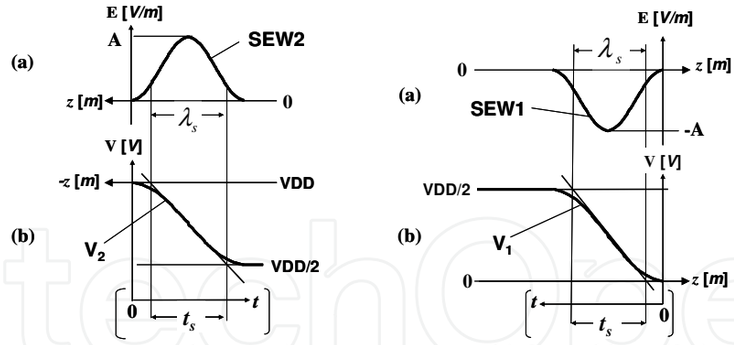


Fig. 5. Equivalent circuit of the SMC including the on-chip inverter

In Fig. 5, VDD is the ideal DC voltage source, Z_1 is the on-chip inverter formed by one stage, however it is formed by several stages in actual use, Q_1 is the PMOS FET, Q_2 is the NMOS FET, R_T is the terminating resistor, "0" is the state that Q_1 is OFF and Q_2 is ON, "1" is the inverse state of it, and VDD supplies VDDV.

A couple of the SEMW is generated when the inverter Z_1 changes to "1" from "0" or the inverter Z_1 changes to "0" from "1". The SEMW travels in the insulator of the transmission line at $\varepsilon_r^{-1/2}$ of the light speed. The normal SMC is a kind of the voltage source circuit. The SEW acts as the leading player in such circuit.

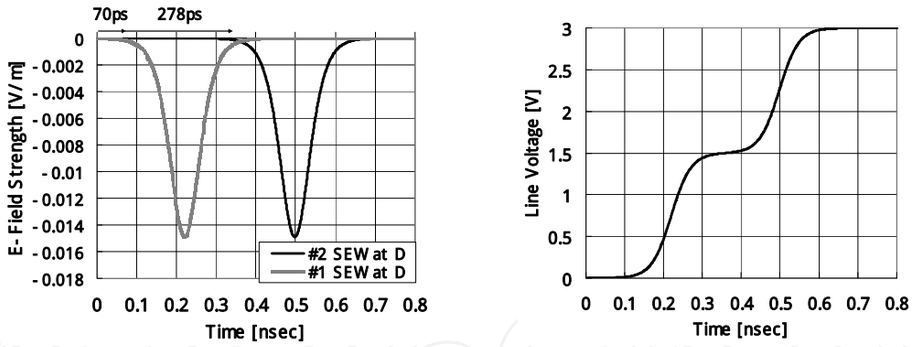
Fig. 6 shows the wave shapes of the SEW and the voltage on the transmission line.



a) Power line (PL) b) Signal line (SL)

Fig. 6. Wave shapes of the SEW and the voltage on the line

In Fig. 6, z shows the traveling direction of the SEW, t shows the time direction which is opposite direction to z, a. (a) shows the SEW2 on the power line (PL), a. (b) shows the falling part of the voltage on the PL, b. (a) shows the SEW1 on the signal line (SL), b. (b) shows the rising part of the voltage on the SL. The SEW1 travels on the SL with charging to 0.5VDDV from 0V and the SEW2 travels on the PL with discharging to 0.5VDDV from VDDV. When the PL has the infinite length or the matched termination, the voltage on the SL and PL remains the half of the source voltage as shown in (b) of Fig. 6. However, the voltage on the SL and PL should reach VDDV finally because the output impedance of VDD is zero.
Fig. 7 shows the calculated wave shapes of the SEW and the rising part of the signal voltage at the point D in Fig.5.



a) SEW b) Signal voltage

Fig. 7. Calculated wave shapes

In Fig. 5 and Fig. 7, the calculation condition is as follows; the gate delay of the inverter is 200ps, ε_r is 4.35, each length of the SL and the PL is 10mm and 20mm, the calculated delay time till the point D from the point C is 70ps, and the calculated delay time till the point A from the point B is 139ps. The generated #1 SEW reaches to the point D after the delay of 70ps. The generated #2 SEW reaches to the point D after the delay of 348ps, because the #2 SEW travels on the PL and it reflects at the point A. The signal voltage is got by the integral of the #1 SEW and #2 SEW because it is formed by charging of the SL by the #1 SEW and #2 SEW. From above, it is clarified that the signal voltage reaches to VDDV from the 0.5VDDV by the reflected SEW generated on the PL and the rise time of the signal depends on length of the PL.
It has been considered conventionally that the low output impedance of the voltage source is effective for only keeping the magnitude of the signal. However, by the SEMW theory, it

is clarified that both low impedance of the voltage source and the short length of the PL are necessary to keep the signal integrity of the SMC.
The SEMW theory first clarified the existence of three kinds of the current on the SMC. The current observed on the transmission line is the first current to follow the Ampère's law. This current has the same wave shape as the SEMW. When the electrostatic energy is taken out from the power source, the current which follows the Ampère's law flows and it is the second current. The magnitude of this current is decided by the source voltage and the characteristic impedance of the transmission line. The electron current for the matched termination resistance flows whenever the SL is being charged. This is the third current.
Te reflection or the bounce on the transmission line of the SMC has been analyzed by using the method of the lattice diagram currently, which has the other names such as the bounce diagram, the echo diagram, or the reflection diagram. This method has been used widely for the design and analysis of the SMC [18]. However this method cannot handle the electromagnetic phenomenon. The SEMW theory enables the analysis of the reflection or the bounce from the point of view of the electromagnetism easily.

3.4 Simulation of the influence of the length of the PL

Fig. 8 shows the equivalent circuit for simulation by HSPICE.

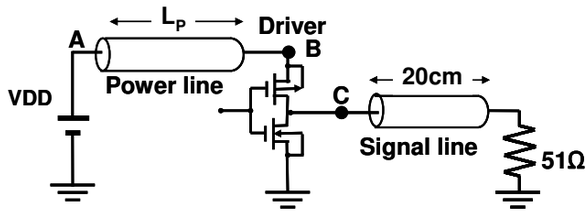
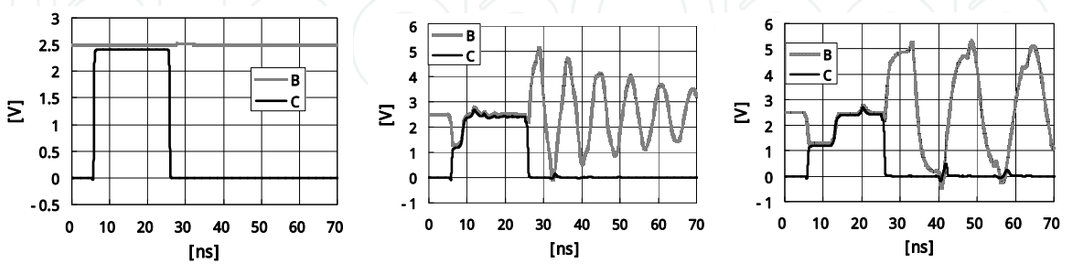


Fig. 8. Equivalent circuit for simulation

In Fig. 8, VDD is the ideal DC voltage source and the out-put voltage is 2.5V. The driver was described by the sub-circuit depending on the design parameter. The calculated characteristic impedance of the PL and the SL were 51.28Ω, which was got from ApsimRLGC®. The simulation result will be reliable in spite of the HSPICE because the lossless transmission line is used.
Fig. 9 shows the simulated voltage of the point B and C at the varied length of the PL.



a) 0cm b) 20cm c. 50cm

Fig. 9. Simulated signal voltage depending on each length of the PL

In Fig 9, the rise time does not increase from the gate delay when the length of the PL is zero and it increases in proportion to the length of the PL, the voltage at the point B in Fig. 8 is vibrating after the turn-off of the driver when the length of the PL is not zero.

When the PL has the length and the electron current exists on the SL, the static magnetic energy exists on the SL and the PL. In this situation, the SEMW is generated on the PL and the SL at the turn-off motion of the driver. The generation of the SEMW on the PL is caused to the electron current on the PL. The SEMW generated on the SL travels to the matched termination and is consumed. However, the SEMW generated on the PL shuttles between the point A and the point B. As the result, the voltage at the point B vibrates.

4. LILL technologies

When the ideal voltage source is located near the on-chip inverter on the PL, it is expected that the rise time of the signal will become close to the gate delay of the on-chip inverter. The vibration on the PL will not occur because the termination resistance does not exist in the SoC. The capacitor cannot function as ideal voltage source. It is caused by the structure of the capacitor which is not the transmission line. When the transmission line has the low impedance and the large loss, this transmission line which was named LILL will be able to function as the ideal voltage source. To get the cooperation from the semiconductor industries is necessary to actualize the on-chip LILL. However, unfortunately the EMW theory and the transmission line technologies are not being applied to their current design rule of the SoC. Therefore, the first development of the LILL was started from the on-board LILL.

4.1 On-board LILL technologies

Many spectra are observed on the board as well as on the chip. They are not caused by the harmonics based on the Fourier transform but are caused by many reflections and many repetitions of the SEMW. The frequency of these many spectra is lower than the MSF.
When the LILL is connected to the power terminal of the SoC closely, the LILL provides the ideal DC source to the SoC and it reflects the EMW including the SEMW at the power terminal. As the result the stability of the SoC will be improved and the EMI on the board will be suppressed. The electromagnetic susceptibility also will be improved by it because it is well known that many troubles of the SoC are caused by the EMW which comes through the PDN. However the rise time of the on-chip inverter will not be shortened enough.
The on-board LILL is most useful when the on-chip LILL technologies are not applied to the SoC and other ICs.

4.1.1 Necessary decoupling performance

All on-chip inverters are connected to the PL in parallel. Therefore, it can say that the PDN causes the EMI. Fig. 10 shows an example of the power current of the DDR2 dual-in-line memory module (DDR2 DIMM).
In Fig. 10, the x-axis shows the frequency allocated to $1GHz$ from $10MHz$ on the log scale, the y-axis shows the S_{21} allocated to $120\text{dB}\mu A$ from $-40\text{dB}\mu A$ on the linear scale. The power current of the DDR2 DIMM was measured by the committee members by using the setup for the kit-module in the rule of VCCI [19]. The magnetic probe which was standardized by IEC in "magnetic probe method" was used for this measurement.
The measured maximum current was $78\text{dB}\mu A$ or $7.9mA$ at $140MHz$. The power of it is $0.31mW$ because the measured input impedance was 5Ω at $140MHz$.
The electric field strength at the distance r from the antenna when the EMW of P watt is radiated from the antenna [20] is

$$E = \frac{7\sqrt{P}}{r} \quad [V/m] \tag{14}$$

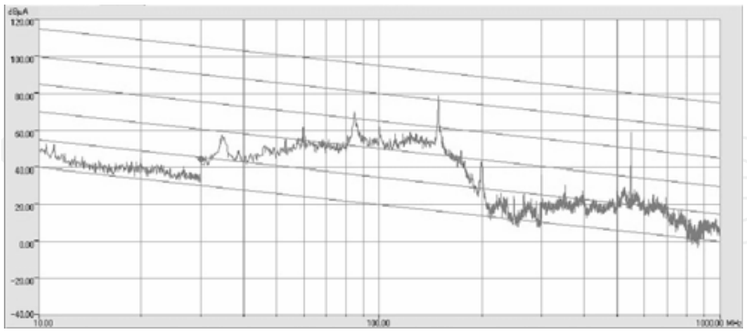


Fig. 10. Measured power current of the DDR2 DIMM

According to the IEC CISPR22, the limit of the electric field at 140MHz from the class B information technology equipment (ITE) is 30dB$\mu V/m$ at the distance of 10m. From (15), E is 12.4mV/m or 82dB$\mu V/m$ when p is 0.31mW. The DRAM module including the DDR2 DIMM is known as one of the devices which cause the interference. Therefore, the attenuation of the power decoupling is hoped to be more than 50dB at 140MHz.

4.1.2 Necessary value of the terminal impedance

The characteristic impedance of the on–board LILL should be small enough than it of the on-chip interconnect.
Fig. 11 shows the analyzing model of the on-chip interconnect as the transmission line.

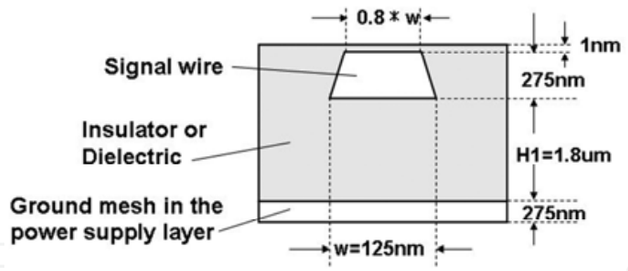


Fig. 11. Analyzing model of the on-chip interconnect

In Fig. 11, this model was formed by quoting the data of the 2006TN in the ITRS 2005. Each ε_r and tanδ of the insulator is 3.2 and 0.001. The simulated characteristic impedance by ApsimRLGC® was 148.5Ω at 200GHz and 143Ω at 1THz. According to the MSF, 200GHz corresponds to the switching time of 1.59ps and 1THz corresponds to the switching time of 0.32ps. The simulated characteristic impedance by MW STUDIO® was 10Ω approximately. When characteristic impedance was calculated by the conventional microstrip equation in TELE, it was 177Ω. When ε_r is 3.2, the intrinsic impedance of the insulator is 210Ω. The characteristic impedance is not defined by the conventional EMW theory. From above, we decided that the conventional equation is most reliable.
As the result, the minimum characteristic impedance of the on-chip interconnect and the PSWL was estimated to 177Ω.

4.1.3 Development of the equation for getting the characteristics

Fig. 12 shows the cross-section of the chip of the on-board LILL.

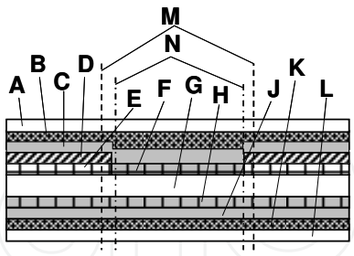


Fig. 12. Cross-section of the chip of the on-board LILL

In Fig. 12, the cross-section view is common to the two sides of the chip. A and L are the silver coating layers, A is the cathode and L is the anode, B and K are the carbon graphite layers, C and J are the conductive polymer layers, E is the etched layer of the aluminum without the conductive polymer, F and H are the etched layer including the conductive polymer, and G is the aluminum layer, N is the boundary of the available chip, and M is the line for cut. D is the masking layer to keep the insulation between the aluminum layer and the conductive polymer layer at the cut surface.

The equations have been improved through prototyping of many numbers of times till now. The extension ratio of the etching layer is

$$k = \frac{C_1 \cdot a}{\varepsilon_0 \varepsilon_r \cdot 2 \cdot 10^{-4}} \tag{15}$$

where C_1 is the capacitance of the capacitor which is made of the etched aluminum foil of $1cm^2$, a is the thickness of the alumina layer on the etching surface.

The impedance of the capacitance of the chip is

$$Z_C = \frac{10^{-4}}{2\pi f C_1 z w} \tag{16}$$

where z is the effective chip length, w is the effective chip width.

The transmission coefficient of the capacitor when it is connected to a point on the way of the transmission line is

$$S_{21C} = \frac{2Z_C}{2Z_C + Z_0} \tag{17}$$

where Z_0 is the characteristic impedance of the transmission line.

The effective thickness of the insulator layer is

$$d_e = \frac{a \cdot Z_I + b_S \cdot Z_S + b_C \cdot Z_C + b_V \cdot Z_V}{Z_I} \tag{18}$$

where each a, b_S, and b_C is the thickness of the insulator layer, the conductive polymer layer, and the effective carbon graphite layer, b_V is the equivalent thickness of the void, and each Z_I, Z_S, Z_C, and Z_V is the intrinsic impedance of the insulator layer, the conductive polymer layer, the carbon graphite layer, and the air.

The characteristic impedance of the LILL chip is

$$Z_{CI} = \sqrt{\frac{\mu_0}{\varepsilon_r \varepsilon_0}} \cdot \frac{d_e}{w \cdot R_a \cdot \sqrt{k}} \tag{19}$$

where R_a is the appearance ratio of the capacitance.
The transmission coefficient of the on-chip LILL caused by the reflection at each edge is

$$S_{21R} = \sqrt{1 - \left(\frac{Z_{CI} - Z_0}{Z_{CI} + Z_0} \right)^2} \tag{20}$$

The transmission coefficient of the on-chip LILL having the finite line length is

$$S_{21RA} = S_{21C} + {S_{21R}}^2 \tag{21}$$

The rate of the absorption loss in each material of the layer is

$$A_M = 1 - e^{\frac{-b_M}{\delta_M}} \tag{22}$$

where b_M is the thickness of each layer, and δ_M is the skin depth of each material of the layer.
The effective attenuation constant at each material of the layer is

$$\alpha_M = \frac{A_M}{2 \cdot Z_{CI} \cdot w \cdot R_a \cdot \sqrt{k} \cdot \delta_M \cdot \sigma_M} \tag{23}$$

The transmission coefficient of the LILL chip caused by the absorption loss is

$$S_{21\alpha} = e^{-\alpha_S \cdot z \cdot R_a \cdot \sqrt{k} \cdot R_S} \tag{24}$$

where a_S is the sum of a_M, and R_S is the shortening ratio by the void.
The transmission coefficient between the terminals by the effect of the surface wave coupling is

$$S_{21T} = \frac{2}{(Z_{CT}/Z_{CI}) + 2} \tag{25}$$

where Z_{CT} is the impedance of the capacitance between the terminals of the LILL.
The transmission coefficient of the LILL with the effect of the surface wave coupling is

$$S_{21} = \sqrt{(S_{21RA} \cdot S_{21\alpha})^2 + {S_{21T}}^2} \tag{26}$$

The terminal impedance of the on-board LILL is

$$Z_L = Z_C + Z_{CI} \tag{27}$$

The terminal impedance of the on-chip LILL with the effect of the surface wave coupling is

$$Z_a = Z_L \left(1 + \frac{120\pi}{1 + Z_{CT}} \right) \tag{28}$$

4.1.4 Prototyping of the on-bard LILL

The on-board LILL has been prototyped for 5 times since 2008.
Fig. 13 shows the examples of the prototype of the on-board LILL

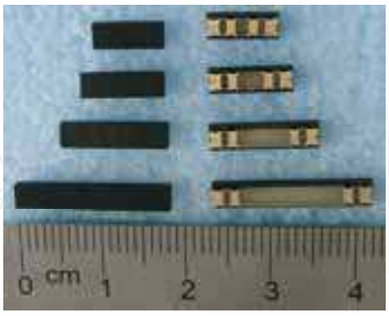
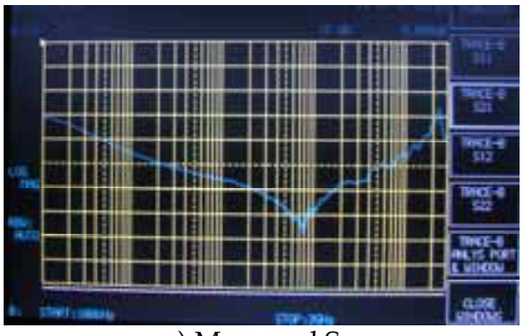
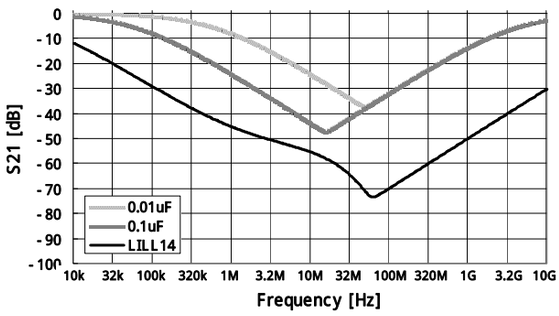


Fig. 13. Prototypes of the on-board LILL

In Fig. 13, each LILL03, LILL05, LILL08, and LILL14 has the line length of 3.5mm, 5mm, 8mm, and 14mm. The conductive polymer layer is formed in the water solution of the microscopic particles of the conductive polymer. The thickness of the chip is 200μm approximately.
Fig. 14 shows an example of the transmission coefficient (S_{21}) of the latest prototype of the LILL14. Fig. 14. a shows the measured S_{21} and Fig. 14. b shows the calculated S_{21}.



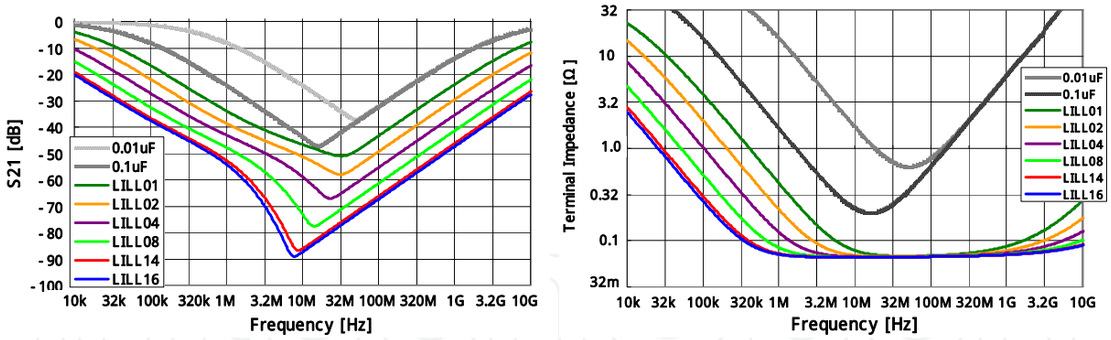
a) Measured S_{21}



b) Calculated S_{21}

Fig. 14. An example of the transmission coefficient (S_{21}) of the latest prototype of the LILL14

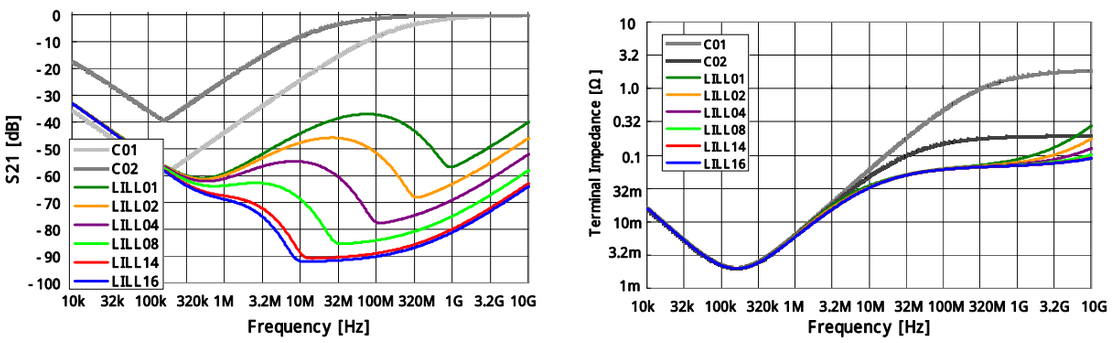
In Fig. 14. b, the calculation condition is as follows; C_1 is 33.9μF, ε_r of the alumina is 8.5, σ_S is 12,000, σ_C is 72,727, R_a is 0.8, R_S is 0.45, w is 1mm at the calculation of (16) and Z_{CI} in (23), w is 1×2mm at the calculation of Z_{CI} in (20), z is 14mm, a is 22.8nm, b_S is 1μm, b_C is 0.92μm, and b_V is 0.8μm, the capacitance for Z_{CT} is 7×10^{-17} F/m.
The calculated S_{21} well matches to the measured value.
Fig. 15 shows the calculated characteristics of the examples of the improved on-board LILL.
In Fig. 15, the calculation condition is same as the improved LILL14 in Fig. 14 except that σ_S is 12,000, b_S is 20μm, b_C is 0.46μm, the numeric following after LILL means the chip length (z). The calculation condition of the characteristics as follows; the numeric following after LILL means the chip length (z), the capacitance for Z_{CT} is 4×10^{-18} F/m, each LILL is used together with the 1mF capacitor and which are connected to the power traces of 40mm×40mm and 10mm×200mm, C01 consists of the 0.1μF capacitor and 1mF capacitor connected to the power trace of 100mm×200mm, and C02 consists of the 0.1μF capacitor and 1mF capacitor connected to the power trace of 10mm×200mm.



a) Transmission coefficient (S_{21}) b) Terminal impedance (Z_a)

Fig. 15. Calculated characteristics of the examples of the improved on-board LILL

Fig. 16 shows the calculated characteristics of the improved on-board LILL on the PCB.



a) Transmission coefficient (S_{21}) b) Terminal impedance (Z_a)

Fig. 16. Calculated characteristics of the improved on-board LILL on the actual PCB

In Fig. 16, at the frequency of lower than 10*MHz*, the decoupling performance of C01 is decuple of C02 approximately and the terminal impedance of C01 and C02 are equal. On the other hand, at the higher frequency than 1*GHz*, decoupling performance of both is zero and the terminal impedance of C01 is decuple of C02. Thus it is difficult to find the optimum solution about both decoupling performance and low impedance on the board when the capacitors are used for the decoupling circuit in the PDN. S_{21} of the LILL02 is -56dB at 140*MHz* and this value satisfies enough the hoped value which is -45dB. Z_a at 140*MHz* is small enough compared with the characteristic impedance of the on-chip interconnect or it of the PSWL.
The improved on-board LILL can decouple effectively the power source and the switching device including the SoC. The power source only provides the electrostatic energy under this situation.
Fig. 17 shows an example of the appearance of the on-board LILL for the commercialization.

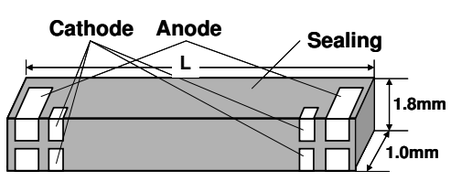


Fig. 17. Example of the appearance

In Fig.17, the improved on-board LILL is sealed by the transfer molding or other equivalent method. Each L means the sum of the chip length and 3.4*mm*. The rated voltage is 3.2*V*. The rated current is more than 10*A* and it depends on the thickness of the lead frame of the anode. The specification of the chip is corresponding to the calculation condition of Fig. 15.
Fig. 18 shows an example of the application of the on-board LILL.

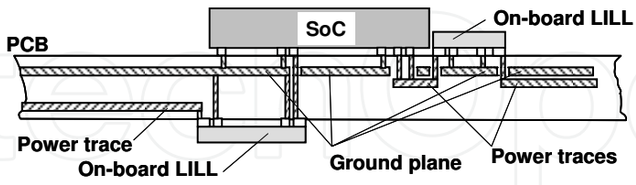


Fig. 18. Example of the application

In Fig. 18, the power traces of the supply-side should be slender because the through holes of the signal traces exist on the power traces when it is formed widely. The embedded LILL has advantage which minimizes the electromagnetic coupling between the terminals and reduces both mounting space and the manufacturing cost.

4.1.5 Comparison of the conventional decoupling components and LILL

Fig. 19 shows the appearance of the chip of the low impedance line component (LILC). The LILC was the first prototyped at NEC in 2000.

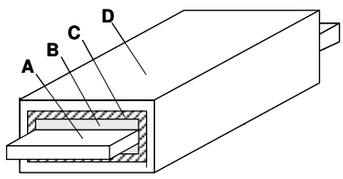
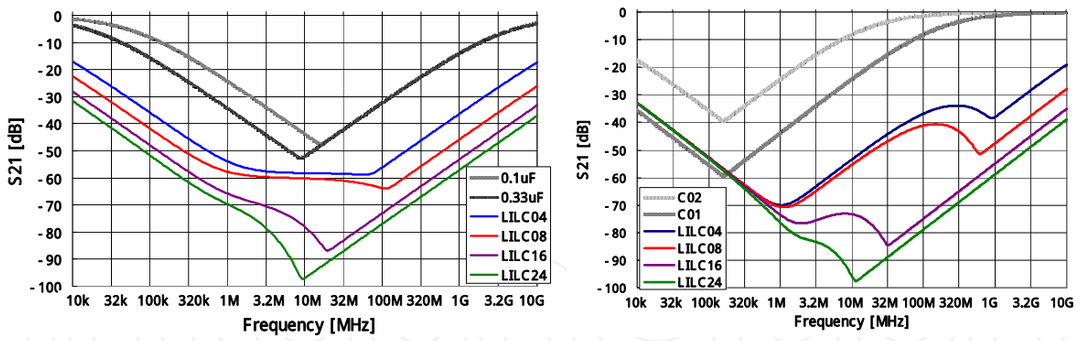


Fig. 19. Outline of the chip of the LILC

In Fig. 19, A is the anode which is formed by scraping the both exposed part of the etched aluminum foil, B is the conductive polymer layer, C is the carbon paste layer, and D is the cathode which is coated by the silver paste. All surfaces except the anode of the etched aluminum foil are covered by the insulation coating formed by the chemical conversion. The chip width is 1.5*mm*. Each LILC04, LILC08, LILC16, and LILC24 has the line length of 4*mm*, 8*mm*, 16*mm*, and 24*mm*.
Fig. 20 shows the calculated transmission coefficient (S_{21}) of the LILC. Fig. 20. a shows the specified S_{21} corresponding to the measuring value of the network analyzer. Fig. 20. b shows S_{21} on the actual PCB.
In Fig.20, the calculation condition is as follows; σ_S is 12,000, C_1 is 66μF, R_a is 1, k is 51.3, R_S is $1/\sqrt{k}$, w is 1.5×2*mm* at the calculation of the capacitance, w is 0.5×2*mm* at the calculation of Z_{CI}, a is 20.3*nm*, b_S is 3μm, b_C is 0 and b_V is 13*nm* for LILC04, b_C is 2.1μm and b_V is 10*nm* for LILC08, b_C is 12μm and b_V is 0 for LILC16, b_C is 2.9μm and b_V is 0 for LILC24, and the capacitance (C_T) for Z_{CT} in relation to the distance between the terminals is 4×10^{-17} F/m. In Fig .20. b, the calculation condition is same as the improved on-board LILL on the actual PCB in Fig. 16.
In Fig. 20. a well matches to measured S_{21} by using the network analyzer.



a) Specified S_{21} b) S_{21} on the actual PCB

Fig. 20. Calculated transmission coefficient (S_{21}) of the LILC

From the calculation result it was clarified that the structure of Fig. 19 has some following defects; the electromagnetic wave attenuates only at the cut surface of the aluminum foil, the formation of the carbon graphite layer on the cut surface is very difficult from the point of view of the quality. In addition, the thick etched aluminum foil is necessary to increase the rated current.

The multilayer structure of the LILC (Multi LILC) can improve the above mentioned defects. However the great side effects develop in addition to the cost increases. The attenuation coefficient is not improved because the escape channel of the EMW increases. In contrast, the terminal-impedance reduces. As the result, S_{21} on the actual PCB will decay from the specified S_{21} because the characteristic impedance of the PL is very smaller than 50Ω.

Table 1 shows the comparison of the decoupling components.

	Capacitor	LILC	Multi LILC	Prototype LILL
Insulation of Cut Surface	Chemical coating			Without treatment
Material of Anode	Etched aluminum			Lead frame
Formation process of Conductive Polymer Layer	Chemical reaction by Conductive Monomer			Coating by Conductive Polymer
Numbers of Anode	Single/ Multiple	Single	multiple	Single
Absorption loss	Zero	Large	Small	Large
Reflection loss	Small	Large	Very Large	Large
Limit factor of Electron current	No limit	Thickness of Aluminum foil	Numbers of Aluminum foil	Thickness of Lead frame
Improvement of Reduction of Decoupling on the PCB	Impossible	To increase the Chip Length		Possible without increasing Chip Length

Table 1. Comparison of the decoupling components

4.2 On-chip LILL technologies

The on-chip LILL should be connected to all of the on-chip inverters on the SoC. Therefore, for example, several tens of thousands of on-chip LILL will be used and each on-chip LILL will be connected to several tens of thousands of the on-chip inverter.

4.2.1 Validation of the function of the LILL and the influence of the length of the PL

Fig. 21 shows the circuit diagram of the test board for the validation.

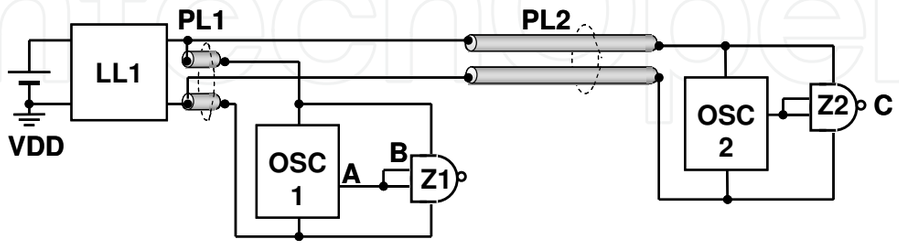
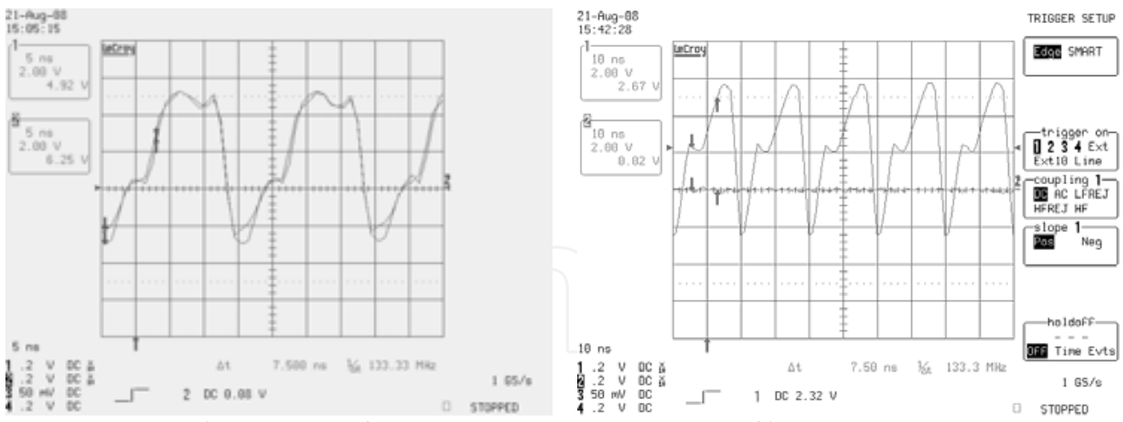


Fig. 21. Circuit diagram of the test board

In Fig. 21, VDD was 5.06V, which was supplied from the commercial power unit, CMX309HWC50MHz was used for the oscillator (OSC1, OSC2), SN 74AS00N was used for the gates (Z1, Z2), no SL were connected to the drivers, the prototype of the on-board LILL was used for LL1, the rated typical rise time of SN74AS00N is 0.5ns, each length of the PL1 and PL2 was 1cm and 36cm, the characteristic impedance of the PL was designed to be 73Ω, each PL was mounted on the insulator layer of the single sided board of FR-4, and each calculated round-trip time of the PL of 1cm-long and 36cm-long is 0.14ns and 5ns.
Fig. 22 shows the measured signal voltage at the point of A, B, and C in Fig. 21.



a) Point A and B b) Point C

Fig. 22. Measured signal voltage

In Fig. 22, the y-axis shows the voltage of 2V step, and the x-axis shows the time which is each 5ns/div. in Fig. 22. a and 10ns/div. in Fig. 22. b.
It were confirmed that the rise time increases to the calculated round-trip time approximately and that the LILL acts effectively as the ideal voltage source. From this experiment, it was clarified that the SEMW generated by each Z1 and Z2 returns to each certainly even though the LILL is shared.

4.2.2 Formation of the on-chip LILL

Fig. 23 shows an example of the layer formation of the on-chip LILL

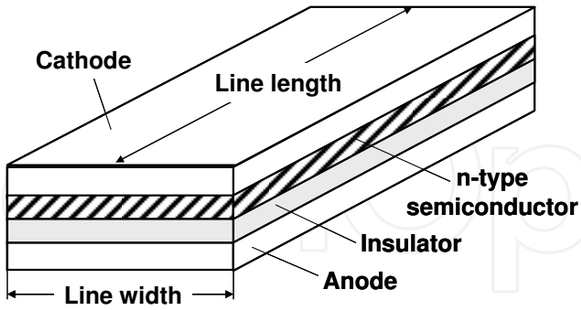
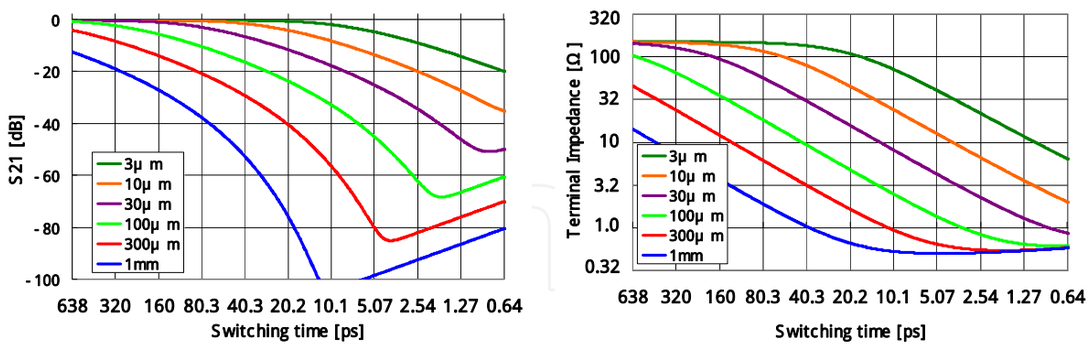


Fig. 23. Layer formation of the on-chip LILL

In Fig. 23, the attenuation appears caused by the n-type semiconductor layer which is made of the organic material or the inorganic material, and the n-type semiconductor and the cathode form the Schottky junction diode. The p-type semiconductor is also permitted. In this case, the p-type semiconductor is located between the anode and the insulator.
The low impedance is got by the thin insulator film of which the relative dielectric constant is large. The attenuation depends on the line length and the conductance of the n-type semiconductor.

4.2.3 Design of the on-chip LILL

The calculation equations for the on-board LILL were used for the on-chip LILL.
Fig. 24 shows the calculated characteristics of the on-chip LILL of line length.



a) Transmission coefficient (S_{21}) b) Terminal impedance (Z_a)

Fig. 24. Calculated characteristics of the on-chip LILL

In Fig. 24, the calculation condition is as follows; σ_S is 10^5 S/m, the thickness of the insulator layer a is $10nm$, b_S is $1\mu m$, ε_r is 8.5, w is $3\mu m$, C_T is 10^{-22} F/m, Z_0 which is the minimum characteristic impedance of the on-chip interconnect is 177Ω, and the switching time is got from the idea of the MSF after calculating to $500GHz$ from $500MHz$.
When the suitable line length is selected, the calculated Z_a is small enough than Z_0 and the transmission coefficient is smaller than -40dB.

5. MILL technologies

The crosstalk is one of the hardest problems for transmitting the signal at high-speeds. The crosstalk does not occur on the DC circuit or the QSCC. Therefore, the crosstalk is a kind of the EMI. According to the SEMW theory, the SEMW forms the signal voltage wave by charging and discharging the transmission line. Nothing except the SEMW can charge and discharge rapidly on the SMC.

The magnitude of the signal voltage should not reduce when the electron current does not exist on the SL. Even if the SL is the lossy line, the SEMW should travel without changing its speed and wave shape except reduction of the magnitude. In addition, as being shown in Fig. 6, the rise time (t_S) of the signal voltage depends on the wave length (λ_S) of the SEMW. Therefore, the wave-shape of the signal voltage should be maintained in the lossy line when the characteristic impedance of the lossy line is matched to it of the signal line. From above discussions, the concept of the MILL was born.

The MILL is the lossy line and the characteristic impedance of it matches the SL. The MILL is connected to the SL near to the driver. The MILL decouples the SEMW between the driver and the receiver on the SL effectively.

5.1 Function of the MILL

Fig. 25 shows the improved SMC by applying the technologies of the LILL and MILL.

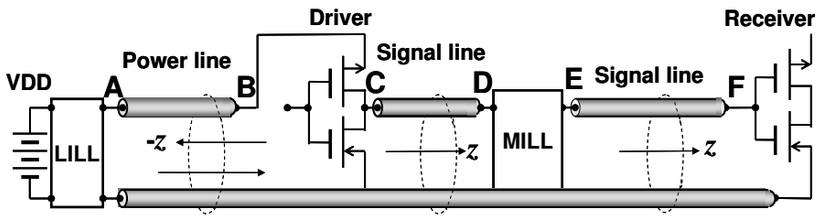


Fig. 25. Improved SMC

In Fig. 25, In Fig. 14, the LILL is connected to VDD and the point A on the PL in series and it forms the ideal power source, the MILL is connected to the point D and the point E on the SL in series, and the matched termination is not used on the SL.

Fig. 26 shows the SEW on the MILL.

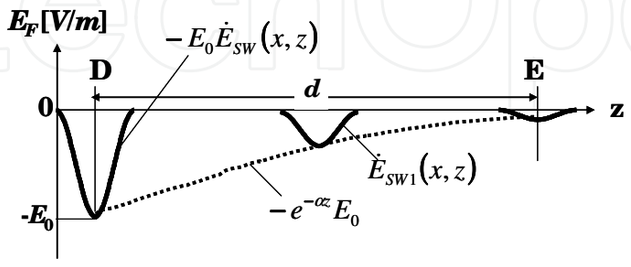


Fig. 26. SEW on the MILL

In Fig. 26, the electric field strength of the SEW on the MILL is

$$\dot{E}_{SW1}(x,z) = -e^{-\alpha z}E_0\dot{E}_{SW}(x,z) \tag{29}$$

where each x is the direction of the thickness, z is the traveling direction of the SL, and a is the attenuation constant.
According to the definition of the electromagnetism, the signal voltage on the MILL is

$$V_1(z) = \int_0^{\lambda_S} \int_0^d \dot{E}_{SW1}(x,z) = e^{-\alpha z} E_0 \int_0^{\lambda_S} \int_0^d \dot{E}_{SW}(x,z) \partial x \cdot \partial z \tag{30}$$

where, λ_S is the wave length of the SEW, d is the thickness of the insulator layer of the MILL. When $x=d$ and $z=\lambda_S$, (30) is

$$V_1(z) = e^{-\alpha z} V_S \tag{31}$$

The charge voltage of the SL at the exponential change of the magnitude of the SEW is

$$V_2(z) = \left(1 - e^{-\alpha z}\right) V_S \tag{32}$$

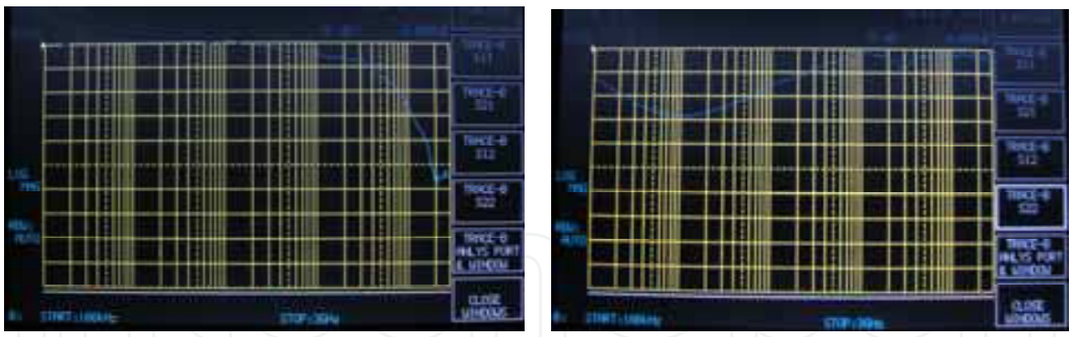
From (31), (32), a total of the signal voltage is

$$V_1(z) + V_2(z) = V_S \tag{33}$$

From above, it is clarified that the wave shape of the signal voltage is kept on the MILL even though the SEMW attenuate on it.
Meanwhile, the crosstalk and bounce on the SL between the point E and F in Fig. 25 will be suppressed because the magnitude of the SEMW is attenuated by the MILL.

5.2 Validation of the function of the MILL

Fig. 27 shows the measured S_{21} and S_{11} of the lab sample of the MILL.



a) S_{21} b) S_{11}

Fig. 27. Measured characteristics of the lab sample of MILL

In Fig. 27, the x-axis shows the frequency allocated to $3GHz$ from $100kHz$ on the log scale, the y-axis is allocated to -100dB from 0dB on the linear scale.
The lab sample of the MILL was made of the carbon graphite, the silver paste, and the polyurethane enamel wire (UEW). The thickness of the carbon graphite layer was $0.1mm$ approximately, the diameter of the UEW was $0.1mm$, the thickness of the insulator of the UEW was $5\mu m$, and the line length was $100mm$. Z_a of the lab sample was designed to 6.8Ω which is very lower than 50Ω, because there was no choice except using the carbon paste for getting the attenuation.

Fig. 28 shows the circuit diagram of the test board.

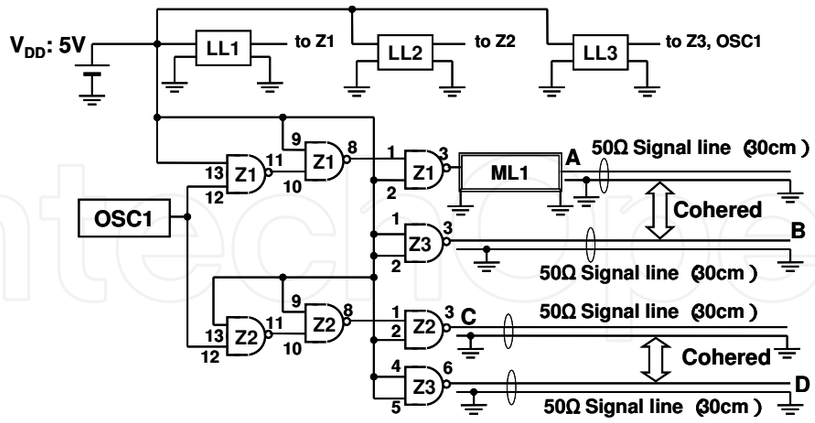


Fig. 28. Circuit diagram of the test board

Fig. 29 shows the measured voltage wave forms on the test board at the point A, B, C, and D in Fig. 28.

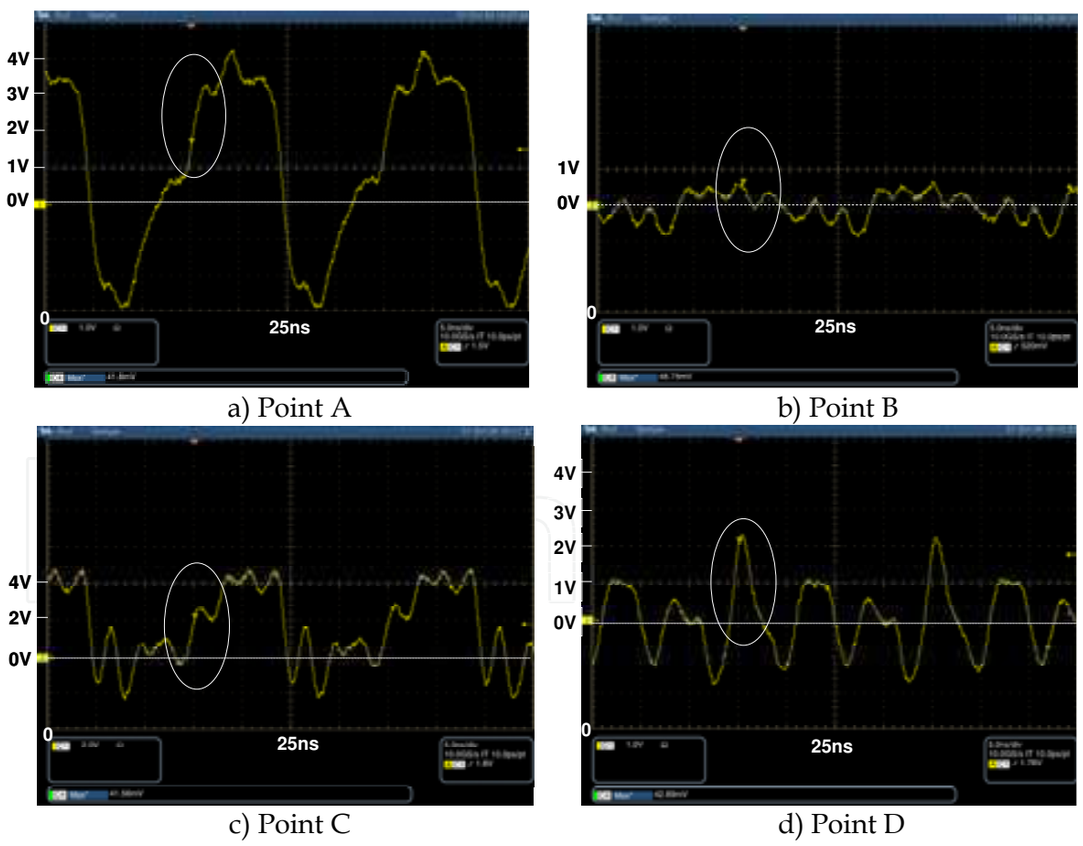


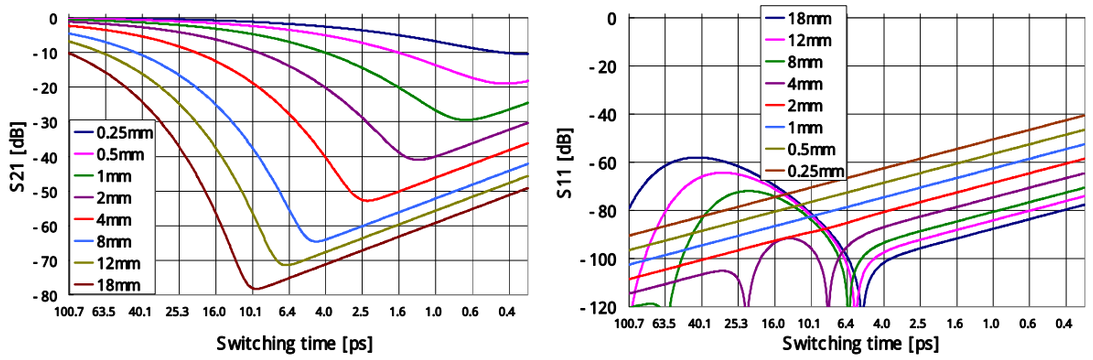
Fig. 29. Measured voltage wave forms on the SL

In Fig. 28, CMX309HWC50MHz was used for the oscillator (OSC1), SN 74AS00N was used for the gates (Z1, Z2, and Z3), LL1, LL2, and LL3 are the prototypes of the LILL14 shown in

Fig.13, the lab sample of MILL was used as ML1, the SL on the test board was formed by the PVC wire and the copper plane, ε_r of the PVC is 4, and the designed characteristic impedance was 50.1Ω. LL1, LL2, and LL3 were connected to all gates by the short wires.
In Fig. 29, the rising time shown in the circle of Fig. 29. a is almost equal to the rising time shown in the circle of Fig. 29. c. However, the crosstalk amplitude in the circle of Fig. 29. b is one quarter of it in the circle of Fig. 29. d. The reduction ratio of the crosstalk is almost equal to measured S_{21} in Fig. 27. a at 637MHz which is the MSF of the rise time of 0.5ns. The vibration is observed in Fig. 29. c, and its cycle time is 4ns approximately. This cycle time is equal to the calculated round trip time of the SEMW on the SL of 30cm long. However the vibration is not exists on the signal voltage in Fig. 29. a.
From above, the basic function of the MILL was validated.

5.3 Design example of the MILL

The layer formation of the MILL is same as the formation of the design example of the on-chip LILL in Fig. 23.
Fig. 30 shows the calculated characteristics of the design example of the MILL depending on each line length.



a) S_{21} b) S_{11}

Fig. 30. Calculated characteristics of the design example of the MILL

In Fig. 30, the equations for the calculation are same as these of the on-chip LILL. The thickness of the insulator was minimized for getting the large attenuation. The line width of the MILL was designed in the way that S_{11} becomes smaller than -40dB. The calculation condition is as follows; the n-type semiconductor is 700S/m, a is 13μm, b_S is 30μm, ε_r is 3.5, w is 55μm, and C_T is 10^{-19} F/m, and Z_0 is 50Ω. When the suitable line length is selected, S_{21} is smaller than -20dB.
In Fig. 25, when above mentioned design examples of the LILL and the MILL are used, and the wire length in the driver and the receiver is shorter than 2.5λs, the improved SMC shown in Fig. 25 will be able to be handled as the QSCC.
When the MILL designed by above way is applied to the SMC, the super-high-speed data transmission by parallel bit will be achieved relatively easily because the crosstalk is suppressed. At the same time, the multiple-value logic and the high-speed serialization/de-serialization (SerDes) will become unnecessary for the present. The MILL technologies are actualized to the on-board component or the on-chip component as with the LILL technologies. The on-board MILL will consist of several MILL chips. Each chip should be

connected to the on-chip drivers by as short wire as possible. The embedded MILL into the circuit board will be useful for increasing the performance and reducing both mounting space and the manufacturing cost.

6. Conclusions

The SEMW theory and both technologies of the LILL and the MILL were presented. The SEMW theory was developed by fusing the EMW theory and the NLU theory for the design and analysis of the SMC. The SMC generates the SEMW. The SEMW has no harmonic waves. Many spectra in the signal voltage are caused by the reflections and the repetitions of the SEMW on SMC. The wave shape of the signal voltage is got by integral of the wave shape of the SEW because the signal voltage is formed by the charging action of the SEW. The timing analysis with the high-accuracy will become possible when the SEMW theory is applied to the tools for the design or analysis. When the MILL is used together with the on-chip LILL, the signal integrity will be improved excellently and the almost all parts of the SMC will be able to be formed as the QSCC. This means that the design of all of the SMC become easy and free from the EMI. However, about the transmission line, more strict design of both characteristic impedance and skew or timing will be required.
The SEMW theory will be supposed to cause the innovation to the method of the manufacturing, design and analysis of the SMC. Improving the completeness of the SEMW theory is the future problem. The technologies of the LILL and MILL will create the emerging industries. The challenge for the commercialization of these technologies by getting the patron is the immediate issues for us. MathCAD Professional® and Excel® were used for all calculations.

7. Acknowledgment

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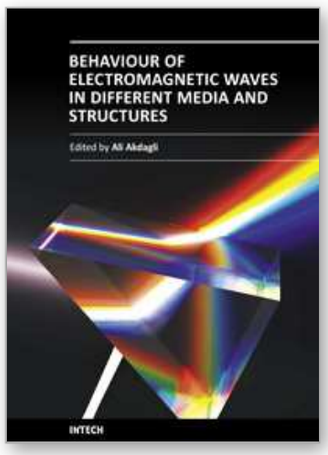

Behaviour of Electromagnetic Waves in Different Media and Structures

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