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# Surface-directed Growth of Nanowires: A Scalable Platform for Nanodevice Fabrication

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## 1. Introduction

Optical lithography continues to be the popular technique for further miniaturization of electronic circuitry and its components. However, as further device miniaturization continues, the complexity of pattern generation and cost increase (ITRS 2006); therefore the use of such techniques becomes limited to high-end applications, such as microprocessor manufacturing. As an alternative, nanomaterials and non-conventional nanofabrication methods, such as “bottom-up” chemical approaches, offer great opportunities in producing useful nanostructure-based devices with potential advantages such as enhanced performance and/or lower cost. A majority of the produced nanomaterials for device applications require post processing (e.g. transfer from a source to a target substrate). For composite structures this transfer is not a concern, but for producing intricate nanodevices with a large scale hierarchical order, this step becomes a bottleneck. Generally, scaling up requires knowledge of surface registries of a large group of nanocrystals on a given surface that is needed for the subsequent fabrication steps. In addressing this issue, we combine a surface-directed nanocrystal growth with conventional lithography to control the registries of laterally grown semiconductor nanowires. In this process, a nanowire is formed using a surface-directed vapor-liquid-solid (SVLS) process inside a Au nanodroplet; the nanodroplet defines the starting point of the nanowire and a single crystal substrate defines its growth direction. We use substrates such as sapphire and gallium nitride and have shown that each crystal promotes its own specific growth directions. Using this platform, nanowires are grown where the nanodevices are expected to be fabricated. In the following, we intend to provide an account of the progress on directed deposition and growth of nanocrystals in the plane of a substrate and existing challenges to interface them with the outside world.

“Bottom-up” fabrication strategies and directed assembly methods have become increasingly attractive in arranging nanostructure in a hierarchical order. One of the key barriers to large-scale integration of functional nanowires and nanocrystals into devices and systems has been their difficulty in parallel interfacing with other device components. A basic prerequisite for reproducibly interfacing, on the order of millions of, nanocrystals is to be able to precisely control their growth sites. Shape of the nanocrystal significantly impacts

the complexity of this process and thus nanocrystals with one elongated dimension fit in better with the available microfabrication protocols. In controlling the growth site of one-dimensional nanocrystals, also referred to as quantum wires, nanorods or nanowires, one popular approach is their growth in a free standing form using a metal-catalyst via a process called vapor-liquid-solid (VLS) (Wagner and Ellis 1964; Haraguchi, Katsuyama et al. 1991; Morales and Lieber 1998). The advantages of this growth technique include uniform composition and electronic structure of nanowires, and the ability to alter their composition by, for instance, introducing a quantum well (Bjork, Thelander et al. 2004) or a heterojunction (Bjork, Ohlsson et al. 2002; Wu, Fan et al. 2002). Furthermore, the VLS technique allows control over the nucleation site of a nanowire such that it is grown where the metal catalyst is deposited (Huang, Mao et al. 2001).

In applications requiring electron-hole recombination or separation, typically a n-p junction is needed that can be formed within a nanowire, either axially or radially (Putnam, Boettcher et al.; Garnett and Yang 2008). In another design, the n-p junction is formed at the contact point of nanowires with the underlying substrate (Dalui, Lin et al.; Fang, Zhao et al.; Park and Yi 2004; Chen, Chang et al. 2009). In both configurations, a top contact is necessary to complete the circuit. To have a functional device, prior to the top contact deposition, a non-conductive spacer is used to fill the void between nanowires (Park and Yi 2004; Sun, Huang et al. 2008; Kelzenberg, Boettcher et al. 2010). Different groups have used this technique for interfacing large ensembles of nanowires in photovoltaic applications; however, filling the void between nanowires can be a cumbersome step as it can force nanowires to collapse or lead to partial filling for closely packed nanowires. In other applications where nanowires need to be integrated in a planar format, the standing nanowires must be removed from the substrate and cast on a different surface. This step typically requires aligning nanowires to enhance the efficiency of interfacing them with other device components. Several strategies aiming at controlling hierarchical order of nanowires have been developed, such as electric field assisted orientation (Smith, Nordquist et al. 2000) and alignment with fluid flow in microchannels (Huang, Duan et al. 2001). Examples of other alignment techniques include the Langmuir-Blodgett technique (Kim, Kwan et al. 2001), assembly of densely packed nanowires using a pattern transfer process (Melosh, Boukai et al. 2003), shear force-alignment of nanowires in thin polymer films (Yu, Cao et al. 2007), and role-printing of nanowires (Yerushalmi, Jacobson et al. 2007). All of these techniques result in planar alignment of nanowires; however, they do not provide control over their surface registries for the successive patterning steps.

In this chapter, we discuss a fabrication technique that has the potential to address the limitations described above. This technique combines a “bottom-up” chemical approach with optical lithography and improves the scalability, precision, and fidelity of integrating nanowires to a platform. We discuss the surface-directed growth concept as well as the different steps necessary for scalable fabrication of some nanowire devices, such as field effect transistors (FETs) and light emitting diodes (LEDs). In the first section, we discuss the growth of ZnO nanowires on *a*-plane sapphire and their application in nanowire FETs. We provide some examples of fabricated nanowire FET devices with a single, two, or several nanowires. Furthermore, we analyze some of the electrical characteristics of individual nanowires and ensembles of nanowires. In the second part of this chapter, we discuss the growth of ZnO nanowires on gallium nitride (GaN), formation of planar arrays of n-p heterojunctions, and their LED behavior.

## 2. Surface-directed growth of ZnO nanowires on sapphire and their charge transport

Zinc oxide is a sensor, piezoelectric, UV light emitter, and transparent semiconductor in the visible spectrum, and as such is a technologically important material (Pan, Dai et al. 2002; Wang 2004; Wang, Song et al. 2007; Pearton, Lim et al. 2008). In its one-dimensional form, ZnO nanowires have been grown using a phase transport process at high temperature, or via a wet chemistry at low temperature (Wagner and Ellis 1964; Pan, Dai et al. 2002; Law, Greene et al. 2005). In the traditional VLS process, as described earlier, the nanocrystal growth is confined within a metal nanodroplet that dewets the substrate in early stages of growth, resulting in free-standing nanowires. In our technique, the metal nanodroplet stays in contact with the substrate during the ZnO growth, allowing the substrate to guide the horizontal growth of the nanocrystal; hence we call it a surface-directed VLS (SVLS) process. As the nanocrystal grows, the Au nanodroplet also moves on the surface while maintaining its interface with the substrate and nanocrystal. This method preserves the advantages of the VLS process while simultaneously allowing for careful control of the nanocrystal growth site and direction. Horizontal nanowires can be grown in a tube furnace at ambient pressure via a physical phase transport process. The anisotropic growth of a nanowire starts at the initial nanodroplet location and continues along the  $[1\bar{1}00]_{\text{sap}}$  of an *a*-plane sapphire as the nanodroplet moves on the surface (Nikoobakht, Michaels et al. 2004). In this direction, the ZnO (*c*-plane) and sapphire (*a*-plane) have a better lattice match along their “*a*” and “*c*” axes, respectively, leading to anisotropic ZnO growth. Intentional anisotropic crystal growth has been previously observed, for instance, in the growth of one-dimensional rare-earth silicides or germanium on Si (Ogino, Hibino et al. 1999; Chen, Ohlberg et al. 2000; Ragan, Chen et al. 2003). These techniques, while resulting in planar growth of nanowires, do not offer the control over their growth site or orientation. Our nanowire-to-device integration strategy includes a two-step photolithography process which is schematically described in Fig. 1. First, small Au pads and global marks are placed on *a*-plane sapphire surface using conventional optical lithography (Fig. 1a). ZnO nanowires are then epitaxially grown on opposing sides of each Au pad in  $[1\bar{1}00]_{\text{sap}}$  direction (Fig. 1b) inside a tube furnace. In the second photolithography step, patterns of metal electrodes are placed on the nanowires (Fig. 1c). To complete the fabrication of the field effect transistors, a third step of photolithography (not shown) is used to place the top gate electrode patterns on the nanowires. Prior to this patterning step, the nanowires are coated with a thin oxide (gate oxide) layer that protects nanowires from direct contact with the gate electrode.

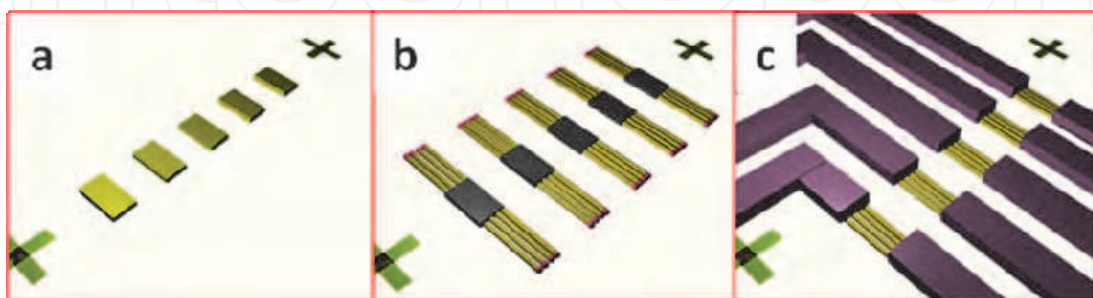


Fig. 1. Fabrication flow for interfacing ZnO nanowires to metal contacts. a) Deposition of Au pads and global marks. b) Planar growth of ZnO nanowires from Au pads. c) Placing metal electrodes using conventional optical lithography.

For preparing microscale Au pads, following photolithography protocols, substrates are coated with a typical photoresist. Patterns of  $1\ \mu\text{m} \times 5\ \mu\text{m}$  pads along with global marks are created on the photoresist. Thin Au films, 1 nm to 3 nm, are deposited on the photoresist using a thermal evaporator. Photoresist lift-off is carried out by sequential submersion of the substrates in two acetone containers (at  $80\ ^\circ\text{C}$ ) for a period of about 25 minutes. The lift-off process is concluded by sequential washing the substrates in hot ( $75\ ^\circ\text{C}$ ) and room temperature ethanol for a total time of 10 minutes. To remove the organic residue, ozone cleaning is performed for about 3-4 minutes, followed by washing in deionized (DI) water, and nitrogen gas drying. At this point a Au-patterned substrate is transferred to the end of the small quartz tube and nanowires are grown according to the procedure described earlier. To grow horizontal ZnO nanowires, a modified approach (Nikoobakht, Michaels et al. 2004) of an earlier method for growing free standing nanowires (Wagner and Ellis 1964; Huang, Wu et al. 2001) was used. Briefly, a ZnO/graphite mixture (0.15 g, 1:1 mass ratio) is loaded on a Si substrate and positioned at the center of an inner tube (13 cm length, 1.9 cm inner diameter). The tube, containing a Au coated sapphire substrate, is inserted into a tube furnace such that the mixed powder is located at the center of the outer tube (80 cm length, 4.9 cm inner diameter). The furnace temperature is set at  $890\ ^\circ\text{C}$  (with a ramp rate of about  $110\ ^\circ\text{C}/\text{min.}$ ) for 10 minutes under 0.6 standard liters per minute (SLPM) flow of 99.99% Ar or  $\text{N}_2$  gas.  $8\ \text{mm} \times 8\ \text{mm}$  *a*-plane sapphire pieces are washed with small cotton swabs and DI water and then blown dry with nitrogen (99.99%). For Au nanodroplets less than 25 nm in size, we observe an in-plane and oriented growth of small diameter nanowires on *a*-plane sapphire. For larger size Au nanodroplets, the population of free-standing nanowires increases.

## 2.1 Directed growth of nanowires on sapphire

In the first photolithography step, the Au pads are deposited such that their short sides are perpendicular to the  $[1\bar{1}00]_{\text{sap}}$  direction of the sapphire wafer (Fig. 2a-c). We have shown that this is a major growth direction of nanowires on the sapphire surface. The identified pad orientation results in a smaller number of nanowires per unit length (discussed later). A closer view of the positioning of the Au pads relative to the nanowire growth direction is shown in Fig. 2(a, b). An atomic force microscopy (AFM) image of a Au pad and its height profile are illustrated in Fig. 2(c-d), which shows an average height of 2.5 nm. Typically, a Au thickness ranging from 2 nm to 8 nm is suitable for horizontal nanowire growth. The thin Au film transforms to nanodroplets that, at higher temperatures, nucleate the nanowires.

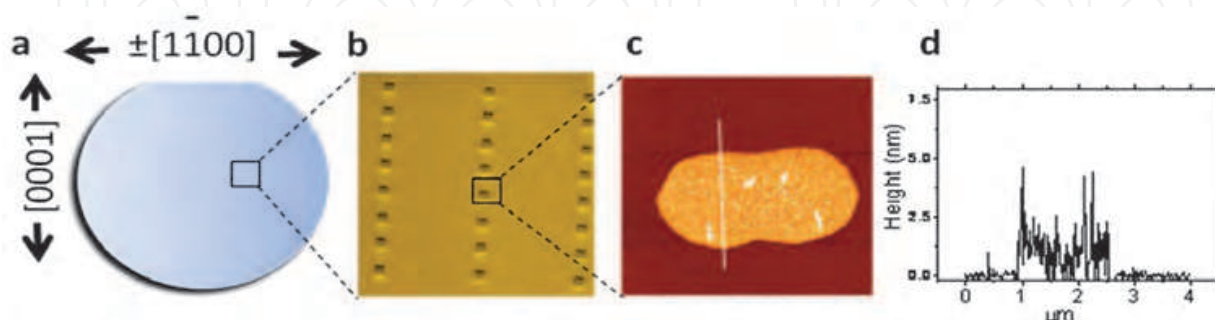


Fig. 2. Orientation of the deposited Au pads on the sapphire wafer. a) Sapphire wafer with its typical *c*-plane cut. b) SEM image of arrays of Au pads deposited on sapphire. c) AFM image of an individual Au pad after photoresist removal. d) Height profile of the Au pad shown in (c).

Only those nanodroplets residing at the two short sides of each Au pad produce horizontal ZnO nanowires (Fig. 3a-b). The group of nanowires shown in the scanning electron microscopy (SEM) image of Fig. 3b is also imaged by AFM (Fig. 3c) to characterize their dimensions and show the strength of this approach in locating a small group of nanowires on a large surface.

The AFM height profile of these nanowires shows that their diameter ranges from 8 nm to 13 nm. Typically, Au pads with 3 ( $\pm 1$ ) nm thicknesses result in nanowires with an average thickness of 11 ( $\pm 3$ ) nm and the nanowire density per pad width is found to be 10 nanowires/ $\mu\text{m}$ . The number of nanowires can be further reduced by decreasing the Au pad size or by increasing the resolution of the optical lithography. Based on SEM and AFM size measurements, the width-to-height ratio of the nanowires is typically found to be close to one; therefore, a semicircular profile or a faceted structure is assumed for horizontal nanowires. This is confirmed by examining the cross-sections of these nanowires, as demonstrated in Fig. 3(d, e). By increasing the number of deposited Au pads on the substrate, the scale of assembly of nanowires can be readily increased (Fig. 4). The directionality of growth is mainly dictated by the underlying substrate, and so this unique growth direction is observed everywhere on the wafer as well as in sapphire wafers from different batches. As shown in Fig. 4, free-standing nanowires grow from the Au nanodroplets that are far from the periphery of the Au pads (Huang, Mao et al. 2001).

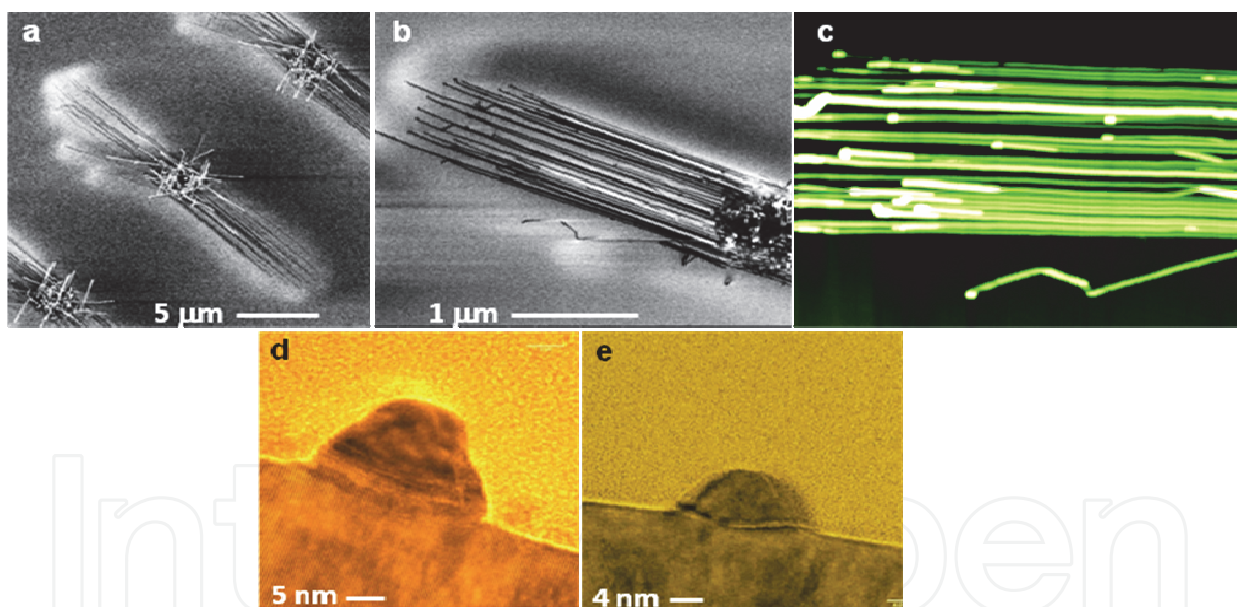


Fig. 3. a-b) SEM images of site-selective growth of horizontal nanowires. c) AFM image of the group of nanowires shown in part (b). d-e) Transmission electron microscope images of cross-sections of two individual nanowires.

## 2.2 Integration of horizontal nanowires with metal contacts

Since the relative positions of nanowires are known with respect to the global marks on the surface (from step 1), integration of the nanowires and metal electrodes can be carried out by aligning these marks with the complementary ones on the second layer of the photolithography mask. Metal electrode patterns are placed on nanowires across the whole 8 mm x 8 mm substrate with a precision that is limited to the resolution of the mask aligner.

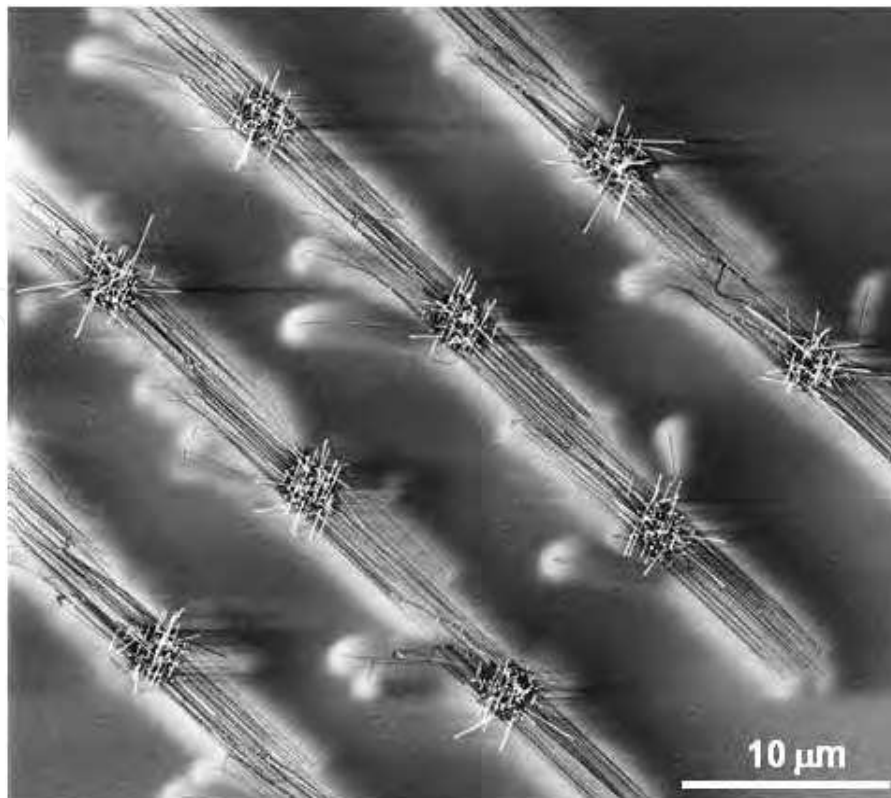


Fig. 4. Groups of horizontal nanowires made from planar arrays of Au pads.

Figure 5a shows a low magnification view of a sapphire wafer after deposition of metal electrodes and metal pads. The highlighted area in this figure is shown in the optical micrograph of Fig. 5b where the Au pads are seen as dark spots located underneath the metal electrodes. Nanowires are not resolved in this figure, but their direction is shown with the black arrow. In the used setup, alignment of nanowires and metal electrodes is such that the left metal contacts reside at one end of the nanowires. The highlighted box in Fig. 5b is further magnified in the SEM image of Fig. 5c in which the original Au pads are marked blue.

Depending on the number of nanowires grown from a given Au pad, a nanodevice can be comprised of single or multiple nanowires. Examples of devices with a few nanowires are shown in Figures 5(c) and 6(a-b). Devices containing double and single nanowires with multiple metal electrodes are shown in Figures 6(c- d). Using this technique, we are able to achieve parallel fabrication of *nanodevices* using a photolithography process with one micron feature resolution. This is in contrast to the current state-of-the-art nanowire-device fabrication in which registries of nanowires are not known and single nanowire devices are typically fabricated randomly in a serial fashion by electron-beam lithography. Single nanowire devices are of great interest, because of their enhanced characteristics that, most likely, smears out in devices containing multiple nanowires; however, single nanowire devices have not been well studied due to the limitation in their large scale formation. As mentioned earlier, by increasing the resolution of the optical lithography, better control over the number of nanowires per growth site is expected; considering the current advances in the semiconductor industry for feature miniaturization, if the deposited Au features can be reduced in size, the present technique has the potential to produce high density of such devices.

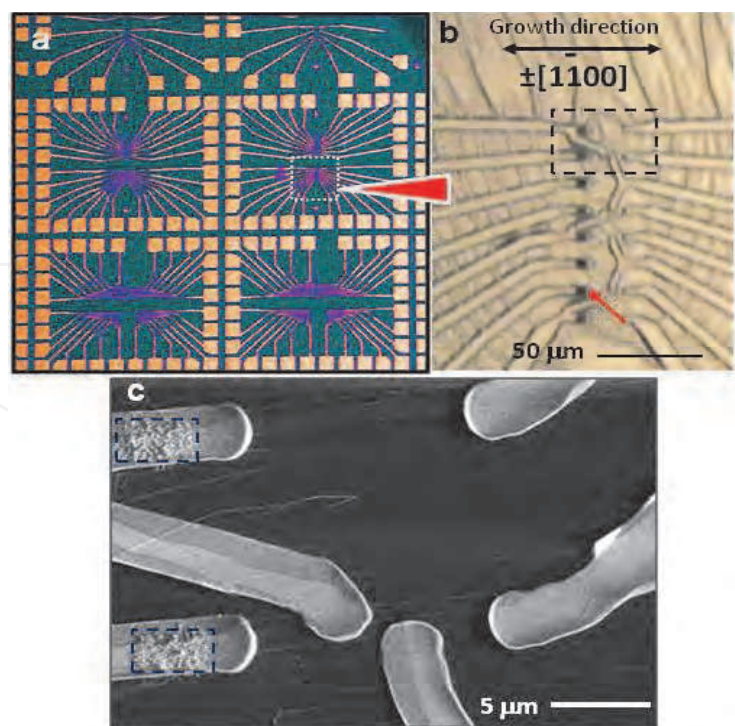


Fig. 5. Scale of placement of metal electrodes on nanowires. a) Low magnification optical image of electrodes and bonding pads. b) The highlighted box in part (a) is magnified here showing the overlap of the dark spots with the left hand side metal electrodes. c) the marked area in part (b) is shown in the SEM image depicting two groups of nanowires originated from two Au pads (marked blue) and their orientation relative to the metal electrodes.

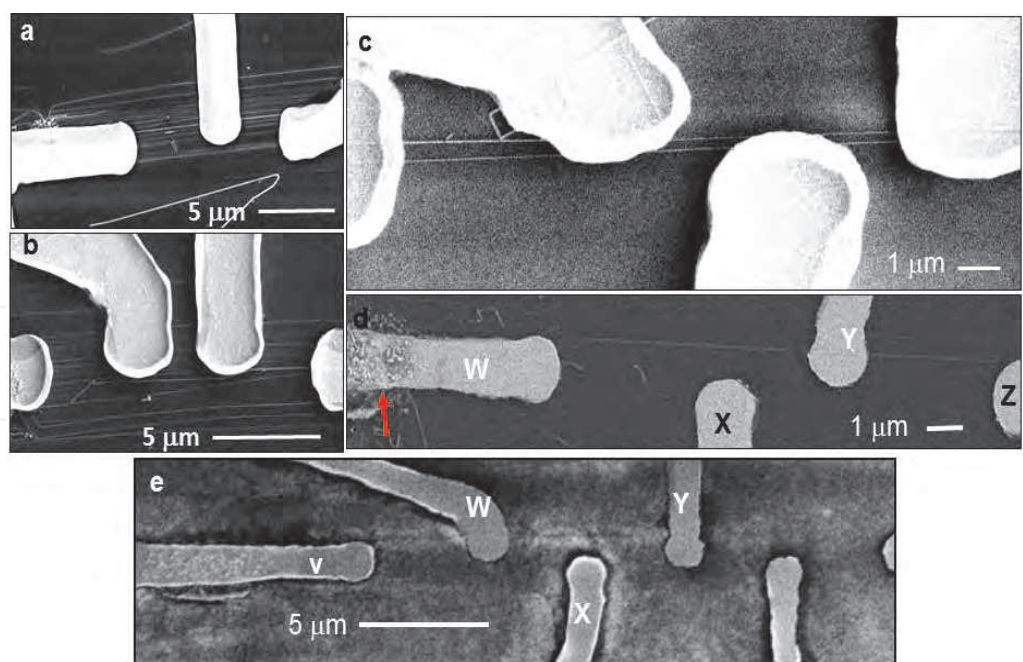


Fig. 6. Examples of fabricated multiple-, double, and single nanowire devices. The electrode patterns and their spacing are defined in the photomask. Aligning the global marks in the 1<sup>st</sup> and 2<sup>nd</sup> mask readily results in overlap of the nanowires with the metal electrodes. Letters V,W, X,Y, and Z in part (d-e) are explained in section 2.3.

### 2.3 Electrical measurements

In a single fabrication process, as described above, more than 600 nanodevices can be prepared composed of both single- and multi- nanowire devices. The results presented here are from three different fabrication processes; more than 20 nanodevices were tested repeatedly over the course of 3 months during which none showed any evidence of degradation or aging. Electrical measurements included two-terminal current vs. voltage (I-V) and transconductance ( $I_{ds}$ - $V_G$ ) were carried out using (Keithley 6430)<sup>1</sup> and (Hewlett-Packard 4140B)<sup>1</sup> source-measure units and a probe station. In the examined nanowires, the channel length ranged from 4  $\mu\text{m}$  to 8  $\mu\text{m}$  and nanowire diameters were between 7 ( $\pm 1$ ) nm to 22 ( $\pm 1$ ) nm. Depending on the length and diameter of the nanowires, the maximum current extracted at a 5V bias ranged from 2 nA to 180 nA. Among tested devices, different types of contacts are observed ranging from Ohmic to Schottky (Fig. 7). As an example, the I-V scan in Fig. 7a was obtained from the device in Fig. 6d (contacts WY) showing an Ohmic contact. In this device the nanowire length between the electrodes was 6.5  $\mu\text{m}$  and its diameter was 12 ( $\pm 1$ ) nm (measured by AFM). The I-V scan in Fig. 7b, corresponding to the device VW (Fig. 6e) with a length of about 4  $\mu\text{m}$  and a width of 22 ( $\pm 1$ ) nm, displays a different behavior. In this case, the linear slopes of the I-V scans indicate the presence of an Ohmic contact, but with two different slopes for reverse and forward biases. The reasons behind the different slopes are not clear, but most likely are contact related. Although metal contact deposition is expected to be fairly homogenous for nanowires on a given substrate, the variation in electrical properties of the nanowires could be influenced by a number of other factors, such as contact contamination or inadequate thermal annealing. The results presented in this study are obtained without thermal annealing of the electrical contacts. Another device behavior is shown in Fig. 7c that has a rectifying behavior. Compared to previous nanowire devices, this nanowire has a diameter of about 7 nm, which is relatively small.

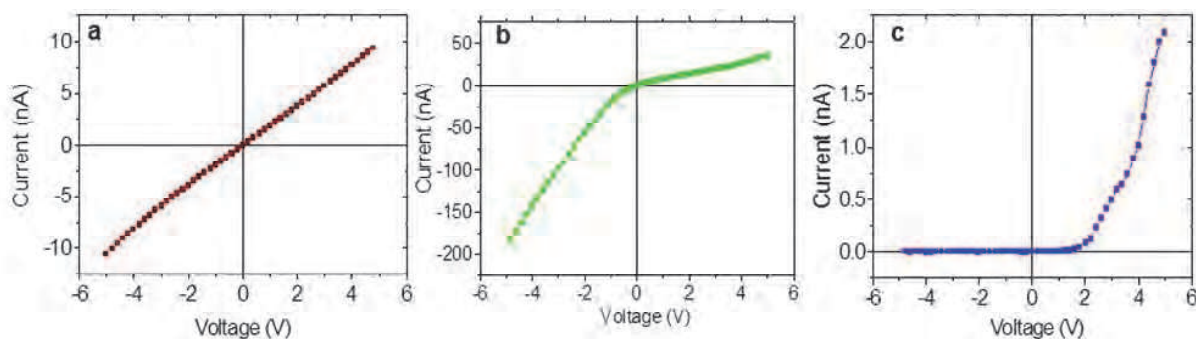


Fig. 7. Two-terminal current vs. source-drain voltage curves for three single NW devices.

The diode like behavior of this device could be due to its Schottky contacts or the smaller diameter of the nanowire. Nonetheless, information on charge transport at this size regime is very limited and more work is required to reach a comprehensive conclusion.

<sup>1</sup> Certain commercial equipment, instruments, or materials are identified in this paper to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Institute of Standards and Technology nor does it imply that the materials or equipment identified are necessarily the best available for the purpose

## 2.4 Modulating the electrical conductivity of nanowires

For these measurements, a top-gated FET design (as illustrated in figure 8) was fabricated. In this design, a thin layer of silicon oxide (100 nm) is first deposited on nanowires using plasma-enhanced chemical vapor deposition (PECVD), followed by deposition of Au metal as gate electrode using optical lithography and thermal metal evaporation.

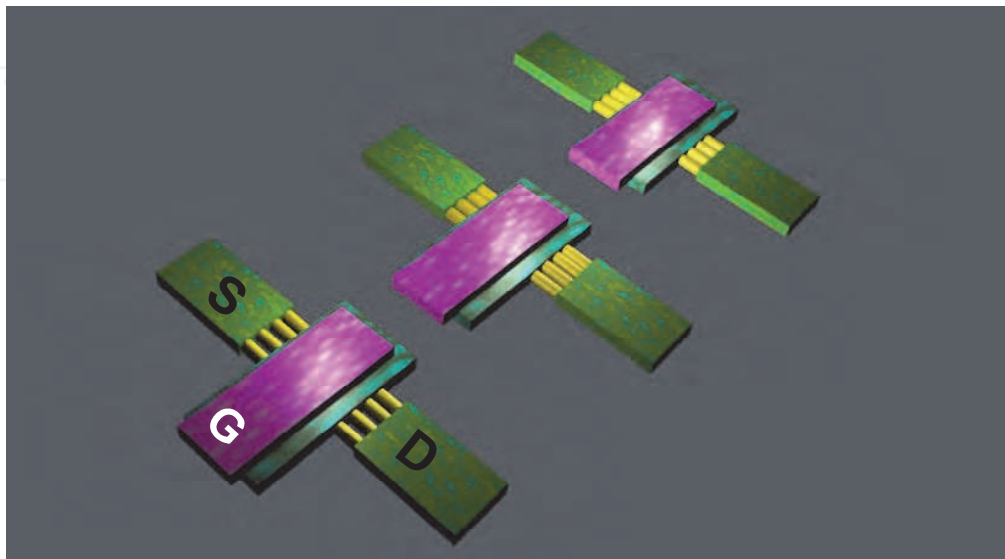


Fig. 8. Top-gated FET nanowires. Source, drain, and gate electrodes are labeled as S, D, and G, respectively.

Here the idea is to modulate the electrical current that passes through the nanowires by applying a voltage to a gate electrode that resides about 100 nm above the nanowires. As-grown ZnO nanowires typically have excess electrons, likely due to oxygen vacancies, and interstitials (Kohan, Ceder et al. 2000), and thus are n-type semiconductors. If that is the case, as gate electrode bias is increased to positive values, the conductivity of the nanowires increases. Typical current vs. source-drain voltage ( $I_{DS}$ - $V_{DS}$ ) scans are shown in Figures 9a and 9b for a multi-nanowire and a two-nanowire device, respectively. At a positive gate bias, the  $I_{DS}$  increases markedly; hence the channel is n-type (Sze 1969). A positive gate bias enables access to electrons (mostly in the valance band) of the nanowires, resulting in an increase in electron density in the conduction band and thus an increase in device conductivity. For a negative gate voltage, due to the repulsion of electrons by gate, the number of electrons in the conduction band decreases and thus the size of the conductive channel decreases. This is the trend that is also observed in nanowire devices at negative gate biases, as can be seen for the negative voltage region in Fig. 9c-d. The plots in this figure demonstrate the gate modulation efficiency ( $I_{DS}$ - $V_G$ ) for a variety of source-drain voltages. For such devices the threshold voltage was found to be about -3V; this is the gate voltage at which nanowires stop charge transport. Since these nanowire devices have an intrinsic conductance at zero gate voltage, by definition they are classified as “depletion mode” FET devices. This behavior can be modeled using the following equation which portrays the idealized characteristic of a insulated-gate field effect transistor (Sze 1969):

$$\frac{dI}{dV_G} = \frac{\mu C}{L^2} V_{ds} \quad (1)$$

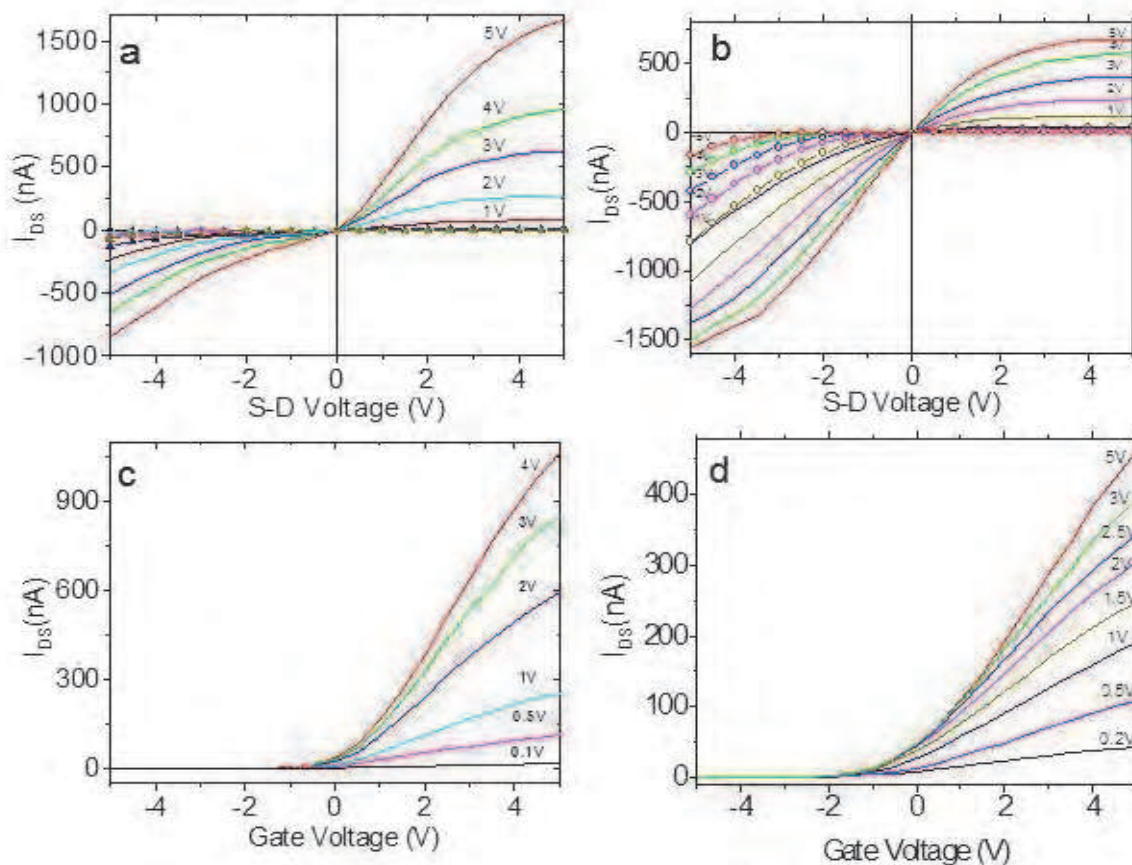


Fig. 9. Current-voltage and transconductance measurements of NW devices.  $I_{DS}$ - $V_{DS}$  data for top-gated FET NW device containing: a) eight NWs, with diameter distribution of  $13 (\pm 5)$  nm and channel length of  $8.5 \mu\text{m}$ . b) two NWs,  $10 (\pm 1)$  nm and  $20 (\pm 1)$  nm in diameter and a channel length of  $6.3 \mu\text{m}$ . The scans were recorded at different gate voltages ranging from -5V to 5V. By increasing  $V_{DS}$ ,  $I_{DS}$  linearly increased in both devices followed by device saturation due to a drastic drop-off in the charge carriers (electrons). When negative gate bias was applied (lines with symbols), channel conductivity gradually decreased to zero. For fixed  $V_{DS}$  values,  $I_{DS}$ - $V_G$  scans were collected for: (c) an eight-NW device. d) a two-NW device. The absence of current saturation in this voltage range indicated low resistivity of the contacts.

In equation (1),  $C$  is the capacitance of the gate that is defined by  $C = 2\pi\epsilon_{SiO_2}\epsilon_0L / \ln(\frac{4h}{d})$ ;  $\epsilon_0$  is

the permittivity of vacuum and  $\epsilon_{SiO_2}$  is relative dielectric of the gate oxide layer.

$L$  is the device length,  $h$  is the oxide thickness, and  $d$  is the nanowire diameter. Using equation (1) and slopes of the graphs at  $V_{DS}$  of 1V in Fig. 9 (c-d), the field-effect mobilities,  $\mu$ , for the multi-nanowire and two-nanowire devices are found to be  $\sim 15 \text{ cm}^2/\text{Vs}$  and  $20 \text{ cm}^2/\text{Vs}$ , respectively. In calculating the mobility, the channel width was assumed to be the sum of the diameters of the nanowires. Although the profile of the nanowires is closer to a semicircular shape, the nanowire profile was considered circular when estimating the field effect mobilities. The on/off current ratios of the devices were found to be about  $10^5$  for a  $V_{DS}$  of 4V. Devices with multiple nanowires show characteristics comparable to those of thicker ZnO nanowires (e.g., 100 nm diameter) (Fortunato, Barquinha et al. 2004). While having smaller individual

diameters (15 nm to 25 nm), they still net a larger total surface area. These could be suitable for sensing application where higher surface area is an advantage.

In examining single nanowire devices,  $I_{DS}$ - $V_{DS}$  measurements were collected at different gate biases for a nanowire with  $14(\pm 1)$  nm diameter and a  $7.1\ \mu\text{m}$  channel length. As seen in figure 10, current intensity that goes through individual nanowires increases as the gate bias voltage increases (under forward bias). This device, compared to the two-nanowire device (Fig. 9b), shows a lower drain current, which could be due to Schottky contacts and the smaller nanowire diameter. Figure 10b shows that the device remains off at zero gate bias, indicating a very small conductive channel width. This defines this type of device as a FET in “enhancement mode”. The threshold voltage was found to be about +1V.

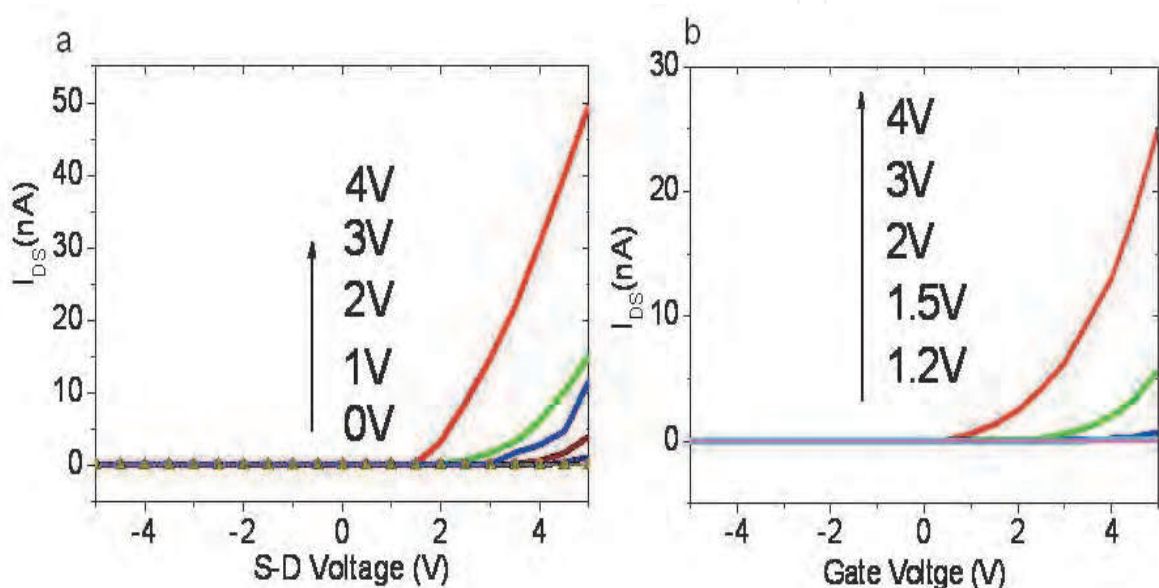


Fig. 10. a)  $I_{DS}$ - $V_{DS}$  scans for a single NW FET. The maximum drain-current at  $V_{DS}$  of 5V increased from 1nA to about 50 nA within 0V to 4V of  $V_G$ . b)  $I_{DS}$ - $V_G$  curves show that the single NW device is not conducting at zero gate bias, which is different from multi-NW devices (9c, d).

Among the tested devices it was noticed that single nanowires with diameters less than 15 nm tended to remain off under no gate bias. The observation of the two different modes in multiple and single nanowire devices is likely due to a decrease in the number of nanowires and also their smaller diameter. In low power applications, a device in the “enhancement mode” is more desirable over the “depletion mode” because there is no gate voltage necessary to turn the transistor off (Fortunato, Barquinha et al. 2004). This is a remarkable property that can be used to tune the characteristics of a nanowire FET. The field effect electron mobility measured for several single nanowire devices was found to be  $4 (\pm 2)\ \text{cm}^2/\text{Vs}$  with an on/off current ratio of at least  $\sim 5 \times 10^4$ . It is notable that the values reported above were obtained for device lengths ranging from  $4\ \mu\text{m}$  to  $8\ \mu\text{m}$ . Nanowire surface engineering, e.g., overcoating nanowires with a material with suitable band gap and lattice constant, is expected to decrease the number of electron scattering sites in the nanowire and therefore improve the electron mobility. Compared to ZnO thin film transistors, ZnO nanowire devices show comparable electron carrier densities ( $10^{18}\ \text{cm}^{-3}$ ) and field effect mobilities, but significantly lower threshold voltages (Fortunato, Barquinha et al. 2004). In all of our fabricated devices the

threshold voltage ( $V_{th}$ ) was found to be between 1V to -4V originating from a gate dielectric thickness of about 60 nm. ZnO nanowire devices are expected to have much lower  $V_{th}$  values and improved device behavior once a high- $\kappa$  and structurally matched dielectric is used. More comprehensive transport studies on single and multi-nanowire are needed to further understand the electrical properties of this new class of nanomaterial.

A multitude of applications using this technique are possible. In the field of crystal growth, use of “mobile metal nanodroplets”, such as Au, could be a new way for planar and localized growth of nanocrystals and their heterostructures. We have extended this approach to other (II-VI or III-V) semiconductor nanowires that have an anisotropic crystal mismatch with their underlying substrate, which is discussed in the following section.

### 3. Surface-directed growth of ZnO nanowires on GaN and their electro-optical properties

In addition to the growth of ZnO on sapphire, more recently SVLS was used for growth of GaAs nanowires on GaAs substrates (Fortuna, Wen et al. 2008). In the present work, we extend this process to formation of high quality heterojunctions of II-VI and III-V semiconductors; a characteristic that has been challenging to realize in homo- and heterojunction growth of these semiconductors (Kozodoy, Ibbetson et al. 1998; Vispute, Talyansky et al. 1998). To demonstrate this concept, we form addressable microarrays of p-n heterojunctions by lateral growth of n-type ZnO nanowires, a II-VI semiconductor with hexagonal structure, on a p-type GaN substrate with a similar crystal structure (Nikoobakht and Herzing 2010). ZnO, a wide band-gap semiconductor, is attracting renewed interest for UV light emission and lasing, piezoelectric devices (Wang and Song 2006), “invisible” circuitry (Nomura, Ohta et al. 2003), and photovoltaics (Law, Greene et al. 2005). Its band gap can be engineered by the addition of Mg or Cd dopants, which are inexpensive and abundant (Pearson, Lim et al. 2008). ZnO also exhibits one of the highest exciton binding energies ( $\sim 60$  meV), which makes it a good candidate for high efficiency UV-visible light emitters. To this end, we show a simple device design that allows charge injection to a large number of laterally grown heterojunctions. This approach could enable formation of a wide range of electrically addressable II-VI and III-V heterojunctions and their easy integration into photonic and lab-on-chip platforms with applications in energy generation and light detection.

The lateral growth of ZnO nanowires takes place on a Au-patterned *c*-plane GaN substrate. Au patterns were deposited either by dispersing Au nanoparticles (10 nm to 40 nm in size) or by using a thermal evaporator. The process is carried out inside a tube furnace that is held at 850 °C, with the substrate placed in a stream of ultra-dry N<sub>2</sub> carrier gas containing Zn and O precursors. The lateral growth of nanowires on GaN in the growth chamber is more sensitive relative to the growth of standing nanowires; for a reproducible growth, care must be taken to place Au coated substrates at the outlet of the small quartz tube (refer to section 2). At high temperature, the resulting Au nanodroplets promote the planar growth of ZnO nanocrystals via the SVLS process, which is influenced by the lattice match and crystal symmetry of the nanocrystals and the substrate. Crystal symmetry clearly demonstrates its effect in a system like ZnO ( $a$ ,  $b=0.32489$  nm) on GaN ( $a$ ,  $b=0.31894$  nm), which contains a lattice mismatch of  $\sim 1.8\%$ . In the simplest case, we observed that using 10 nm to 40 nm Au nanoparticles dispersed on GaN, the substrate directs the growth in six equivalent directions of  $\langle 10\bar{1}0 \rangle$  with a hexagonal symmetry as shown in Figure 11(a,b).

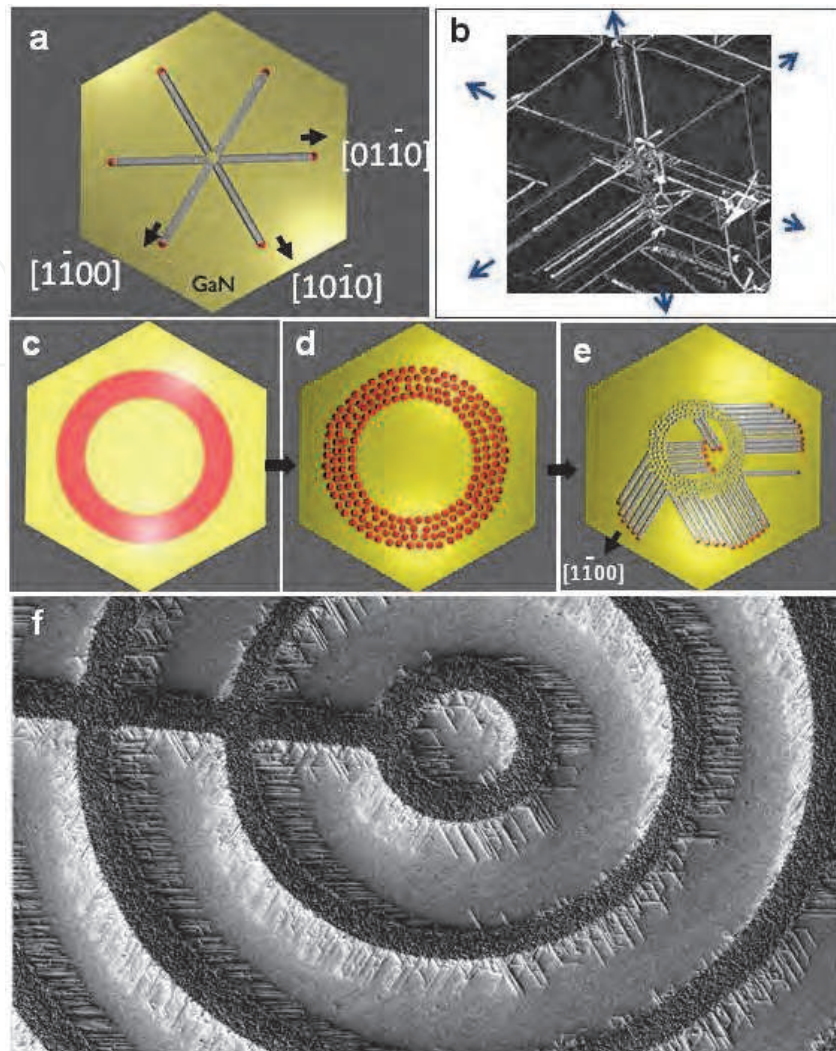


Fig. 11. a) Schematic showing the six-fold symmetry of the surface-directed VLS growth of ZnO nanocrystals using Au nanoparticles (red circles) on c-plane GaN and b) its corresponding electron micrograph illustrating these growth directions. c) The circular drawing in red represents the Au pattern deposited on GaN via standard photolithography, which in part (d) converts to nanodroplets at elevated temperatures. e) The Au nanodroplets at the boundaries of the circular pattern result in horizontal nanowires. f) Arrays of p-n heterojunctions made from n-type ZnO nanowires grown on p-type GaN.

The observed six-fold symmetry confirms the contribution of the underlying substrate in determining the growth direction. The site selectivity of the growth is shown by Au patterning a GaN surface and growth of ZnO nanostructures. In this process, a photolithographically-generated Au pattern with a thickness of  $8 (\pm 2)$  nm (Fig. 11c) at elevated temperatures ( $500\text{ }^{\circ}\text{C}$  -  $700\text{ }^{\circ}\text{C}$ ) converts to packs of Au nanodroplets (Fig. 11d). As shown in Figure 11e, at a temperature range of  $840\text{ }^{\circ}\text{C}$  -  $900\text{ }^{\circ}\text{C}$ , while the ZnO phase transport is in progress only Au nanodroplets formed at the perimeter of a Au pattern have the opportunity to laterally move on the substrate and form nanowires. Nanowires preferentially grow in three directions and are all electrically connected via the ZnO backbone that can be seen as the dark-gray circular pattern.

The nanowire width stays constant during its lateral growth, indicating that diffusion of Au to the nanowire facets and reduction in the volume of the Au nanodroplets remains insignificant for nanodroplets smaller than 20 nm (Hannon, Kodambaka et al. 2006). When the diameter of the Au nanodroplets increases above 20 nm, the nanowires acquire a new dimension by growing in the  $[0002]_{\text{ZnO}}$  direction (normal to the substrate plane). Utilizing this observation, by depositing Au patterns as shown in Figure 12a with thickness of  $10 (\pm 2)$  nm to  $17 (\pm 2)$  nm (step 1), it is possible to laterally grow ZnO nanowalls. Steps 2 and 3 in this figure represent the formation of Au nanodroplets followed by growth of ZnO nanowalls, respectively. The schematic in step 3 illustrates tilted view of an assembly. Following these steps results in assemblies of ZnO nanowalls and standing nanowires as seen in Figure 12b. This assembly is grown from 5 mm long Au lines with  $5 \mu\text{m}$  of width and  $20 \mu\text{m}$  pitch. In this figure, patterned Au lines are deposited parallel to the  $[10\bar{1}0]$  direction of GaN in order to allow the lateral growth of ZnO nanowalls in only two directions ( $[01\bar{1}0]$  and  $[1\bar{1}00]$ ).

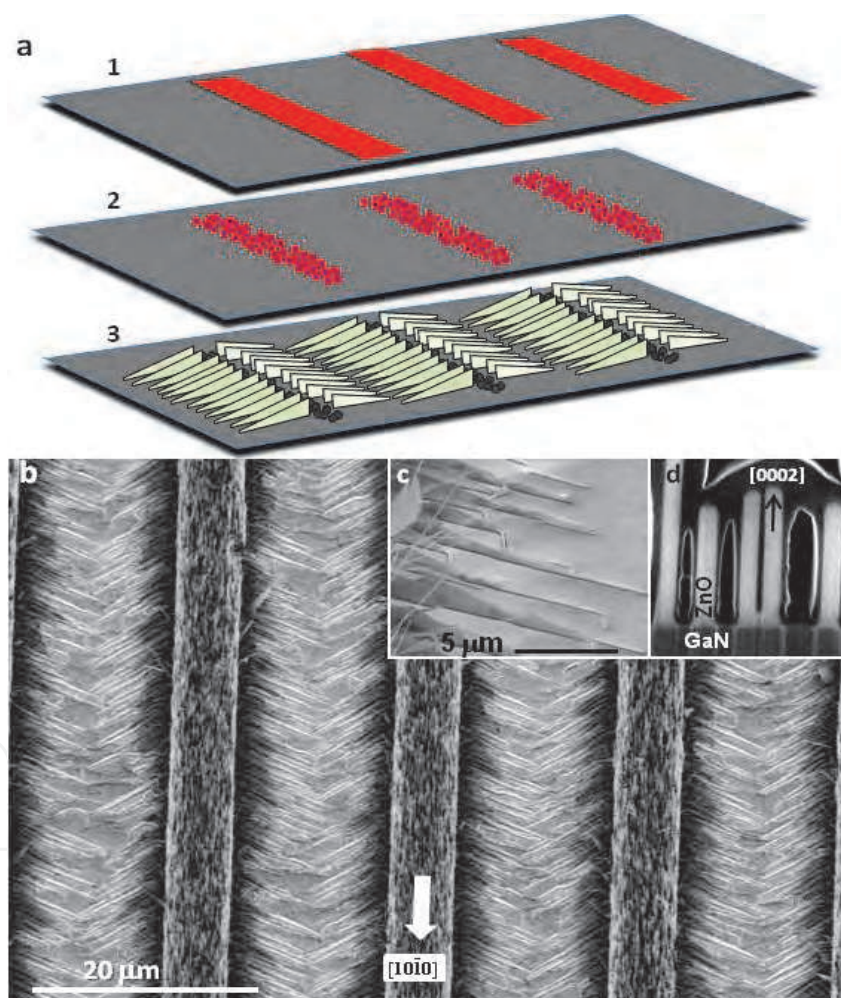


Fig. 12. a) Steps for growing assemblies of laterally grown ZnO nanowalls. b) An assembly of ZnO nanowalls grown from a periodic array of Au lines with a film thickness of  $15 (\pm 2)$  nm, width of  $5 \mu\text{m}$  and length of 5 mm. Au lines are deposited along the  $[10\bar{1}0]_{\text{GaN}}$ . c) A tilted SEM view of ZnO nanowalls in a small section of the assembly from part (a). d) STEM image of cross-sections of a group of ZnO nanowalls showing their upright growth in  $c$ -direction and their four major facets.

Examining the cross-sections of closely packed ZnO nanowalls (Figure 12b) shows they are vertical ZnO slabs with four dominant facets that can grow a few microns in the direction normal to the interface. Due to the large number of Au nanodroplets formed at the perimeter of each Au line, a high density of nanowalls can be grown, which is advantageous in applications such as photovoltaics and photodetection where the surface area is important.

Figure 13 shows that the height of a nanowall gradually decreases toward its leading end, indicating that its vertical growth most likely is due to a slower self-catalytic process (Wang, Kong et al. 2003). Previously, in the case of ZnO nanocantilevers, self-catalytic growth was attributed to the formation of Zn clusters on the (0002) polar surface of ZnO nanowires (Wang, Kong et al. 2003). Since nanowalls are only observed in the case of larger sized Au nanodroplets, it is possible that a larger volume Au nanodroplet also results in formation of Zn cluster (at its eutectic point) that promotes the growth in the ZnO [0002] direction.

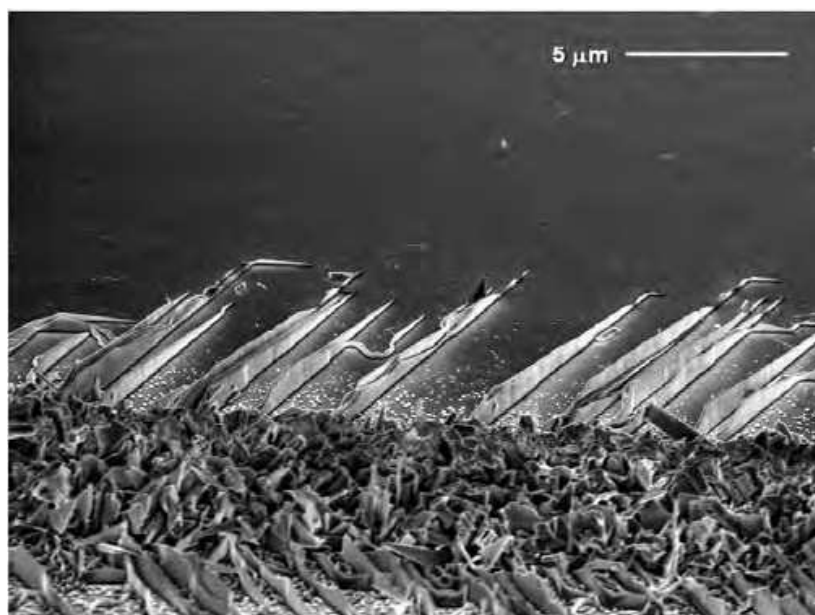


Fig. 13. Tilted view of grown ZnO nanowalls on GaN. The height decreases toward the leading end of nanowalls.

### 3.1 ZnO-GaN p-n heterojunctions and fabrication of nano-LEDs

The present technique is suitable for fabricating II-VI nanowire-based devices on III-V semiconductor substrates including GaN and its other combinations, such as InGaN and AlGaN, to realize platforms for tunable light emission and detection. As an example, in Figure 14a, a simple strategy is demonstrated for fabricating arrays of electrically-driven, light-emitting, p-n heterojunctions formed at the interface between ZnO nanowires or nanowalls and the GaN substrate.

The GaN substrate is *c*-plane and 5 μm thick, which is grown on *c*-plane sapphire. The GaN layer is doped with Mg at a concentration of  $5 \times 10^{17} \text{ cm}^{-3}$  (purchased from TDI<sup>1</sup>). In this technique, since the relative location of nanowire arrays are known, metal contacts can be readily deposited via standard photolithography over the ZnO backbones. A representative image of a three-layer (metal/ ZnO nanowalls /GaN) structure is shown in Figure 14b, where the top metal electrode (Ti-Au) deposited on the ZnO backbone is highlighted in

yellow. During the device operation, the metal contacts on the ZnO backbones allow electron injection into nanowires or nanowalls and hole injection to the p-GaN side. The location, size and shape of the light emitting devices can be controlled by depositing Au catalyst patterns ranging from a few microns to several millimeters with triangular, circular, and square shapes (Nikoobakht and Herzing 2010).

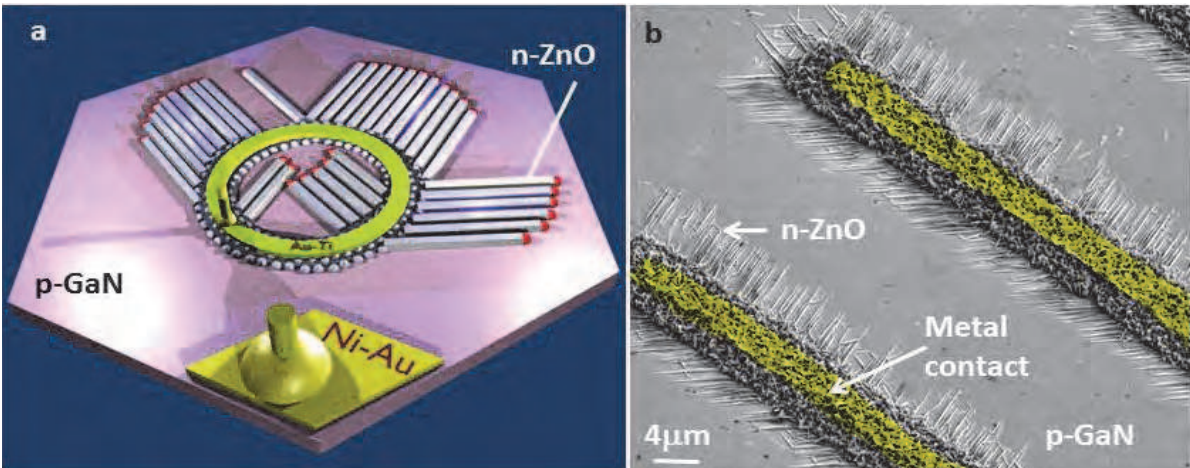


Fig. 14. a) Schematic showing a tilted view of an electrically-driven array of p-n heterojunctions made from n-type ZnO nanowalls on p-type GaN. In this cartoon, the GaN substrate is shown as a hexagon. b) SEM image of the tilted view of a device is illustrated; the yellow color indicates the deposited metal electrode on the ZnO backbone. All other device layers are labeled in the figure.

Current-voltage (I-V) characteristics of the as grown n-p heterojunctions exhibit rectifying behavior for small and large groups of nanowires or nanowalls. Multiple devices were repeatedly operated from -25 V to 27 V in order to examine the structural and functional stability of the p-n heterojunctions. Results in Figures 15a and 15b, respectively, show the I-V scans of a 5 mm x 5 mm n-p heterojunction array and a 100 μm-size array.

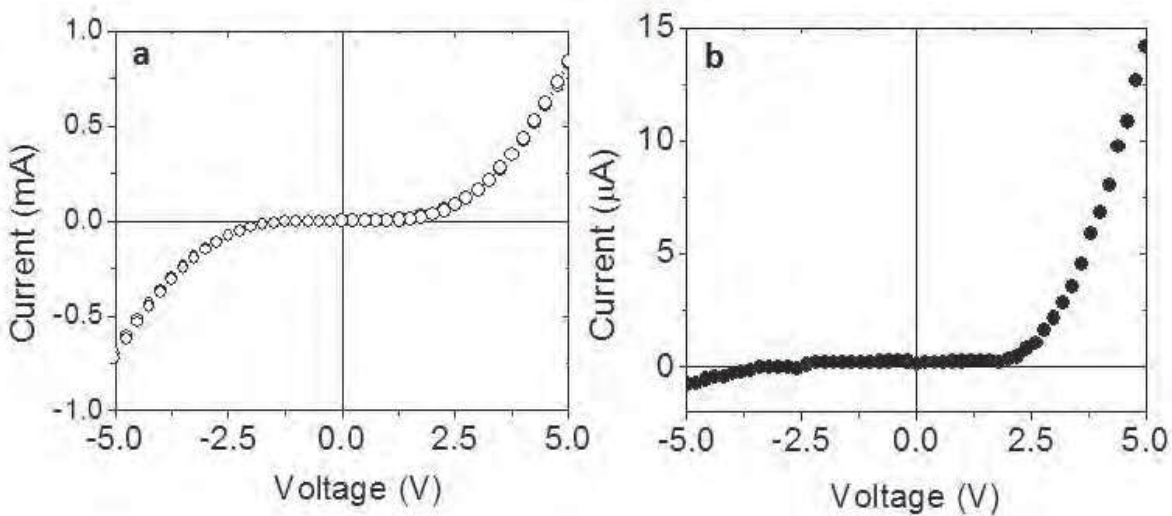


Fig. 15. I-V scans of two nanowall-LED devices with lateral dimensions of: a) 5 mm and b) 100 μm.

As seen in these figures, the injected current is substantially higher in larger sized devices, due to the larger number of involved nanowires as well as the contribution of the ZnO backbone in conducting the charges to the GaN layer. We typically observe a turn on voltages of 2.7 V to 3.8 V ( $\pm 0.2$ ), breakdown voltages of 3V to 9V, and a diode ideality factor ranging from 3 to 3.4, which are comparable to those of free-standing heterojunction nanowires (Nikoobakht and Herzing 2010) (Tian, Zheng et al. 2007).

### 3.2 Electrically-driven light emission of p-n heterojunction arrays

In the fabricated devices, the dopant concentration of the GaN layer is  $5 \times 10^{17} \text{ cm}^{-3}$  and the carrier concentration of the ZnO nanowires is about  $1 \times 10^{18} \text{ cm}^{-3}$  (based on previous electrical measurements (Nikoobakht 2007)). Upon applying a DC voltage to metalized arrays of p-n heterojunctions made from ZnO nanowalls on p-GaN, individual heterojunctions in the array independently emit light, as can be seen from the electroluminescence (EL) image in Figure 16a. This image was collected from part of a device with a faceted-spiral pattern (inset) containing a millimeter-long ZnO backbone that is under an injection current of  $\sim 0.9 \text{ mA}$  at +7V. Results show that both nanowires and nanowalls emit along their entire length in contrast to the mechanically formed p-n junctions where emission originates only from the parts of a nanowire that are in contact with the substrate (Lee, Kim et al. 2007; Zimmmler, Stichtenoth et al. 2008). Another EL emission example of a nanowall-based p-n heterojunction array with lateral dimensions of 5 mm x 5 mm is illustrated in Figure 16b. The dark lines in this image are the metal contacts that block some of the emitted light. The strength of this growth technique is that it allows large scale charge injection into planar nanowire LEDs with a unique control that is difficult to achieve using other techniques.

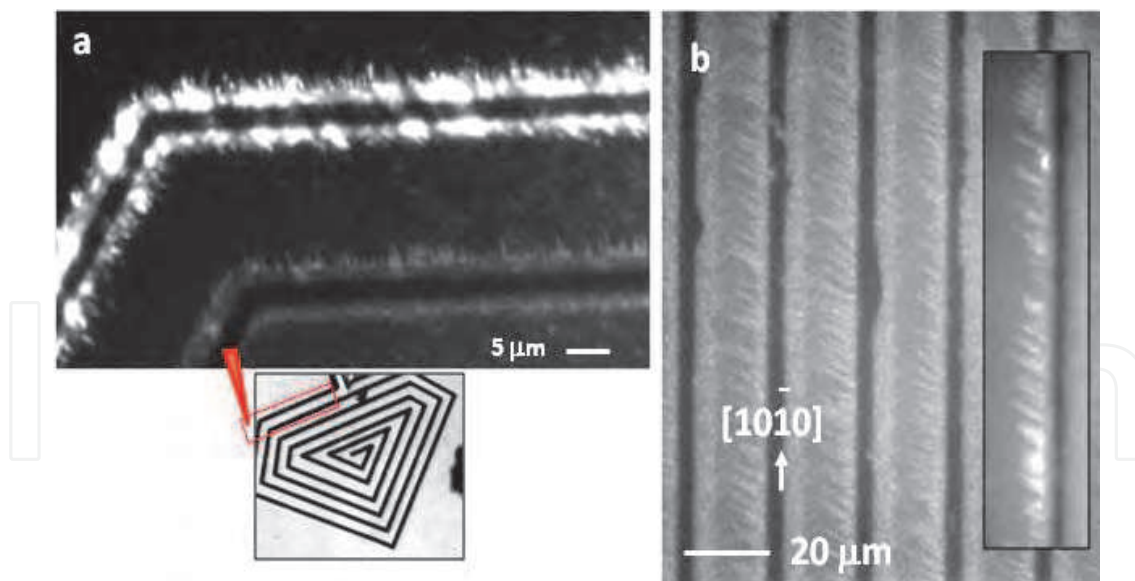


Fig. 16. a) The electroluminescence image of a group of emitting p-n heterojunctions that is part of a millimeter-long nanowall array with a ZnO backbone in the shape of a faceted spiral, which is shown in the optical image in the inset. In this example, the injected current is  $\sim 0.9 \text{ mA}$  at +7V. b) The electroluminescence image of a 5 mm-long array of emitting nanowall p-n heterojunctions with a  $20 \mu\text{m}$ -pitch array spacing. The arrays are formed along the specified direction relative to the GaN *m*-planes. The inset shows the same array, but emitting under a forward injection current of 0.02A.

In order to further probe electro-optical characteristics of these heterojunctions, the EL spectra of a number of heterojunction arrays with different shapes and sizes (from 100  $\mu\text{m}$  to 5 mm) were collected at voltages from -25 V to 27 V using an optical fiber mounted above an active device. Figure 17a illustrates an example in which two spectra are collected from a large array of nanowall p-n heterojunctions (EL image shown in Figure 16b) under a forward bias from 9V to 25V. The strong excitonic emission of the device at about 390 nm agrees well with the photoluminescence (PL) of ZnO nanowalls at 380 nm (Fig. 17b), indicating that holes are injected into the n-type ZnO. This is also in agreement with the brightly emitting nanowires in Figure 16 (a-b) showing that the majority of the charge recombination occurs in the ZnO region. The strong emission and the narrow spectral bandwidth (32 nm FWHM) are indicative of a low density of interface states that depress the radiative recombination probability. The inset of Figure 16a shows the blue emission of a 5 mm<sup>2</sup>-array of p-n heterojunctions at 20 V with an injection current of 0.017 A. The collective emission of the p-n heterojunctions is intense enough that can be observed by the unaided eye.

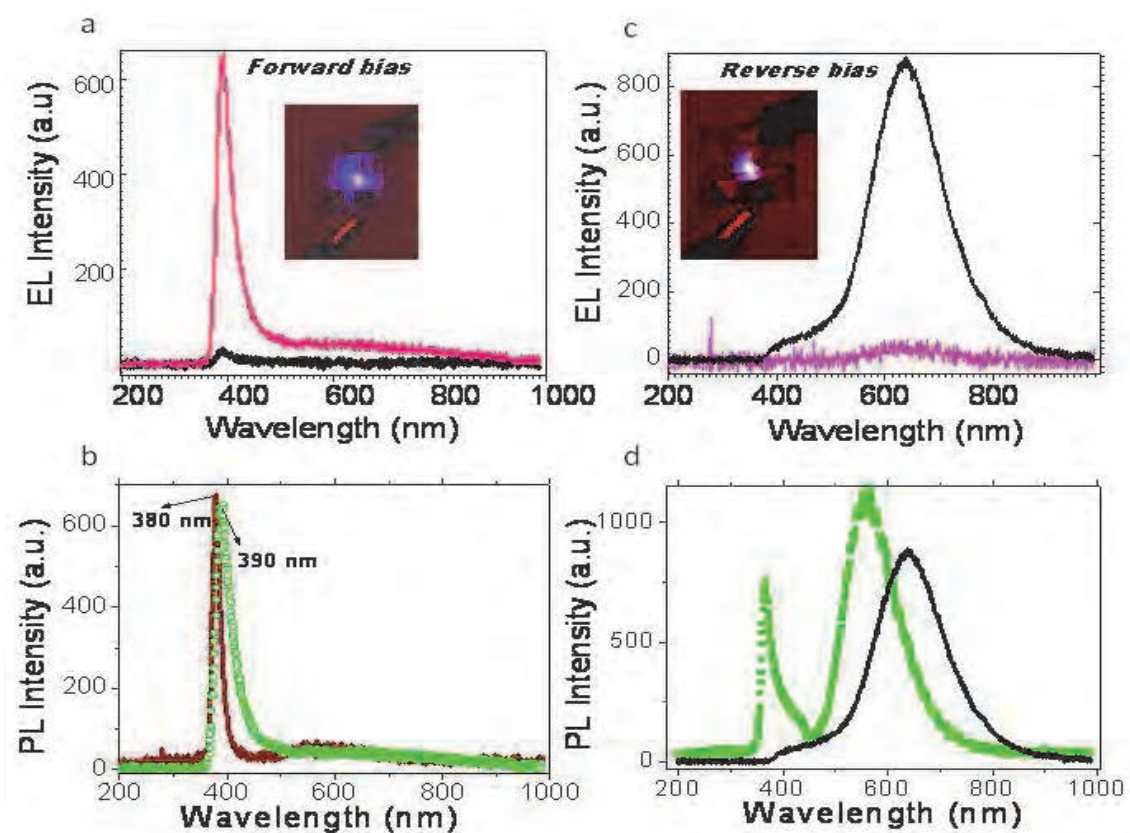


Fig. 17. a) EL spectra of a p-n heterojunction array (similar to the array in Fig.16b) with a lateral dimension of 5 mm under a forward bias of -13 V to -25 V (injection current of 0.01 A to 0.036 A). Inset shows the blue emission of the corresponding device at a forward bias of 20V collected using a digital camera after 30s of exposure time. b) EL emission of p-n heterojunctions at forward bias (circle symbol) and its good agreement with PL emission of the p-n heterojunctions (solid line). c) EL emission at 640 nm from the same array, but under a reverse bias of +7 V to 15V (0.003-0.011A injection current). Inset shows the orange emission of the same device at a reverse bias of 20 V. d) Compares EL emission at 640 nm at a reverse bias (solid line) with PL of p-GaN substrate (square symbol).

By applying reverse bias voltages above 6V, i.e., beyond the break down voltage of the examined devices, we observe a bright orange emission with a wavelength centered at 640 nm (1.95 eV) as shown in the spectra of Figure 17c and inset. This emission is different from PL emission of p-GaN (black curve-Fig. 17d), which also indicates that the charge recombination does not occur in the GaN layer. Although this is still under study, we note that the 640 nm emission intensity decreases as the surface area of the ZnO backbone-GaN decreases. This drop in intensity also coincides with a better rectifying behavior and an increase in the breakdown voltage from 4 V to more than 9 V in smaller size devices (refer to Figures 15 a-b).

Results suggest that the ZnO backbone has a contribution to this emission; nonetheless we do not observe this emission in the PL of the corresponding devices on GaN (brown curve-Fig. 17b). With regard to the electronic states involved in this emission, we tentatively attribute the EL emission under the reverse bias to a transition from an intrinsic shallow state (such as  $\text{Zn}_i$ ) to an intrinsic deep state such as oxygen vacancies. The shape of the EL emission spectrum does not change by increasing the injection current in both reverse and forward biases. However, by increasing the injected current ( $I$ ) the intensity of the emitted light first grows then reaches a mild saturation at higher voltages. This could be an indication of a limited charge carrier concentration at the junction, heating effects, or increase in non-radiative processes. In addition to ZnO, we observe the lateral growth for  $\text{Ti}_2\text{O}_3$  and GaN on substrates such as  $\text{Al}_2\text{O}_3$  (Nikoobakht 2007) and GaN, which possess hexagonal or trigonal/ rhombohedral crystal structures.

#### 4. Conclusion

A nanodevice fabrication method is described which is based on the combination of a “bottom-up” chemical method and conventional optical lithography. Compared to other available techniques, this method controls the surface registries of nanocrystals for successive fabrication steps. The chemical method provides the horizontal growth of nanowires from individual Au nanodroplets, and their alignment is dictated by the underlying substrate. Nanowires are grown where the devices are to be fabricated, and the need for nanowire transfer or alignment is eliminated. This SVLS growth of nanowires for a wide group of materials is likely, especially III-V and II-VI semiconductors, since growth of their free-standing forms has already been reported using this process (Fortuna, Wen et al. 2008). The present technique maintains the strength of the VLS-based methods in growth of axial and core-shell heterojunctions, while allowing control of their hierarchical assembly through surface-directed processes. The flexibility in material combination and the ability to grow dense arrays of laterally grown nanowires/nanowalls could lead to the development of novel heterojunctions that are electrically addressable on relevant scales. Due to the unique control over the location and orientation of arrays of nanowires afforded by this technique, and its compatibility with conventional microfabrication methods, it is expected to impact the field of scalable nanowire-based devices by enabling the realization of numerous structural combinations and device concepts.

#### 5. Acknowledgment

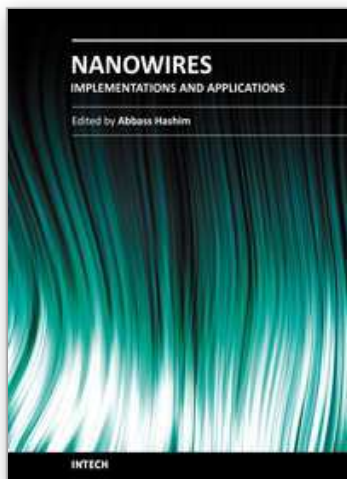
We would like to thank Dr. S. Eustis for collecting the TEM images of cross-sections of nanowires.

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## **Nanowires - Implementations and Applications**

Edited by Dr. Abbass Hashim

ISBN 978-953-307-318-7

Hard cover, 538 pages

**Publisher** InTech

**Published online** 18, July, 2011

**Published in print edition** July, 2011

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